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Doctoral Dissertation

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Electronic Circuit Design Laboratory

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Abstract

To increase spectral efficiency, transmitters usually send only one of the information carrying sidebands centered around a single radio-frequency carrier. The close-lying mirror, or image, sideband will be eliminated either by the filtering method or by the phasing method. Since filter Q-values rise in direct relation to the transmitted frequencies, the filtering method is generally not feasible for integrated microwave transmitters. A quadrature modulator realizes the phasing method by combining signals phased at quadrature (i.e. at 90° offsets) to produce a single-sideband (SSB) output. In this way output filtering can be removed or its specifications greatly relieved so as to produce an economical microwave transmitter. The proliferation of integrated circuit (IC) technologies since the 1980s has further boosted the popularity of quadrature modulator as an IC realization makes possible the economical production of two closely matched doubly balanced mixers, which suppress carrier and even-order spurious leakage to circuit output. Another strength of IC is its ability to perform microwave quadrature generation accurately on-chip, and thereby to avoid most of the interconnect parasitics which could ruin high-frequency quadrature signaling.

Nevertheless, all quadrature modulator implementations are sensitive to phasing and amplitude errors, which are born as a result of mismatches, from the use of inaccurate differential signaling, and from inadequacies in the phasing circuitry itself. A 2° phase error is easily produced, and it reduces the image-rejection ratio (IRR) to -30 dBc. Therefore, as baseband signals synthesized by digital signal processing (DSP) are sufficiently accurate, this thesis concentrates on analyzing and producing the microwave signal path of a direct-conversion quadrature modulator with special emphasis on broadband, multimode radio-compatible operation.

A model of the direct-conversion quadrature modulator operation has been developed, which reveals the effect the circuit non-linearities and mismatch-related offsets have on available performance. Further, theoretical proof is given of the well-known property of improving differential signal balance that cascaded differential pairs exhibit. Among the practical results, a current reuse mixer has been developed, which improves the transmitted signal-to-noise-ratio (SNR) by 3 dB, with a maximum measured dynamic range of +158 dB. The complementary bipolar process was further used to extend the bipolar push-pull stage bandwidth to 9.5 GHz. At the core of this work is the parallel switchable polyphase (PP) filter quadrature generator that was developed, since it makes possible accurate broadband IQ generation without the high loss that usually results from the application of PP filtering. Two IQ modulator prototypes were realized to test simulated and theoretically derived data: the 0.8 μm SiGe IC achieves an IRR better than -40 dBc over 0.75-3.6 GHz, while the 0.13 μm digital bulk CMOS IC achieves better than -37 dBc over 0.56-4.76 GHz. For this IRR performance the SiGe prototype boasts the inexpensive solution of integrated baluns, while the CMOS one utilizes a coil-transmission line hybrid transformer at its LO input to drive the switchable PP filters.

Keywords: SSB transmitter, direct-conversion quadrature modulator, SiGe, digital CMOS, microwave frequencies.

Tiivistelmä

Taajuuksien käytön tehostamiseksi lähettimet lähettävät yleensä vain toisen informaatiota sisältävistä sivukaistoistaan yhdelle radiotaajuuksiselle kantoaallolle keskitettynä. Viereinen peilitaajuus eli sivukaista vaimennetaan joko suodattamalla tai vaiheistamalla signalointia sopivasti. Koska suodattimen hyvyysluvut nousevat suorassa suhteessa käytettyyn taajuuteen, ei suodatusmenetelmä ole yleensä mahdollinen mikroaaltotaajuusalueen lähettimissä. Kvadratuurimodulaattori toteuttaa vaiheistusmenetelmän yhdistämällä 90-asteen vaihesiirroksin vaiheistetut signaalit yksisivukaistaisen lähetteen tuottamiseksi. Näin voidaan korvata lähdön suodatus joko kokonaan tai lieventämällä vaadittavia suoritusarvoja, jolloin mikroaaltoalueen lähetin voidaan tuottaa taloudellisesti. Integroitujen piiriratkaisujen yleistyminen 1980-luvulta lähtien on edesauttanut kvadratuurimodulaattorin suosiota, koska integroidulle piirille voidaan taloudellisesti tuottaa kaksi hyvin ominaisuuksiltaan toisiaan vastaavaa kaksoisbalansoitua sekoitinta, ja nämä tunnetusti vaimentavat kantoaaltovuotoa ja parillisia harmoonisia piirin lähdössä. Toinen integroitujen piirien vahvuus on kyky tarkkaan mikroaaltoalueen kvadratuurisignalointiin samalla piirillä, jolloin vältetään suurin osa kytkentöjen parasiittisista jotka muutoin voisivat tuhota korkeataajuuksisen 90-asteen vaiheistuksen.

Kaikki kvadratuurimodulaattorit ovat joka tapauksessa herkkiä vaiheistus- ja amplitudieroille, joita syntyy komponenttiarvojen satunnaishajonnasta, epätarkan differentiaalisen signaloinnin käytöstä, ja itse vaiheistuspiiristön puutteellisuuksista. Kahden asteen vaihevirhe syntyy helposti, ja tällöin sivukaistavaimennus heikkenee -30 dBc:n tasolle. Tämänvuoksi, ja olettaen että digitaalisella signaaliprosessorilla luotu kantataajuuksinen signalointi on riittävän tarkkaa, tämä väitöskirja keskittyy kvadratuurimodulaattorin mikroaaltotaajuuksisen signaalipolun analysointiin ja tuottamiseen painottaen erityisesti laajakaistaista, monisovellusradioiden kanssa yhteensopivaa toimivuutta.

Kvadratuurimodulaattorin toimintamallia on kehitetty siten, että mallissa huomioidaan epälineaarisuuksien ja piirielementtien satunnaishajontojen vaikutus saavutettavalle suorituskyvylle. Lisäksi on teoreettisesti todistettu sinänsä hyvin tunnettu peräkkäin kytkettyjen vahvistinasteiden differentiaalisen signaloinnin symmetrisyyttä parantava vaikutus. Käytännön tuloksista voidaan mainita kehitetty virtaakierrättävä sekoitin, joka parantaa signaali-kohinasuhdetta +3 dB, suurimman mitatun dynaamisen alueen ollessa +158 dB. Samaa komplementaarista bipolaariprosessia käytettiin edelleen bipolaarisen vuorovaihe-asteen kaistan levittämisessä 9.5 GHz:iin. Yhtenä tämän työn tärkeimmistä tuloksista on kehitetty kytkimin valittavista rinnakkaisista monivaihesuodattimista koostuva kvadratuurigeneraattori, jolla on mahdollista tuottaa laajakaistaista IQ-signalointia ilman suurta häviötä joka yleensä liittyy monivaihesuodattimien käyttöön. Kaksi IQ-modulaattoriprototyyppiä toteutettiin simuloitujen ja teoreettisesti mallinnettujen tulosten testaamiseksi: 0.8 μm SiGe integroitu piiri saavuttaa paremman sivukaistavaimennuksen kuin -40 dBc yli 0.75-3.6 GHz, kun taas 0.13 μm digitaalipiirien tuottamiseen tarkoitetulla CMOS prosessilla toteutettu integroitu piiri saavuttaa paremman sivukaistavaimennuksen kuin -37 dBc taajuusalueella 0.56-4.76 GHz. Näihin sivukaistavaimennuksiin SiGe prototyyppi pääsee edullisesti integroiduin symmetrointimuuntajin, kun taas CMOS piirillä käytetään kela-siirtojohto-

tyyppistä yhdistelmämuuntajaa LO-sisääntulossa josta ajetaan erikseen kytkettäviä monivaihe-suodattimia.

Asiasanat: yksisivukaistainen lähetin, suoramuunnos kvadratuurimodulaattori, SiGe, digitaali-CMOS, mikroaaltotaajuusalue.

Preface

This work was started as the result of an initiative on the part of MICRO ANALOG SYSTEMS OY as part of the TEKES ORAVAT-program in 1998-2002, continued with support from the Academy of Finland, and finally concluded as part of the TEKES ELMO program in 2004-2006 for Nokia Telecommunications. Texas Instruments is acknowledged for the fabrication of the CMOS and the complementary SiGe prototype ICs, with special thanks to Tuomas Hollman and Jaakko Ketola for fabrication support.

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Finally, I would like to thank my parents for their exceptional support, and I would also like to mention my in-laws for their efforts for us, and all my other friends and relatives for their encouragement.
Above all, this book is dedicated to Kirsi, Taru, Säde, Kati, Pia, and Leo.

Esa Tiiliharju
Helsinki, December 2006

Symbols and Abbreviations

Symbols

A_v	voltage gain
ΔA	amplitude error of differential signals
$\Delta\phi$	phase error of differential signals
f_{MAX}	maximum oscillation frequency
f_T	unity gain frequency
g_m	transconductance
I_{DD}	current dissipated from the voltage supply
3^{RD}	third-order harmonic product
3RD-rej	third-order harmonic products rejection
2^{ND}	second-order harmonic product
IIP_3	input-referred third-order intercept point
2ND-rej	second-order harmonic products rejection
P_{1dB}	input-referred 1 dB compression point
N_{BW}	noise bandwidth
N_{floor}	noise floor
N_{+20MHz}	noise floor at a +20 MHz offset from the wanted tone
$N_{+190MHz}$	noise floor at a +190 MHz offset from the wanted tone
OIP_3	output-referred third-order intercept point
ω_{BB}	baseband signal angular frequency
ω_{LO}	local tone angular frequency
OP_{1dB}	output-referred 1 dB compression point
α, β	differential pair small-signal coefficients

β	transistor forward current gain
$\Delta\mathrm{DR}$	dynamic range improvement
ϵ	measure of imbalance for cascaded differential pairs
γ, δ	small-signal model coefficients for cascaded differential pairs
$\in$	part-of
$\pm 2\mathrm{ND}$	up-converted second harmonics products
$\pm 3\mathrm{RD}$	up-converted third harmonics products
$\Re^+$	positive real
σ	linearization factor
θ	phase-error factor
$\mathrm{P_{DD}}$	power dissipated from the voltage supply
ϕ	phase difference of signals
$\mathrm{P_{OUT}}$	output power
$\mathrm{S_{11}}$	two-port reflection coefficient, a.k.a. input return loss
$\mathrm{S_{22}}$	two-port reflection coefficient, a.k.a. output return loss
$\mathrm{S_{21}}$	forward transmission coefficient (gain)
$\mathrm{V_{DD}}$	voltage supply
A	baseband signal amplitude
$\mathrm{a_0}$	offset factor
$\mathrm{a_1}$, $\mathrm{b_1}$	linear baseband gain factors
$\mathrm{a_2}$, $\mathrm{b_2}$	second-order baseband distortion factors
$\mathrm{a_3}$, $\mathrm{b_3}$	third-order baseband distortion factors
$\mathrm{A_c}$, $\mathrm{A_s}$	linear LO tone gain factors
$\mathrm{A_i}$, $\mathrm{A_q}$	linear baseband gain factors
adBx	local common-mode gain factor
adBx1	local gain factor for the linear term
adBx3	local gain factor for the third-order term
B	local signal amplitude
$\mathrm{c_1}$, $\mathrm{d_1}$	linear LO tone gain factors
$\mathrm{c_2}$, $\mathrm{d_2}$	second-order LO tone distortion factors

c_3, d_3	third-order LO tone distortion factors
CM	baseband common-mode gain factor
g_o	bipolar small-signal model channel conductance
i(t)	time-dependent in-phase signal
K_{BB}	baseband gain to mixer load
loi(t)	time-dependent in-phase local tone
loq(t)	time-dependent quadrature-phased local tone
Nx	noise sources as x=i, q, xi, or xq
Oc	offset of the in-phase local input
Oi	offset of the in-phase baseband input
Oq	offset of the quadrature-phase baseband input
Os	offset of the quadrature-phase local input
q(t)	time-dependent quadrature-phased signal
r_π	bipolar small-signal model base-emitter resistance
r_o	bipolar small-signal model channel resistance
s(t)	time-dependent quadrature modulator output signal

Abbreviations

16-QAM	QAM with 16 constellation points
2.5G	second-and-a-half-generation wireless telephone technology
2G	second-generation wireless telephone technology
3G	third-generation wireless telephone technology
64-QAM	QAM with 64 constellation points
DEV	relative element value tolerances
LOT	absolute element value tolerances
ACPR	adjacent channel power ratio
BB	baseband
BER	Bit-error rate
BiCMOS	bipolar process with CMOS components

CDMA	code division multiple access
CGCS	common-gate common-source transistor connection
CMOS	complementary metal oxide semiconductor
CMRR	common-mode rejection ratio
DA	digital-to-analog
DC	direct current
DR	dynamic range
DSP	digital signal processing
EDGE	enhanced data-rate for gsm evolution
EER	envelope elimination and restoration
EVM	error-vector-magnitude
FET	field-effect transistor
GMSK	gaussian minimum shift keying
GPRS	general Packet Radio Service
GSM	global system for mobile communications
gsm	global System for Mobile communications
I	in-phase
IC	integrated circuit
$\text{ideal}_{x,y}$	ideal output rotating phasor x- and y components
IF	intermediate frequency
IQ	in- and quadrature phased
IRR	image-rejection ratio
LCR	inductor-capacitor-resistor resonant circuit
LO	Local tone, i.e. synthesized microwave carrier
LSB	lower sideband
MB-OFDM	multiband OFDM
MIM	metal-insulator-metal semiconductor structure
MOS(FET)	metal-oxide-semiconductor (field-effect)) transistor
NMOS	n-channel MOSFET
NPN	bipolar transistor with P-doped base

OFDM	orthogonal frequency-division multiplexing
OPLL	offset phase-locked loop
PA	power amplifier
PAR	peak-to-average ratio
PLL	phase-locked loop
PMOS	p-channel MOSFET
PNP	bipolar transistor with N-doped base
PP	polyphase
Q	filter quality factor
Q	quadrature-phased
QAM	quadrature amplitude modulation
QPSK	quadrature phase-shift keying
QVCO	voltage-controlled oscillator with quadrature outputs
RC	resistor-capacitor circuit
$\text{real}_{x,y}$	realized output rotating phasor x- and y components
RF	radio frequency
RFIC	radio frequency integrated circuit
SAW	surface Acoustic Wave
SDR	software-defined radio
SFG	signal-flow-graph
SiGe	silicon bipolars with germanium-doped transistor bases
SMA	Sub-Miniature A Connector
SNR	signal-to-noise ratio
SSB	single-sideband
TDR	transmitted dynamic range
UMTS	universal Mobile Telecommunications System
USB	upper sideband
UWB	ultra-wideband
VCO	voltage-controlled oscillator
VNA	vector network analyzer
W-CDMA	wideband CDMA
WLAN	wireless local-area network

Contents

1. Introduction

A wireless radio transmitter applies a coded and modulated signal on a radio frequency carrier wave for subsequent transmission and reception. Ideally, transmission does not add noise and/or distort the transmitted signal, but this is hardly ever the case. Distortion spreads the transmitted signaling to interfere with other users, and transmitted noise might desensitize the user's own receiver block. Therefore, the use of radio frequencies is tightly controlled, i.e. regulated, by government agencies such as ETSI in Europe and FCC in the USA.

Different modulation schemes are used, according to desired power and spectral efficiencies [1]: 2G cellular services use power-efficient phase modulation schemes such as GMSK, used to build gsm-services. This makes possible perfect audio transmission, but offers very limited data capabilities in the range of 60 kbit/s. As the emerging 2.5 and 3G services (EDGE, UMTS) target much higher data transmission rates at a minimum of several hundred kilobits per second, this reflects on the chosen modulations as well. Accordingly, the predominant spectrally efficient modulation formats (QPSK, 16-QAM, 64-QAM, OFDM) manipulate both the amplitude and phase of the transmitted signal so as to pack several bits into each transmitted symbol. In fact, the hugely successful wireless local area networks (WLANs) have recently introduced OFDM in a 55 Mbit/s system operating in the 2.4 GHz frequency band (802.11g).

The penalty for the increased data rates is that the simultaneous manipulation of amplitude and phase results in variable envelope signaling; for OFDM peak-to-average-ratios (PAR) in the range 8-13 dB are commonplace. To maintain reasonable power amplifier (PA) efficiencies, transmitter linearity and spectral purity now have increased significance: a spectrally pure transmitter makes possible the application of a non-linear efficient PA. Transmitters can thus be classified into non-linear (constant envelope) and linear (variable envelope) transmitters [2, 3]. One of the most successful non-linear transmitters is the offset phase-locked loop (OPLL), which utilizes the PLL filtering action to fulfill tight GSM noise specifications [4]. This dominant 2G transmitter is shown in Fig. 1.1.

1.1 Linear transmitters

To assess different linear transmitter types, the software-defined radio (SDR), or at least the multistandard radio requirements of broadband, linear, and low-noise radio transmissions, have to be considered in a world of radio standards rapidly evolving towards higher bitrate operation.

1.1.1 Two-step transmitter

The two-step, or super-heterodyne, transmitter can also be described as the filtering method of frequency translation; one or more intermediate frequencies (IFs) are used in order to relax the specifications of individual circuit blocks. In particular, this approach yields high-quality receivers which are immune to the PA pulling of the frequency synthesizers and exhibit low-noise signal transmission. The complexity of the resulting hardware is high and the use of off-chip SAW-filters is costly and should be avoided, especially since lead-free soldering will

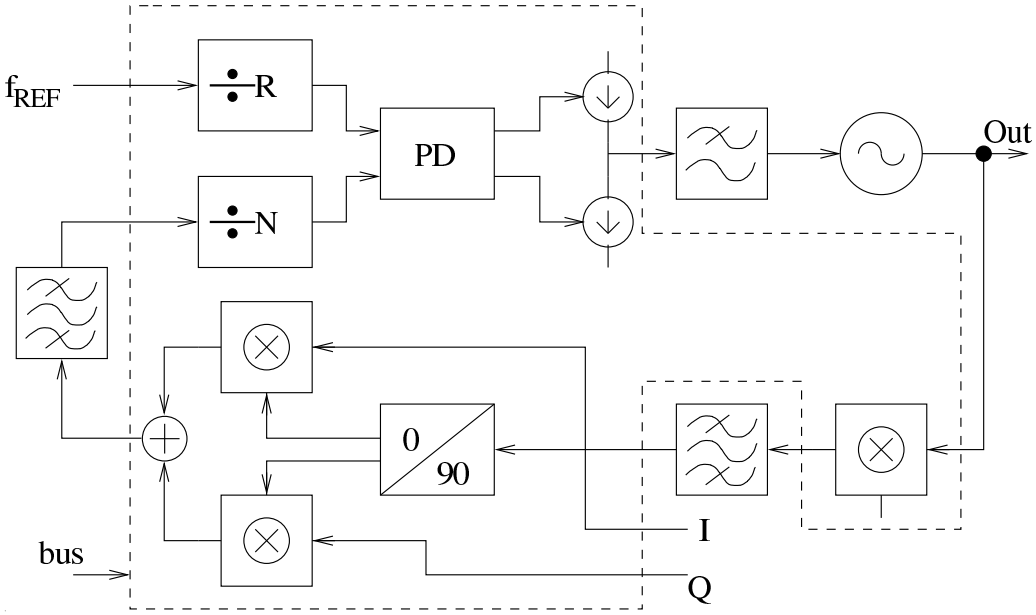


Figure 1.1: The OPLL up-conversion loop for GSM transmitters [4].

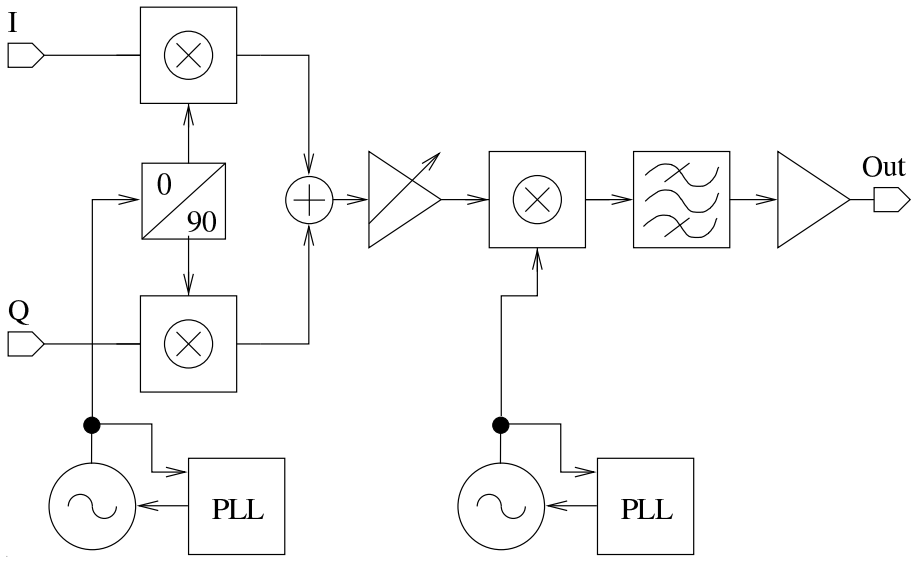


Figure 1.2: The two-step or super-heterodyne transmitter.

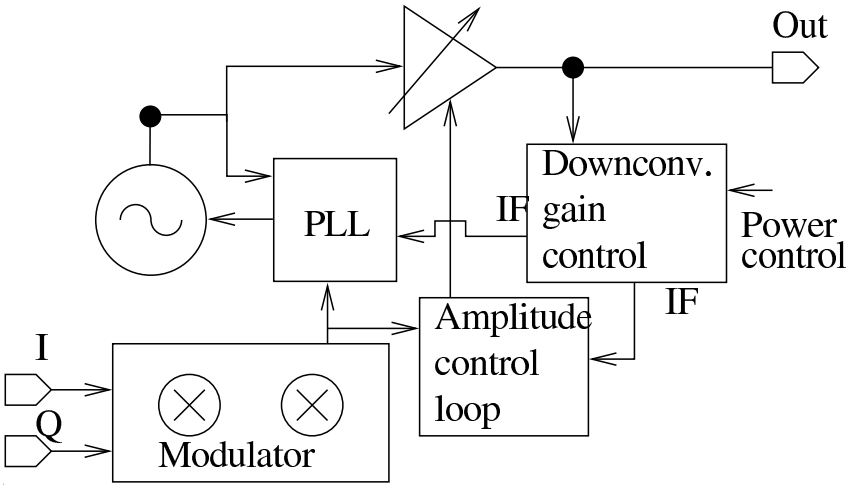


Figure 1.3: The polar loop transmitter with closed-loop PA-control [6].

become globally mandatory in the near future. The complexity of the hardware is evident from the block diagram of a typical two-step transmitter in Fig. 1.2. In fact, filters with no (or limited) tuning range and complex frequency planning involved severely restrict the application of this topology in multi-mode radios.

1.1.2 Polar loop transmitters

Recently, envelope elimination and restoration (EER), or the Kahn method of transmission [5], have been used to realize multimode GSM/EDGE transmitters [6, 7]. The one in [6] is also GPRS-compatible with the PA inside its amplitude and phase control feedback loops; the use of the topology in Fig. 1.3 results in a measured PA efficiency of 35% while fulfilling EDGE-specifications with +27 dBm at the antenna. The polar loop approach, however, results in complex hardware with the need for custom PA to accommodate amplitude control. Amplitude and phase control loop bandwidths need to be carefully matched so as to prevent spectral re-growth and instability. Since both realizations [6,7] include phase-locked loops, their usability for wider signal bandwidth system (e.g. W-CDMA) up-conversion is questionable.

1.1.3 Direct-conversion quadrature modulator

Since both polar loop transmitters and two-step transmitters include a quadrature modulator for I/Q up-conversion, it has the least hardware complexity and is the most integrable transmitter type. This simplicity is also evident in the direct-conversion quadrature modulator block diagram shown in Fig. 1.4, where only one frequency synthesizer is used. Such an IQ modulator is also compatible with broadband signaling, such as MB-OFDM for ultra-wideband (UWB physical layer proposal in [8]), and, as third-party vendors can be used, decades of PA research can be tapped for linearized or linear PAs so as to rapidly attain acceptable system performance. Alas, a good quadrature modulator performance is sensitive to DC offsets, signaling accuracy, noise, and distortion. Deviations from exact quadrature signaling (signals at 90° offsets) give rise to an unwanted sideband. The microwave carrier or local (LO) may leak to the output and destroy signal integrity through several mechanisms, such as: baseband offset; LO phasing errors, and package/bonding wire antenna effects. Different control circuits or direct digital up-conversion have been suggested as remedies for better signal quality. However, although impressive, both approaches fail to offer broadband drop-in functionality, and their performance is limited to either

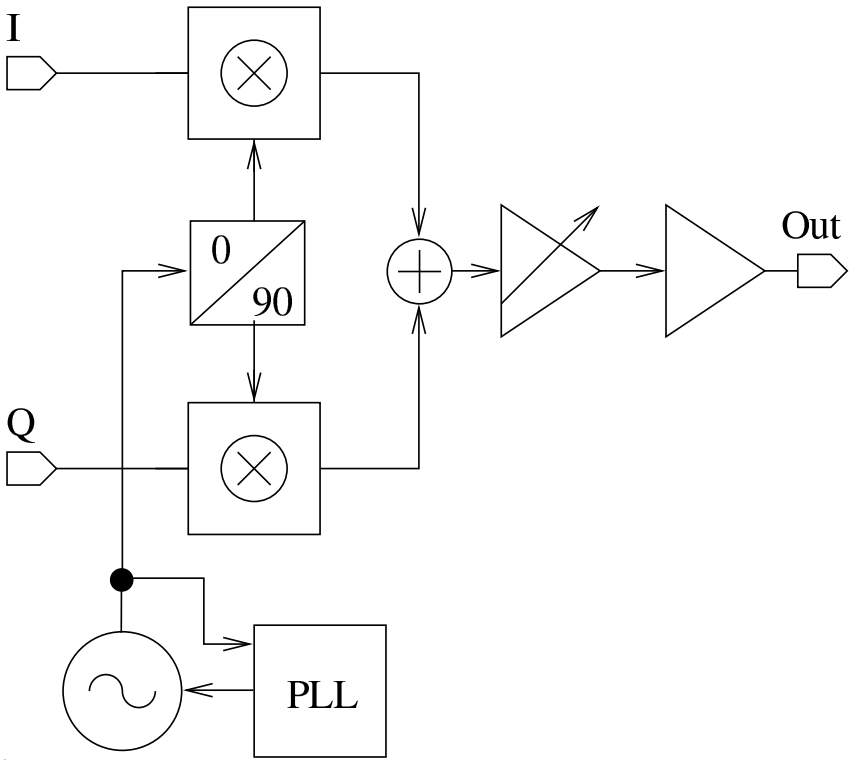


Figure 1.4: A direct-conversion quadrature modulator with high power amplifier (HPA) buffering.

spot-frequency operation [9] or sinc-effect baseband oversampling [10, 11]. Both approaches share the microwave LO phasing to quadrature (IQ-signaling) as the performance limiting factor.

To illustrate how the IQ modulator specifications differ depending on the specific application, the published performance for a 3G basestation transmitter [12] and for a multistandard WLAN (802.11a/b/g) application [13] are shown in Table 1.1. The 3G basestation application is a good example of the need to minimize modulator error-vector-magnitude (EVM), as the total system EVM specification is 17.5% (QPSK) but still only a maximum EVM of 5% (max) has been specified to the modulator. This has been done to increase PA efficiency with the variable-envelope modulation, since a high EVM margin allows the PA to be used deeper in its non-linear, efficient mode of operation.

Table 1.1: Published buffered quadrature modulator performance for 3G and WLAN applications.

		3G	WLAN	
			2.4 GHz	5 GHz
P_{OUT}	[dBm]	+41	-4	-4
IRR	[dBc]	-30	-40	-40
OP_{1dB}	[dBm]	+3	—	—
OIP_3	[dBm]	+13	+17	+13
EVM	[%]	5	3.2	3.6
I_{DD}	mA	—	137	
V_{DD}	V	—	1.8/1.6-3.6	

The set of WLAN specifications is another good example of high bitrate wireless communications, but targeted to be used at a much shorter range than the 3G device. For the 3G device a higher transmitted power is needed to keep the basestation geographical cell size economically feasible, whereas a high power WLAN transmission could be detrimental to other applications roaming in the same unlicensed frequency bands. Use of the higher bitrate WLAN modes of operation (55 Mbit/s) dictates that a minimum IRR performance of -40 dBc has to be achieved [14]. The reason for the increased IRR specification is that the OFDM modulation used for the high bitrates needs accurate phasing, unless it starts to fold its subcarriers onto each other.

1.2 Research contribution

This thesis work concentrates on microwave signal integrity in the context of direct-conversion quadrature modulators: integrated balun and quadrature signaling accuracy and mismatch evaluation are at the core of this work. LO frequency synthesis, and power amplifier design are extensive topics in their own right, but they have been treated as being outside the scope of this thesis work. Reference to these issues is only made where it is helpful in defining practical available broadband performance from a quadrature modulator.

Four radio frequency integrated circuits (RFICs) were fabricated in support of this thesis. The technologies used for the first three prototypes are illustrative of underlying development trends in 2000-2004, as linewidths dropped from 0.8 μm to 0.13 μm while processes varied from BiCMOS, through SiGe, to a digital CMOS process. The fourth prototype was implemented in an experimental 0.4 μm complementary SiGe process with an emphasis on finding improved mixer and buffer structures.

The first IC was a mixer realized in a 0.8 μm BiCMOS process with electrical design and measurements done by the author, and layout by Mr. Aki Friman. The second IC was realized by the author alone in a 0.8 μm SiGe with two major test blocks: the first block was an accurate integrated balun for microwave frequencies, and the second block applied the developed balun in a completely integrated quadrature modulator implementation. Also the third IC was implemented solely by the author in a 0.13 μm digital CMOS process to test a novel quadrature generator for microwave frequencies, and its application in a direct-conversion quadrature modulator. The fourth IC was realized by Mr. Harri Pellikka in an experimental 0.4 μm complementary SiGe process as a set of mixer and buffer test blocks with key circuit ideas originating from the author, and with the reported current reuse mixer designed solely by the author. Mr. Juhani Aalto from Nokia Mobile Phones did a special study project on four well-known linearized mixer structures (simulations) for this work, according to specifications and instructions from the author. The simulated characteristics have been included in this work as part of discussion on the implemented low-voltage class AB Gilbert mixer in 0.8 μm SiGe.

The results of the experimental work have been partially reported in several journals and conference publications, and reference to these publications will be made where relevant. Most of the material in the journal articles [15, 16, 17, 18] is included in this work and the material is further presented in [19, 20, 21, 22, 23, 24, 25].

The key contributions of this thesis are: extension of a previously published linear direct-conversion quadrature modulator model to include non-linearities in each signal path, and analysis to reveal their effect on available circuit performance; theoretical proof of the well-known property of improving signal balance that cascaded differential pairs exhibit; and the first parallel switchable polyphase filter realization for broadband quadrature generation at microwave frequencies. Other practical results included in support of this thesis are: one of the most accurate integrated baluns ever published operating up to 3.7 GHz; a direct up-conversion current reuse mixer realization which improves transmitted dynamic range by +3 dB; the topology and

extension of the operation of the bipolar push-pull stage to nearly 10 GHz; best published broadband IRR performance for a completely integrated IQ modulator realization in 0.8 μm SiGe, and the use of the realized switchable polyphase filter in a 0.13 μm digital CMOS quadrature modulator implementation which has an image-rejection ratio of -37 dBc in 0.56-4.76 GHz.

1.3 Organization of the thesis

In Chapter 2 the existing quadrature modulator theory will be reviewed and developed further, with emphasis on performance limitations. Each sub-block is briefly introduced, and its impact on quadrature modulator performance and usability will be discussed. Chapter 3 precedes Chapter 4 with a description of different possible integrated baluns for the 0-6 GHz frequency range, where distributed elements are not yet applicable but parasitics easily destroy differential LO signal balance. Chapter 4 presents the core of this work: possible integrated broadband quadrature generation circuits for microwave frequencies are described in this chapter. Analysis leading to the realized switchable parallel polyphase filters is given, and the realized prototypes are described. In Chapter 5 the impact of low-voltage operation on the Gilbert mixer is discussed, several pre-amplifier biased low-voltage topologies are introduced, and the mixers chosen for this thesis work are analyzed. This analysis is complemented in Chapter 6 by evaluation of the PA driver buffers and of their impact on system performance. Chapter 7 compares broadband direct-conversion quadrature modulator realizations, and finally the material presented is discussed and conclusions are given in Chapter 8.

2. Quadrature modulator theory

The principle of operation of a quadrature modulator is simple: two multipliers are used to modulate baseband signals (information) on to a carrier wave (the local, LO signal). As the signaling involved is carefully phased at 90° (quadrature) offsets, this makes possible the transmission of the wanted sideband while suppressing the other, unwanted, sideband.

This kind of single-sideband (SSB) generation has been known since the 1950s, but its current popularity is attributable to the success of the integrated circuit, since only closely spaced transistors and passives on the same silicon die produce the required levels of inter-element matching economically enough. With perfect distortionless devices no filtering is needed, and this results in spectrally pure transmission. However, distortion and noise always hinder performance, whereas device mismatches produce signal phase and amplitude errors which destroy circuit performance.

Therefore, this chapter first introduces the ideal quadrature modulator operation principle [26], then defines possible non-idealities and their effect on the performance of a quadrature modulator. Application of the first-order error model [27] and its extension with a third-order distortion model [28] completes the discussion of non-ideal quadrature modulator performance. Finally, the derived equations are simplified to quantify available performance, and system noise performance is estimated to check whether system level decisions could affect quadrature modulator noise behavior and its dynamic range. To conclude this chapter, the adjacent channel power ratio (ACPR) and error vector magnitude (EVM) characteristics will be introduced.

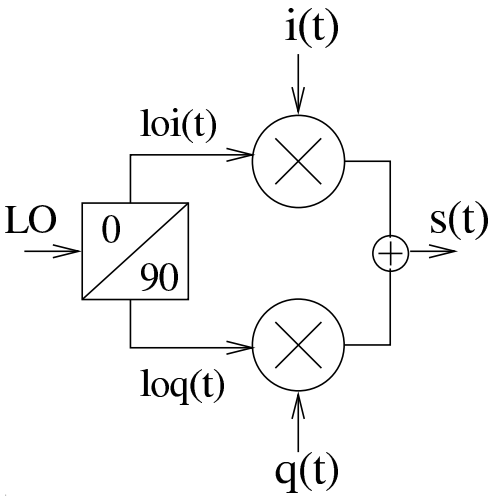


Figure 2.1: The ideal quadrature modulator implementation.

2.1 The ideal quadrature modulator

The ideal quadrature modulator has been dubbed the image canceling mixer [26], in recognition of the fact that the multiplication and summing of in-phase (cosine) and quadrature (sinusoidal) signals selects the wanted sideband, while suppressing the unwanted one. The block diagram for such a modulator in Fig. 2.1 includes an LO quadrature generator symbol (0/90), two multipliers, and a summing node. The in-phase i(t) and quadrature q(t) signaling definitions are:

$$\begin{aligned} i(t) &= cos(\omega_{\mathrm{BB}}\, t) \\ q(t) &= cos(\omega_{\mathrm{BB}}\, t + 90^{\circ}) = -sin(\omega_{\mathrm{BB}}\, t) \end{aligned} \tag{2.1}$$

Correspondingly, the LO in-phase loi(t) and quadrature loq(t) signals are defined as:

$$\begin{aligned} loi(t) &= cos(\omega_{\mathrm{LO}}\, t) \\ loq(t) &= cos(\omega_{\mathrm{LO}}\, t + 90^{\circ}) = -sin(\omega_{\mathrm{LO}}\, t) \end{aligned} \tag{2.2}$$

Summing the two mixer products $\mathrm{i(t)\,loi(t)}$ and $\mathrm{q(t)\,loq(t)}$ selects the lower sideband (LSB), while taking the difference selects the upper sideband (USB). In angular frequencies the upper and lower sidebands are defined as:

$$\begin{aligned} &\text{USB: } \omega_{\mathrm{LO}} + \omega_{\mathrm{BB}} \\ &\text{LSB: } \omega_{\mathrm{LO}} - \omega_{\mathrm{BB}} \end{aligned} \tag{2.3}$$

For an up-converter application, USB is the preferable desired tone; advantageously, with differential signaling the negative $-\mathrm{q(t)\,loq(t)}$ can be produced by crossing the differential signal lines across the analog ground [29]. USB output (at quadrature phase) can also be produced by interchanging the baseband, or the carrier, in-phase, and quadrature waveforms. The quadrature modulator output s(t) resulting from the subtraction of the in-phase and quadrature mixer products is:

$$\begin{aligned} s(t) &= i(t)\, loi(t) - q(t)\, loq(t) \\ &= \frac{1}{2} cos\left((\omega_{\mathrm{LO}} - \omega_{\mathrm{BB}})t\right) + \frac{1}{2} cos\left((\omega_{\mathrm{LO}} + \omega_{\mathrm{BB}})t\right) \\ &\quad - \left[\frac{1}{2} cos\left((\omega_{\mathrm{LO}} - \omega_{\mathrm{BB}})t\right) - \frac{1}{2} cos\left((\omega_{\mathrm{LO}} + \omega_{\mathrm{BB}})t\right)\right] \\ &= cos\left((\omega_{\mathrm{LO}} + \omega_{\mathrm{BB}})t\right) \end{aligned} \tag{2.4}$$

Since (2.4) predicts complete suppression of the LSB at $\omega_{\mathrm{LO}} - \omega_{\mathrm{BB}}$, it conflicts with the known sensitivity of any quadrature modulator to amplitude and phase errors in its quadrature signaling. These errors raise the spurious content of the transmitted signaling so that it is quite dissimilar to the ideal SSB response. Thus, the different non-idealities that produce these errors, and their effects on circuit performance are discussed in the following section.

2.2 The non-ideal quadrature modulator

Even with perfect quadrature signaling, the non-idealities and mismatches of implemented circuitry will have a deleterious effect on the performance of the quadrature modulator. The static offsets produced by mismatches give rise to spurious (unwanted) tones, and dynamic offsets in the form of different weighing factors of distortion-created harmonics [30] give rise to errors that usually increase with frequency, while circuit performance decreases. To model this, single

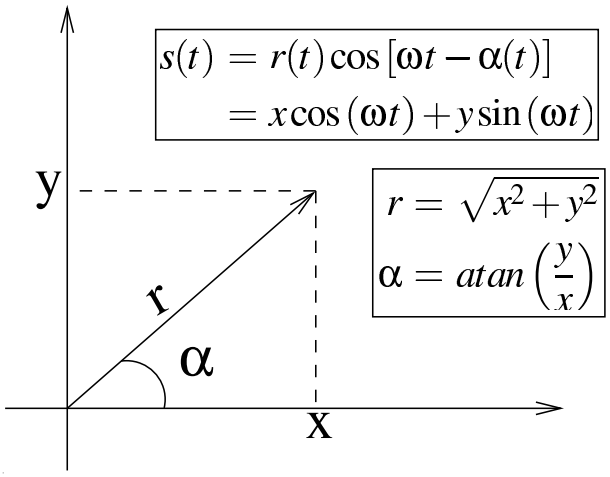


Figure 2.2: Vector representation of a single tone in envelope phase (r, α) and the orthogonal (x, y) coordinates.

gain ΔA and phase error $\Delta\phi$ factors could be introduced in the baseband [31], or in carrier signaling [32]. The first approach also introduces an offset factor O to model circuit mismatches. Whether the ΔA and $\Delta\phi$ error factors should be inserted in the baseband or in carrier signaling is really of no concern: both approaches produce exactly the same quadrature modulator output signal s(t). Thus it is convenient to study the baseband-centered error model [31], which will give added insight with the offset factor O. Therefore, the in-phase modulating signal i(t) in (2.1) can be re-defined as:

$$i(t) = \Delta A\, cos(\omega_{\mathrm{BB}}\, t + \Delta\phi) + O \tag{2.5}$$

Application of (2.5) in (2.4) and manipulation with trigonometric identities gives s(t) as:

$$\begin{aligned} s(t) \;=\; & cos\left((\omega_{\mathrm{LO}} + \omega_{\mathrm{BB}})\, t\right) && \left[\frac{1}{2}\Delta A\, cos(\Delta\phi) + \frac{1}{2}\right] \\ +\; & sin\left((\omega_{\mathrm{LO}} + \omega_{\mathrm{BB}})\; t\right) && \left[-\frac{1}{2}\Delta A\, sin(\Delta\phi)\right] \\ +\; & cos\left((\omega_{\mathrm{LO}} - \omega_{\mathrm{BB}})\; t\right) && \left[\frac{1}{2}\Delta A\, cos(\Delta\phi) - \frac{1}{2}\right] \\ +\; & sin\left((\omega_{\mathrm{LO}} - \omega_{\mathrm{BB}})\; t\right) && \left[\frac{1}{2}\Delta A\, sin(\Delta\phi)\right] \\ +\; & O \end{aligned} \tag{2.6}$$

From (2.6) new spurious products can be discovered: 1) the unwanted lower sideband now has a finite value, and 2) the offset factor O leaks as a DC component to the output. Since the offset O can be filtered out by the application of a DC block which acts as a high-pass filter, it is not harmful to transmitter operation, whereas the LSB tone lies near the desired USB at an offset of $-2\,\mathrm{f_{BB}}$. Therefore, its magnitude in relation to that of the USB tone has to be defined. To define individual tone magnitudes, the connection between each signal envelope phase and the orthogonal presentations shown in Fig. 2.2 can be utilized by treating the cosine and sinusoid terms for each tone as orthogonal unity vectors. By analogy, the bracketed terms in (2.6) can now be defined as the x and y coordinates, and corresponding vector magnitude (r) and phase

(α) terms are therefore known. In this way it is possible to define the image-rejection ratio (IRR) relation $|\mathrm{LSB}|/|\mathrm{USB}|$. To define IRR (in decibels) (2.6) can be developed to:

$$\begin{aligned} IRR = & \ 20\, log_{10} \left(\frac{|LSB|}{|USB|} \right) \\ = & \ 10\, log_{10} \left(\frac{\Delta A^2 - 2\Delta A cos(\Delta\phi) + 1}{\Delta A^2 + 2\Delta A cos(\Delta\phi) + 1} \right) \end{aligned} \tag{2.7}$$

For the plotting of image-rejection contours in a $\Delta\mathrm{A}\Delta\phi$-plane (2.7) can be solved to give:

$$\Delta\phi \ = \ \arccos \left(\frac{1}{2} \frac{\left(1 + \Delta A^2\right)}{\Delta A} \frac{\left(1 - 10^{\dfrac{IRR}{10}} \right)}{\left(1 + 10^{\dfrac{IRR}{10}} \right)} \right) \tag{2.8}$$

The image-rejection contours corresponding to (2.8) are plotted in Fig. 2.3, with the lower window depicting image-rejection values at better than -50 dBc; for this kind of performance gain and phase errors should lie within 0.1 dB and 0.4°, respectively.

The described use of two to three linear, time-invariant error factors {ΔA, $\Delta\phi$, O} in quadrature modulator signaling is, in fact, a subset of the first-order error model quadrature modulator application, which will be described in the following subsection.

2.2.1 The first-order error model

Application of the first-order error model transforms the ideal quadrature modulator in Fig. 2.1 to the form shown in Fig. 2.4: the previously defined single gain ΔA and offset error O factors (2.5) have been replaced by four positive real gain $\mathrm{A_{i,q,s,c}}$ and four real offset (Oi, Oq, Oc, Os) factors, respectively. The phase error factor $\Delta\phi$ has been inserted as θ in the LO phasing block, which operates at microwave frequencies in implementations and is therefore the most probable error source. Actually, the LO quadrature generator block has been explicitly drawn from the outset to mirror the fact that for best performance this high-frequency block should always be placed adjacent to the multipliers, preferably on the same IC. Thus, the quadrature modulator output $\mathrm{s(t)}$ can be defined as:

$$\begin{aligned} s(t) \ = \ & \left(Ai \ \cdot \cos\left(\omega_{\mathrm{BB}}\, t\right) + Oi\right) \left(Ac \ \cdot \cos\left(\omega_{\mathrm{LO}}\, t\right) + Oc\right) \\ & - \left(-Aq \ \cdot \sin\left(\omega_{\mathrm{BB}}\, t\right) + Oq\right) \left(-As \ \cdot \sin\left(\omega_{\mathrm{LO}}\, t + \theta\right) + Os\right) \end{aligned} \tag{2.9}$$

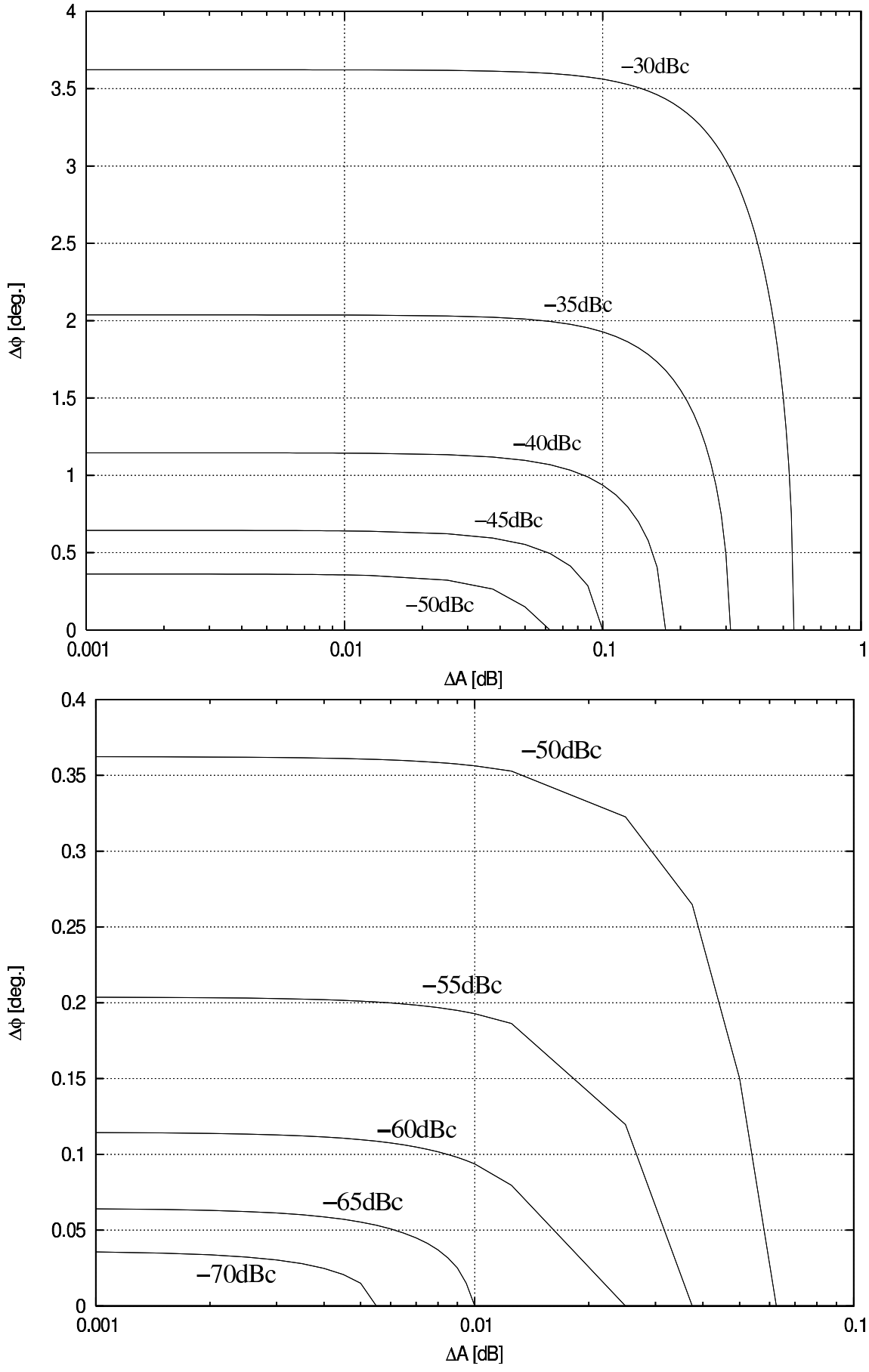


Figure 2.3: Image-rejection ratios in gain vs. phase error plane.

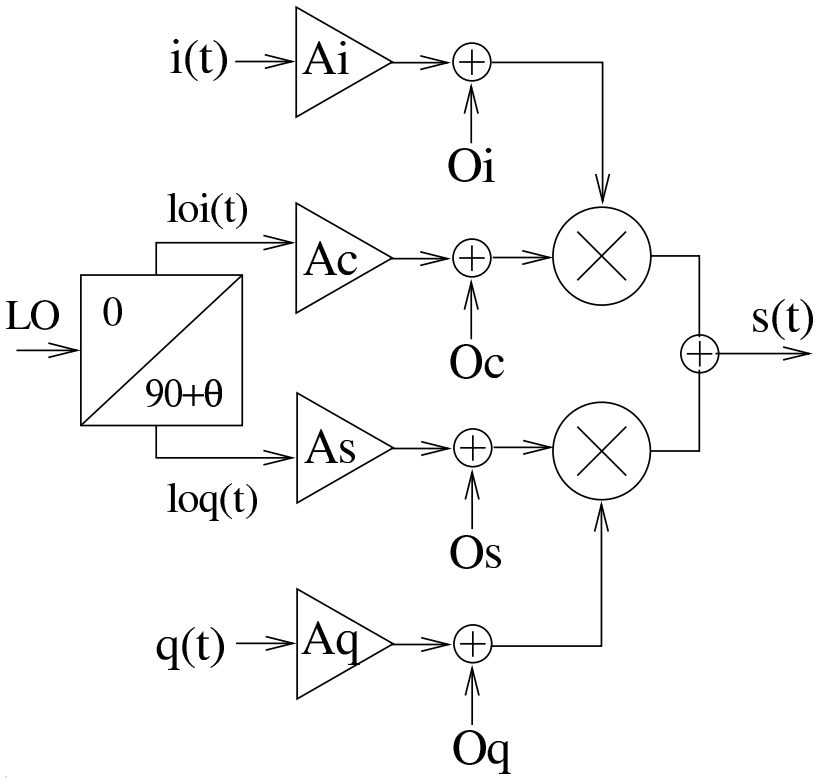


Figure 2.4: The quadrature modulator complemented with the first-order error model.

After the application of trigonometric identities and re-arrangement by tone, the quadrature modulator output is expanded to:

$$\begin{aligned}
s(t) \;=& \cos\left(\left(\omega_{\mathrm{LO}}+\omega_{\mathrm{BB}}\right)t\right) && \left[\frac{Ai\,Ac}{2}+\frac{Aq\,As\,\cdot cos(\theta)}{2}\right]\\
&+\; sin\left(\left(\omega_{\mathrm{LO}}+\omega_{\mathrm{BB}}\right)\,t\right) && \left[-\frac{1}{2}\,Aq\,As\,\cdot sin(\theta)\right]\\
&+\; cos\left(\left(\omega_{\mathrm{LO}}-\omega_{\mathrm{BB}}\right)\,t\right) && \left[\frac{Ai\,Ac}{2}-\frac{Aq\,As\,\cdot cos(\theta)}{2}\right]\\
&+\; sin\left(\left(\omega_{\mathrm{LO}}-\omega_{\mathrm{BB}}\right)\,t\right) && \left[\frac{1}{2}\,Aq\,As\,\cdot sin(\theta)\right]\\
&+\; cos\left(\omega_{\mathrm{LO}}\,t\right) && [Oi\,Ac\,+\,Oq\,As\,\cdot sin(\theta)]\\
&+\; sin\left(\omega_{\mathrm{LO}}\,t\right) && [Oq\,As\,\cdot cos(\theta)]\\
&+\; cos\left(\omega_{\mathrm{BB}}\,t\right) && [Ai\,Oc]\\
&+\; sin\left(\omega_{\mathrm{BB}}\,t\right) && [Aq\,Os]\\
&+ && [Oi\,Oc-Oq\,Os]
\end{aligned} \tag{2.10}$$

which gives IRR and LO rejection (LO-rej) definitions as:

$$IRR=\frac{LSB}{USB}=\sqrt{\frac{\left(\frac{AiAc}{AqAs}\right)^2-2\frac{AiAc}{AqAs}cos(\theta)+1}{\left(\frac{AiAc}{AqAs}\right)^2+2\frac{AiAc}{AqAs}cos(\theta)+1}} \tag{2.11}$$

$$LO - rej \;=\; \frac{LO}{USB} \;=\; 2\frac{Oq}{Aq}\sqrt{\frac{\left(\frac{OiAc}{OqAs}\right)^2 - 2\frac{OiAc}{OqAs}sin(\theta) + 1}{\left(\frac{AiAc}{AqAs}\right)^2 + 2\frac{AiAc}{AqAs}cos(\theta) + 1}}$$

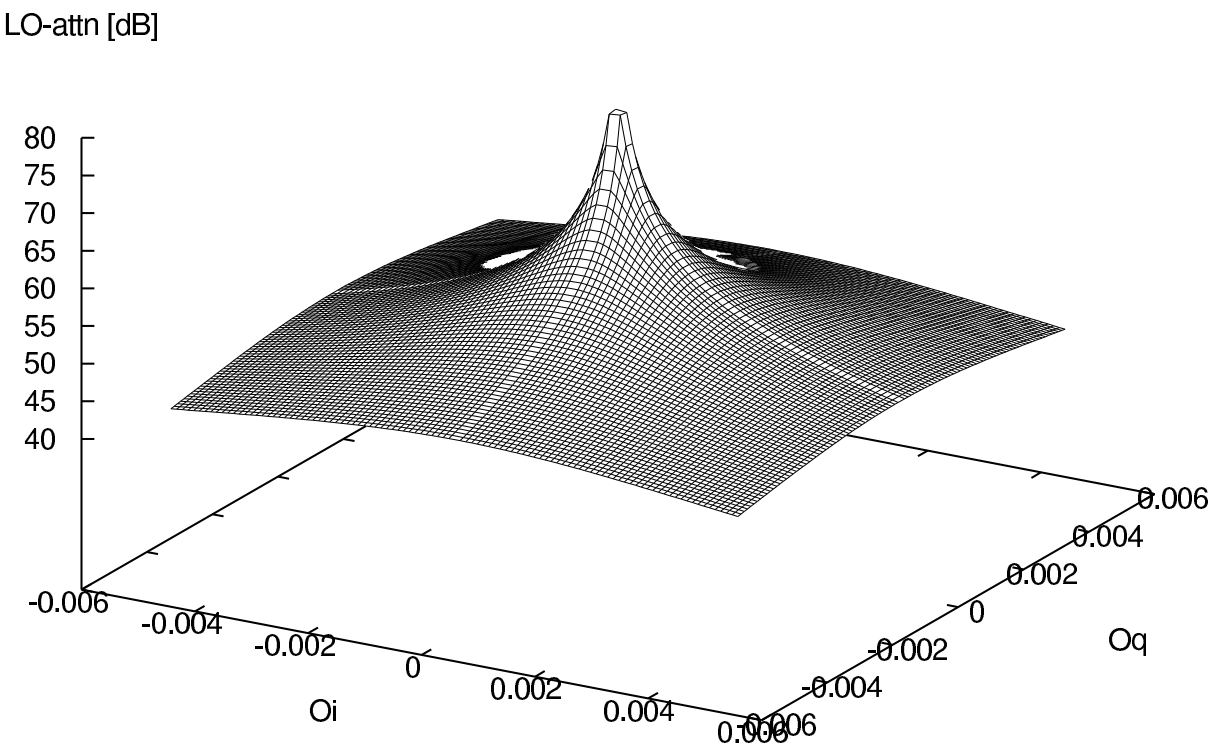


Figure 2.5: LO attenuation as a function of offset voltages.

Apparently, application of the first-order model offset factors (Oi, Oq, Oc, Os) adds LO and BB leakage to quadrature modulator output (2.10), while the previously defined IRR expression (2.7) still holds if following substitutions are made: $\Delta\mathrm{A} = (\mathrm{A_i A_c})/(\mathrm{A_q A_s})$ and $\Delta\phi = \theta$. For transmitter applications, LO leakage lies close to the desired tone and should be minimized, while any tones at (baseband) signal frequencies are filtered by DC-blocks. Interestingly, the high-frequency LO path offsets Oc and Os only show in the baseband and DC-components, while the baseband offsets Oi and Oq induce LO leakage to the output.

To minimize LO leakage, the offsets Oi and Oq should be kept as low as possible, or they can be utilized as tuning voltages [33] to null LO leakage and mirror signal (image tone) altogether. This is illustrated by the graph in Fig. 2.5, where LO attenuation values have been plotted as a function of Oi and Oq. LO attenuation is defined as the inverse of LO rejection from (2.11), and it has been used to improve the readability of the produced graph. The data has been plotted at 100 points per axis for:

$$\begin{aligned} (Oi, Oq) \;&\in\; (-0.005 \ldots 0.005) \\ A_i &= A_q = 1, \\ A_c &= 1.0116,\; A_s = 1 \text{ and } \theta = 0.937^\circ \end{aligned} \tag{2.12}$$

The offset values correspond to a real offset in $\pm 5\mathrm{mV}$ with 1-V signal amplitudes fed to the system shown in Fig. 2.4, and other coefficients define system IRR as -40 dBc with no baseband

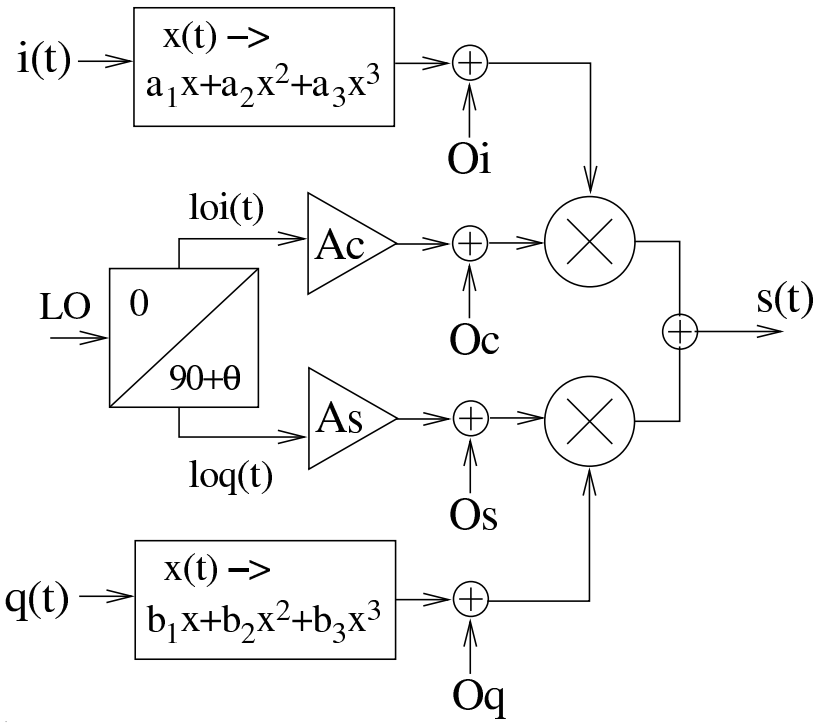


Figure 2.6: A quadrature modulator model with third-order non-linearities.

gain error. Since infinite LO attenuation is predicted by (2.11) at the coordinate origin, zero has been replaced by ± 0.0001 to give a maximum attenuation of 77 dB. Correspondingly, the minimum attenuation shown is 43 dB, and this value will be achieved at the coordinate extremes ± 0.005.

Thus, the application of the offset voltages to tune out LO leakage is clear, i.e. in the event of physical offset voltages at $\mathrm{Oi} = 0.0025$, $\mathrm{Oq} = -0.0025$, the system can be tuned from the 49 dB attenuation towards infinite attenuation by decreasing Oi and by increasing Oq towards zero. An iterative approach has to be applied in order to determine the correct direction for each tuning, but the principle of LO leakage nulling is well established by Figs. 2.4-2.5 and by (2.11). The possibility of nulling the unwanted sideband is not as clear, however, since the offset terms Oi and Oq are not explicitly shown in (2.11). The dc-offsets might affect IRR values through setting the input transistor/device bias points and thereby their gain coefficients $\mathrm{A_{i,q,s,c}}$ values, but the issue will not be pursued further as it is implementation-dependent.

Additionally, further quantification of the first-order model results is not meaningful, since in any practical direct-conversion quadrature modulator non-linearities produce a multitude of spurious tones in the near vicinity and further from the desired tone. Such distortion-spread energy folds on most output tones (also on the desired USB) and creates a multitude of new tones. In practical communication systems this non-linear circuit behavior causes spectral splatter, which raises noise level and/or blocks adjacent channel communications. Therefore, the next subsection will describe quadrature modulator operation in the presence of distortion.

2.2.2 Operation in the presence of distortion

In [34] the power series representation of non-linear circuits is deemed valid for small signal variations around the bias point, i.e. at distortion levels $-30\mathrm{dBc}$ below the desired tone. Admittedly, the Volterra-series modeling [35] produces fundamentally more correct results as it includes phase-information as well, but the resulting complex expressions are not applicable for

extracting qualitative information of system performance. Complemented with the dc offset factor a_0 to represent any memoryless non-linear system transfer function [28], the power series representation for a real circuit output y(t) can be given as:

$$y(t) \;=\; a_0 \;+\; a_1\, x(t) \;+\; a_2\, x^2(t) \;+\; a_3\, x^3(t) \;+\; \ldots \tag{2.13}$$

The application of a sinusoid as an input x(t) to such a system gives rise to a vast multitude of tones. To avoid cluttered equations, and since higher order series coefficients diminish rapidly, non-linearities have been limited up to third order terms. This results in the quadrature modulator model shown in Fig. 2.6, where the baseband input co-efficients shown in Fig. 2.4 have been replaced by two third-order polynomials with either positive or negative real coefficients $a_{1,2,3}$ and $b_{1,2,3}$, and where the offset factors Oi and Oq replace the dc factor a_0 in (2.13). Since baseband distortion has now been modeled, it is appropriate to re-define i- and q-signaling to include signal amplitude A as in:

$$\begin{aligned} i(t) \;&=\; A\, cos(\omega_{\mathrm{BB}}\, t) \\ q(t) \;&=\; A\, cos(\omega_{\mathrm{BB}}\, t \;+\; 90^{\circ}) \;=\; -A\, sin(\omega_{\mathrm{BB}}\, t) \end{aligned} \tag{2.14}$$

After the application of the re-defined baseband signaling the resulting 30-term expression for the quadrature modulator output is given as:

$$\begin{aligned} s(t) \;=& cos\left((\omega_{\mathrm{LO}} \pm \omega_{\mathrm{BB}})\; t\right) \\ & \left[\pm As\left(\frac{1}{2}b_1\, A \;+\; \frac{3}{8}b_3\, A^3\right)\; cos(\theta) \;+\; \frac{a_1\, A\, Ac}{2} \;+\; \frac{3\, a_3\, A^3\, Ac}{8}\right] \\ +\; & sin\left((\omega_{\mathrm{LO}} \pm \omega_{\mathrm{BB}})\; t\right) \\ & \left[\mp As\left(\frac{1}{2}b_1\, A \;+\; \frac{3}{8}b_3\, A^3\right)\; sin(\theta)\right] \\ +\; & cos\left(\omega_{\mathrm{LO}}\, t\right)\left[\left(Oq\, As \;+\; \frac{1}{2}b_2\, A^2\, As\right)\; sin(\theta) \;+\; Oi\, Ac \;+\; \frac{a_2\, A^2\, Ac}{2}\right] \\ +\; & sin\left(\omega_{\mathrm{LO}}\, t\right)\left[\left(Oq\, As \;+\; \frac{1}{2}b_2\, A^2\, As\right)\; cos(\theta)\right] \\ +\; & cos\left((\omega_{\mathrm{LO}} \pm 2\omega_{\mathrm{BB}})\, t\right)\left[-\frac{1}{4}b_2\, A^2\, As \cdot sin(\theta) + \frac{a_2\, A^2\, Ac}{4}\right] \\ +\; & sin\left((\omega_{\mathrm{LO}} \pm 2\omega_{\mathrm{BB}})\, t\right)\left[-\frac{1}{4}b_2\, A^2\, As \cdot cos(\theta)\right] \\ +\; & cos\left((\omega_{\mathrm{LO}} \pm 3\omega_{\mathrm{BB}})\, t\right)\left[\mp\frac{1}{8}b_3\, A^3\, As \cdot cos(\theta) + \frac{a_3\, A^3\, Ac}{8}\right] \\ +\; & sin\left((\omega_{\mathrm{LO}} \pm 3\omega_{\mathrm{BB}})\, t\right)\left[\pm\frac{1}{8}b_3\, A^3\, As \cdot sin(\theta)\right] \end{aligned} \tag{2.15}$$

When (2.15) is compared to (2.9), it is apparent that distortion re-divides output power by folding it on USB, LSB, and LO tones, and by creating up-converted second ($\pm$2ND) and third-order ($\pm$3RD) harmonics at $\omega_{\mathrm{LO}} \pm 2\omega_{\mathrm{BB}}$ and $\omega_{\mathrm{LO}} \pm 3\omega_{\mathrm{BB}}$, respectively. In fact, the second-order coefficients $\{a_2,\ b_2\}$ factor LO and 2ND to the quadrature modulator output, while the third-order coefficients $\{a_3,\ b_3\}$ fold power on 3RD, USB and LSB tones. The $\pm$ and $\mp$ notation has been used to make a distinction between tones such as USB and LSB, which only differ in

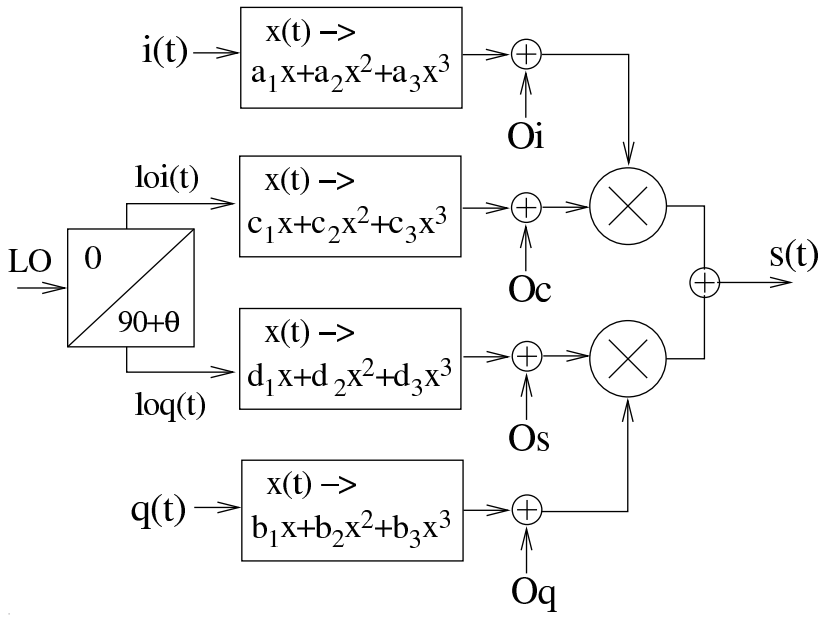


Figure 2.7: Complete quadrature modulator model with third-order non-linearities and offsets.

the polarity of their expressions. Furthermore, the baseband leakage terms $\mathrm{N} * \omega_{\mathrm{BB}}$ (and thereby the offset terms Oc and Os) and higher order LO tones (2*ω_{LO}, 3*ω_{LO}) have been expunged from (2.15) in order to develop a compact expression for quadrature modulator output.

However, for a complete model of non-linear circuit behavior, it is prudent to apply the power-series distortion model in the LO path, too. This makes it possible to develop the quadrature modulator model shown in Fig. 2.6 to the one in Fig. 2.7, where the LO path input coefficients shown in Fig. 2.4 have been replaced by two third-order polynomials with either positive or negative real coefficients $c_{1,2,3}$ and $d_{1,2,3}$, and where the offset factors Oc and Os replace the dc factor a_0 in (2.13). Since LO path distortion has now been modeled, it is appropriate to re-define the loi and loq signals in a manner similar to (2.14) so as to include local signal amplitude B:

$$\begin{aligned} loi(t) &= B\,cos(\omega_{\mathrm{LO}}\,t) \\ loq(t) &= B\,cos(\omega_{\mathrm{LO}}\,t + 90^{\circ}) = -B\,sin(\omega_{\mathrm{LO}}\,t) \end{aligned} \tag{2.16}$$

After application of the re-defined signaling (2.14) and (2.16) the resulting 60-term expression for the quadrature modulator output is given as:

$$\begin{aligned} s(t) =& cos\left((\omega_{\mathrm{LO}} \pm \omega_{\mathrm{BB}})\,t\right) \\ & \left[\pm\left(\frac{b_1\,A\,d_1\,B}{2} + \frac{3\,b_1\,A\,d_3\,B^3}{8} + \frac{3\,b_3\,A^3\,d_1\,B}{8} + \frac{9\,b_3\,A^3\,d_3\,B^3}{32}\right)\cos(\theta)\right. \\ & \left. + \left(\frac{a_1\,A\,c_1\,B}{2} + \frac{3\,a_1\,A\,c_3\,B^3}{8} + \frac{3\,a_3\,A^3\,c_1\,B}{8} + \frac{9\,a_3\,A^3\,c_3\,B^3}{32}\right)\right] \\ & + sin\left((\omega_{\mathrm{LO}} \pm \omega_{\mathrm{BB}})\,t\right) \\ & \left[\mp\left(\frac{b_1\,A\,d_1\,B}{2} + \frac{3\,b_1\,A\,d_3\,B^3}{8} + \frac{3\,b_3\,A^3\,d_1\,B}{8} + \frac{9\,b_3\,A^3\,d_3\,B^3}{32}\right)\sin(\theta)\right] \\ & + cos\left(\omega_{\mathrm{LO}}\,t\right) \\ & \left[\left(d_1\,B\,Oq + \frac{d_1\,B\,b_2\,A^2}{2} + \frac{3\,d_3\,B^3\,Oq}{4} + \frac{3\,d_3\,B^3\,b_2\,A^2}{8}\right)\sin(\theta)\right. \end{aligned}$$

$$
\begin{aligned}
&+ c_1\,B\,Oi + \frac{c_1\,B\,a_2\,A^2}{2} + \frac{3\,c_3\,B^3\,Oi}{4} + \frac{3\,c_3\,B^3\,a_2\,A^2}{8}\Bigg] \\
&+ \mathit{sin}\,(\omega_{\mathrm{LO}}\,t) \\
&\quad \left[\left(d_1\,B\,Oq + \frac{d_1\,B\,b_2\,A^2}{2} + \frac{3\,d_3\,B^3\,Oq}{4} + \frac{3\,d_3\,B^3\,b_2\,A^2}{8}\right)\right]\cos(\theta) \qquad (2.17) \\
&+ \mathit{cos}\,((\omega_{\mathrm{LO}} \pm 2\omega_{\mathrm{BB}})\,t) \\
&\quad \left[-\left(\frac{b_2\,A^2\,d_1\,B}{4} + \frac{3\,b_2\,A^2\,d_3\,B^3}{16}\right)\sin(\theta) + \frac{a_2\,A^2\,c_1\,B}{4} + \frac{3\,a_2\,A^2\,c_3\,B^3}{16}\right] \\
&+ \mathit{sin}\,((\omega_{\mathrm{LO}} \pm 2\omega_{\mathrm{BB}})\,t) \\
&\quad \left[-\left(\frac{b_2\,A^2\,d_1\,B}{4} + \frac{3\,b_2\,A^2\,d_3\,B^3}{16}\right)\cos(\theta)\right] \\
&+ \mathit{cos}\,((\omega_{\mathrm{LO}} \pm 3\omega_{\mathrm{BB}})\,t) \\
&\quad \left[\mp\left(\frac{b_3\,A^3\,d_1\,B}{8} + \frac{3\,b_3\,A^3\,d_3\,B^3}{32}\right)\cos(\theta) + \frac{a_3\,A^3\,c_1\,B}{8} + \frac{3\,a_3\,A^3\,c_3\,B^3}{32}\right] \\
&+ \mathit{sin}\,((\omega_{\mathrm{LO}} \pm 3\omega_{\mathrm{BB}})\,t) \\
&\quad \left[\pm\left(\frac{b_3\,A^3\,d_1\,B}{8} + \frac{3\,b_3\,A^3\,d_3\,B^3}{32}\right)\sin(\theta)\right]
\end{aligned}
$$

Again, the developed s(t) expression yields qualitative information on the propagation of different distortion components through the quadrature modulator in Fig. 2.7. The detection of model coefficients $(a,b,c,d)_{1-3}$ from (2.17) reveals that LO chain distortion coefficients $c_{2,3}$ and $d_{2,3}$ fold mixing products on the USB, LSB, and LO tones in a manner analogous to the factors $a_{2,3}$ and $b_{2,3}$ in (2.15). The coefficients and offsets are distributed per tone as: $a_{1,3}$, $b_{1,3}$, $c_{1,3}$, $d_{1,3}$ for USB and LSB; a_2, b_2, $c_{1,3}$, and $d_{1,3}$ fold on LO and 2ND; and a_3, b_3, $c_{1,3}$, and $d_{1,3}$ fold on 3RD. The offsets Oi and Oq again produce LO leakage, while Oc and Os show up at lower frequencies as before. No assessment of which coefficients have an expanding or subtracting effect on each tone will be performed, since solving (2.17) for different tone magnitudes produces results that are too cluttered. For example, 34 terms need to be summed and have their square root taken in order to calculate USB magnitude. Therefore, the next subsection will first simplify the quadrature modulator model shown in Fig. 2.7, then quantify by choosing numerical values for the remaining coefficients.

2.2.3 The simplified distortion model

Since the LO path second-order coefficients (c_2,d_2) and offsets (Oc, Os) do not transmit to quadrature modulator output s(t) (2.17), these factors can be omitted from the circuit model. Further, it is assumed that baseband mismatch can be sufficiently described by the offset factors Oi and Oq, and by a common-mode gain factor CM, which multiplies $a_{1,2,3}$ to replace $b_{1,2,3}$. This approach assumes that no significant deviation occurs in the higher-order coefficients $a_{2,3}$ and $b_{2,3}$ as a result of parasitics, which is usually well justified at the relatively low baseband signal frequencies. To test whether a corresponding common-mode gain factor could also be used in the LO path, the $d_{1,3}$ factors have been replaced with:

$$
\begin{bmatrix} d_1 \\ d_3 \end{bmatrix} = \begin{bmatrix} adBx1\,c_1 \\ adBx3\,c_3 \end{bmatrix}, \text{where } (\text{adBx1,adBx3}) \in \Re^{+} \qquad (2.18)
$$

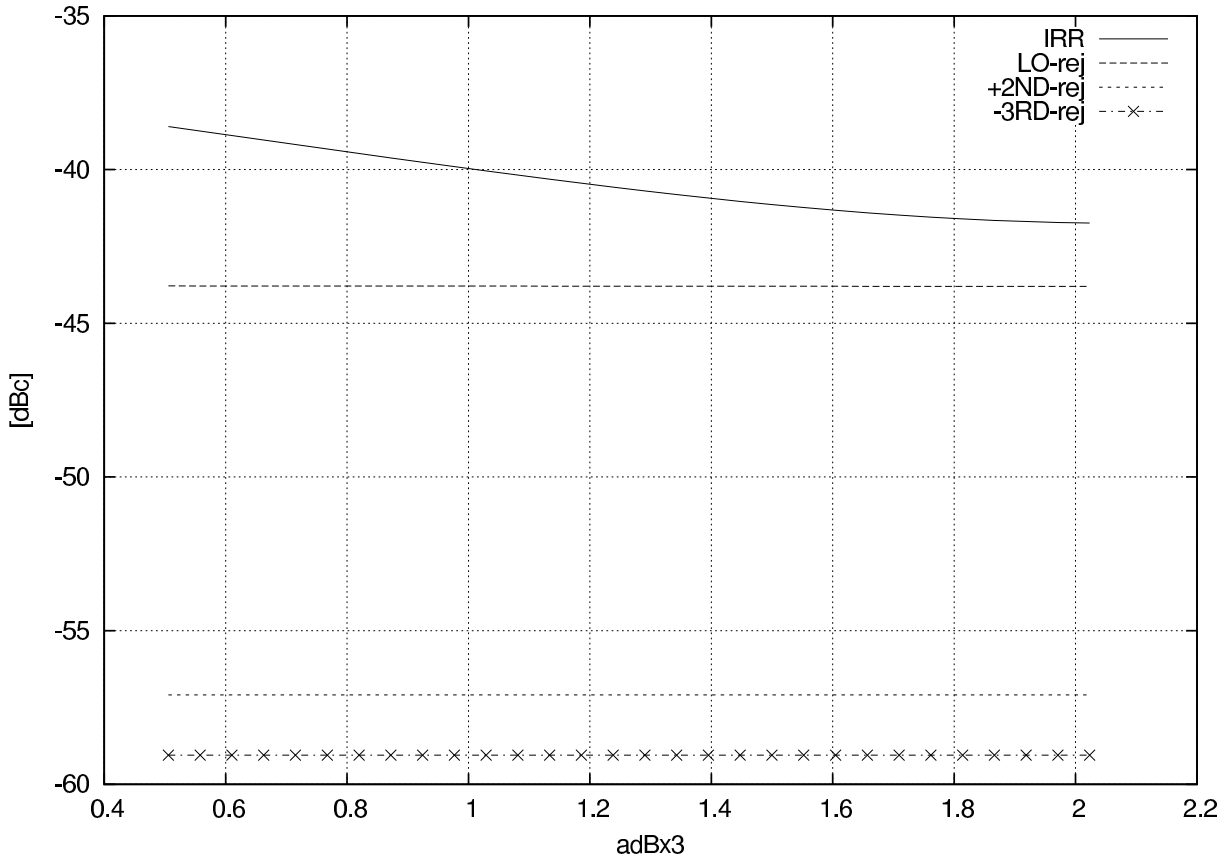


Figure 2.8: Spurious rejections vs. 3rd-harmonic coefficient adBx3.

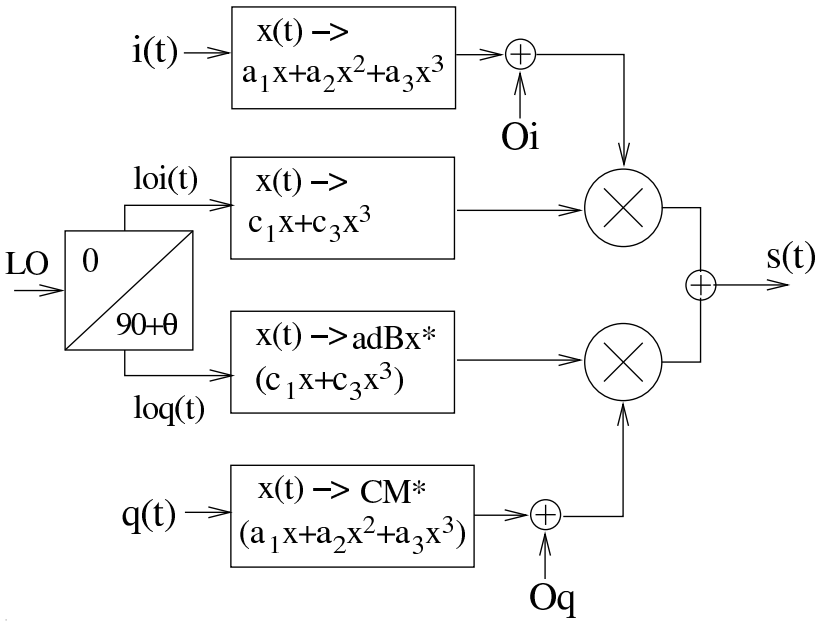


Figure 2.9: The simplified quadrature modulator model.

By varying the third-order adBx3 parameter in the range of $(0.5:2) \times \mathrm{adBx1}$ and through observation of changes in tone magnitude, it is now possible to determine whether a finite deviation of adBx3 from adBx1 has a significant effect on system performance. To represent a typical quadrature modulator, the system coefficients and signal amplitudes have been set as:

$$\begin{aligned} A = 0.5,\ CM = 1,\ Oi = 1e-3,\ Oq = 1.5e-3 \\ a_1 = 1,\ a_2 = |a_1| \cdot 0.79433 \cdot 10^{-2},\ a_3 = -a_1 \cdot 1.77828 \cdot 10^{-2} \\ B = 1,\ c_1 = 1,\ c_3 = -c_1 \cdot 0.014125 \\ \Delta A \equiv adBx1 = 0.1dB \triangleq 1.0116, \text{ and } \theta = 0.937^\circ \end{aligned} \tag{2.19}$$

This corresponds to a modulator with an ideally balanced baseband stage with -42 dBc and -35 dBc of 2ND and 3RD harmonic rejections, respectively; the LO path 3RD harmonic rejection is set at -37 dBc, while an LO path imbalance of 0.1 dB/0.937° sets a nominal IRR=-40 dBc.

After evaluation of (2.17) with the given coefficients, the rejections for the four highest spurious tones are plotted in Fig. 2.8. The labeling (IRR, LO-rej, 2ND-rej, 3RD-rej) corresponds to the rejections of the image, LO, and higher second and lower third harmonic products, respectively. The depicted IRR values vary from -42 dBc to -39 dBc, while the other tones remain constant. In fact, IRR variation leaps from 1 dB (B=0.5) to 7 dB for the LO signal amplitude B=2, but as the tested ±6 dB adBx3 deviation from adBx1 is much larger than could be expected for circuits realized on the same RFIC, both adBx1 and adBx3 can be replaced with a single positive real-parameter adBx.

The quadrature modulator model for this is shown in Fig. 2.9, and the resulting 60-term expression for its output in (LO-3RD…LO+3RD) is given by:

$$\begin{aligned} s(t) \ =& \cos\left((\omega_{\mathrm{LO}} \pm \omega_{\mathrm{BB}})\, t\right) \\ & \left[\pm\frac{1}{32}\, AB\left(9\, a_3\, A^2 c_3\, B^2 + 12\, a_1\, c_3\, B^2 + 16\, a_1\, c_1 + 12\, a_3\, A^2 c_1\right) CM adBx\, \cos(\theta)\right. \\ & \left. + \frac{1}{32}\, AB\left(9\, a_3\, A^2 c_3\, B^2 + 12\, a_1\, c_3\, B^2 + 16\, a_1\, c_1 + 12\, a_3\, A^2 c_1\right)\right] \\ & + \sin\left((\omega_{\mathrm{LO}} \pm \omega_{\mathrm{BB}})\, t\right) \\ & \left[\mp\frac{1}{32}\, BCM\, AadBx\, \sin(\theta)\left(9\, a_3\, A^2 c_3\, B^2 + 12\, a_1\, c_3\, B^2 + 16\, a_1\, c_1 + 12\, a_3\, A^2 c_1\right)\right] \\ & + \cos\left(\omega_{\mathrm{LO}}\, t\right) \\ & \left[\frac{1}{8}\, B\, adBx\left(6\, Oq\, c_3\ B^2 + 8\, Oq\, c_1\ + 3\, CM\, a_2\, A^2 c_3\, B^2 + 4\, CM\, a_2\, A^2 c_1\right)\sin(\theta)\right. \\ & \left. + \frac{1}{8}\, B\left(8\, Oi\, c_1 + 6\, Oi\, c_3\, B^2 + 4\, a_2\, A^2 c_1 + 3\, a_2\, A^2 c_3\, B^2\right)\right] \\ & + \sin\left(\omega_{\mathrm{LO}}\, t\right) \\ & \left[\frac{1}{8}\, adBx\, B\cos(\theta)\left(6\, Oq\, c_3\, B^2 + 4\, CM\, a_2\, A^2 c_1 + 3\, CM\, a_2\, A^2 c_3\, B^2 + 8\, Oq\, c_1\right)\right] \\ & + \cos\left((\omega_{\mathrm{LO}} \pm 2\omega_{\mathrm{BB}})\, t\right) \\ & \left[-\frac{1}{16}\, a_2\, B\, A^2\, CM\, adBx\left(4\, c_1\ + 3\, c_3\, B^2\right)\sin(\theta)\right. \\ & \left. + \frac{1}{16}\, Ba_2\, A^2\left(3\, c_3\, B^2 + 4\, c_1\right)\right] \end{aligned} \tag{2.20}$$

$$
\begin{aligned}
&+\ sin\left(\left(\omega_{\mathrm{LO}} \pm 2\omega_{\mathrm{BB}}\right) t\right) \\
&\qquad \left[-\frac{1}{16}\, a_2\, A^2\, CM\, adBx\, B \cos\left(\theta\right) \left(4\, c_1 + 3\, c_3\, B^2\right)\right] \\
&+\ cos\left(\left(\omega_{\mathrm{LO}} \pm 3\omega_{\mathrm{BB}}\right) t\right) \\
&\qquad \left[\mp\frac{1}{32}\, a_3\, A^3 B\, CM\, adBx\, \left(4\, c_1 + 3\, c_3\, B^2\right) \cos\left(\theta\right) + \frac{1}{32}\, a_3\, A^3 B\, \left(3\, c_3\, B^2 + 4\, c_1\right)\right] \\
&+\ sin\left(\left(\omega_{\mathrm{LO}} \pm 3\omega_{\mathrm{BB}}\right) t\right) \\
&\qquad \left[\pm\frac{1}{32}\, CM\, a_3\, A^3 adBx\, B \sin\left(\theta\right) \left(4\, c_1 + 3\, c_3\, B^2\right)\right]
\end{aligned}
$$

Thus, although evaluation of the resulting quadrature modulator model in Fig. 2.9 will still produce a 60-term expression for s(t), expressions for USB, LSB, 2ND and 3RD tone magnitudes have now become quite un-cluttered; only LO magnitude has 10 terms whose square root needs to be taken. Solving (2.20) for individual tones results in:

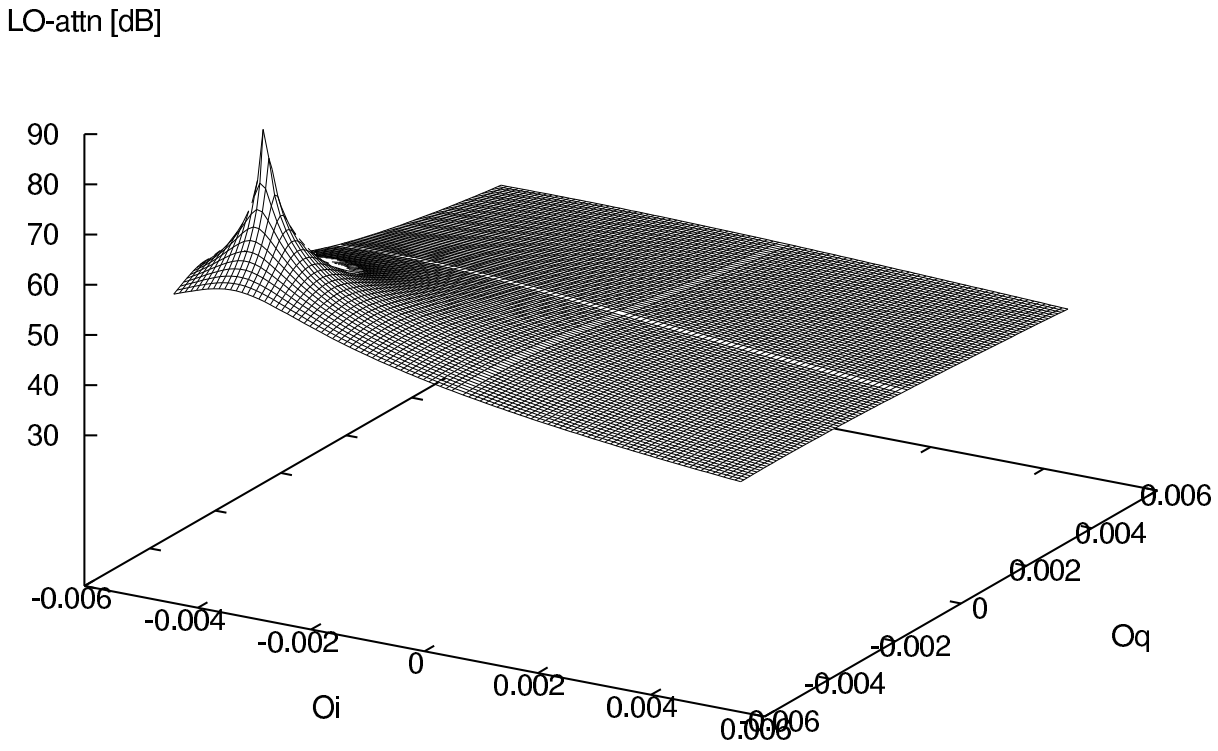
$$
\begin{aligned}
USB &= \frac{1}{32}\, \left(4\, c_1\, B + 3\, c_3\, B^3\right) \left(4\, a_1\, A + 3\, a_3\, A^3\right) \sqrt{CM^2 adBx^2 + 2\, CM\, adBx\, \cos\left(\theta\right) + 1} \\
LSB &= \frac{1}{32}\, \left(4\, c_1\, B + 3\, c_3\, B^3\right) \left(4\, a_1\, A + 3\, a_3\, A^3\right) \sqrt{CM^2 adBx^2 - 2\, CM\, adBx\, \cos\left(\theta\right) + 1} \\
LO &= \frac{1}{8}\, \left(4\, c_1\, B + 3\, c_3\, B^3\right) \\
&\qquad \sqrt{2\, adBx\, \left({a_2}^2\, A^4\, CM + 2\, a_2\, A^2\, Oq + 4\, Oi\, Oq + 2\, Oi\, CM\, a_2\, A^2\right) \cdot} \\
&\qquad \sqrt{\sin\theta + \left(2\, Oi\, +\, a_2\, A^2\right)^2 + adBx^2\, \left(2\, Oq + CM\, a_2\, A^2\right)^2} \\
\pm 2ND &= \frac{1}{16}\, a_2\, A^2\, \left(4\, c_1\, B + 3\, c_3\, B^3\right) \sqrt{CM^2 adBx^2 - 2\, CM\, adBx\, \sin\left(\theta\right) + 1} \\
\pm 3RD &= \frac{1}{32}\, a_3\, A^3\, \left(4\, c_1\, B + 3\, c_3\, B^3\right) \sqrt{CM^2 adBx^2 \mp 2\, CM\, adBx\, \cos\left(\theta\right) + 1}
\end{aligned}
\tag{2.21}
$$

which gives a definition for IRR as:

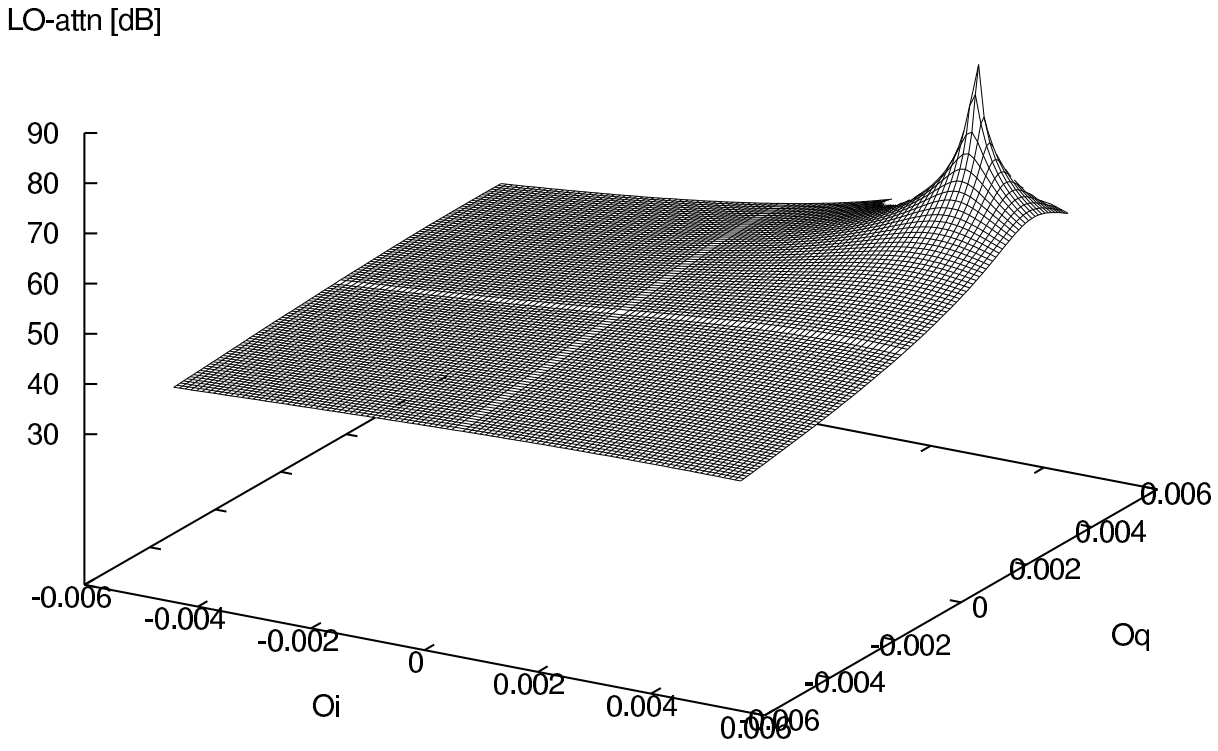
$$
IRR = \sqrt{\frac{CM^2 adBx^2 - 2\, CM\, adBx\, \cos\left(\theta\right) + 1}{CM^2 adBx^2 + 2\, CM\, adBx\, \cos\left(\theta\right) + 1}} \tag{2.22}
$$

A comparison of (2.22) with (2.7) and (2.11) suggests that the product of factors CM and adBx combines to form the amplitude error ΔA in (2.7). Therefore, the rest of the spurious tones could be viewed as given per a particular IRR performance, and these are now defined as:

$$
\begin{aligned}
LO - rej &= \frac{4}{4a_1\, A + 3a_3\, A^3} \cdot \\
&\qquad \sqrt{\frac{2\, adBx\, \left({a_2}^2\, A^4\, CM + 2\, a_2\, A^2\, Oq + 4\, Oi\, Oq + 2\, Oi\, CM\, a_2\, A^2\right) \cdot}{\sin\theta + \left(2\, Oi\, +\, a_2\, A^2\right)^2 + adBx^2\, \left(2\, Oq + CM\, a_2\, A^2\right)^2}} \\
&\qquad \sqrt{\frac{\sin\theta + \left(2\, Oi\, +\, a_2\, A^2\right)^2 + adBx^2\, \left(2\, Oq + CM\, a_2\, A^2\right)^2}{CM^2 adBx^2 + 2\, CM\, adBx\, \cos\left(\theta\right) + 1}} \\
\pm 2ND - rej &= \frac{2a_2\, A}{4a_1 + 3a_3\, A^2} \sqrt{\frac{CM^2 adBx^2 - 2\, CM\, adBx\, \sin\left(\theta\right) + 1}{CM^2 adBx^2 + 2\, CM\, adBx\, \cos\left(\theta\right) + 1}} \\
-3RD - rej &= \frac{a_3\, A^2}{3a_3\, A^2 + 4a_1} \\
+3RD - rej &= -3RD - rej\, \cdot\, IRR
\end{aligned}
\tag{2.23}
$$

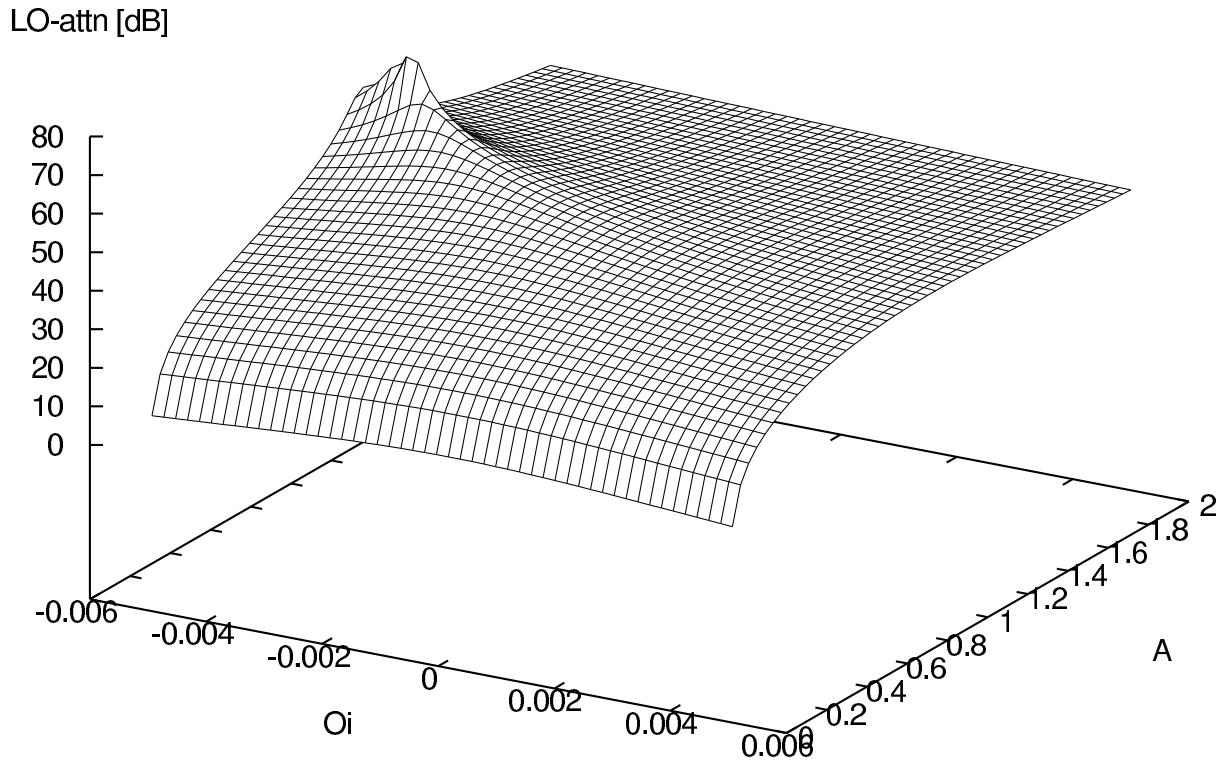


(a)

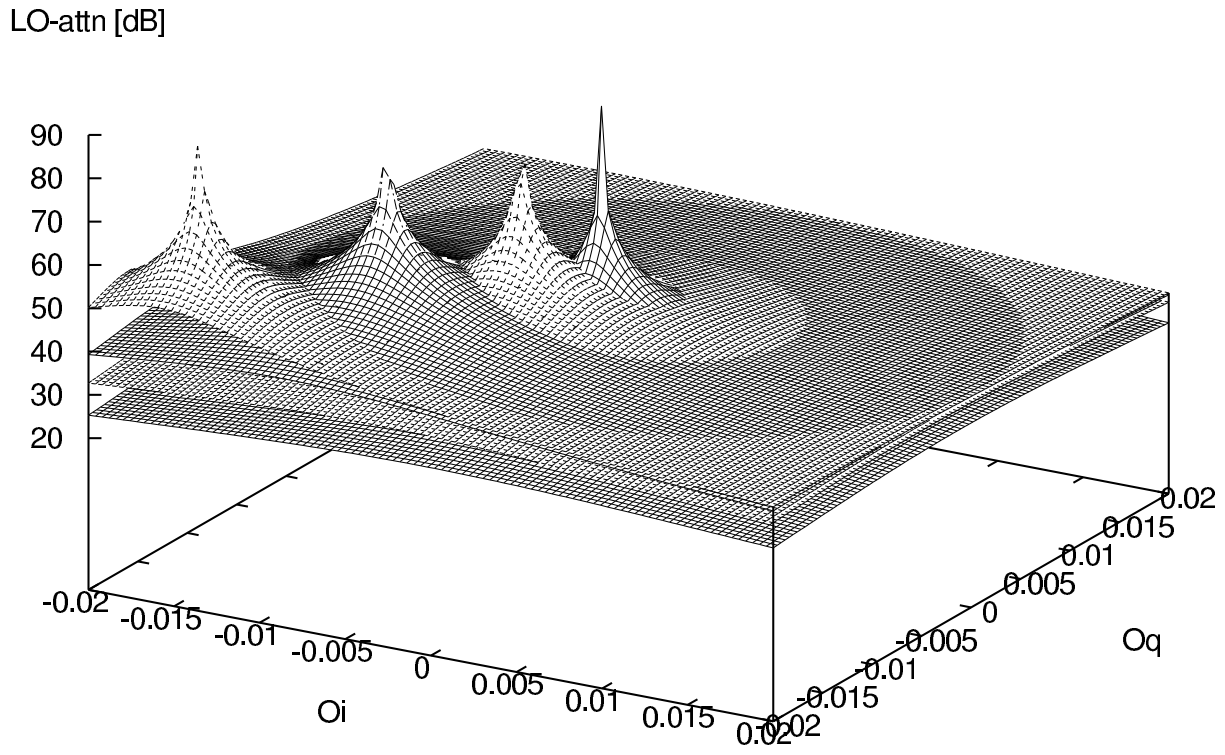


(b)

Figure 2.10: Circuit non-linearities move infinite LO attenuation a) from $(\mathrm{Oi}, \mathrm{Oq}) = (0, 0)$ to (-0.004,-0.004) when a_2>0, and b) from $(\mathrm{Oi}, \mathrm{Oq}) = (0, 0)$ to (0.004,0.004) when a_2<0.



(a)



(b)

Figure 2.11: LO attenuation dependence on signal amplitude A for a) different Oi-values while Oq=-0.004, and for b) four A-values in 0.5:2.

The LO-rej definition in (2.23) shows the importance of including the second-order coefficient a_2 in the quadrature modulator model, as it reveals LO leakage dependence on baseband signal amplitude A. Surprisingly, LO leakage does not depend on LO signal amplitude B, since B is canceled out during the division of the LO by the USB tone, as defined in (2.21). To test what practical implications the a_2 factor has, the defined LO-rej expression has been numerically evaluated using the IRR=-40 dBc case in (2.19) for a signal amplitude of A=1. Comparison of the resulting LO attenuation vs. offset factor Oi and Oq plots in Fig. 2.10 to Fig. 2.5 indicates that distortion moves the maximum available LO attenuation location but does not necessarily cancel it. In fact, distortion maxima move diagonally further from origo in direct relation to increasing second-order distortion, but only the nominal $a_2 = -42\mathrm{dBc}$ case is plotted in Fig. 2.10 to demonstrate the effect of a_2 polarity. Both negative and positive a_2 values need to be evaluated, since with perfect differential signaling even-order tones cancel. Therefore, the a_2 factor is the result of circuit mismatches and its polarity cannot be predicted with any certainty.

The dependence of LO attenuation on signal amplitude A is depicted in Figs. 2.11(a)-2.11(b) for the nominal IRR=-40 dBc quadrature modulator in (2.19). Fig. 2.11(a) predicts non-existent LO attenuation for low signal amplitudes, while Fig. 2.11(b) shows LO attenuation maxima diagonal loci towards $\mathrm{Oi} = \mathrm{Oq} = -0.02$ for four A-values in increasing order from 0.5 to 2. The predicted dependence on signal amplitude A makes the re-calibration of possible tuning circuitry mandatory each time the amplitude changes, but environmental and biasing changes, i.e. device state changes, also necessitate re-tuning. The physical explanation for such intensive tuning requirements is the fact that any change in second-order distortion causes an LO attenuation locus similar to the one shown in Fig. 2.11(b).

A comparison of the upper (+3RD) and lower (-3RD) third harmonic rejections in (2.23) gives an explicit explanation of the measured imbalances between the two tones, since IRR values are typically much lower than 3RD-rej values. In contrast to the second-order term, the polarity of the third-order coefficient a_3 is set as opposite to that of the circuit's linear gain factor a_1 in anticipation of compressive behavior with increasing signal amplitudes [28]. Compression of the signal, together with the transmitted noise, directly limits quadrature modulator performance in a linear transmitter by setting the dynamic range available for modulations. Quadrature modulator linearity is also directly related to transmitter efficiency, since it dictates the required power back-off from the PA's non-linear but more efficient region of operation. Therefore, the next section will apply the developed theory to describe the large signal, noise, and transmitted dynamic range of a quadrature modulator.

2.3 Quadrature modulator characteristics

A common test the performance of a quadrature modulator is the SSB test, in which the output spectrum is evaluated using real quadrature signaling. The spectrum should give a realistic view of the performance of the quadrature modulator in TX operation, and this will be discussed in the next subsection.

2.3.1 SSB performance

The evaluation of the individual tone magnitudes in (2.21) for the IRR=-40 dBc case (2.19) is straightforward and it gives the SSB spectrum shown in Fig. 2.12. Since the developed modeling does not include the frequency response of the quadrature modulator circuit blocks, the data are shown centered at a numeral LO of 2016.5, with the BB frequency set at 4. The spectrum confirms the predicted non-symmetry of 3RD-rej, but more importantly it correctly predicts the rise of the even-order 2ND and LO tones to within 10 dB of the LSB, yet the total imbalance

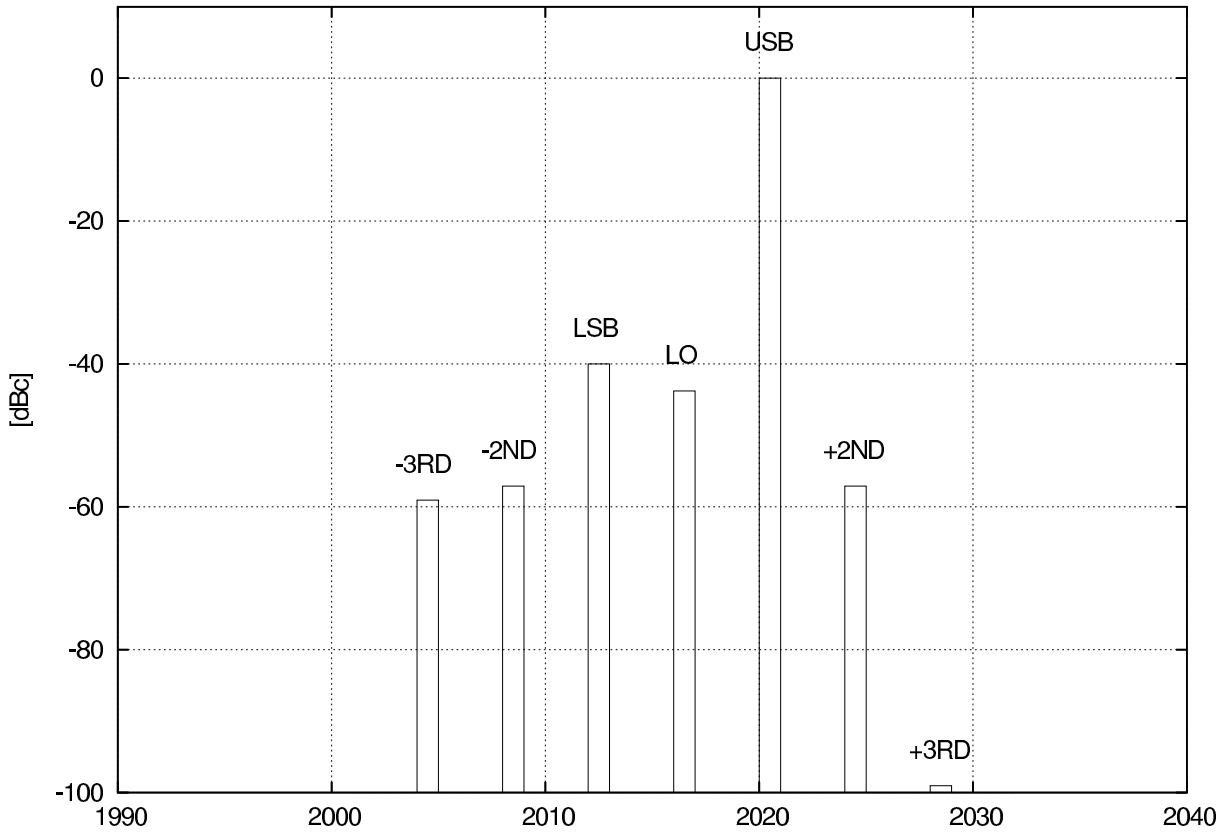


Figure 2.12: Output spectrum for the simplified IRR=-40 dBc IQ modulator model.

of the baseband and local signaling paths was defined as only 0.1 dB and 0.937°. Qualitatively, the modeled spectrum corresponds well with the measurements made for this work, and comparison of the depicted 2ND and 3RD harmonics gives a clear indication that OIP_3 alone is not a sufficient characteristic for quadrature modulator nonlinearity. Next, this work proceeds with OP_{1dB} and noise performance modeling, as these characteristics are needed for the definition of the available TDR performance. The derivation of the TDR concludes this section.

2.3.2 Calculation of OP_{1dB}

The definition of the transmitted dynamic range (TDR) as the relation of quadrature modulator output power at the 1 dB compression OP_{1dB} to its output-referred noise floor (N_{floor}) power, both integrated over the same bandwidth, requires re-examination of the developed simplified quadrature modulator model in order to obtain the relevant expressions for OP_{1dB} and N_{floor}. A graphical definition of OP_{1dB} using the defined USB expression (2.21) and numerical values for the IRR=-40 dBc case (2.19) is shown in Fig. 2.13, where straight horizontal and vertical lines mark the output- and input-referred 1 dB compression points on the y- and x-axes, respectively. For 250 data points the numerical values are OP_{1dB}=8.1638 dB and P_{1dB}=9.2369 dB.

In order to derive expressions for OP_{1dB} and P_{1dB}, a linear version of the defined USB-tone (2.21) is needed. In this way the frequency translation or mixing effect on quadrature modulator gain is included in the modeling. It is straightforward to derive such a linearized USB tone by setting the baseband non-linearity term a_3=0 in the original USB expression. Therefore, dividing

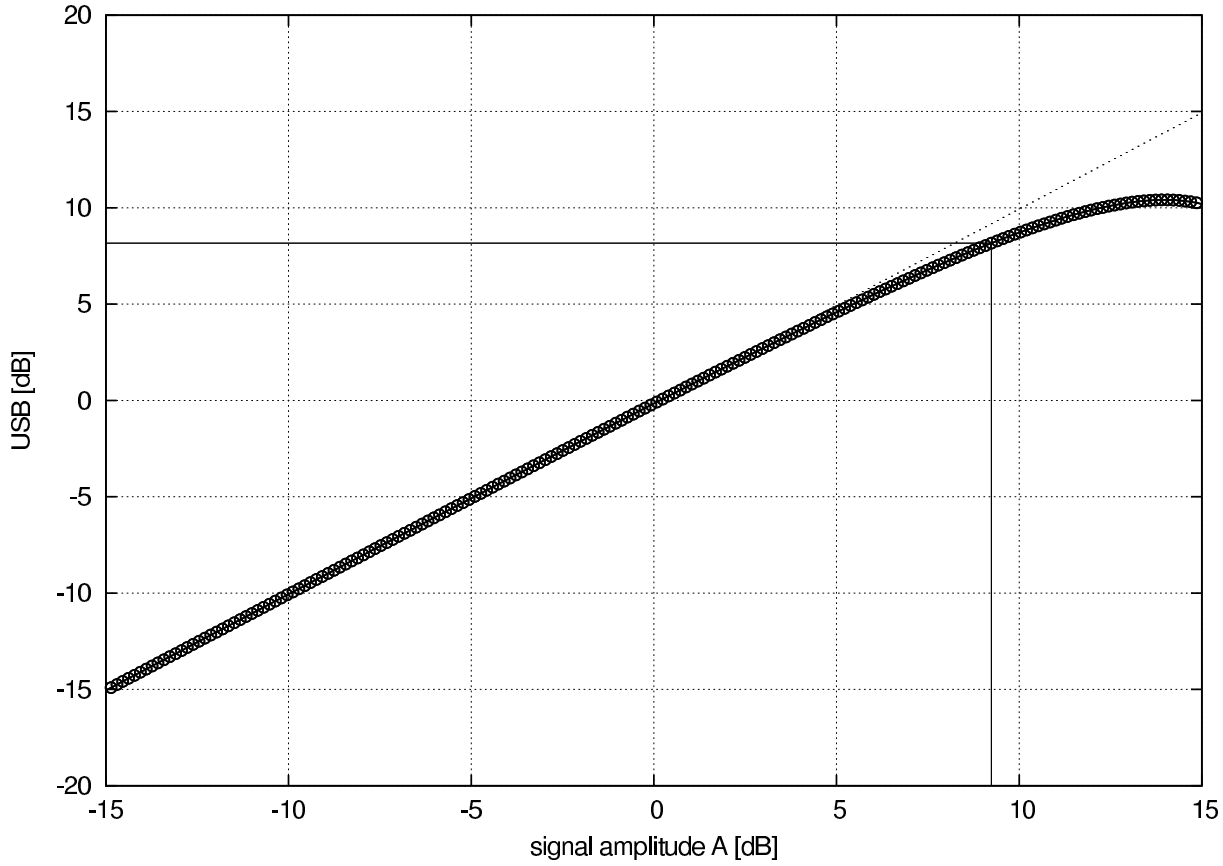


Figure 2.13: Derivation of $\mathrm{OP_{1dB}}$ for the simplified IRR=-40 dBc IQ modulator model.

the result by the original non-linear version of the USB and equating it with the numeral value 1.122, corresponding to the required +1 dB compression, results in:

$$\frac{4\,a_1}{4\,a_1 + 3\,a_3\,A^2} = 1.122 \tag{2.24}$$

Solving (2.24) for the input signal amplitude A and equating the result with $\mathrm{P_{1dB}}$ gives the desired input-referred 1 dB compression point as:

$$\mathrm{P_{1dB}} \;=\; \sqrt{0.145|\frac{a_1}{a_3}|} \tag{2.25}$$

The developed $\mathrm{P_{1dB}}$ can be used to define $\mathrm{OP_{1dB}}$ by replacing the input signal amplitude A in (2.21) with it to give the desired output-referred 1 dB compression point as:

$$\mathrm{OP_{1dB}} \;=\; \frac{1}{9}\left(4\,c_1\,B + 3\,c_3\,B^3\right)\left(a_1\,\mathrm{P_{1dB}}\right)\sqrt{CM^2 adBx^2 + 2\,CM\,adBx\,\cos\left(\theta\right) + 1} \tag{2.26}$$

Checking the developed equations (2.25-2.26) using the IRR=-40 dBc case (2.19) coefficients gives $\mathrm{OP_{1dB}}$ and $\mathrm{P_{1dB}}$ values as 8.0481 dB and 9.1137 dB, respectively. As these values lie within 0.1 dB of the corresponding graphically derived values, it is safe to say that the two models match. Incidentally, the developed $\mathrm{P_{1dB}}$ expression (2.25) is in agreement with the corresponding definition for amplifiers in [28], which, by analogy, indicates that the reference-defined relation for $\mathrm{IIP_3}$ and $\mathrm{P_{1dB}}$ should also be applicable to modulators. Therefore, the $\mathrm{P_{1dB}}$/$\mathrm{IIP_3}$

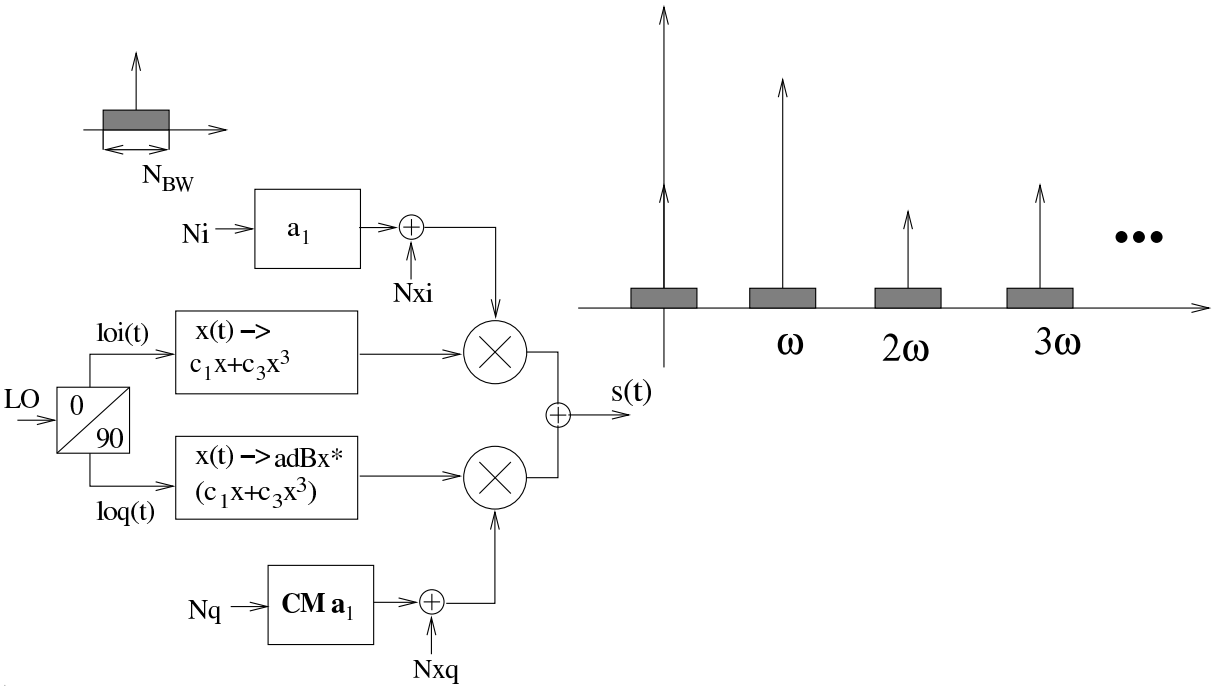


Figure 2.14: Noise up-conversion in a quadrature modulator from baseband (Ni, Nq) and internal (Nxi, Nxq) noise sources.

relation is repeated here for the sake of completeness, and since this work is concerned with transmitters, the output-referred OP_{1dB}/OIP_3 relation has also been given to give:

$$\mathrm{IIP_3} = \mathrm{P_{1dB}} + 9.6\,\mathrm{dB} \tag{2.27}$$

$$\mathrm{OIP_3} = \mathrm{OP_{1dB}} + 10.6\,\mathrm{dB} \tag{2.28}$$

The +1 dB difference between the 9.6 dB and 10.6 dB terms compensates for output signal compression. A somewhat different approach is needed to evaluate quadrature modulator operation in the presence of noise, but as noise sets a lower limit on available TDR, this will be discussed in the next subsection.

2.3.3 Operation in the presence of noise

System noise can be represented with un-correlated noise sources reduced at its input port [36], either as voltage and/or current noise sources. Noise powers over a given bandwidth (e.g. in dBm/Hz) can be summed to obtain the total noise from several un-correlated noise sources. Thus, the quadrature modulator power gain response to each independent noise source at its input will be estimated separately, and the output noise powers summed for an estimate of $\mathrm{N_{floor}}$ power.

To obtain the quadrature modulator noise response, four un-correlated noise sources (Ni, Nq, Nxi, Nxq) have been used to replace the i- and q-inputs and offsets Oi and Oq of the simplified modulator model in Fig. 2.9. The Ni and Nq noise sources represent noise at the mixer signal input ports, for example from a digital-to-analog (DA) converter or from a general 50 Ω source, while the Nxi and Nxq noise sources represent internal mixer noise. The resulting quadrature modulator noise model is shown in Fig. 2.14, where each input noise source is assumed to be upconverted as folded around LO harmonics, with a finite noise bandwidth $\mathrm{N_{BW}}$ as shown in Fig. 2.14; since infinite $\mathrm{N_{BW}}$ would signify infinite noise power, this is a reasonable assumption.

No overlaps of the up-converted $\mathrm{N_{BW}}$'s will be modeled; for most direct-conversion quadrature modulator applications the fraction $\omega_{\mathrm{LO}}/\omega_{\mathrm{BB}}$ is high enough to justify this.

However, it is assumed that the noise sources Ni and Nq are similar and that their combined noise power at the modulator output is twice that from the single source Ni^2. Likewise, the noise power from the sources Nxi and Nxq is obtained by doubling the system response for the single noise source Nxi. This assumption is justified by the symmetry required for the proper operation of any quadrature modulator. To obtain the noise at the quadrature modulator output, the system response to Ni is first determined as:

$$\begin{aligned} ONi &= a_1\, Ni \left(c_1\, B \cos\left(\omega\, t\right) + c_3\, B^3 \left(\cos\left(\omega\, t\right)\right)^3 \right) \\ &= a_1\, Ni \left(c_1\, B \cos\left(\omega\, t\right) + \frac{1}{4}\, c_3\, B^3 \cos\left(3\,\omega\, t\right) + \frac{3}{4}\, c_3\, B^3 \cos\left(\omega\, t\right) \right) \end{aligned} \tag{2.29}$$

After the selection of noise components multiplied by $\cos\omega\,\mathrm{t}$, the ONi can be redefined as:

$$ONi = \left(Bc_1 + \frac{3}{4}\, c_3\, B^3 \right) a_1\, Ni \tag{2.30}$$

Substitution of $\mathrm{a_1\,Ni}$ in (2.30) with Nxi yields the respective noise response ONxi. Thus, after summing of the terms ONi and ONxi, the results can be multiplied by 2 to get the total quadrature modulator $\mathrm{N_{floor}}$ at its output as:

$$\mathrm{N_{floor}} = 2 \left(Bc_1 + \frac{3}{4}\, c_3\, B^3 \right)^2 \left(a_1^2 Ni^2 + Nxi^2 \right) \tag{2.31}$$

This $\mathrm{N_{floor}}$ expression would lend itself well to the traditional input-referred noise formulation, but this train of thought should be avoided as division by the linear power gain factor $\mathrm{a_1^2}$ would assimilate two inputs which are physically at 90° offsets to each other. Hence, to compare noise to input signaling the developed $\mathrm{N_{floor}}$ expression (2.31) should be divided by 2 so as to reduce it to a single input. After this the (single) input-referred quadrature modulator DR is easy to define, and it gives a correct picture of the available performance, whereas mathematically combining two IQ-inputs to a total input amplitude would be incorrect. The defined $\mathrm{N_{floor}}$ (2.31) and $\mathrm{OP_{1dB}}$ (2.26) expressions will next be compared in order to gain an understanding of the maximum dynamic range available.

2.3.4 Transmitted dynamic range

To define the available TDR of the modulator, squared $\mathrm{OP_{1dB}}$ will be divided by the defined $\mathrm{N_{floor}}$ to give TDR as:

$$\begin{aligned} TDR &= \frac{\mathrm{OP_{1dB}}^2}{\mathrm{N_{floor}}} \\ &= \frac{8}{81} \left(2\, CM\, adBx\, \cos\left(\theta\right) + 1 + CM^2 adBx^2 \right) \cdot \frac{{a_1}^2 \mathrm{P_{1dB}}^2}{{a_1}^2 Ni^2 + Nxi^2} \end{aligned} \tag{2.32}$$

This definition states that a quadrature modulator TDR is defined by one constant, by one mismatch dependent factor and by the mixer DR. Since for all practical purposes the mismatch dependent factor with (adBx, CM, θ) can be replaced by the real constant 4, and since the power dB-operator is $10\log_{10}()$ the defined TDR in decibels is:

$$\begin{aligned} TDR &= -10 + 6 + \frac{{a_1}^2 \mathrm{P_{1dB}}^2}{{a_1}^2 Ni^2 + Nxi^2} \\ &= -4dB + \mathrm{DR(Mxr)} \end{aligned} \tag{2.33}$$

Hence, the cost of a quadrature modulator application is approximately a -4 dB decrease in a mixer DR.

2.4 ACPR and EVM

ACPR and EVM have become increasingly important figures of merit with the increased use of complex digital modulation schemes, and they are typically defined as an intrinsic part of the specifications of a communication system. A graphical definition ACPR is given in Fig. 2.15, and it is used to specify the maximum magnitude of noise and distortion products which the transmitter can produce on an adjacent channel at a specified output power. An increase of such sidelobes is a measure of inadequate linearity, either in the modulator itself or in the whole transmitter chain, including the PA.

The error vector is the difference between the ideal rotating phasor and its distorted real counterpart, as shown in Fig. 2.16. Its magnitude, or error-vector-magnitude (EVM), is typically specified as a percentage of the total signal root-mean square (RMS) value, and it is used to get a realistic comprehensive picture of the performance of the system, since it includes all channel imperfections, such as linear imbalances, noise, and distortion [37]. For a single measurement the EVM can be defined as:

$$\text{EVM} \;=\; 100 \cdot \sqrt{\frac{(\text{real}_x - \text{ideal}_x)^2 + (\text{real}_y - \text{ideal}_y)^2}{(\text{ideal}_x)^2 + (\text{ideal}_y)^2}} \tag{2.34}$$

Therefore definition of the EVM as a function of linear IQ modulator gain and phase imbalances [38] is incomplete, since distortion effects dominate EVM-performance, at least if high power stages such as the PA [39] have been included. To test whether this could be the case for IQ modulators, the *ideal* i.e. wanted quadrature modulator response is redefined from (2.4) to include linear channel coefficients (a_1, c_1) and signal amplitudes (A, B). This makes comparison to the distorted real signaling possible, and leads to the redefined expression for quadrature modulator output:

$$s(t) \;=\; a_1 I(t) c_1 B \cos(\omega t) + a_1 Q(t) c_1 B \sin(\omega t) \tag{2.35}$$

The defined equation does not preclude any IQ-modulation type, as general time-dependent terms I(t) and Q(t) have been used to represent the in-phase and quadrature BB signaling. Therefore, the ideal vector x- and y- components can now be defined as:

$$\begin{aligned} \text{ideal}_x \;&= a_1 c_1 B \cdot I(t) \\ \text{ideal}_y \;&= a_1 c_1 B \cdot Q(t) \end{aligned} \tag{2.36}$$

To define the realized modulator output $\text{real}_{\text{x,y}}$ the quadrature modulator model in Fig. 2.9 has been used, again with the general time-dependent terms I(t) and Q(t) as signal inputs. The resulting expressions will not be repeated here, as they are too complex but numerical evaluation will be performed instead. To be able to do this, the general I(t) and Q(t) terms were replaced by the sinusoids (2.14) already used during development of the quadrature modulator models in this chapter. Use of the sinusoids yields results which are comparable e.g. with the calculated $\text{OP}_{1\text{dB}}$ performance shown in Fig. 2.13.

The relevance of the calculated EVM values to previous results is guaranteed as the coefficient defined for the IRR=-40 dBc modulator example (2.19) have been used for numerical estimation of the developed models. A 50 point evaluation in one cycle T ($\omega\,\text{T} \;=\; 2\pi$) is done to include all peak EVM values resulting from the use of the sinusoidal BB signaling. Such 50 point evaluations have been calculated for each input amplitude included in the study, and the

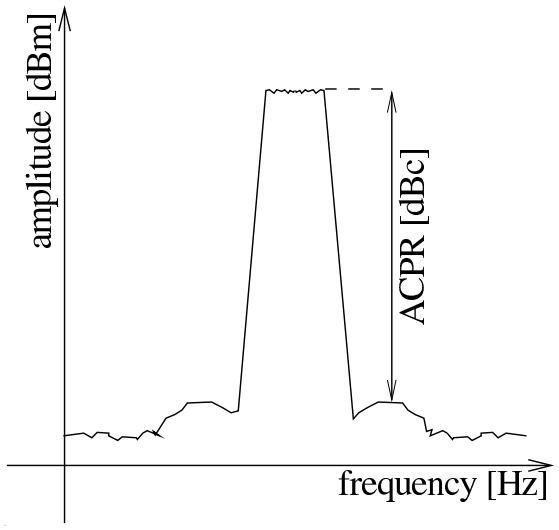


Figure 2.15: ACPR definition.

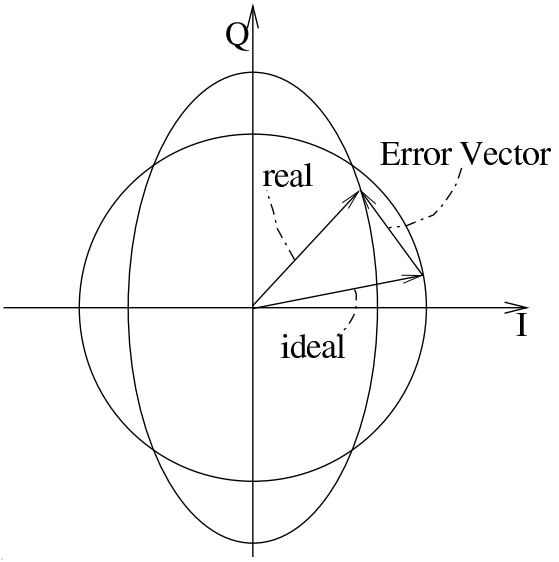


Figure 2.16: Error vector magnitude graphical definition.

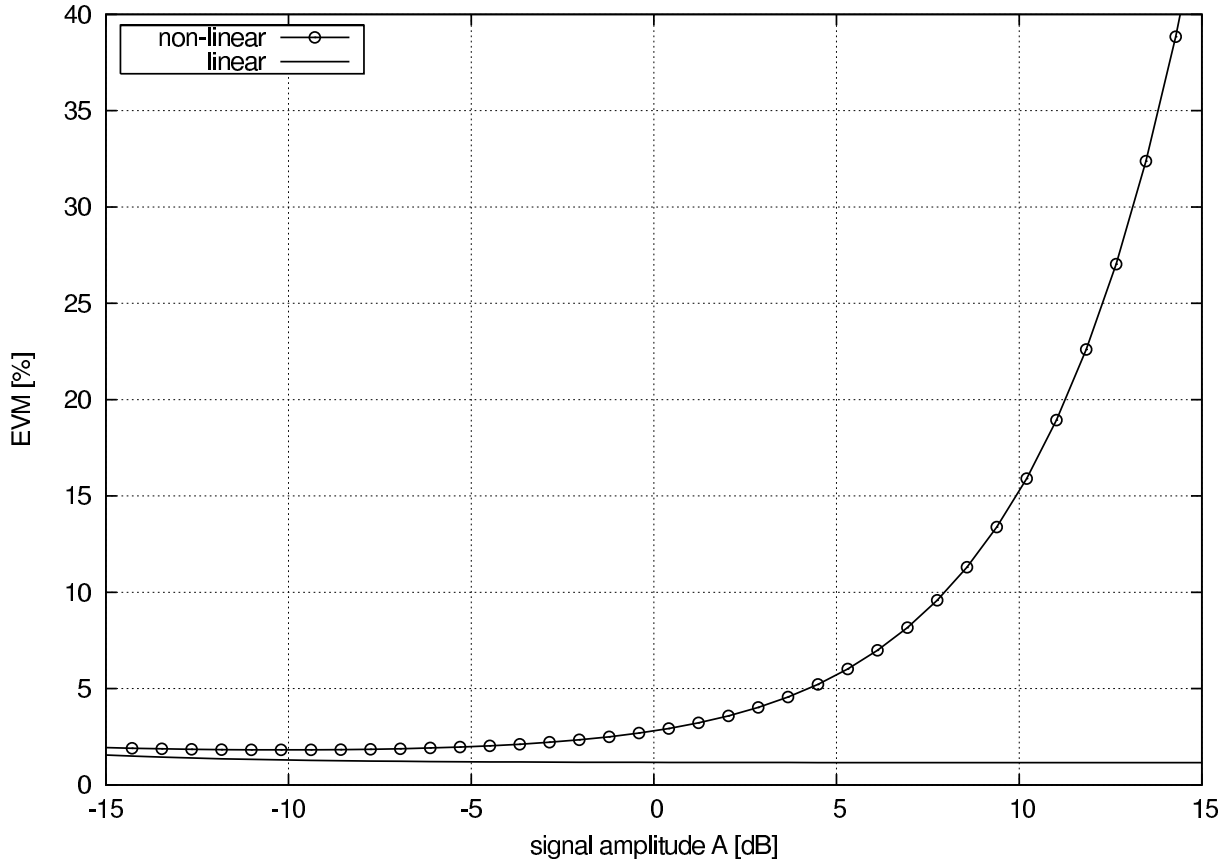


Figure 2.17: EVM values calculated with the non-linear and linear quadrature modulator models for the IRR=-40 dBc example.

resulting $\mathrm{EVM_{RMS}}$ values are shown in Fig. 2.17 annotated as *non-linear*. A linearized model has also been developed by setting the non-linear coefficients to zero. The resulting EVM values calculated for the derived *linear* model establish a lower bound for EVM performance, which is dependent on matching and signaling accuracy. From the depicted data it is obvious, that while linear mismatch coefficients might suffice for EVM modeling with small signal amplitude excitations, it is mandatory to include distortion-related effects at higher amplitudes.

2.5 Evaluation of theory

It is illustrative to compare the schematic of a practical direct-conversion quadrature modulator realization shown in Fig. 2.18 to the developed simplified quadrature modulator in Fig. 2.9: the quadrature modulator schematic in Fig. 2.18 complements the developed simplified model by introducing differential signaling, which is (always) used in integrated modulators to improve LO leakage, even-order distortion, noise, and the power supply ripple attenuation of the implemented circuitry. At baseband frequencies differential signaling is usually readily available, but at microwave frequencies discrete couplers or on-chip baluns are utilized for best performance. To emphasize this, Fig. 2.18 uses signal-flow-graph (SFG) coupler symbols for the LO and OUT signals, while it directly inputs differential BB signaling.

Differential signaling, however, is always imperfect, with finite phase and gain errors causing imbalance between the in- (0°) and out-of-phase (180°) signaling. Therefore, to determine whether these imperfections invalidate any of the developed quadrature modulator models, their effect at each signal port will be considered next:

LO Since a single sinusoid is input as an LO signal, its gain and amplitude imbalances have already been taken into account in the developed models as gain coefficients (c_1, c_3, and adBx) and as a phase error factor (θ).

BB BB signaling imbalances are often insignificant as a result of the fact that these lower-frequency signals can be derived from ubiquitous digital-signal-processor (DSP) units with perfect fidelity. However, increasing signaling bandwidths [8] will probably change this, as demand for increasing data rates dictates broadband BB operation. In fact, the developed quadrature modulator model shown in Fig. 2.9 has an implicit provision for gain and phase imbalances, as the even-order coefficient would cancel with perfectly differential BB signaling/amplification. The common-mode amplitude error between the i- and q-inputs has already been covered by the inclusion of the factor adBx, and manipulation of the trigonometric identities shows that the phase errors of both the BB and LO signals can be assimilated in the previously used LO path phase error factor θ.

OUT In contrast, replacement of the ideal summation node $\oplus$ at the quadrature modulator output with a non-ideal differential-to-single-ended block, as shown in Fig. 2.18, represents a difficult problem for the previously defined quadrature modulator model: real signaling with a plethora of tones is fed as an input to a complex differential-to-single-ended combiner, where the branches are multiplied by factors of the form $\mathrm{gain} \cdot \mathrm{e}^{\mathrm{j}\theta}$. This means, that envelope-phase format arithmetics will no longer be usable and that the results will be unintelligible.

Similarly, output buffer non-linearities have not been modeled so as to avoid extremely cluttered equations, but on the basis of the literature [47, 28] it is obvious that self-mixing and increasing sidelobes will occur as a result of these non-linearities. Qualitatively, these

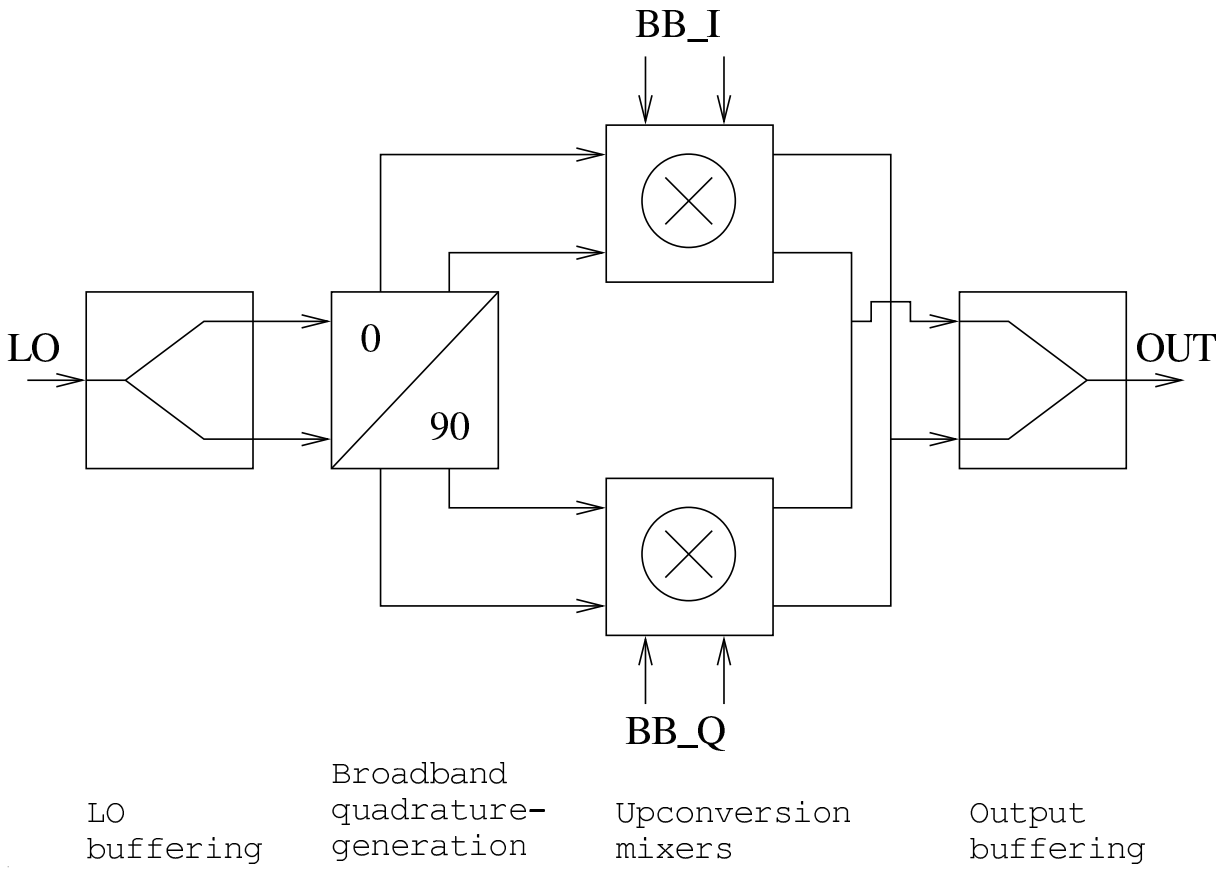


Figure 2.18: Practical quadrature modulator realization with differential signaling.

Table 2.1: Hardware of different reported quadrature modulators.

		LO buffering	Broadband quadrature-generation	Upconversion mixers	Output buffering
[16]	2004	XFMR+diffpair	switchable PP	Gilbert AB	diffpair+eF
[18]	2003	Integ.balun	PP	Gilbert AB	totem-pole
[10]	2005	XFMR	div-by-2	digital	XFMR
[40]	2004	XFMR+diffpair	PP	mod. Gilbert	XFMR
[41]	2001	XFMR+diffpair	PP-amp-PP	mod. Gilbert	totem-pole
[42]	1998	XFMR	PP	resistive	single-ended
[43]	1997	buffer	tunable RC-CR	FET ringmixer	XFMR
[44]	1996	—	tunable RC-CR	mod. Gilbert	XFMR
[45]	1996	buffer	tunable RC-CR	Gilbert	XFMR
[46]	1993	—	tunable RC-CR	Gilbert	totem-pole

XFMR: off-chip transformer.

phenomena have already been described in Fig. 2.9, and the quantitative effects of cascading are best described by the calculation of characteristics such as the output-referred third-order intercept point (OIP_3).

The following chapters will study the building blocks of the broadband quadrature modulator shown in Fig. 2.18 in the order of `LO buffering`, `Broadband quadrature generation`, `Upconversion mixers`, and `Output buffering`. This order follows a straight path from microwave synthesized LO input towards output OUT with the idea of defining the desired performance of each stage, the compromises made in their most common realizations, and the solutions proposed in this thesis. These solutions or hardware decisions are compared to the blocks used in eight prominent quadrature modulators in Table 2.1; the data will serve as a basis for the following chapters.

3. LO buffering

Integrating a broadband single-ended-to-differential phase-splitter (balun) on silicon is problematic for frequencies below 6 GHz, since: 1) waveguide or other distributed element based solutions consume too much area; 2) lumped-element baluns are narrowband/area-consuming, and 3) compact transistor-based solutions are generally not very good. Since 0.8-6 GHz is used in contemporary wireless standards such as WLAN, UMTS, etc., there is a demand for an accurate integrated balun solution.

One important phase-splitter application example could be driving a broadband I/Q-modulator with a differential signal at microwave frequencies, as in Fig. 2.18, but according to the tabulated list of hardware used in Table 2.1 this is generally not the case. One major reason for this is that in such an application, signals need to be very accurately balanced for proper circuit operation: a maximum $\Delta\phi$ of 1.1° and a maximum ΔA of 0.2 dB can be tolerated for a -40 dBc IRR. To accomplish this for broadband high-performance modulators, such as the 0.8-2.7 GHz quadrature modulator in [41], off-chip transformers (XFMR) could be used for the single-ended-to-differential-conversion of LO signals. This is not a desirable solution, however, since it introduces extra complexity and cost to the system.

3.1 LO buffer specifications

Intuitively, LO buffer distortion should be kept as low as possible, but according to the derived expressions for quadrature modulator spurious tone suppression in (2.23), the LO chain gain and distortion factors $c_{1,3}$ cancel. This means that the spectral purity near the transmitted channel is unaffected by LO chain distortion. However, poor balance in LO signaling will rapidly reduce system image and local and second harmonic spurious tone rejections, whether it is caused by mismatch issues and/or generally unacceptable circuit performance. This is also detected in (2.22-2.23), where the relevant IRR, LO-rej and 2ND-rej expressions include the LO chain mismatch or unbalance modeling factors adBx and θ. However, according to (2.21), LO chain distortion will compress the transmitted power and it will generate harmonics outside the frequency range of interest. These might self-mix and fold power to the frequency range of interest and thus distort transmission.

Noise should be as low as possible, since a noisy buffering amplifier increases LO signal phase noise and part of the generated excess noise leaks to the quadrature modulator output and raises the system noise floor. Withal, the developed theory (2.23) explicitly predicts that LO chain amplitude and phase errors/imbalances will lead to poor quadrature modulator performance; consequently the remainder of this chapter will first concentrate on the theoretical modeling of available single-ended-to-differential conversion accuracy, after which several realized baluns will be introduced and analyzed so as to gain an insight into the current state of the art.

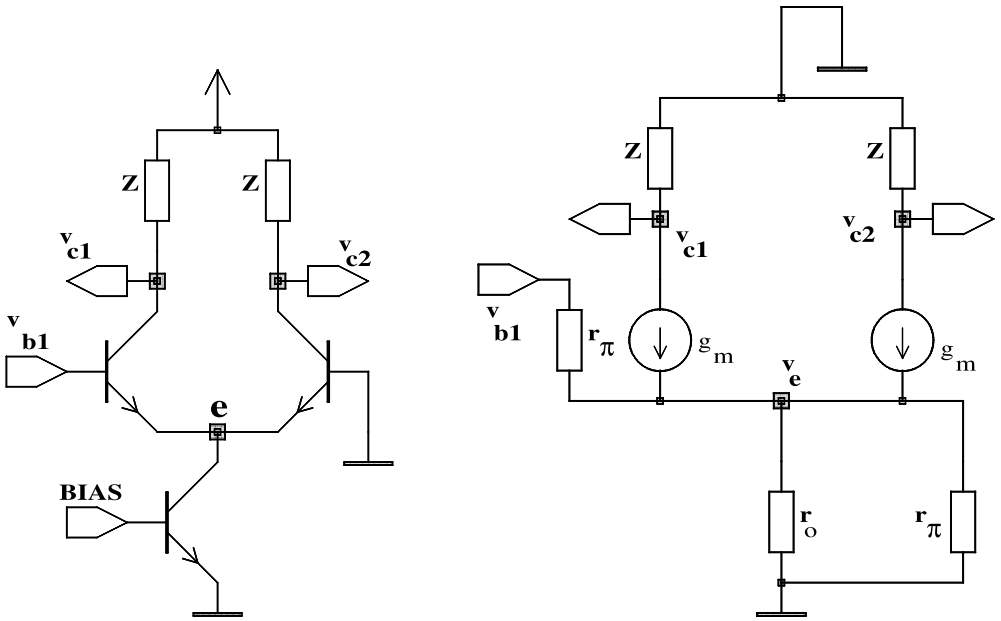


Figure 3.1: (a) Differential pair used as a phase-splitter, and (b) its small-signal model.

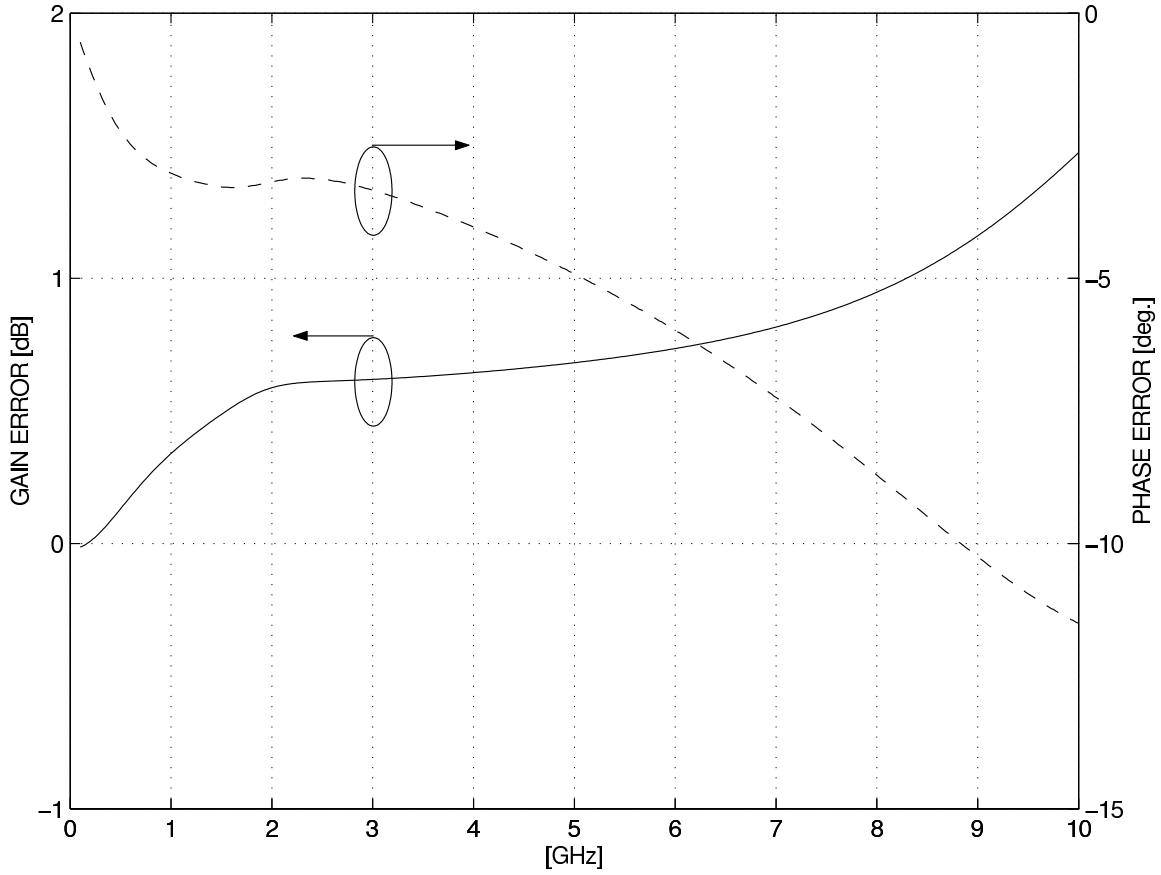


Figure 3.2: Simulated differential pair gain and phase errors vs. frequency.

3.2 Differential pair phase-splitting

Fig. 3.1(a) depicts a bipolar differential pair connected as a phase-splitter. This particular amplifier was realized in 0.8 μm SiGe with f_T=35 GHz. Its simulated performance includes 13 dB of low-frequency voltage gain, 40 GHz 0dB-bandwidth, and 7.1 mA current drawn from a 2.5 V supply. These results were obtained using an ideal (voltage) signal source with infinitely small source impedance and inductively-peaked resistive loading.

Using nodal voltages ($v_{c1,2}$ and v_{b1}) as state-variables the amplifier in Fig. 3.1(a) can be presented in matrix form as:

$$\begin{bmatrix} v_{c1} \\ v_{c2} \end{bmatrix} = \begin{bmatrix} \alpha & \beta \\ \beta & \alpha \end{bmatrix} \begin{bmatrix} v_{b1} \\ 0 \end{bmatrix} = \begin{bmatrix} \alpha v_{b1} \\ \beta v_{b1} \end{bmatrix} \tag{3.1}$$

From (3.1) it can be seen that perfect single-ended-to-differential conversion (outputs $v_{c1} \equiv v_{c2}$) is possible, if $\alpha \equiv \beta$. To define the coefficients α and β linear operation is assumed; the resulting small-signal model is shown in Fig. 3.1(b). To further simplify analysis, the use of an ideal signal source, as in [36], is assumed. Therefore, the requisite equations for nodal analysis of Fig. 3.1(b) are:

$$v_e \; node: \; v_{b1}\left(\frac{1}{r_\pi} + g_m\right) - v_e\left(2g_m + 2\frac{1}{r_\pi} + \frac{1}{r_o}\right) = 0 \tag{3.2}$$

$$v_{c1} \; node: \; v_{c1} = -g_m\left(v_{b1} - v_e\right) Z \tag{3.3}$$

$$v_{c2} \; node: \; v_{c2} = g_m v_e Z \tag{3.4}$$

Solving (3.2) and (3.3) for v_{c1} and (3.2) and (3.4) for v_{c2}, and comparing the results to (3.1) yields definitions for α and β as:

$$\alpha = -\frac{\left(r_o\, r_\pi\, g_m + r_o + r_\pi\right) Z g_m}{2\, r_o\, r_\pi\, g_m + 2\, r_o + r_\pi} \tag{3.5}$$

$$\beta = \frac{g_m\, Z r_o\, \left(r_\pi\, g_m + 1\right)}{2\, r_o\, r_\pi\, g_m + 2\, r_o + r_\pi} \tag{3.6}$$

Dividing (3.5) by (3.6) makes possible the definition of α in terms of β as:

$$\alpha = -\underbrace{\left(1 + \frac{r_\pi}{r_o\, \left(r_\pi\, g_m + 1\right)}\right)}_{(1+\epsilon)} \beta \tag{3.7}$$

Since both $g_m r_\pi >> 1$ and $g_m r_o >> 1$, a small error quantity ϵ $(0 < \epsilon << 1)$ is defined to represent the fractional part of the equation. Thus any differential pair is intrinsically asymmetric as a balun. Although the intrinsic asymmetry predicted by (3.7) is very small near DC, it rapidly gets worse with increasing frequency. This is caused by parasitic capacitance in parallel with the current source resistance r_o, which transforms it to a frequency-dependent complex impedance z_o. To improve the differential pair common-mode rejection (CMR), the cascoding of current source transistors or an inductively compensated current source as in [48] could be used. Alas, the cascoding of the current-source transistors is not an option since it is not compatible with the specified 2.5 V supply, and the specified broadband operation precludes the use of integrated coils, as these will resonate with ubiquitous parasitics to produce a narrowband response.

The asymmetry of the differential pair balun is also evident in the simulated gain-phase error plot in Fig. 3.2, where balun operation is near-perfect at DC but rapidly gives worse results

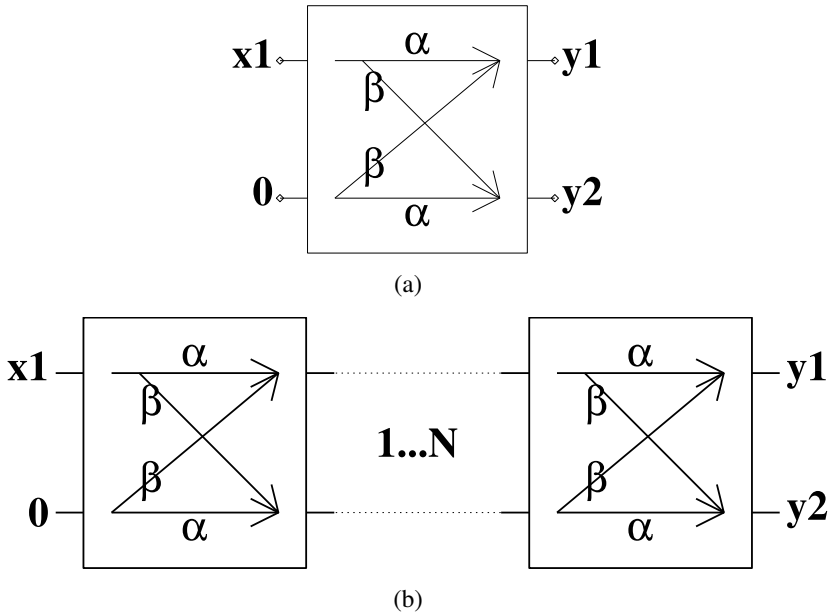


Figure 3.3: Differential pair block diagrams connected as a) one-stage and b) cascaded phase-splitters.

at higher frequencies. Targeting WLAN/W-CDMA applications, the simulated gain and phase errors at 2.4 GHz are +0.6 dB and -3.1°, respectively. The maximum gain error peaks at +1.5 dB, while phase error varies between -11.5°...-0.6°.

3.3 Cascaded phase-splitting

A block diagram presentation of a single-stage differential pair phase-splitter is given in Fig. 3.3(a). This block diagram is a symbolic representation of a differential pair phase-splitter. Thus a comparison of Fig. 3.1(a) and Fig. 3.3(a) justifies equating signals (v_{B1}, v_{C1}, and v_{C2}) with their state variable (x_1, y_1, and y_2) counterparts, respectively.

The block diagram presentation is used to model a cascade of 1...N similar differential pairs, which are connected as a 0/180° phase-splitter. This model is shown in Fig. 3.3(b). It can be described with a chain matrix equation as:

$$\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \underbrace{\begin{bmatrix} \alpha & \beta \\ \beta & \alpha \end{bmatrix} \cdots \begin{bmatrix} \alpha & \beta \\ \beta & \alpha \end{bmatrix}}_{\text{N}} \begin{bmatrix} x_1 \\ 0 \end{bmatrix} = \begin{bmatrix} \gamma\, x_1 \\ \delta\, x_1 \end{bmatrix} \tag{3.8}$$

$$\text{, where } N \geq 1 \qquad \text{for all } N \in \mathbb{Z}^+.$$

Now, recalling definition (3.7), performing the necessary algebraic manipulations makes possible the presentation of factors γ and δ as a function of ϵ for all positive integer values N as:

$$\begin{bmatrix} \gamma \\ \delta \end{bmatrix} =$$

$$\text{1-stage} : \begin{bmatrix} -(1+\epsilon) \\ 1 \end{bmatrix} \beta^1$$

$$
\begin{aligned}
&\text{2-stages:} \left[\begin{array}{c} 2+2\,\epsilon+\epsilon^2 \\ -\left(2+2\epsilon\right) \end{array} \right] \beta^2 \\
&\text{3-stages:} \left[\begin{array}{c} -\left(4+6\,\epsilon+3\,\epsilon^2+\epsilon^3\right) \\ 4+6\,\epsilon+3\,\epsilon^2 \end{array} \right] \beta^3 \\
&\text{4-stages:} \left[\begin{array}{c} 8+16\,\epsilon+12\,\epsilon^2+4\,\epsilon^3+\epsilon^4 \\ -\left(8+16\,\epsilon+12\,\epsilon^2+4\,\epsilon^3\right) \end{array} \right] \beta^4 \\
&\text{5-stages:} \left[\begin{array}{c} -\left(16+40\,\epsilon+40\,\epsilon^2+20\,\epsilon^3+5\,\epsilon^4+\epsilon^5\right) \\ 16+40\,\epsilon+40\,\epsilon^2+20\,\epsilon^3+5\,\epsilon^4 \end{array} \right] \beta^5 \\
&\quad \ldots
\end{aligned}
\tag{3.9}
$$

To complete this set of definitions, a generalized form for the factors γ and δ for N-cascaded blocks can be written as:

$$
\begin{aligned}
&\left[\begin{array}{c} \gamma \\ \delta \end{array} \right] = \left[\begin{array}{c} (-1)^{\mathrm{N}} \left(P_{\mathrm{N}-1}+\epsilon^{\mathrm{N}}\right) \\ (-1)^{\mathrm{N}-1} P_{\mathrm{N}-1} \end{array} \right] \\
&\quad , \textit{where} \\
&\quad \begin{cases} N & \in \mathbb{Z}^+. \\ P_{\mathrm{N}-1} & \text{is a (N-1)-degree polynomial:} \\ & \sum_{i=0}^{N-1} c_{\mathrm{i}} \epsilon^i, \text{for all } c_{\mathrm{i}} \in \mathbb{Z}^+ \end{cases}
\end{aligned}
\tag{3.10}
$$

Dividing γ by δ, as defined in (3.10), makes possible the definition of γ in terms of δ and a small error factor $\epsilon^{'}$ as:

$$
\gamma = -\left(1+\epsilon^{'}\right)\delta = -\left(1+\frac{\epsilon^{\mathrm{N}}}{P_{\mathrm{N}-1}}\right)\delta \tag{3.11}
$$

A comparison of the error terms ϵ and $\epsilon^{'}$ in (3.7) and (3.11) can be used in estimating the effect cascading has on phase-splitter accuracy. Assuming that accuracy is *increased* by cascading leads to the following inequality:

$$
\begin{aligned}
&\epsilon^{'} < \epsilon \Leftrightarrow \frac{\epsilon^{\mathrm{N}}}{P_{\mathrm{N}-1}} < \epsilon \\
&\Rightarrow \frac{\epsilon^N - \epsilon P_{\mathrm{N}-1}}{P_{\mathrm{N}-1}} < 0
\end{aligned}
\tag{3.12}
$$

Combining the definition of $\mathrm{P}_{\mathrm{N}-1}$ in (3.10) and the definition of ϵ as a small positive error factor ($0 < \epsilon << 1$) constitutes proof for (3.12). Thus cascading *reduces* the phase-splitting errors of differential pair baluns■

To quantify the available improvement in cascaded phase-splitting, ϵ is set to 0.4 and the values of γ (3.11) are calculated: -(1.4000, 1.0571, 1.0093, 1.0015, 1.0003, ...)δ. Thus a 40% mismatch is reduced to 5.7% after the addition of one stage, or in decibels from 3 dB to 0.5 dB. The mathematical 40% mismatch estimate used might be seen as somewhat exaggerated so as to make the point, but in reality the order of magnitude is correct, and such characteristics are often seen as e.g. balun amplitude imbalance characteristics.

3.4 Integrated baluns

Active phase-splitters that have been reported include single-transistor, common-gate-common-source (CGCS) or differential pair implementations; recently, integrated transformers have also become available for lower microwave applications.

3.4.1 Single-transistor phase-splitters

Usually, single-transistor phase-splitters have too much phase error as a result of circuit parasitics. Fig. 3.4 depicts an example of a single transistor balun, where FET drain and source nodes are used as outputs; as is well-known, the inverting (drain) and non-inverting (source) node impedances differ substantially. The impedance seen at the drain node is formed by the parallel connection of the channel conductance g_o and several parasitic capacitances, such as the gate-to-drain C_{gd}, and drain-to-bulk C_{db} capacitances. In contrast, the device transconductance g_m seen at the source node is in most cases so high that it dominates circuit source impedance estimates. This inherent imbalance has a deleterious effect on the performance of a single FET circuit as a balun, and the reported [49] ΔA=1 dB (gain error) and ϕ=176° (phase difference) values are in agreement with this, as these *simulated* results were reported as best possible for a single FET balun optimized for use in a Personal Communication Systems (PCS) application at 950 MHz.

To correct the inherent imbalance of the single FET balun, [50] proposed the use of a pair of cross-connected correcting transistors, as shown in Fig. 3.5. However, this is not a promising candidate for a broadband balun solution, for two reasons: 1) seven integrated capacitors (excluding output buffering) are needed to make it work, so there is an increase in IC area and a great deal of parasitic capacitance involved, and 2) for better balance each transistor should have equal gain from the gate to the source/drain terminals: this limits the topology to use in low-gain applications. The combination of these two points does not imply good broadband performance for this topology, but the reported *simulated* gain and phase values from 1 GHz to 2 GHz support claims for improved accuracy: ΔA=-0.2 dB and ϕ=178°.

3.4.2 Modified CGCS topology

In [51] a CGCS topology is defined as having a good broadband amplitude balance, while its phase difference is usually poor. In contrast, the modified CGCS topology shown in Fig. 3.6 realizes both good amplitude and phase balances with measured performance at: ΔA=0.5 dB and ϕ=178°-180.2°. A problem with this topology is the reported -5 dB loss per branch, despite the 0.13 μm technology used.

3.4.3 Differential pair baluns

Therefore, as any differential pair offers the possibility of implementing gain in the signal path, it should be the chosen starting-point for a lower microwave range phase-splitter implementation. One such implementation is the emitter-follower-driven differential pair shown in Fig. 3.7, with a reported performance of: ΔA=1 dB and ϕ=180.7°-186° in 0.5-5 GHz.

In [53] an asymmetrical feedback LCR network is suggested as a means for improving differential pair phase-splitting performance with ΔA=$\pm$1 dB and ϕ=180°$\pm$1°. However, the asymmetrical LCR feedback implementation shown in Fig. 3.8 makes achieving good broadband performance an intensive design task, as the LC feedback operates at a single resonance frequency and as its location is dependent on circuit parasitics, whereas their values depend on the supply voltages and the biasing point of the circuit.

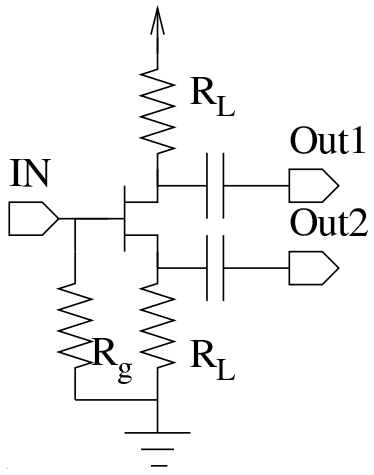


Figure 3.4: One FET as a balun [49].

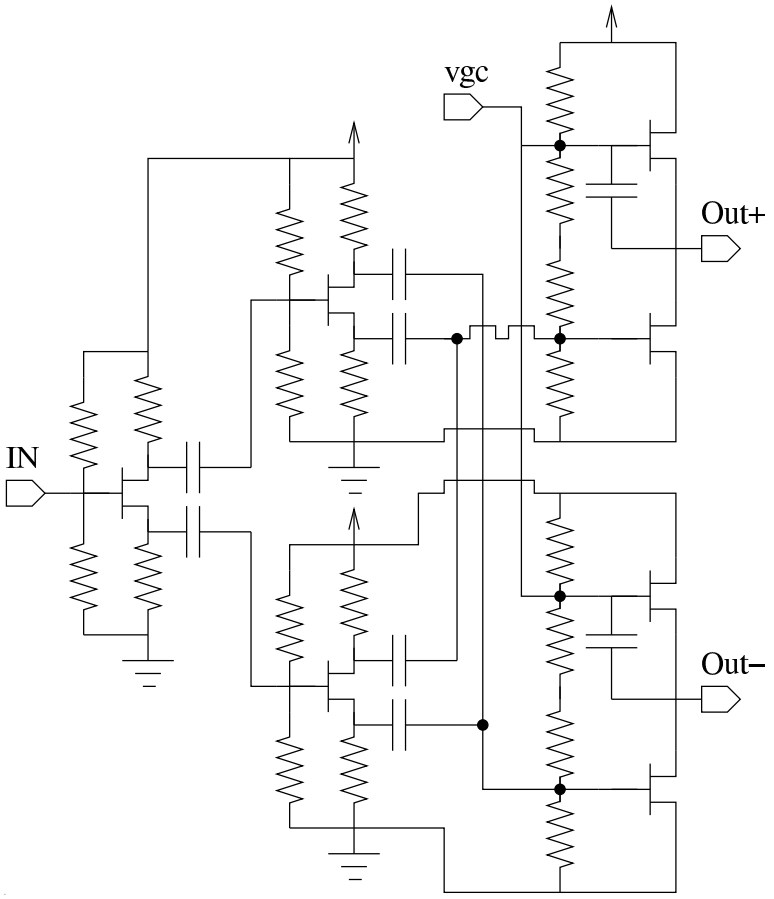


Figure 3.5: Cross-connected FETs correct single FET balun response [50].

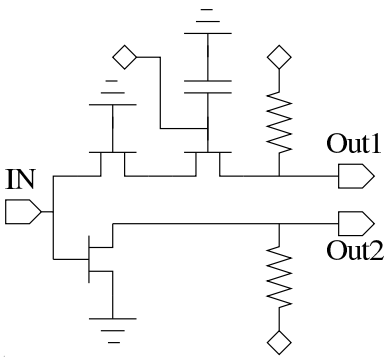


Figure 3.6: The CGCS-balun principle [51].

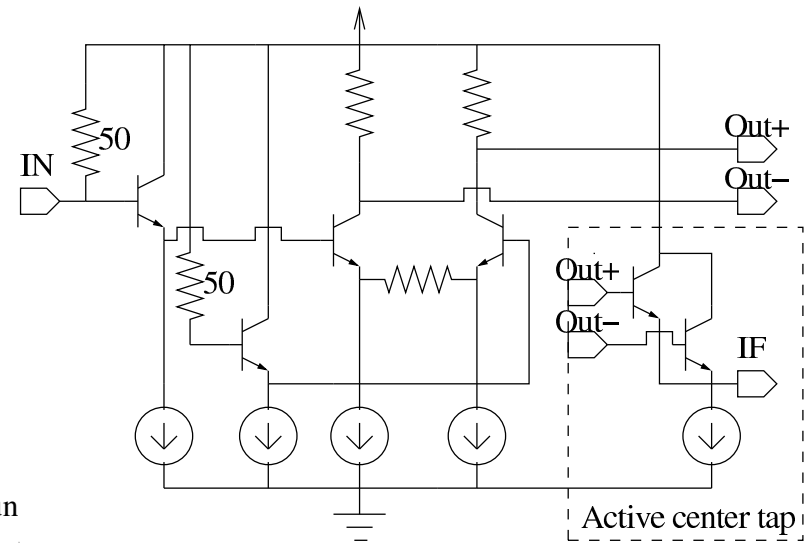


Figure 3.7: Linearized emitter-follower driven differential pair as a balun [52].

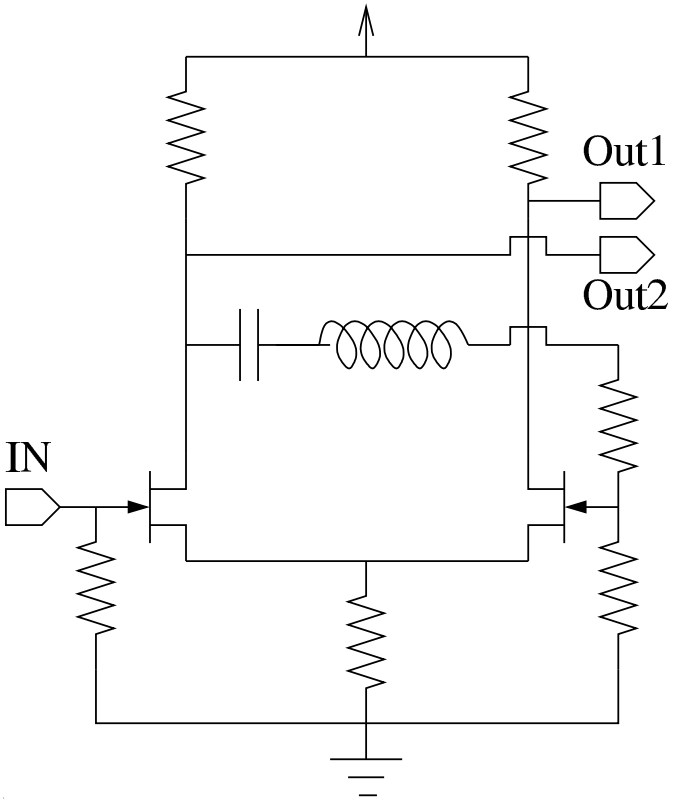


Figure 3.8: A differential pair balun with a correcting feedback LCR-network [53].

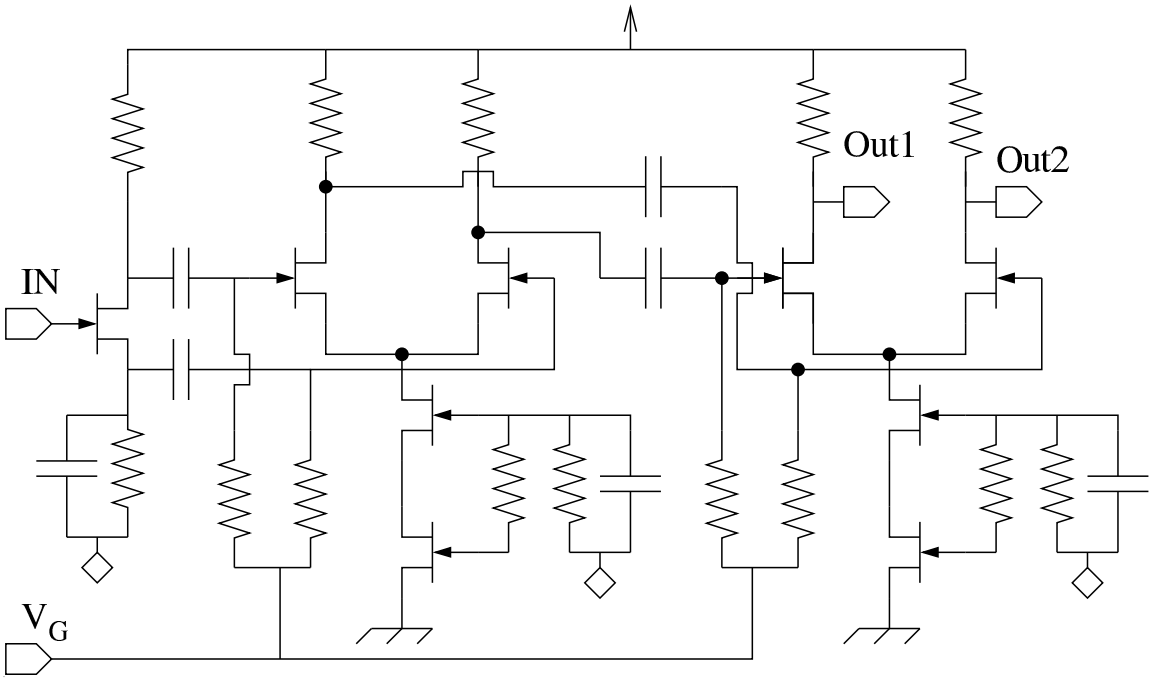


Figure 3.9: Cascaded differential pairs used as a balun [54].

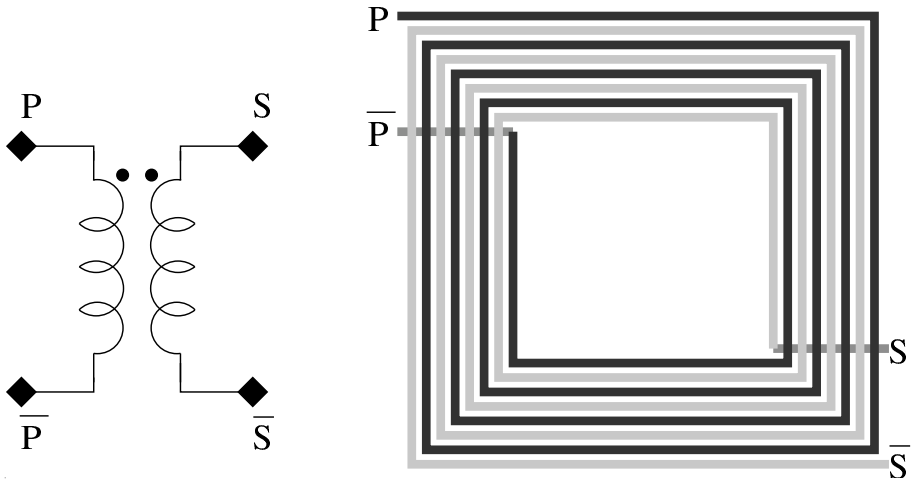


Figure 3.10: An integrated transformer example with layout and schematic symbol shown.

To improve even-order signal rejection, differential pairs can be cascaded: [54] uses a single-transistor balun to drive a cascade of two differential pairs, as shown in Fig. 3.9. The circuit implementation achieves good phase-splitter performance at ΔA=$\pm$0.25 dB and ϕ=180°$\pm$1° in 0.2-5 GHz. For this performance, a 1 μm epitaxial GaAs MESFET technology with air bridges and MIM capacitors was used.

3.4.4 Monolithic transformers

Integrated planar transformers in silicon technologies – see Fig. 3.10 – have been developing rapidly, with stacked implementations in standard digital CMOS already available [55, 56]. The self-resonant frequencies of these devices are already high enough to make possible applications in communications circuitry, where such devices make possible low-distortion operation at significantly lower power dissipation and noise levels than with active circuitry [57]. Simultaneous matching and balun functions are possible with correct turn ratios. For example, mixer output differential-to-single-ended conversion and matching have been realized with a monolithic balun in [58]. This WLAN/HIPERLAN2 transmitter front-end also uses a stacked transformer for its LO signal single-ended-to-differential conversion.

Nevertheless, monolithic transformers have not been used in the RFICs included in this book, as such devices were not available at the time of their fabrication. Additionally, for the particular case of *broadband* IQ modulator LO signal single-ended-to-differential conversion, it is not altogether clear that the achievable channel balance as measured in ΔA and $\Delta\phi$ would be sufficient, since an amplitude difference exists between the output ports as a result of interwinding capacitance. Therefore, to correct signal balance and to add isolation, a transformer could be utilized in cascade with a differential amplifier.

3.5 The realized 0.8 μm SiGe balun

For the RFIC prototype realization of Fig. 3.3(b), a cascade of two (N=2) differential pairs was realized. Since broadband operation extends to several gigahertz, three design issues arise: 1) parasitic capacitances should be taken care of for higher bandwidths; 2) the effect of process variation on phase-splitting accuracy should be determined, and 3) the input-matching circuitry to 50 Ω has to introduce a minimum amount of error in the circuit's phase-splitter function.

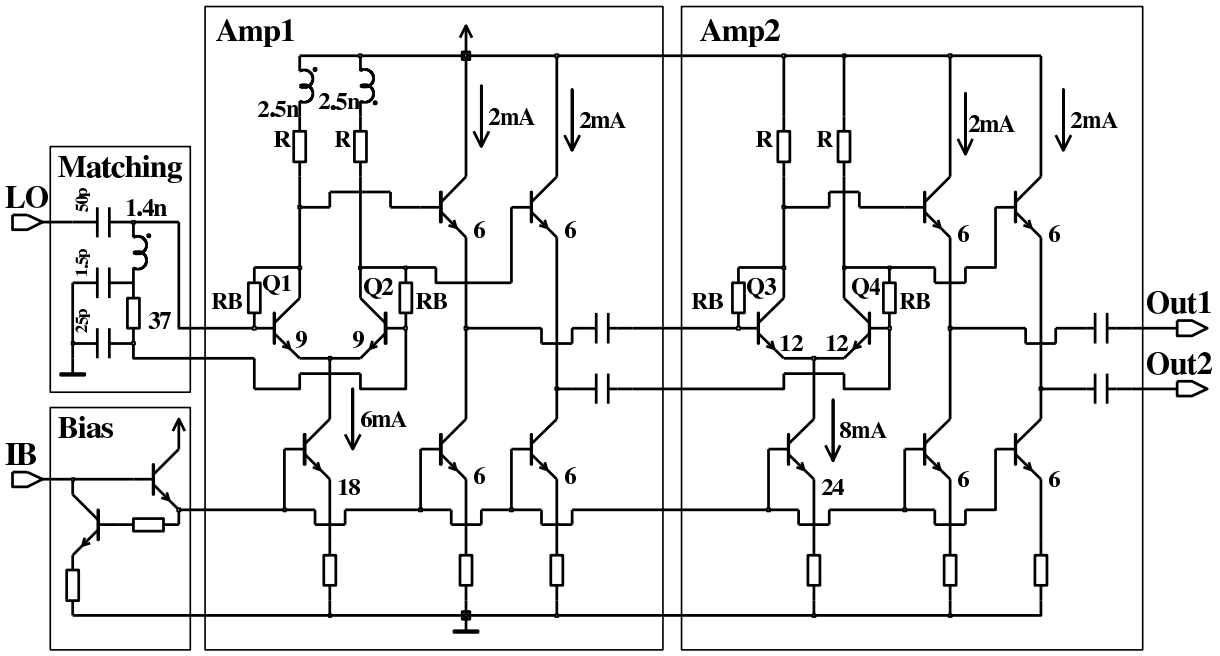


Figure 3.11: Cascaded differential pair phase-splitter circuit with matching circuit details shown.

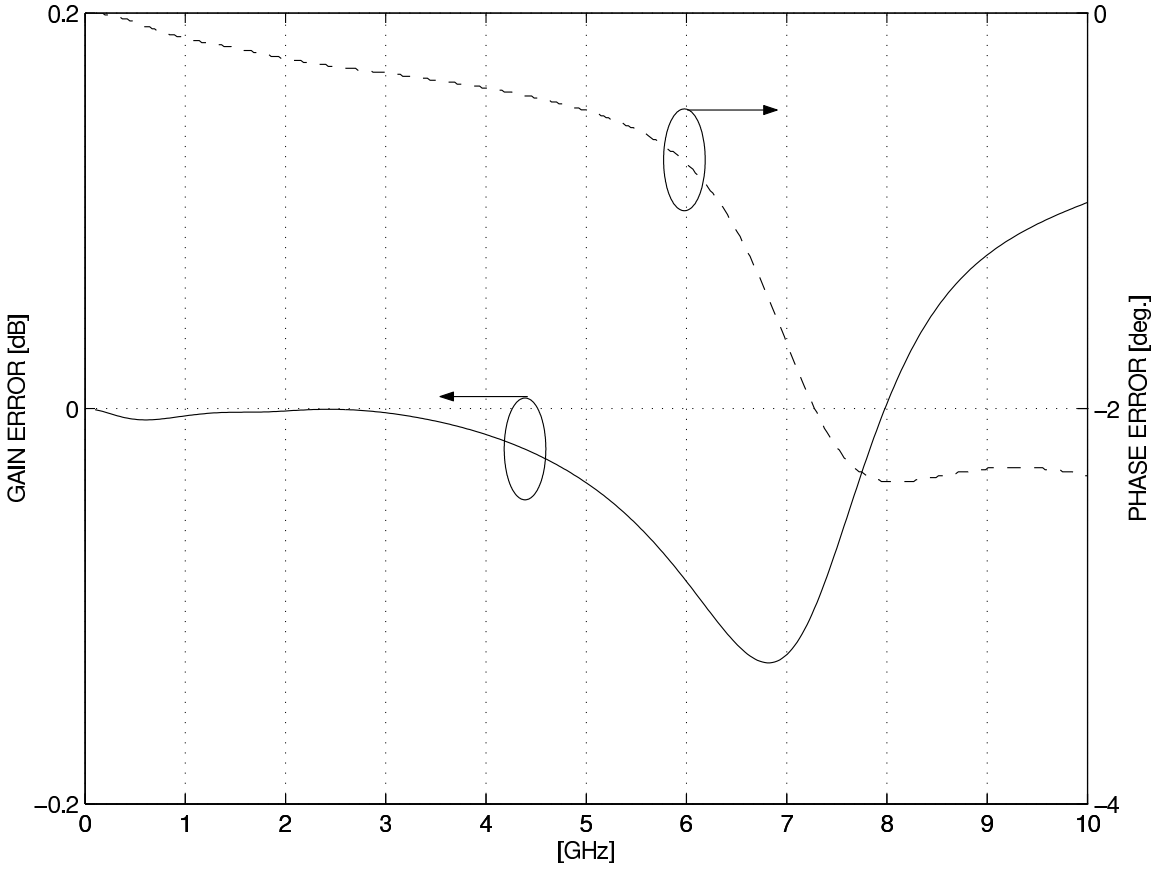


Figure 3.12: Simulated gain and phase errors of the cascaded phase-splitter vs. frequency.

3.5.1 Implementation of the cascade

The implemented phase-splitter is shown in Fig. 3.11 with emitter areas (length in μm, minimum width of 0.8 μm used) and branch currents annotated to the figure. The RFIC was realized in the AMS 0.8 μm SiGe process with f_T=35 GHz. The process supports high-density poly-to-poly capacitors and integrated coils and it has a high-ohmic resistor module. In fact, the integrated feedback resistors (marked as RB) for biasing amplifier input transistor pairs were realized using high-ohmic resistors. At 8.7 kΩ they do not interfere with the phase-splitting function of the circuit.

The differential pairs were buffered with emitter-followers in order to let each stage perform its balun function without interference, and to maximise bandwidth. This was especially important for the quadrature modulator application [21], where a lossy multi-stage polyphase filter was used for phasing the LO signal at 90° (quadrature) offsets. The resulting amplifier blocks are marked as `Amp1` and `Amp2`, where the `Amp1` input stage is a buffered realization of the differential pair in Section 3.2. Both differential pairs (Q_{12}, Q_{34}) were implemented as small-signal amplifiers without resistive linearization, since simulations predicted that the best broadband balun operation would be attained in this way. Beneficially, this produces high gain, which coincides with the design goal of lowering the required LO drive level to the quadrature modulator.

As another bandwidth-increasing measure, the resistive loads R of the first amplifier `Amp1` were inductively gain peaked [59] for approx. double the bandwidth of the circuit. Integrated 2.5 nH planar coils were used for this purpose, since no high Q-values are needed. In fact, this could be used to advantage by including part of the resistive load into the planar coil; this would make possible the use of narrow metal paths for minimum area coils with less parasitic capacitance [60]. However, for the discussed prototype, this approach has not been used because of the limited realization time and to minimize the risk of failure.

The improved phase-splitter operation of the cascaded differential pair phase-splitter is also evident when the simulated gain-phase error data shown in Fig. 3.12 are compared to the corresponding data for the single-stage in Fig. 3.2. Near-perfect phase-splitting is predicted by the data simulated for a cascade of two differential pairs, as the gain and phase errors at 2.4 GHz are -0 dB and -0.3°, respectively. The maximum gain error varies between -0.1...+0.1 dB, while the phase error varies between -2.4°...0°. A comparison of the simulated values for a single and for a cascaded differential pair $\Delta A \Delta\phi$-values at 2.4 GHz shows a definitive improvement in accuracy for the cascaded version: gain and phase errors are reduced by 0.6 dB and 2.8°, respectively.

A downside of the cascaded differential pair phase-splitter approach is increased current dissipation, but it should be noted that: a) improved phase-splitter operation is inherent in cascading, and no current increase in a single differential pair will correct this; b) there is no output buffering (and corresponding parasitics) in the comparison differential pairs, and c) at higher frequencies gain has to be divided between stages in many applications.

3.5.2 Process variations

To assess the tolerance of cascaded differential pair phase-splitter performance of process variations, statistical simulations were performed. Mean (μ) and standard deviation (σ) of ΔA and $\Delta\phi$ at 2.4 GHz were tabulated in Table 3.1 after 500 Monte-Carlo runs. Similar data were tabulated for the differential pair for comparison purposes. The importance of Monte-Carlo simulations in assessing realistically attainable circuit performance (and yield) is based on the fact that different circuit elements share layers in modern processes. Thus imitating process variations by perturbing a single element value is admittedly fast, but perhaps too inaccurate.

Table 3.1: Simulated Monte-Carlo variations at 2.4 GHz for 500 runs.

		differential pair		cascaded phase-splitter	
		ΔA	$\Delta\phi$	ΔA	$\Delta\phi$
nominal		+0.6 dB	+3.1°	+0.0 dB	+0.3°
LOT	μ	+0.6 dB	+3.3°	-0.0 dB	+0.3°
	σ	+0.1 dB	+1.0°	+0.0 dB	+0.1°
DEV	μ	+0.6 dB	+3.1°	+0.0 dB	+0.3°
	σ	+0.0 dB	+0.2°	+0.0 dB	+0.1°
LOT & DEV	μ	+0.6 dB	+3.4°	-0.0 dB	+0.3°
	σ	+0.1 dB	+1.1°	+0.0 dB	+0.2°

Two types of Monte-Carlo simulations were performed: `LOT` and `DEV`. In the `LOT`simulations each element of the same type (e.g. all NPN transistors) is modeled with the same Monte-Carlo solution, while in `DEV` each element has an individual Monte-Carlo result. Thus `LOT`-simulations imitate die-to-die variation, while `DEV` is good for modeling element-to-element variation. The `DEV`-results shown in Table 3.1 were obtained using the foundry-provided `LOT`-parameters by dividing each variation by 20. This 5% relation was chosen to reflect the fact that the matching between the elements in an integrated circuit is very good. Both the `DEV`- and `LOT`-results in Table 3.1 closely correspond to tabulated nominal $\Delta A \Delta\phi$ values, which complies with the known robustness of the differential pair. However, recorded σ-values for the differential pair $\Delta\phi$ at (1.0°, 0.2°, 1.1°) suggest a much higher variance in performance, when compared to the corresponding σ-values for the cascaded differential pair phase-splitter (0.1°, 0.1°, 0.2°).

Table 3.2: Simulated values for the cascaded differential pair phase-splitter at 2.4 GHz.

ΔA	0 dB	OP_{1dB}	-6 dBm
$\Delta\phi$	0.3°	P_{1dB}	-18 dBm
S_{21}	+7 dB	2ND-rej	-53 dBc
S_{11}	-14 dB	3RD-rej	-31 dBc
S_{22}	-10 dB		
P_{DD}=58.5 mW, I_{DD}=23.4 mA, V_{DD}=2.5 V			

3.5.3 Matching to 50 Ω with integrated passives

The matching of the input of the cascaded differential pair phase-splitter (NPN base at 700 Ω/∼400 fF) to 50 Ω was realized with the circuit block marked `Matching` in Fig. 3.11. An integrated passive matching circuit was chosen for two reasons: 1) to save power, and 2) to improve the large signal behavior of the circuit for increased P_{1dB} values. Another demand on a matching circuit is that it should not disturb phase-splitter operation. To accommodate both matching and un-spoilt phase-splitter operation, large on-chip capacitors (50/25 pF) connected to an inductively-peaked resistive pole were designed.

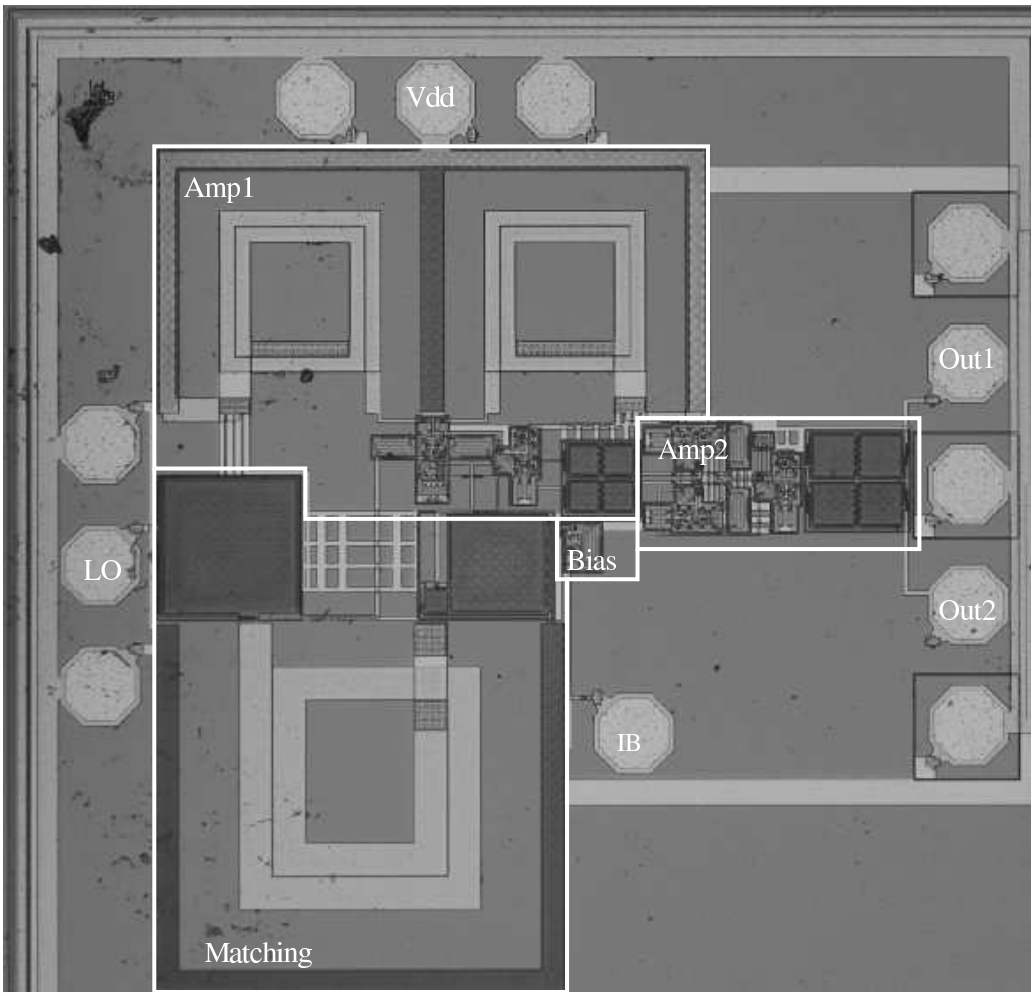


Figure 3.13: Micrograph of the 0.8-μm 1.2 mm $\times$ 1.2 mm SiGe RFIC.

Simulations with layout-extracted parasitics suggest good matching, with input return loss values below -10 dB in 0.4-6.3 GHz. A comparison of simulated gain and phase errors shows that the realized matching circuit has a negligible effect on phase-splitter performance and the suppression of even-order harmonics is good. A -3 dBm signal power backoff from the tabulated compression point of P_{1dB}=-18 dBm improves the suppression of the third harmonic (3RD) to -37 dBc (-31 dBc). Simulated performance data at 2.4 GHz in typical mean conditions are summarized in Table 3.2.

As the ambient temperature was swept from -55°C to +110°C, the resulting $\Delta A \Delta \phi$-values held at the tabulated values, while the corresponding gain of the circuit varied from +10 dB at -55°C to +4 dB at +110°C. This confirms the expected robustness of the differential pair phase-splitting action, while use of on-chip current-driven bias block facilitates the simple addition of PTAT biasing for constant gain values.

3.5.4 Measurement Results

A micrograph of the realized 0.8 μm SiGe RFIC is shown in Fig. 3.13. The chip measures 1.2 mm $\times$ 1.2 mm , including the pad arrangements to accommodate GSG-type (ground-signal-ground) wafer probing. The pad and circuit block labeling corresponds to the schematics in Fig. 3.11, while all unmarked pads were connected to the circuit ground at the RFIC circumfer-

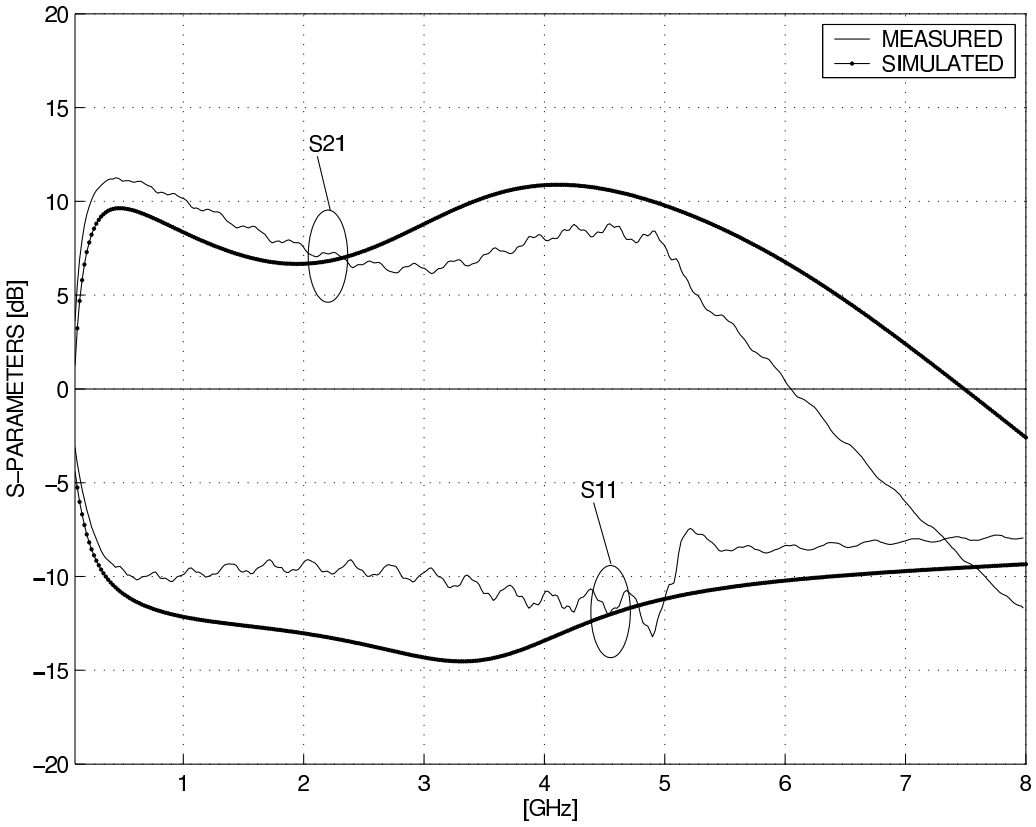


Figure 3.14: Comparison of measured s_{11} and s_{21} with simulated data.

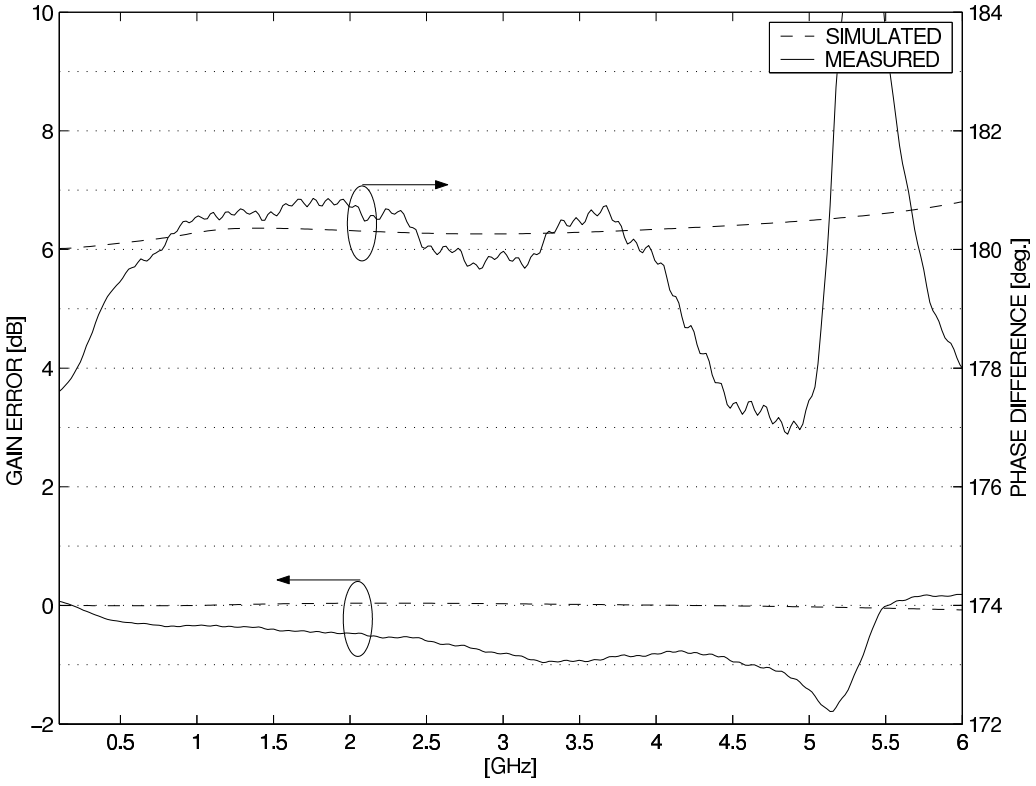


Figure 3.15: Comparison of measured ΔA and ϕ with simulated data.

ence. To facilitate calibration to RFIC, a GSGSG-type probe with two signal (S) lines was used: the two outputs were each calibrated using calibration standards realized on a 50 Ω impedance standard substrate (ISS) block. During the calibrations, the cable for the unused output was terminated with a broadband 50 Ω load, while the other cable was connected to the vector network analyzer (VNA). Switching between the cable terminations (VNA, 50 Ω) made it possible for the GSGSG probe to be kept fixed on the RFIC. To ensure the validity of the corresponding calibration sets, the two output cables were kept fixed for most of their length.

The resulting two sets of measured gain and phase values were subtracted in order to define the amplitude and phase error of the differential output. A narrow 4% smoothing window was applied to the measured data in order to filter out random noise without introducing a significant systematic error into the results. The measured scattering parameters s_{11} and s_{21} are shown in Fig. 3.14 in comparison to the simulated data. The simulated values were obtained using a layout extracted netlist with a parasitics description. The difference between the measured and simulated s_{21} values at higher frequencies reflects inductor model inaccuracy. The measured $\Delta A\phi$-data under nominal conditions are displayed in Fig. 3.15, where the gain error is better than -1 dB up to 4.6 GHz, and the phase difference is 179.7-180.9° in 0.6-4.1 GHz. Thus good phase-splitter performance was achieved for nearly a decade of variation in input frequency. The results shown in Figs. 3.14-3.15 were measured with the RFIC drawing 22.8 mA from a 2.5 V supply. This 57 mW biasing point was chosen to produce maximum quadrature modulator power output [21] with a reasonably clean spectrum. The application of a modern smaller minimum line width technology should significantly reduce both the power and current dissipation of the circuit.

To test the sensitivity of the realized balun circuit to different operating conditions, its point of operation was tuned as follows: a) the supply voltage was swept from 2 V to 3.6 V in 0.4 V steps with nominal bias, and b) the current bias was tuned to keep the current dissipation of the circuit between 15.2 mA to 26.2 mA in 3.7 mA steps from the nominal 2.5 V supply. The results from these measurements are plotted in Figs. 3.16(a)-3.17(b):

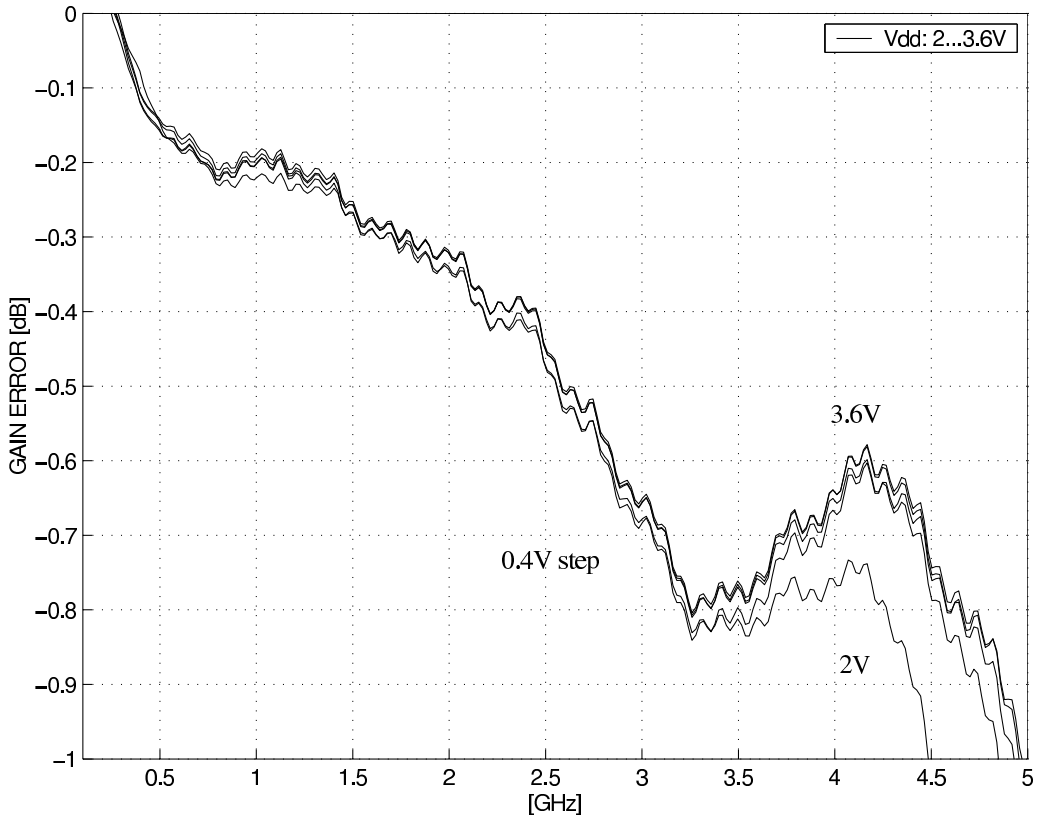
(a) only data measured using a 2 V supply plot at an offset from an otherwise tightly-knotted group in both ΔA and ϕ results in Figs. 3.16(a)-3.16(b). This is an expected result for the 2.5-5.5 V technology used;

(b) phase difference peaks above 182° for the I_{DD}=15.2 mA current dissipation; gain error performance remains practically unaffected (to within 0.25 dB) for each biasing point.

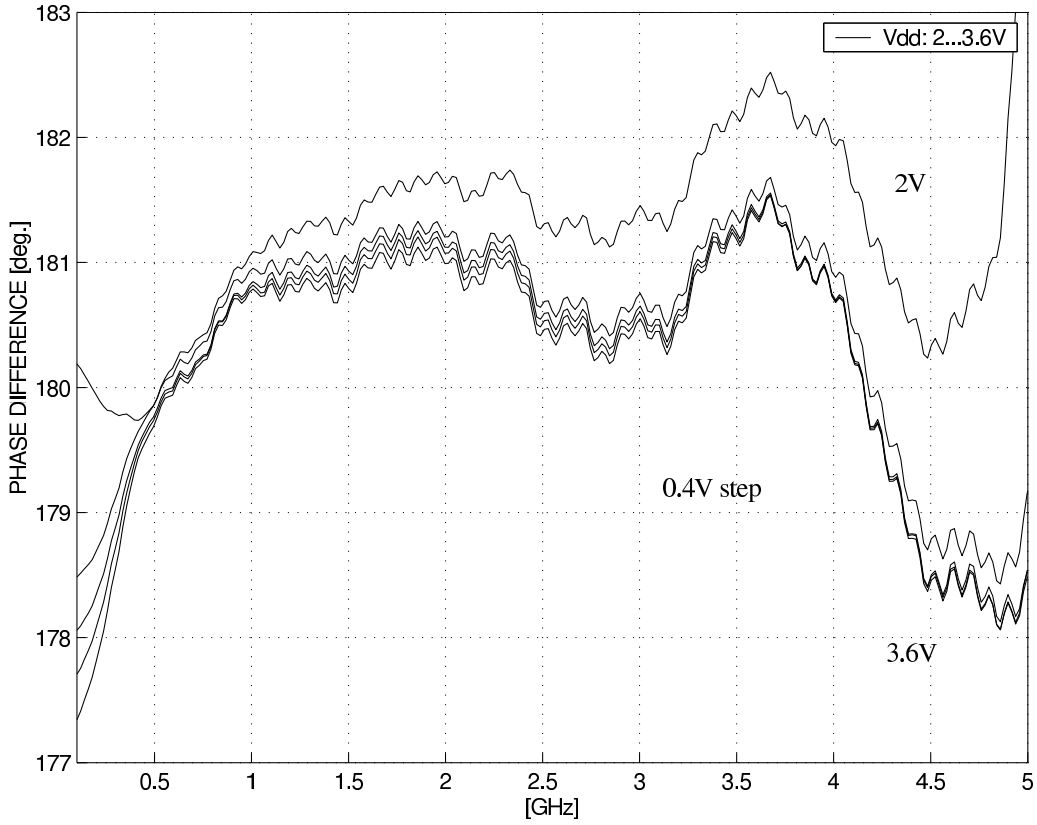
These results at different biasing points demonstrate the genuine robustness of the cascaded differential pair phase-splitter balun approach, while the use of inductor gain peaking and a passive broadband matching circuit aided the achievement of a near-decade phase-splitter performance with a regular SiGe technology. The proposed circuit compares well with the performance values reported for state-of-the-art solutions [54, 53], despite the fact that it is measured with output buffering intended for driving a difficult RC load in a quadrature modulator application.

3.5.5 Application to a broadband quadrature modulator

The proposed balun circuit was originally developed as an integrated single-input LO buffer for the direct-conversion quadrature modulator in [21]; this approach avoids the use of two parallel cascaded differential pairs and tuning circuitry, as in [46]. There were two design objectives for the proposed balun: 1) it should drive the quadrature modulator with a nearly perfectly balanced LO signal so as to give better spectral purity of mixing products, and 2) it should have high gain,

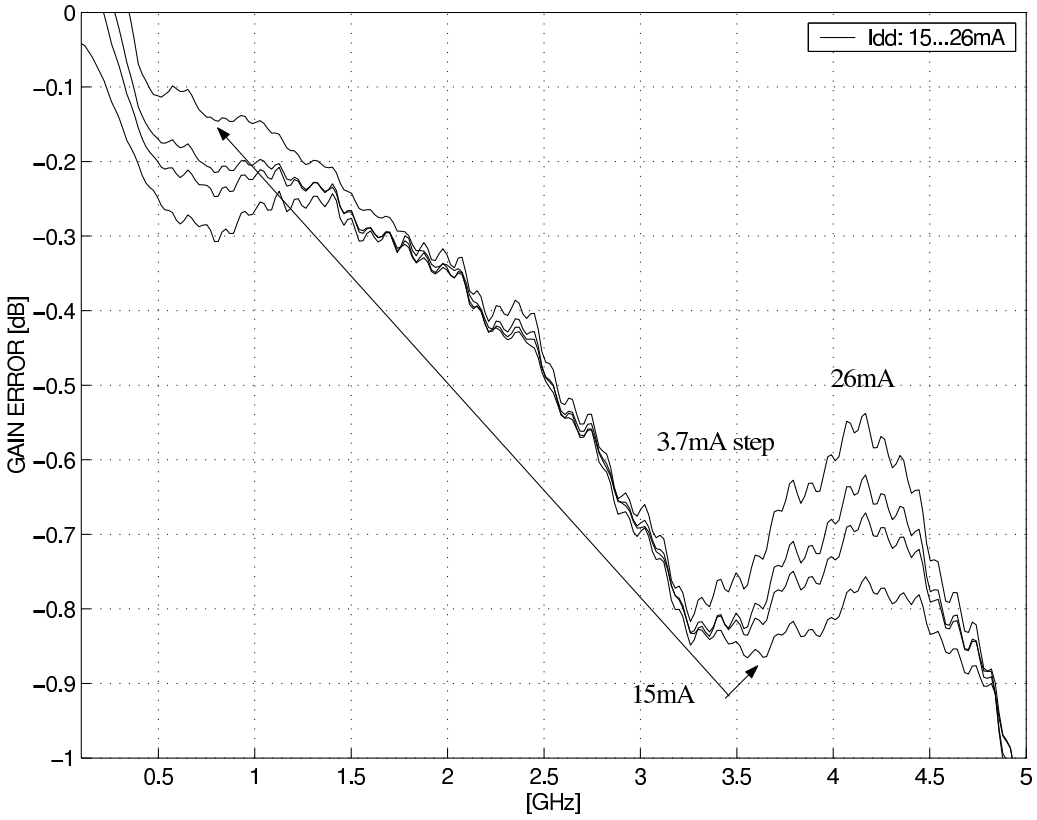


(a)

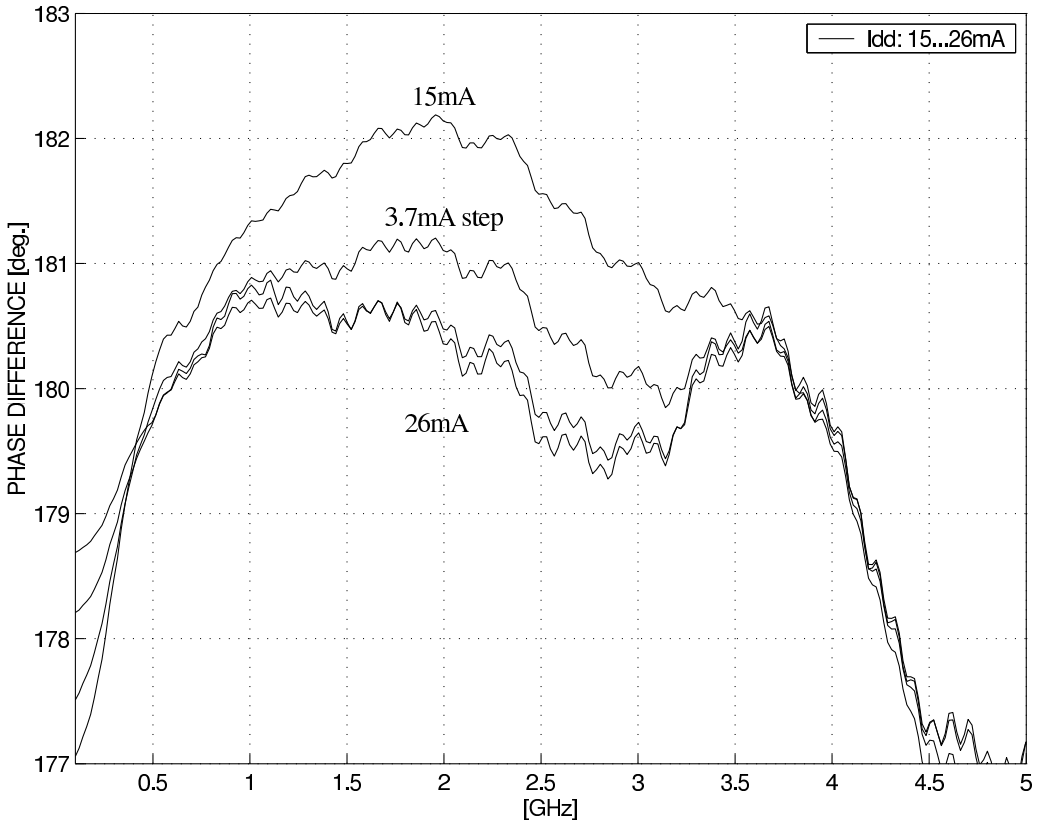


(b)

Figure 3.16: Measured (a) gain errors and (b) phase-differences vs. supply voltage V_{DD}.



(a)



(b)

Figure 3.17: Measured (a) gain errors and (b) phase-differences as circuit is biased to draw supply currents I_{DD}: 15...26mA.

Table 3.3: Quadrature modulator characteristics simulated with different LO buffers.

		ideal	proposed	diffpair
P_{OUT}	[dBm]	-17	-17	-17
IRR	[dBc]	-53	-50	-50
LO-rej	[dBc]	$-\infty$	-93	-61
3RD-rej	[dBc]	-48	-48	-48
2ND-rej	[dBc]	$-\infty$	$-\infty$	-98
N_{+20MHz}	[dBm/Hz]	-152	-146	-151
$\mathcal{L}$@500 kHz	[dBc/Hz]	-135	-128	-134
S_{22}	[dB]		-17	
S_{11}	[dB]	-4		-13
LO @2.4 GHz	[dBm]	-9	-21	-9
BB @1 MHz	[mv_{RMS}]		252	
I_{DD}	[mA]	25	47	35
V_{DD}	[V]		2.5	

so that the quadrature modulator can be driven with a low power LO source; this contributes to achieving a low LO leakage level at the quadrature modulator output.

To test whether the design goals were met, the quadrature modulator in [21] was characterized with three different LO buffers: the *proposed* phase-splitter circuit was compared against an *ideal* transformer and a single-stage differential pair (*diffpair*). The tabulated results in Table 3.3 indicate that better spectral purity with a lower LO power can be achieved using the proposed balun instead of a single differential pair.

The image-rejection ratio (IRR) and third harmonic (3RD) suppression are dominated by quadrature-generation accuracy and mixer distortion, but the suppression of even-order spurious products depends on the differential signal balance. The tabulated carrier (CRR) and second harmonic (2ND) rejection ratios show a definitive improvement for the proposed balun circuit. Second harmonics rejection even surpasses the -100 dB limit set for the use of $-\infty$ in Table 3.3. One obvious disadvantage of cascading is higher thermal noise; this will have an adverse effect on LO signal phase noise [61], but on the other hand the increased isolation of such buffering should prevent VCO pulling by the PA.

3.6 The realized 0.13 μm CMOS balun

For the CMOS realization of Fig. 3.3(b) a cascade of two buffered differential pairs was used; The near-submicron feature sizes of the 0.13 μm digital CMOS-process made possible a straightforward repetition of the 0.8 μm SiGe-balun design with a few key differences.

3.6.1 Implementation

The CMOS cascade implementation is shown in Fig. 3.18, connected as an LO balun with a 50 Ω termination at the unused input. The device benefits from its fine lithography with low parasitics

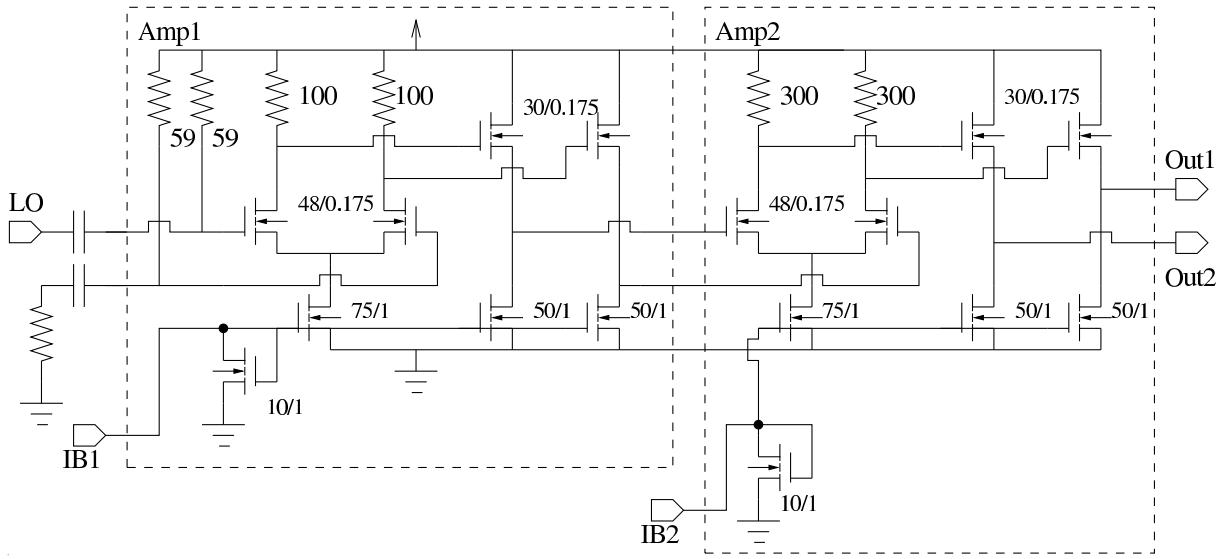


Figure 3.18: CMOS version of the cascaded differential pair phase-splitter circuit connected as a balun with the unused input terminated with 50 Ω to ground.

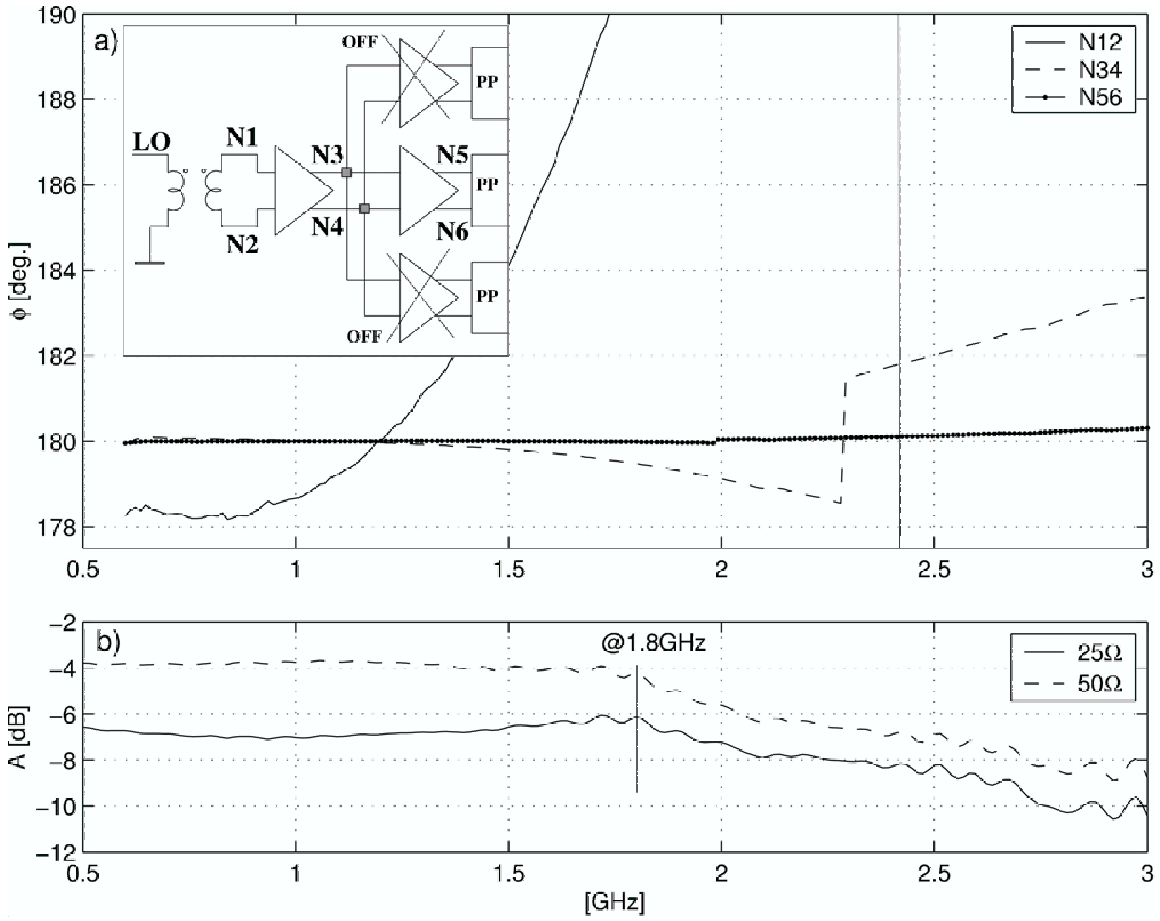


Figure 3.19: Simulated a) LO signal phase difference ϕ after each cascaded LO input stage, and b) voltage transfer function of the XFMR with ideal 25 Ω and 50 Ω loads.

Table 3.4: Comparison of integrated balun measured performances.

		[18]	[51]	[53]	[52]	[54]
ΔA	[dB]	-1	0.5	$\pm$1	1	$\pm$0.25
$\Delta\phi$	[deg.]	179.0:180.3	178:180.2	180$\pm$1	180.7:186	180$\pm$1
Op.range	[GHz]	0.4-3.7	0.5-4	0.5-4	0.5-5	0.2-5
S_{21}	[dB]	+7	-5	NA	NA	NA
I_{DD}	[mA]	23	NA	3.8	NA	NA
V_{DD}	[V]	2.5	NA	3	5	NA
Process	[μm]	0.8 (SiGe)	0.3 (GaAs)	0.5 (GaAs)	2 (GaAs)	1.0 (GaAs)
Type		amp	CGCS	amp	amp	amp
		2003	2003	1998	1996	1986

by rejecting the use of gain-peaking inductors as unnecessary for the intended range of applications in 0.8-6 GHz, and as another IC-area saving measure the LO port matching inductor and capacitors of the SiGe balun were replaced by resistive matching with 59 Ω integrated resistors to RF-ground. The resulting IC-area, excluding the pads, is 120 μm$\times$ 66 μm – a mere 0.8% of the respective SiGe balun area of 960 μm$\times$ 1060 μm. In contrast, because of the priority given to good matching between the differential signal branches, the drawn channel lengths were set to 0.175 μm instead of the process minimum of 0.13 μm. Although this means that a higher current has to be dissipated in order to achieve the same gain-bandwidth (GBW) performance, it is not a prohibiting factor for applications below 6 GHz since a 0.18 μm NMOS transistor already achieves an f_T of 72 GHz and an f_{MAX} of 28 GHz [62]. Larger transistor area should reduce mismatch-induced ΔA and $\Delta\phi$ [63], and combining this with good layout techniques such as multi-finger MOS transistors and the close proximity and similar orientation of the devices will contribute positively towards minimizing of mismatch related effects.

3.6.2 Application to a broadband quadrature modulator

In the final quadrature modulator application, however, it was necessary to use an off-chip surface mount transformer [64] for preliminary LO signal single-ended-to-differential conversion, as the bonding wire inductances disturbed balun performance. Ideally, the cascaded CMOS-balun should improve the coarsely balanced differential LO signal, as shown in Fig. 3.19: a simplified schematic of the LO buffering chain is inset in Fig. 3.19a, which depicts simulated phase balances. The simulated phase balances at the balun (N12), LO input amplifier (N34), and selection amplifier (N56) outputs have been extracted using a measured transformer s-parameter model supplied by the manufacturer. The resulting phase error graphs predict an almost perfectly balanced signal at the second amplifier output (N56), despite the less-than-perfectly balanced input from the off-chip balun (N12). This signal balancing effect will be limited by parasitics such as bonding wire inductances, and matching between the circuit devices. The inherent gain roll-off of the transformer from 1.8 GHz is shown in Fig. 3.19b, where its voltage transfer functions with ideal 25 Ω and 50 Ω loads are depicted. This is a limitation, as CMOS mixers need "hard" switching for proper operation.

3.7 Summary

In this chapter theoretical analysis has been applied to show that a cascade of two or more differential pairs is *fundamentally* more accurate as a phase-splitter than a single, stand-alone differential pair. Theoretically, a 40% mismatch in a single differential pair phase-splitter is converted to much smaller values of 5.7% or 0.9% by a cascade of two or three similar stages, respectively.

The measured amplitude error of the realized 0.8 μm SiGe balun is better than -1 dB up to 4.6 GHz, while phase difference stays between 179.7-180.9° in 0.6-4.1 GHz. This phase-splitter performance for a variation of nearly a decade in input frequency has been achieved without tuning. A comparison with other integrated baluns in Table 3.4 suggests equal or better performance than rival implementations in expensive GaAs processes. Biasing point sweeps produce near-nominal performance, so the circuit has good tolerance of variation in biasing point and parasitics. This claim for robust operation is backed by statistical simulations, which in fact predict improved tolerance of process variations for the proposed phase-splitter. Application of the phase-splitter to a direct-conversion quadrature modulator produces lower transmitted spurious signal levels at the cost of higher noise and power dissipation. However, as this performance has been achieved with lower LO power, it is possible to utilize this in frequency synthesizer design.

CMOS-implementation of the cascaded amplifier balun was only measured as part of an integrated direct-conversion quadrature modulator reported in [16, 19]. As this prototype was wire bonded to the printed circuit board (PCB), the limitations imposed by bonding wire parasitic inductances became apparent, and for partial compensation an off-chip coil-transmission line hybrid transformer had to be used. Better performance should be achieved by use of an integrated transformer to replace the off-chip balun, but most importantly the bonding wire lengths should be further minimized. In fact, a PCB redesign has been performed and the results will be further discussed as part of the text on quadrature generators.

4. Broadband quadrature generation

According to the quadrature modulator hardware list in Table 2.1, tunable RC-CR circuits dominated broadband LO signal quadrature generation until such techniques were recently replaced by different polyphase (PP) filter implementations. This is partially true, but the importance of div-by-2 circuits should not be underestimated; emerging technologies such as broadband quadrature VCOs should also be addressed for the sake of completeness.

4.1 Quadrature generator specifications

In [14], it is stated that in order to use the high bitrate modes of the 802.11a/g WLAN-standards [65, 66], transmitters (and receivers) should achieve better than 40 dB of sideband rejection; theoretically this translates to a maximum $\Delta\phi$ of 1.1° and to a maximum ΔA of 0.2 dB. Since these errors include both BB and LO buffering phase and amplitude errors, the quadrature generation block should, in practice, outperform the given 1.1°/0.2 dB level of *accuracy* in all process corners and in the given operating temperature range with a margin corresponding to the anticipated absolute element value variations. In practice, this translates to the design of a PP filter for a broader bandwidth than is actually needed. Realizing this in broadband operation at microwave frequencies is a demanding task: in this book broadband is defined as a device which operates over a frequency range covering at least an octave of bandwidth at gigahertz frequencies. Therefore low sensitivity of the realized quadrature generator to processing related mismatch errors is a design priority.

Broadband operation with sufficient gain is essential for easy multi-mode use of a quadrature modulator. Design scalability is also desirable; by scalability it is meant that the design is easy to understand and that it translates effortlessly from one technology to another. Therefore designs without tuning or post-fabrication steps should be favored as the most economical solutions. In contrast, the required quadrature generator linearity is a complex issue which has already been briefly discussed in Section 3.1. To summarize the prior findings, it seems that according to the developed theory (2.23), linear operation is not a design priority, as LO harmonics are not predicted to directly fold to the transmission band. This finding is readily supported by the popularity of the div-by-2 quadrature generation technique, which ideally produces square-wave LO signaling rich in harmonic content.

At the lower limits of the system dynamic range, noise should be as low as possible, since a noisy quadrature generation circuit increases LO signal phase noise and part of it leaks to quadrature modulator output to raise the system noise floor. This directly limits the transmitted signal-to-noise ratio (SNR) of the modulator. Apart from noise, a lossy circuit might attenuate LO signaling to such an extent that circuit phase noise performance might be jeopardized. Theoretically, a div-by-2 circuit excels in this regard, as circuit phase noise is reduced by the frequency division factor 2, and gain is high in such an active circuit. This advantage is only diminished by the fact that all div-by-2 implementations exhibit noise of their own, and this might somewhat reduce their phase noise advantage.

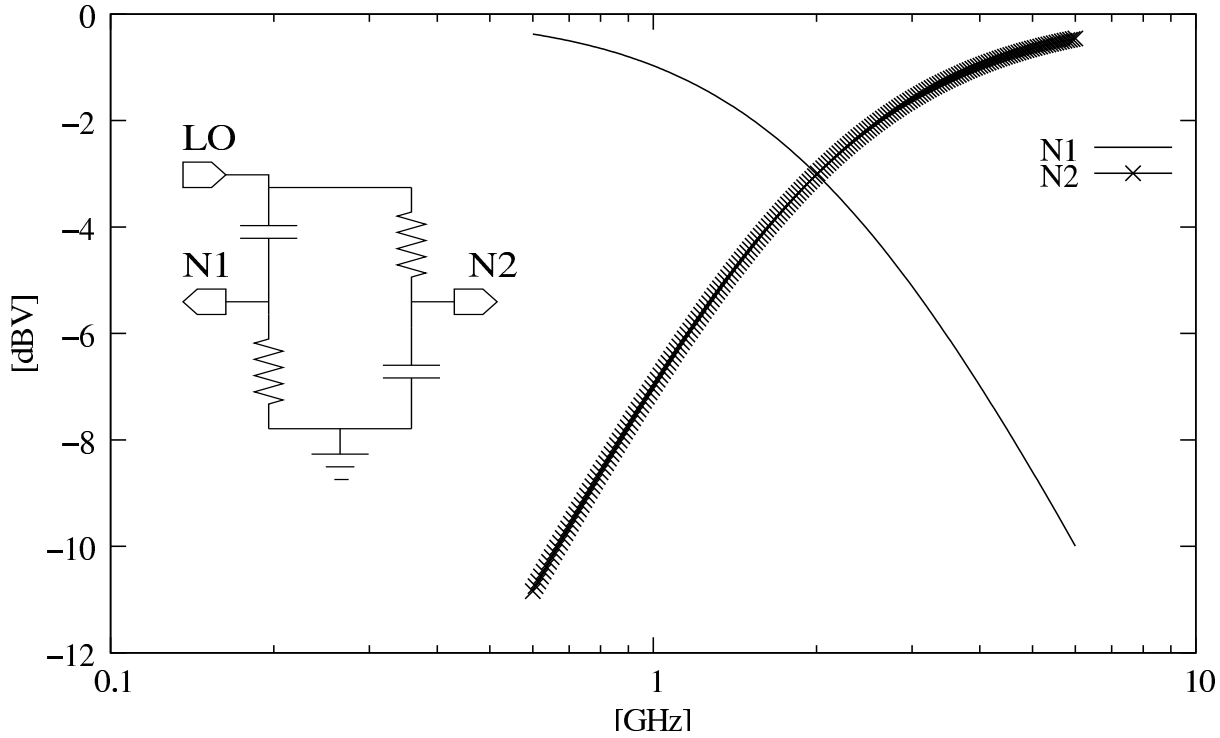


Figure 4.1: Amplitude responses of RC-CR loop in-phase (N1) and quadrature (N2) outputs with the schematic inserted.

4.2 Integrated quadrature generators

The following subsections will discuss the most prominent techniques for accurate broadband quadrature generation; actually, most of the topologies have been used in one of the tabulated reference quadrature modulators.

4.2.1 RC-CR quadrature generation networks

The basic RC-CR loop is not a broadband device because of its narrowband amplitude response, and this is apparent from the voltage-mode simulation results shown in Fig. 4.1, where a realized RC-CR quadrature generator has been inset. Designed for a center frequency of 2 GHz, the element values are 75 Ω and 1.06 pF. With ideal resistors and capacitors used, the simulated phase response is, ideally, at quadrature offsets over an unlimited bandwidth, and this could be usable in broadband quadrature modulators. Although implementation parasitics limit the achievable results, it is worth dwelling on a few basic RC-CR implementations and also to study more sophisticated methods used to utilize this basic block in broadband modulators.

The tuning of the RC-CR response can be realized e.g. by implementing the capacitors as varactors; these are tunable capacitors which are readily available in any bipolar process by different connections of the bipolar transistor [67]. By using such a varactor-tuned RC-CR network for LO phasing, [44] reported a direct-conversion quadrature modulator with an IRR performance of -35 dBc over an octave bandwidth of 0.8-2 GHz. However, the use of this approach requires the design of automated controlling circuitry, with its associated complexities.

In [45] the RC-CR network response is improved by buffering its output with limiter amplifiers, a technique which should equalize amplitude responses. The key to limiter usage for this purpose is the fact that with sufficiently high input signals amplifiers saturate and they produce effectively equal output amplitudes over relatively large input signaling variations. As a result,

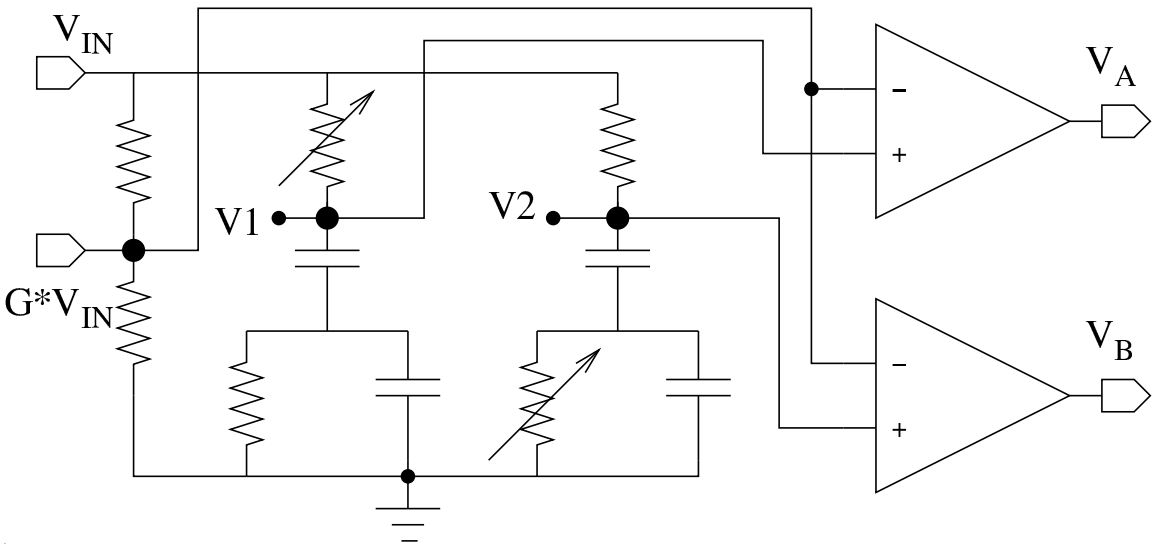


Figure 4.2: Principle of the allpass RC phasing network [46].

30 dB of sideband suppression was reported over an octave bandwidth of 1.2-2.3 GHz. The quoted IRR performance is not sufficient for forthcoming applications, and although the situation might be partly explained by the low reported f_T of the process at 15 GHz, this approach was rejected for fear of triggering AM-to-PM-conversion [34,43] of LO signaling resulting from the operation of limiter amplifiers in compression.

A similar effect is produced by the fact that the RC-CR loop technique is prone to harmonics, i.e. distorted LO signaling will convert to a finite phase error [28] if it is input to a system with a broadband 90°phase response. A time-domain T/4 shift should produce N times 90° phase shift for the Nth harmonic. If this is not the case, phase error will be produced.

4.2.2 Allpass RC networks

Allpass RC networks have been applied to quadrature generation with respectable results: an IRR performance of -40 dBc over a two-octave input frequency variation in 0.7-3.0 GHz has been reported [46]. A schematic illustrating the idea is shown in Fig. 4.2, and despite the increase of part count in comparison to the simple RC-CR loop, this device should tolerate fabrication mismatches fairly well. A normalized allpass filter design theory and the required number of stages for a given IRR over a specified range of frequencies were developed in [68]. However, analysis of the proposed allpass quadrature generator network in [69] reveals that tuning is necessary to make it work for modern OFDM-modulated communications devices, since the best possible ΔA and $\Delta\phi$ performance quoted is 0.5 dB and 2° in 0.7-3.5 GHz, respectively.

4.2.3 Feedback RC networks

Feedback with RC networks is an old idea, but in this chapter the term refers to the improvement of the quadrature generation performance of an RC-CR loop by using them. In [43] buffered RC-CR quadrature outputs are sampled and integrated to control the tunable resistors in the RC-CR loop of a 0.25-4.0 GHz IQ modulator for a general-purpose test signal generator. This feedback loop-enhanced RC-CR quadrature generator is equipped with limiting post-amplifiers in order to improve amplitude matching to cover the required broadband performance with a variation of over four octaves in input frequency. With these measures the quadrature modulator stability vs. time and temperature is improved to such an extent that the measured IRR=-60 dBc at 880 MHz

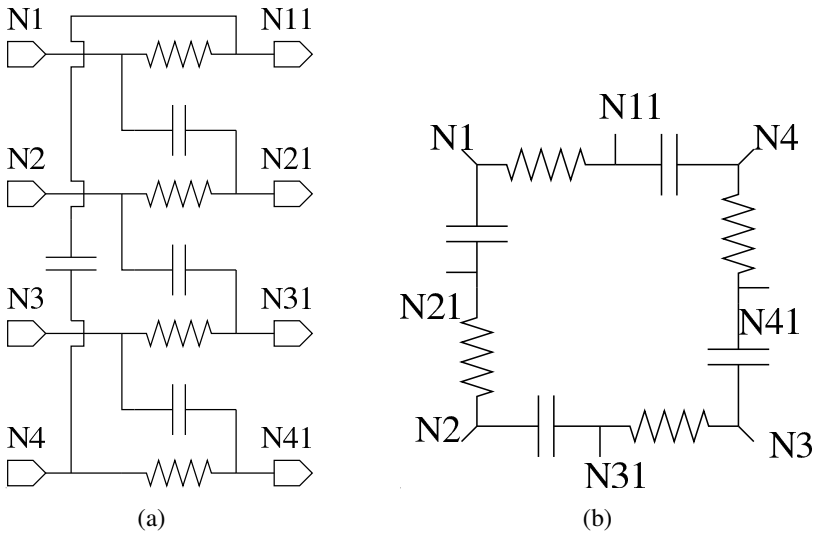


Figure 4.3: (a) A single polyphase filter stage, and (b) its ring representation.

over a 24 h time period and a 30°C temperature variation is shown. Without feedback the IRR varies in relation to ambient temperature from below -70 dBc up to -40 dBc, but the system uses post-fabrication calibration to achieve this performance.

4.2.4 Polyphase quadrature generation

Polyphase filtering for quadrature generation was originally proposed by Gingell [70] under the name *Sequence Asymmetric Polyphase Networks*. Gingell's term *asymmetric* refers to the ability of a PP network to selectively pass or attenuate signals according to phase; this type of network belongs to the Hilbert class of filters and its functional asymmetry is utilized in direct-conversion receivers to attenuate unwanted channels. In contrast, a PP filter schematic is *symmetric*, as shown by the single polyphase filter stage in Fig. 4.3. Since a single-stage PP filter is, in most cases, too narrowband to tolerate absolute resistor and capacitor value variations, applications usually use a higher number of stages. Two- to three-stage polyphase filters are mostly used, as the number of stages is limited by concerns about available quadrature accuracy over a given BW vs. the amount of loss which can be tolerated. A three-stage PP filter with typical in-phase (p) and out-of-phase (m) LO connections is depicted in Fig. 4.4; in it each successive stage improves differential LO signal phasing to quadrature over a given bandwidth. In fact, the LO connection shown produces only phasing error, while its amplitude balance is perfect and limited only by the differential LO input balance. This situation changes with different versions of LO input connections; by e.g. grounding two of the filter inputs, part of its error is shifted to the amplitude domain; in [71] coarsely pre-generated quadrature LO signaling was input to a three-stage PP filter to avoid the inherent 3 dB loss associated with the differential-to-quadrature conversion.

Functional asymmetry was utilized in [72] to develop voltage-mode expressions for the relation of in-phase and quadrature outputs V_I/V_Q, which are now defined as V_I=V_0-V_{180} and as V_Q=V_{90}-V_{270} with reference to the three-stage PP filter schematic shown in Fig. 4.4. The output expression has been derived for an ideal polyphase filter with Rin=0, $R_L = \infty$, and C_L=0 and it is given as:

$$\frac{V_Q(s)}{V_I(s)} = \frac{s\left(R_1C_1 + R_2C_2 + R_3C_3\right) - s^3\left(R_1R_2R_3C_1C_2C_3\right)}{1 - s^2\left(R_1R_2C_1C_2 + R_1R_3C_1C_3 + R_2R_3C_2C_3\right)}, \text{ where } s = j2\pi f. \quad (4.1)$$

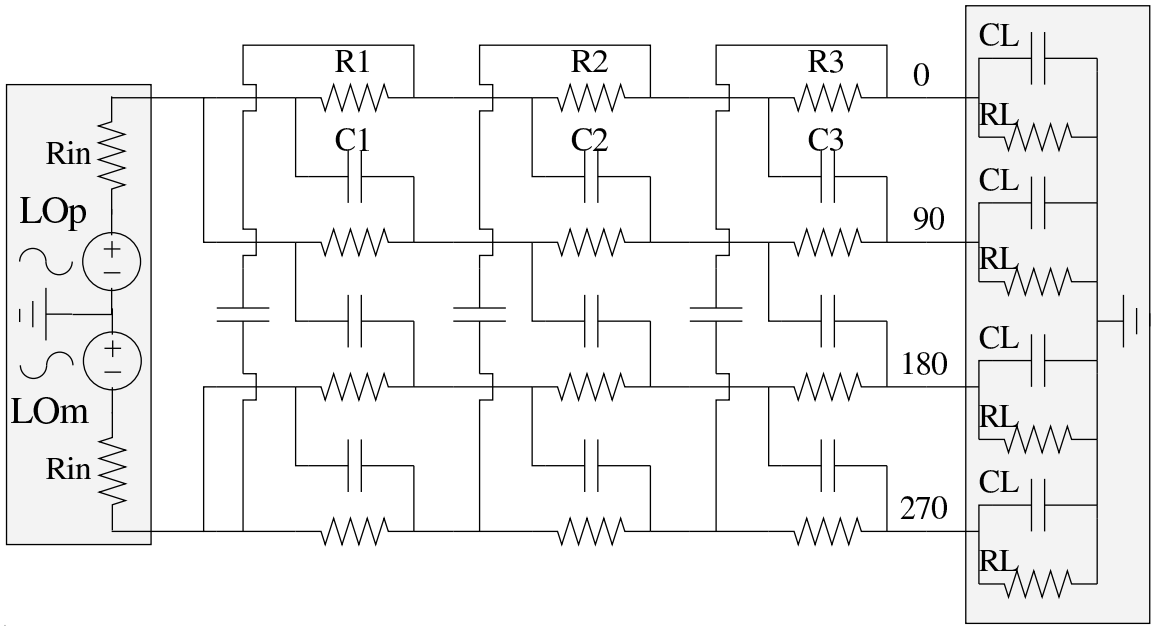


Figure 4.4: A three-stage polyphase filter converts the differential LO signal to four quadrature phases.

If an equiripple implementation is assumed with logarithmically spaced poles, it is possible to develop comparison graphs for available IRR vs. bandwidth for any number of stages, but such graphs for Hilbert filters are already available in e.g. [73, 68]. Study of these graphs shows the effect that variations in the absolute RC value have on the available IRR performance: a $\pm 20\%$ RC time constant variation widens the application bandwidth correspondingly, thus reducing the available IRR for any given filter. In contrast, a polyphase filter tolerates mismatches well: a worst-case IRR=-45 dBc for a quadrature generator with an octave bandwidth for 100 Monte-Carlo runs using a 1% un-correlated device mismatch model was simulated in [72]. The bulk of the results lie close to ideal performance, with σ-values at 0.24° and $4 \cdot 10^{-4}$ for phase and amplitude errors, respectively. The simulations predict decreasing σ-values with an increasing number of stages, with the given σ-values corresponding to an IRR of -54 dBc for the cited 3-stage case.

Three-stage polyphase filters were used in two of the tabulated reference modulators shown in Table 2.1 to achieve IRR values better than -34 dBc over a bandwidth of two octaves [40, 42], respectively. The achieved IRR performance is in line with the predicted -40 dBc performance [73] for an ideal three-stage implementation for a two-octave bandwidth. The 6 dB difference between the ideal and reported results is the cumulative effect of imperfect differential signaling, device mismatches, and the natural difficulty of reducing circuit performance at higher frequencies. Withal, apart from the concerns about gain bandwidth presented, loss remains as the main possible brake on the use of PP filter, mainly because of its detrimental effect on LO phase noise performance. However, inaccurately generated IQ signaling reduces sideband rejection, and the PP technique excels in this regard, with good tolerance of device mismatches. A two-stage polyphase filter has in fact been shown as a viable alternative for LO phasing [13] to realize a transceiver which fulfils the specifications of the 802.11a/b/g WLAN variants without tuning.

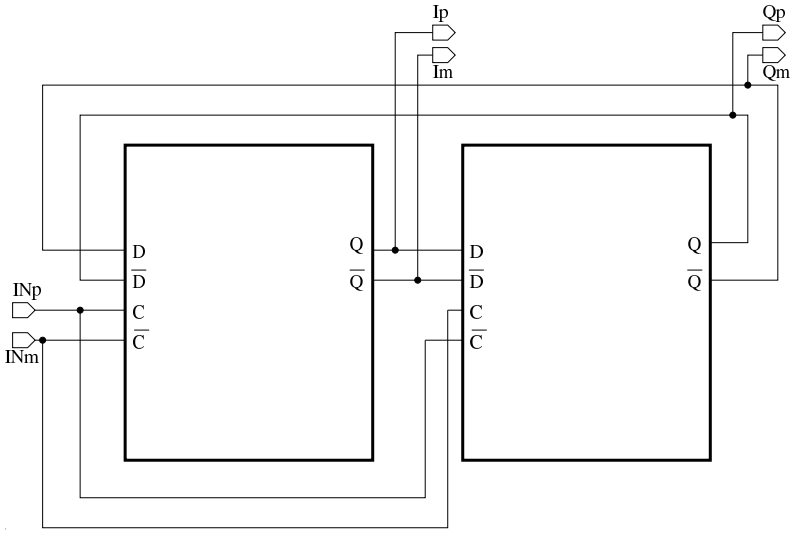


Figure 4.5: Div-by-2 circuit realized with D-flip-flops.

4.2.5 The div-by-2 quadrature generator

The div-by-2 quadrature generator shown in Fig. 4.5 is well-known, possibly as it is easily realizable for high-frequency operation with emitter-coupled logic (ECL) D-flip-flops. The technique works well both in bipolar and CMOS technologies, and prototypes have been tested for this work in both technologies. The annotations in Fig. 4.5 use the characters 'p' and 'm' for positive and negative differential signals, respectively; correspondingly e.g. the input pins were annotated with 'INp' and 'INm' instead of the 'LO' labeling usually used in this work to emphasize that the VCO now has to operate at twice the transmission LO frequency. This can also be seen as an advantage, as LO pulling is no longer a hazard as a result of the PLL operating at a different frequency than the PA. As already mentioned, circuit phase noise performance should also be good, providing there is no excess penalty in designing the VCO/PLL to operate at twice the transmitted frequency.

The div-by-2 approach requires a perfectly bi-phased clock signal with a 50% duty cycle, i.e. differential LO signaling with 0 dB/0° amplitude and phase errors, respectively. Producing such accurately differential signaling at twice the transmitted frequency is a difficult task, even with an on-chip VCO realization. In a broadband multimode direct-conversion quadrature modulator with an externally generated LO signal, this is a major performance limitation. For example, if the single-ended-to-differential conversion is performed by using an external surface-mountable hybrid chip transformer, its amplitude error could typically be ca. 3 dB and the phase error several degrees up to 3 GHz. Better differential signaling can be achieved through the use of cascaded differential pairs as an integrated balun [17,18]. However, even this approach produced an amplitude error of 1 dB and a phase error of ca. 1° below 4 GHz, with non-existent bonding wires and their parasitic inductances (co-planar waveguide probes were used). The imperfect LO signaling could also be corrected by using a cascade of two div-by-2 circuits or with an adjustable correcting circuit [74]. Both approaches have limitations: 1) the problem with the cascaded div-by-2 approach is that it requires the LO signal to be generated at 4 times the application frequency, while it is still subject to element mismatch errors, and 2) the patented correcting circuit approach requires the application of an external tuning voltage, and its application band might be limited by the realized feedback loop.

The continuation paper [75] on the feedback loop approach should be mentioned as it presents test data on a div-by-2 performance as it is driven by distorted LO signaling. To ac-

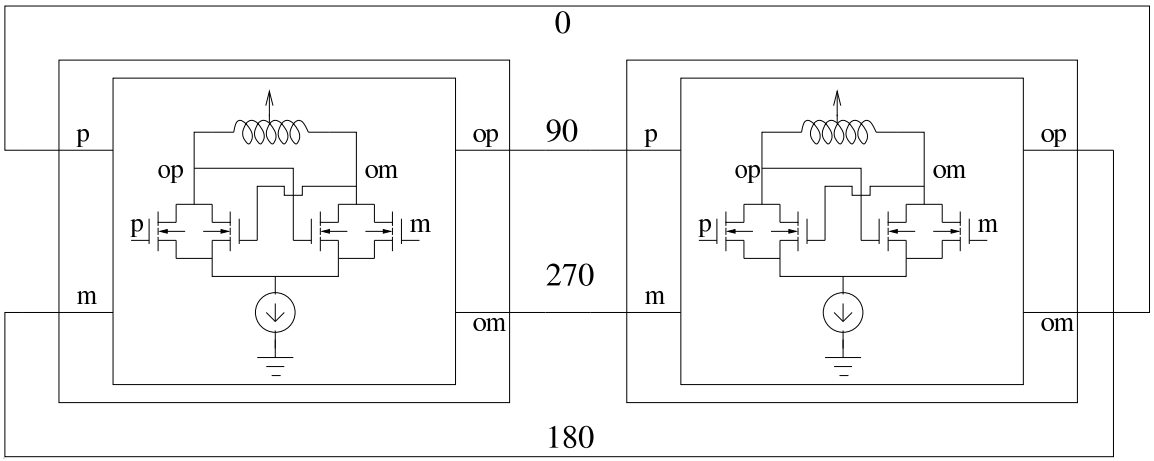


Figure 4.6: Two VCOs connected as a QVCO to produce LO phases at 90° offsets.

complish this, a non-linear amplifier was used as an LO input buffer, and it was cascaded with a variable attenuator for power control purposes. The resulting signaling input to the div-by-2 circuit had a duty cycle of 66%, which naturally produced IQ signaling with a large, 30°, phase error. The issue here is whether the signal imbalance was caused by harmonics or just by badly-balanced differential amplification. The latter was eliminated in the paper by producing results on the feedback div-by-2, as it was driven with both distorted and pure sinusoid signaling at different input powers. The results show that a linear-in-decibels relation between the phase error vs. input power was established when the circuit was driven with the distorted source. This phenomenon did not occur with the pure sinusoidal source, at least not until the input powers increased and distorted the loop circuitry.

4.2.6 Quadrature VCOs

The feedback configuration of two oscillators as a quadrature voltage-controlled oscillator (QVCO) forces an interleaved mode of oscillation on the individual VCOs; otherwise, the waveforms cancel and no oscillation exists. This produces the quadrature phases (0/90/180/270) shown in Fig. 4.6. The topology was first suggested in [76] for use in the 900 MHz frequency range and later implemented with modifications in 0.35 μm CMOS for the 1.8 GHz band in [77]. Both implementations produce accurate quadrature signaling: the first achieves an IRR of -46.5 dBc at 830 MHz, while the latter paper reports better than -52 dBc over the tuning range from 1.55 GHz to 1.85 GHz, with measured phase noise at better than -140 dBc/Hz at a 3 MHz offset from the carrier. Clearly, the given performance is otherwise acceptable, but the given tuning ranges do not meet the requirement for an octave bandwidth, and the addition of buffering to avoid PA pulling could reduce application bandwidths somewhat.

A substantially wider tuning range was realized in [78], where a 0.13 μm CMOS technology was used to realize a continuously tunable QVCO operating from 0.75 to 2.2 GHz. On the schematic level, the proposed LO synthesizer uses the well-known offset mixing principle for LO generation by multiplying the original oscillation waveforms with another signal to form the final desired carrier frequency. In this case the offset frequency was synthesized by dividing the original LO signal by 2 or 4; this method widens the initial $\pm 20\%$ tuning range of the QVCO to $\pm 50\%$. Thus an application bandwidth of nearly two octaves is shown, but the reported phase noise performance is mediocre, with a worst case value -120 dBc/Hz at a 1 MHz offset from the 2.185 GHz carrier. Since tuning is needed to correct the reported worst-case $\Delta\phi$=6° performance

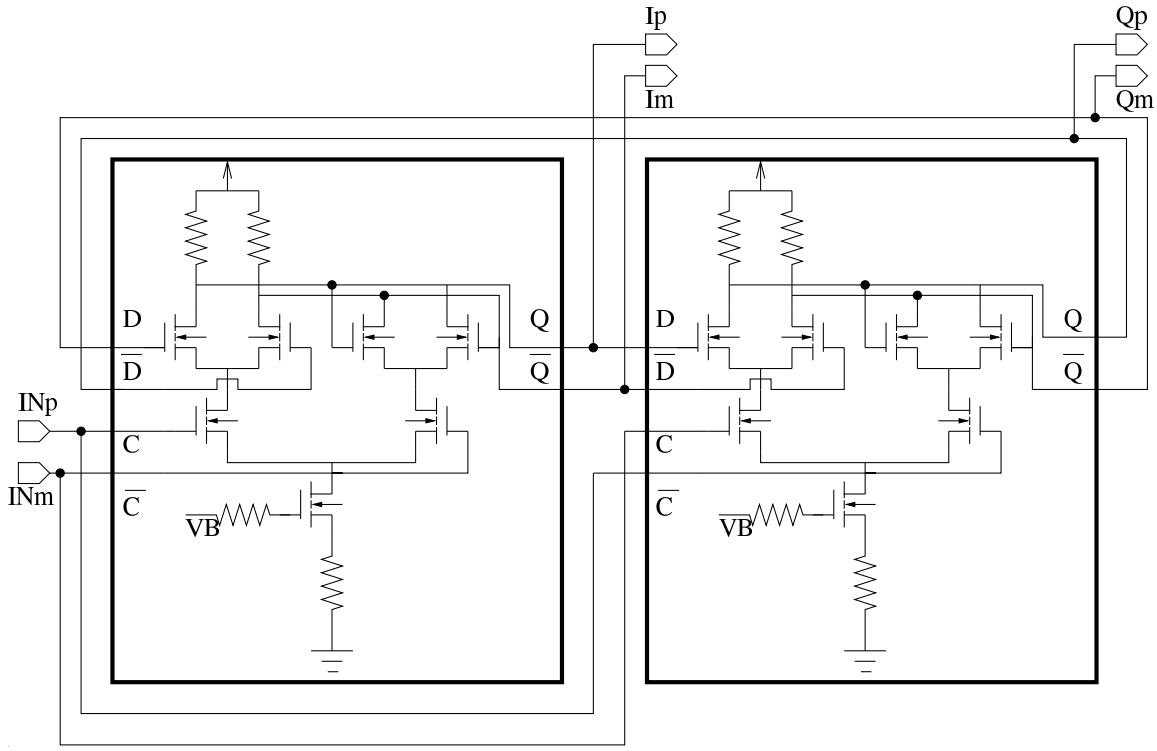


Figure 4.7: Div-by-2 cell realization in 0.13 μm CMOS.

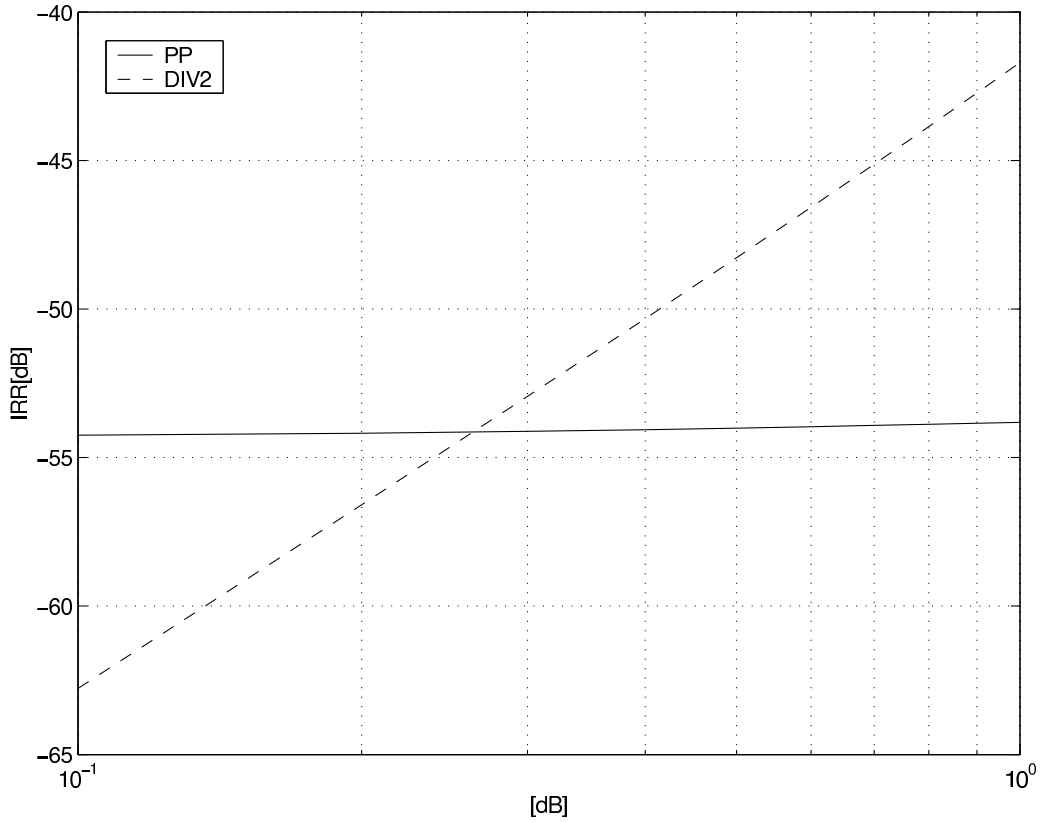
to a value of 2°, and prominent spurious products are shown, this approach does not fall within the acceptable limits of this thesis.

4.3 The tested 0.13 μm CMOS divider

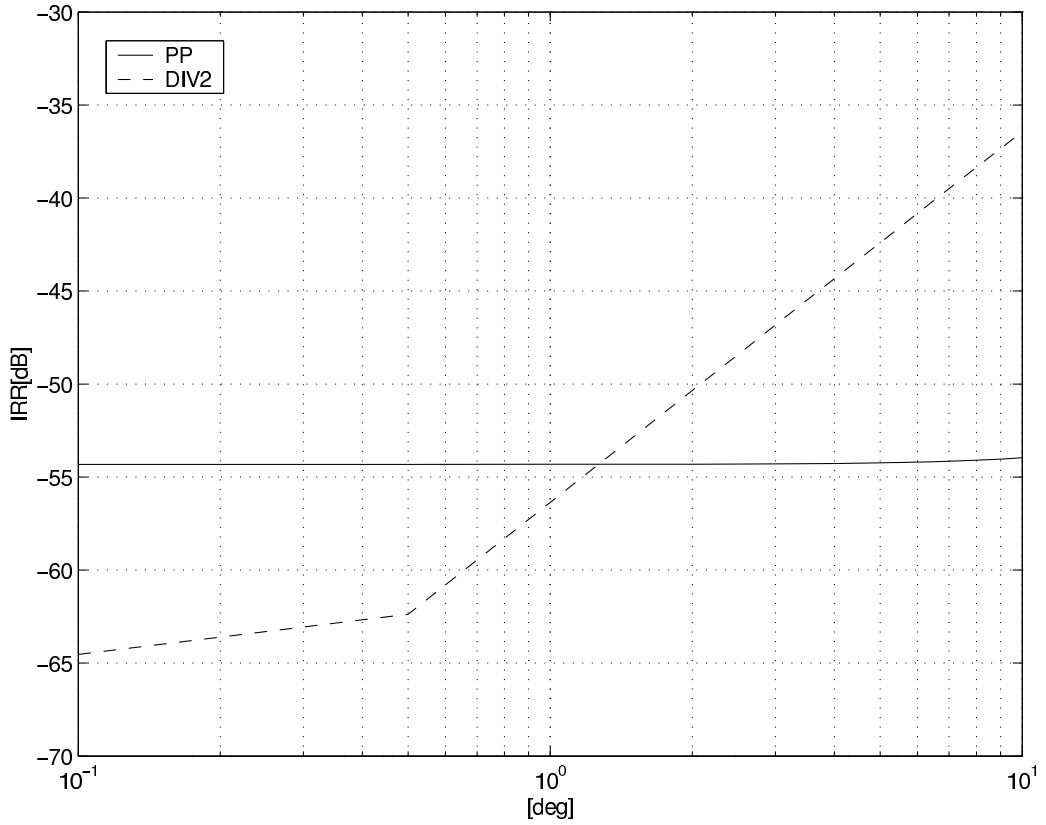
The CMOS realization of the ECL D-flip-flop div-by-2 circuit is shown in Fig. 4.7. Designed in 0.13 μm digital CMOS, the device is DC stable and its implementation is straightforward. To quantify the effect of amplitude and phase errors on this div-by-2 performance, the CMOS realization in Fig. 4.7 was used to drive two mixers connected as a quadrature modulator. Amplitude and phase errors at the 4 GHz LO input frequency were swept between 0.1-1 dB and 0.1-10°, respectively. The simulated IRR results are compared in Figs. 4.8(a)-4.8(b) to the data which were obtained by driving the quadrature modulator by a 3-stage buffered polyphase filter at 2 GHz. By means of a comparison of the best broadband balun performance given in this work (1 dB/1°) to Figs. 4.8(a)-4.8(b), we extrapolate IRR values of -42 dBc and -57 dBc, which means a performance for the div-by-2 case that is inferior by ca. 12 dB. Combining this result with the fact that typical balun performance is much worse than (1 dB/1°), it is expected that polyphase filtering should produce better image rejection in the presence of practical differential signaling.

4.4 The tested 0.4 μm complementary SiGe dividers

The 0.4 μm complementary SiGe div-by-2 circuit shown in Fig. 4.9 was developed as a response to the limited low-voltage performance of the classic three-stacked transistor circuit (obtained by replacing the NMOS transistors with properly dimensioned NPN ones). The two-stacked transistor topology is low-voltage-compatible, but depending on dc block values which are integrable its low-frequency performance is limited. The divider action might mitigate this low-frequency



(a)



(b)

Figure 4.8: IQ modulator IRR performance vs. a) amplitude, and b) phase error, when it is using a div-by-2 (DIV2) or a 3-stage polyphase filter (PP).

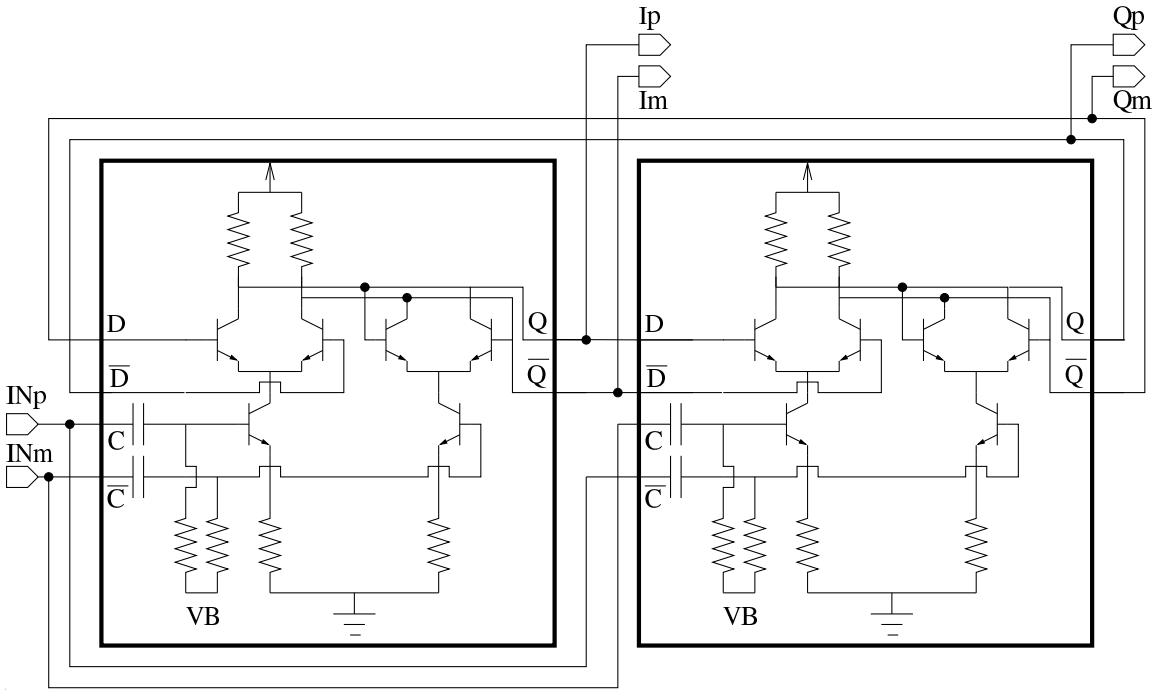


Figure 4.9: Div-by-2 cell low-voltage version in a 0.4 μm complementary SiGe-process.

vs. die area tradeoff as the signal input is at twice the desired output frequency. This means that the input dc blocks can be designed to be smaller for a given lowest desired frequency-of-operation. Nevertheless, when high-frequency operation was tested using a 3.3 V supply, the divider action of the classic div-by-2 circuit ended at an output frequency of 2.2 GHz, whereas the developed low-voltage div-by-2 continued to operate up to 3.4 GHz.

4.5 The realized 0.8 μm SiGe polyphase network

The first of the two quadrature generators realized for this thesis is a brute force approach for accurate broadband quadrature generation: the resulting five cascaded stages shown in Fig. 4.10 were designed with their nominal pole frequencies at 0.5, 1.0, 1.9, 3.4, and 6.7 GHz. Quadrature modulator application [18] of this multistage PP filter resulted in an IRR performance better than -40 dBc in 0.75-3.6 GHz, as the quadrature generator was driven by the integrated cascaded differential pair balun shown in Fig. 3.11. This approach, with its higher-than-usual number of PP filter stages, was used in order to test Gingell's [70] premise that each consecutive stage improves signal phasing, and that only last-stage components need tolerances commensurate with the stop band requirements. Thus the largest resistor values of the designed polyphase RC network were implemented furthest from the LO inputs shown. This practice of successively raising resistor values is also recommended in [73], and simulated values predict a +2 dB gain increase with this arrangement as compared to a reversed order of resistors.

Still, the application of such a high number of stages in cascade results in a nominal loss of ca. 15 dB in the filter passband, which it is uneconomical to compensate for, especially at microwave frequencies. A closer look at the simulated results, however, suggests that the amount of loss saturates in such a way that the response of a five-stage filter is virtually indistinguishable from that of a three-stage one. Another enabling factor is the bipolar technology used, which has transistors that do not require switching to be as hard as CMOS transistors would. Therefore, contrary to the limiting amplifier buffering [45] technique, no amplifying stage was inserted after

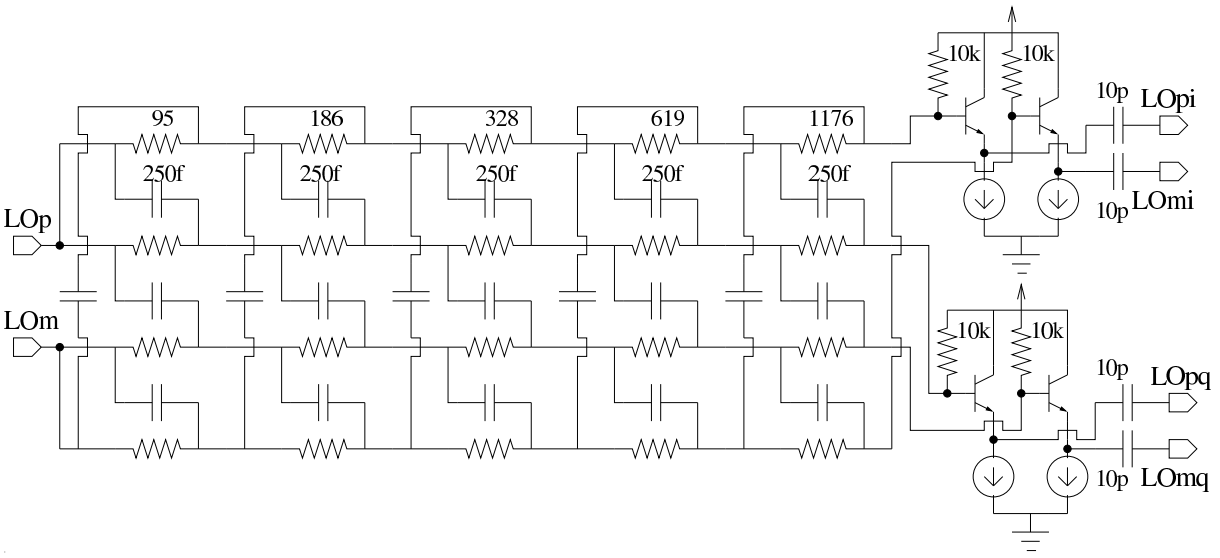


Figure 4.10: The 5-stage buffered polyphase filter realized in 0.8 μm SiGe.

the polyphase filter; only emitter-follower stages drive the quadrature modulator mixers with the generated quadrature signal. The use of bipolar transistors allows this, as the switching quad NPN devices saturate quickly as a result of exponential transfer characteristics ($I_C=I_S e^{V_{BE}/V_T}$, where V_T=26 mV at room temperature). This early onset of saturation limits the attainable performance increase from amplified LO signals, while the benefits of emitter-follower stage buffering include: reduced system complexity; reduced power dissipation; no high-value Miller capacitance loading of the polyphase filter, and minimum possible distortion of the quadrature signaling.

4.6 The realized 0.13 μm CMOS switchable PP

The second quadrature generator for this thesis was implemented in a 0.13 μm digital CMOS technology. The chosen technology precludes the use of a very high-degree PP filter, since CMOS mixers require "hard" clocking with high LO signal amplitudes, and delivering it would be problematic without limiters. Nevertheless, to cover over two octaves of input frequency with an IRR performance -40 dBc or better, four or more polyphase filter stages have to be cascaded [73, 68]. To compensate for the loss of a four-stage polyphase filter, buffers could be inserted in the filtering chain [41], but this solution might interfere with the polyphase filtering action and distort quadrature phase generation.

One possible solution is the use of parallel switchable polyphase filters for broadband quadrature generation, as proposed in [16, 19]. Parallel PP filters allow good broadband IRR performance, while minimizing the losses inherent in PP filtering. The schematic of the proposed quadrature generator in Fig. 4.11 depicts three parallel polyphase filter blocks implemented for different operating bands. The filter blocks are labeled I, II, and III, corresponding to their nominal application bands of 0.8-1.6, 1.6-3.2, and 3.2-6.4 GHz. Beneficially, these filters should combine to produce an accurate quadrature response over a three-octave bandwidth, with a much higher IRR than could be achieved using a single PP filtering block. This virtual higher-degree polyphase filter operates without the inherently high loss of such a physical device. Selection between different operating bands is straightforward, through amplifier bias currents, since differential pairs are used as switches. Each filter has a bias current input Iselect for a current

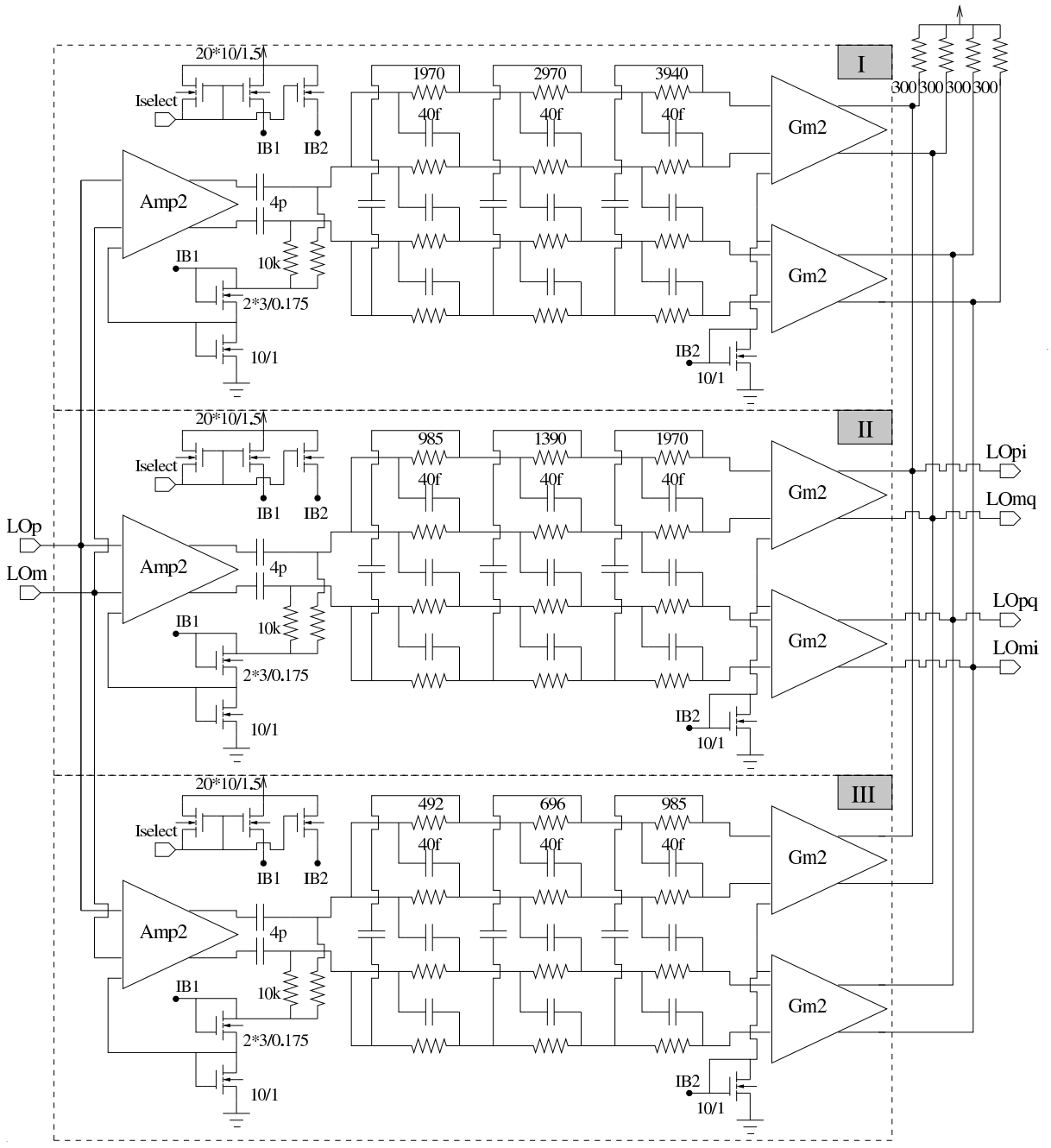


Figure 4.11: The parallel switchable polyphase filter quadrature generator realized in 0.13 μm digital CMOS.

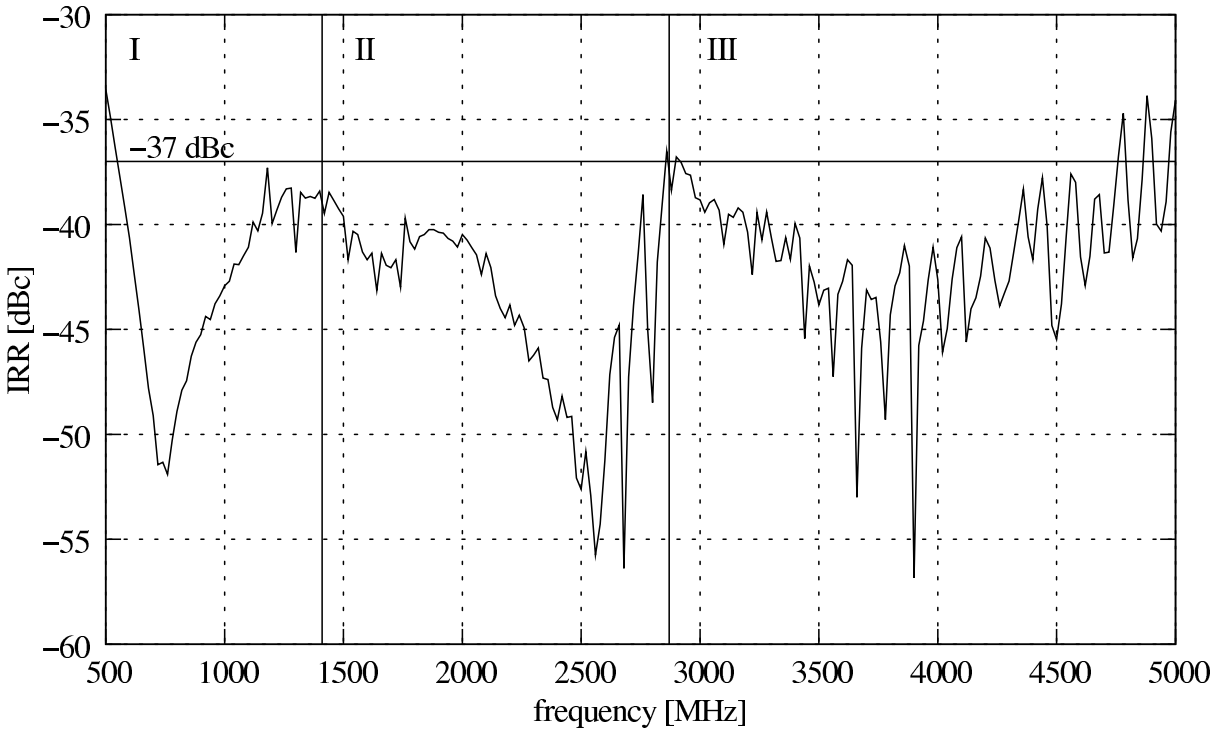


Figure 4.12: The realized switchable PP filter performs accurate quadrature generation for a variation in input frequency of over three octaves.

mirror, which distributes bias to the input and output buffers through the bias taps Ib1 and Ib2. To reduce current dissipation, the biasing chains are scaled to a current mirroring ratio of 1:10 to the main devices. The output buffers are labeled Gm2 to signify the fact they are copies of the transconductance part of the input buffer Amp2, and that their outputs are loaded with the shared 300 Ω loads. The use of four resistors instead of 12 simplifies the connection of the LO signaling to the mixers.

Each application frequency band could have tailored buffering and/or a different number of RC stages. Thus, the quadrature modulator response could be equalized by the application of higher power or by using a smaller number of stages at higher frequencies. In this first prototype, however, each switchable polyphase block has a similar 3-stage topology. To study the performance available, SPICE models for an off-chip balun, for a 0.3 nH lumped element approximation of bonding wires, and for bonding pads were added to the proposed PP filter quadrature modulator application. The resulting simulated image-rejection performance of around -60 dBc agrees well with the theory [68]. Simulated quadrature modulator single-sideband (SSB) spectra predict +7 dB higher output power for the proposed circuit at 1.96 GHz than that obtained using a 4-stage comparison network. This output power difference increases to +9 dB at 2.4 GHz with gain roll-off. Thus a quadrature modulator-circuit produces 5-7$\times$ more power with the proposed technique. Adding this much compensating gain to the output buffer increases current dissipation and is bound to produce spurious effects and noise harmful to signal integrity. Thus it should be noted that both of the 4- and 3-stage networks produce IRR results comparably around the -60dBc level at 1.96 and 2.4 GHz (-0.5 to +3.6 dBc for the proposed 3-stage technique). With its superior power output, the proposed technique consequently looks like the best alternative for practical broadband quadrature generation in the lower microwave range.

Testing the circuitry with two different PCBs which only differed in bond wire lengths established the predicted sensitivity of the cascaded differential pair balun operation on bond wire

Table 4.1: Comparison of measured quadrature generator performances.

		IRR [dBc]	Op.range [GHz]	$\overline{\text{Op.range}}$	Type	Tech.
[16][1]	2004	-37	0.56-4.76	8.5	xPP3	0.13 μm CMOS
[18]	2003	-40	0.75-3.6	4.8	PP5	0.8 μm SiGe
[78]	2005	-34	0.75-2.2	2.9	QVCO	0.13 μm CMOS
[10]	2005	-39	0.1-2.6	26	div-by-2	0.13 μm CMOS
[40]	2004	-34	0.7-2.7	3.9	PP3	SiGe
[41]	2001	-28	0.8-2.7	3.4	PP2-amp-PP2	compl.bip.
[42]	1998	-35	0.6-3.0	5	PP3	0.25 μm CMOS

[1] Measured for this book with improved PCB.

inductances (ca. 1 nH/mm). The second, improved, PCB with 1 mm shorter bonding distances yielded an IRR=-37 dBc in 0.56-4.76 GHz instead of the previously reported IRR=-39 dBc in 0.6-2.5 GHz. The seemingly huge difference between the two test sets is easily explained by the deterioration of the LO balun performance: simulated values predict limited single-ended-to-differential bandwidths with increasing bonding wire lengths. Therefore the second PCB with 1 mm shorter bonding wires is capable of accepting LO input from bulky SMA-baluns, which operate far beyond the 3 GHz upper limit of the hybrid one. This second set of IRR results is repeated in Fig. 4.12, with the realized usable ranges of filter blocks I, II, and III annotated to it.

4.7 Summary

In this chapter different broadband quadrature generators have been analyzed, and the results of their quadrature modulator applications are collected in Table 4.1. On the basis of these results, the quadrature generators proposed for this work can be said to combine the best IRR performance for the broadest bandwidths, rivaled only by the div-by-2 approach. However, the latter has a limited upper frequency at 2.6 GHz.

To summarize the findings of this chapter, a div-by-2 quadrature generator should always be used if the specifications can be met with it, because in this way hardware design time is kept short, no LO pulling occurs, and there is a possible phase noise advantage. A polyphase filter, either switchable or not, might be the best alternative if the IRR specifications are demanding, differential signaling is inaccurate, or if designing a frequency synthesizer for the $2\times$ frequency required by the div-by-2 block is too costly.

5. Up-conversion mixers

According to the quadrature modulator hardware list in Table 2.1, the Gilbert mixer or one of its modifications is used in six out of the eight reference modulators, whereas the two remaining circuits utilize resistive mixer topologies. Incidentally, the Gilbert cell in Fig. 5.1(a) could also be called the Bilotti cell with equal justification, as it was originally proposed by two independent authors in the 1968 ISSCC, and later both were reported in the JSSC special issue on the conference [79, 80]. However, in keeping with common practice this work uses the term *Gilbert mixer* or *Gilbert cell* for this mixer. The following material will first discuss broadband up-conversion mixer specifications, with emphasis on the Gilbert mixer, and this material is followed by a description of the mixers used in the tabulated reference modulators. Analysis of the four mixers realized for this work will conclude this chapter.

5.1 Mixer specifications

To limit the scope of this work, it is prudent to say that Gilbert mixer operation has been thoroughly described over the years in well-known texts such as [36]. Barrie Gilbert has also devoted a few pages to the subject in [47], which covers other RF mixer topologies, too. Academic work has analyzed noise and distortion, both for bipolar [81, 82, 83] and for CMOS [84, 85, 86] technologies, whereas Volterra-series based linearity analysis has been proposed [87] to include phase effects in the mixer linearity models. This doubly-balanced mixer (DBM) device makes it possible to implement a good signal-to-noise-ratio, works well with moderate LO powers, and because of its fully differential structure, it suppresses LO and even-order harmonics at its output. In other words, isolation between mixer ports is good, and it easily surpasses respective performance of passive ring mixers. The following section will therefore describe Gilbert mixer operation; discuss some of the findings on its linearity and noise from the cited literature, and conclude this part of the text in a study on Gilbert cell low-voltage operation.

5.1.1 Gilbert mixer operation

Although the cited references concentrate on down-conversion Gilbert mixers, their findings can be applied to up-conversion mixer design if some key differences are kept in mind: foremost is the fact that an up-conversion mixer typically operates on-chip as part of an integrated transmitter and therefore in voltage-mode, so there is no need to match any of the mixer input or output ports to a 50 Ω impedance. Only the baseband inputs are driven by off-chip signal sources, but as these operate at relatively low frequencies, a standing wave connection is easily avoided. For example, a (high) baseband frequency of 100 MHz has a wavelength of 3 meters in free space, and therefore almost any distance is short enough to eliminate the need for a matched input port. Another difference from down-conversion mixers is that the output of an up-converting mixer is a high-frequency node, and therefore switching quad transistor current densities need to be high enough for high-frequency operation. Finally, broadband operation makes the use of LC-

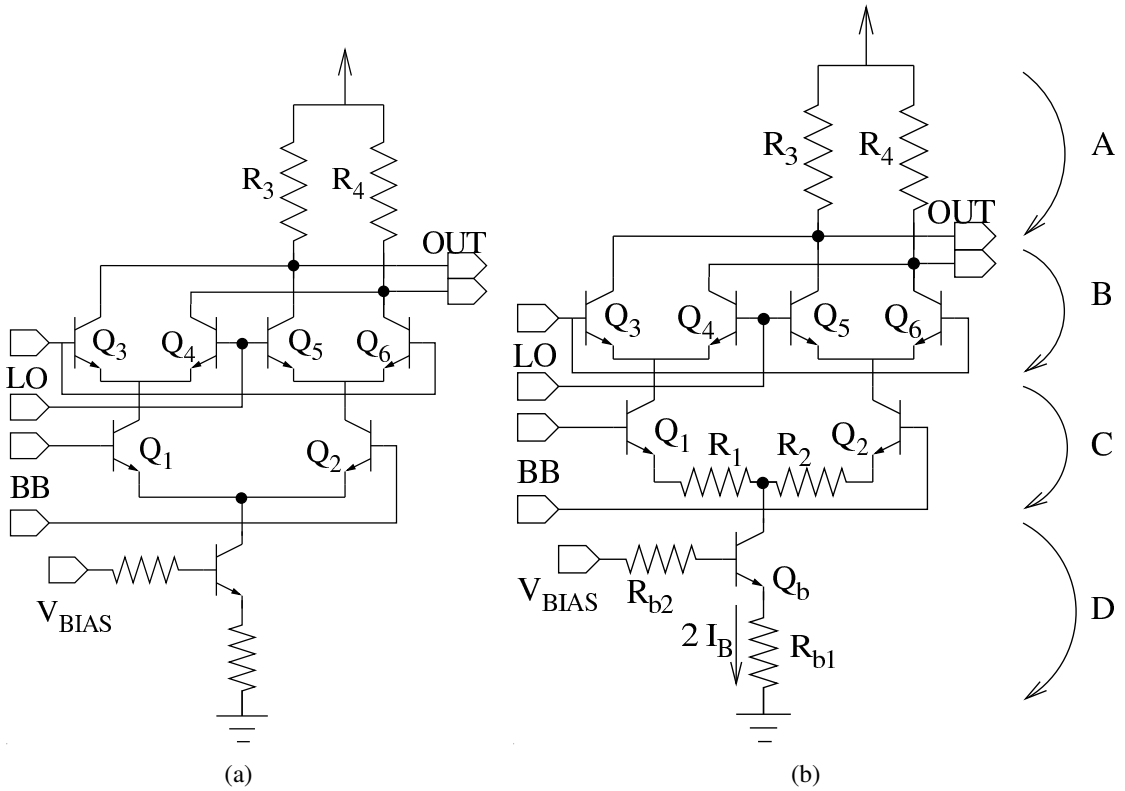


Figure 5.1: Gilbert mixer with the switching quad Q_{3-6} and its driving transconductor $Q_{1,2}$ as a) originally presented, b) with linearized BB input and with voltage loss annotations A, B, C, and D.

tank circuit mixer loads quite impossible, which means that the designer has to deal with more difficult gain-linearity tradeoffs.

Textbook analysis of the Gilbert mixer gain [30] assumes that the switching quad transistors are driven hard enough for them to operate as ideal switches which are either 'ON' or 'OFF'. With the LO wiring shown in Fig. 5.1(a), this results in a complete switch of polarity of the baseband driven currents, and the signal is chopped around odd multiples of the LO frequency; therefore this circuit is also called a *balanced modulator*. After low-pass filtering of the higher-frequency terms, the output signal is given as:

$$s(t) \;=\; \frac{K_{BB} \cdot v_{BB}}{\pi} \left[\cos(\omega_{\mathrm{LO}} + \omega_{\mathrm{BB}})t + \cos(\omega_{\mathrm{LO}} - \omega_{\mathrm{BB}})t\right] \tag{5.1}$$

, where s(t) stands for the output signal, $\mathrm{v_{BB}}$ is the baseband signal, $\mathrm{v_{LO}}$ is the modulating LO signal, $\mathrm{K_{BB}}$ is the baseband gain to mixer load, and the π term is known as the conversion loss factor. To continue, the USB at (ω_{LO}+ω_{BB}) is again defined as the wanted tone. This makes it possible to define $\mathrm{v_{OUT}}$ as:

$$v_{OUT} \;=\; \frac{K_{BB} \cdot v_{BB}}{\pi} \tag{5.2}$$

An LO signal peak-to-peak amplitude at approximately four times the thermal voltage ($\mathrm{V_T}$=26 mV at room temperature) is sufficient to produce the desired switching action, whereas a CMOS realization would need a higher LO amplitude as a result of NMOS transistor lower gain. To improve circuit linearity, the baseband transistors are usually linearized. The most popular approach is to use emitter-degenerating resistors such as the resistors $\mathrm{R_{1,2}}$ shown in Fig. 5.1(b). Therefore, after defining $\mathrm{R_L}$ as the value of the resistive loads $\mathrm{R_{3,4}}$, and R as the value of the linearizing resistors $\mathrm{R_{1,2}}$, the baseband gain factor can be defined as $\mathrm{K_{BB}} = 2\,\mathrm{R_L}/\mathrm{R}$.

5.1.2 Linearity and noise

Mixer linearity is more important than noise performance in transmitter applications, as the user can choose transmitted signal levels at an appropriate distance from the noise floor. Linearity limits system DR by setting its upper bound through signal compression, whereas mixer noise defines the lower bound for system TDR and therefore the range available for different modulations. In [81] a linearized version of the Gilbert cell is analyzed for down-conversion applications. The DBM device is much like the one shown in Fig. 5.1(b), with the difference that the linearizing resistors $\mathrm{R_{1,2}}$ can be implemented with inductors or with capacitors in parallel with resistors for improved noise performance. The use of reactive degeneration circuits results in improved noise figures, but the relatively low baseband frequencies in up-conversion applications preclude the use of reactive degeneration. Luckily, resistive degeneration is more linear, and its use also improves the matching between the input devices [36]. It can be shown, that emitter-degeneration increases the dynamic range of the mixer by:

$$\Delta DR \;=\; 20\log_{10}\left(\frac{1+1.7\sigma}{\sqrt{1+2\sigma}}\right) \tag{5.3}$$

, where $\sigma = (\mathrm{I_B\,R})/(2\mathrm{v_T})$, and the terms correspond to the mixers shown in Figs. 5.1(a)-5.1(b). Thus the application of a linearizing voltage loss $\mathrm{I_B\,R} \;=\; 100\mathrm{mV}$ gives a DR improvement of 13.2 dB, whereas 200 mV results in an improvement of 18.8 dB.

Withal, the Gilbert cell is a six-port device, and the performance available also depends on the LO signal amplitude it is driven with. Generally, it is thought that a large LO amplitude improves mixer noise performance, as the switching quad $\mathrm{Q_{3-6}}$ transistors spend less time in transition between the ON and OFF states conducting current and noise. However, practical LO

amplitude is limited by supply voltage, current dissipation, isolation, and linearity considerations; e.g. already as early as 1986 [83] simulated and measured values concurred to show an increase in third-order harmonics (IM3) when high LO amplitudes were used. Recently, in [88] a 0.45 μm CMOS DBM implementation has been shown to have a gain peak at an LO amplitude of +3 dBm, after which the measured gain values start decreasing. To conclude the discussion of the three-stacked transistor mixer, the next subsection discusses its low supply voltage limitations.

5.1.3 Low supply voltage limitations

To study the effect of low supply voltage limitations on the performance of the Gilbert mixer, the voltage drops across the different parts of the mixer are annotated in Fig. 5.1(b). To represent a practical broadband design, the BB input stage transistors $Q_{1,2}$ have been linearized by the emitter-degenerating resistors $R_{1,2}$, and loading resistors $R_{3,4}$ have been used. The annotated voltage losses stand for:

A After defining R_L as the value of the resistive loads $R_{3,4}$, the voltage loss V_A can be defined as $V_A = R_L \cdot I_{BIAS}$.

B General design experience and reference literature such as [36, 30] suggest the definition of a voltage drop from the collector to the emitter of a bipolar transistor as ca. V_{CE}=0.9 V to make the device operate in its active, desired, mode of operation. Therefore V_B will be set to 0.9 V.

C To define the voltage loss over the emitter degenerated input pair, it is first necessary to set the desired region of operation for the transistors $Q_{1,2}$. For this application the input transistors should operate in their active region of operation for the device transconductances g_m to be high enough to sustain linearized operation with good matching. Thus, after the linearizing resistor $R_{1,2}$ values have been defined as R, the voltage loss V_C can be defined as $V_C = R \cdot I_{BIAS} + 0.9V$.

D The current source stage transistor Q_b is the first one to drop to the saturated region of operation, so its V_{CE} requirement could realistically be set to ca. 0.2 V, but the tail current transistor should remain in the active region of operation for better matched mixer currents I_{BIAS}, which are important in an IQ modulator application. This results in the following definition for V_D: $V_D = R_{b1} \cdot 2\,I_{BIAS} + 0.9V$.

Summing the defined voltage losses over A, B, C, and D gives an expression for the minimum voltage loss in a Gilbert mixer as:

$$V_{\Sigma ABCD} = (R_L + R + 2R_{b1})\ I_{BIAS} + 2.7V \tag{5.4}$$

Since (5.4) defines the minimum usable supply voltage as being greater than 2.7 V, it is clear that the digital CMOS-driven trend towards decreasing voltages makes the use of the original Gilbert mixer, with its three stacked transistors, difficult. Especially in the case of an RF application with moderate to high currents, the problem is aggravated by voltage losses in the device resistors. To quantize this phenomenon, the bias current is set at I_{BIAS}=2 mA and the resistors at R_L=400 Ω, R=75 Ω, and R_{b1}=100 Ω to correspond to a typical up-conversion mixer. The use of the defined values in (5.4) gives the minimum usable supply voltage as 4.05 V, which is already too high for many applications.

The following section describes the mixers used in the tabulated reference quadrature modulators shown in Table 2.1, after which the first of the mixers realized for this work will be discussed.

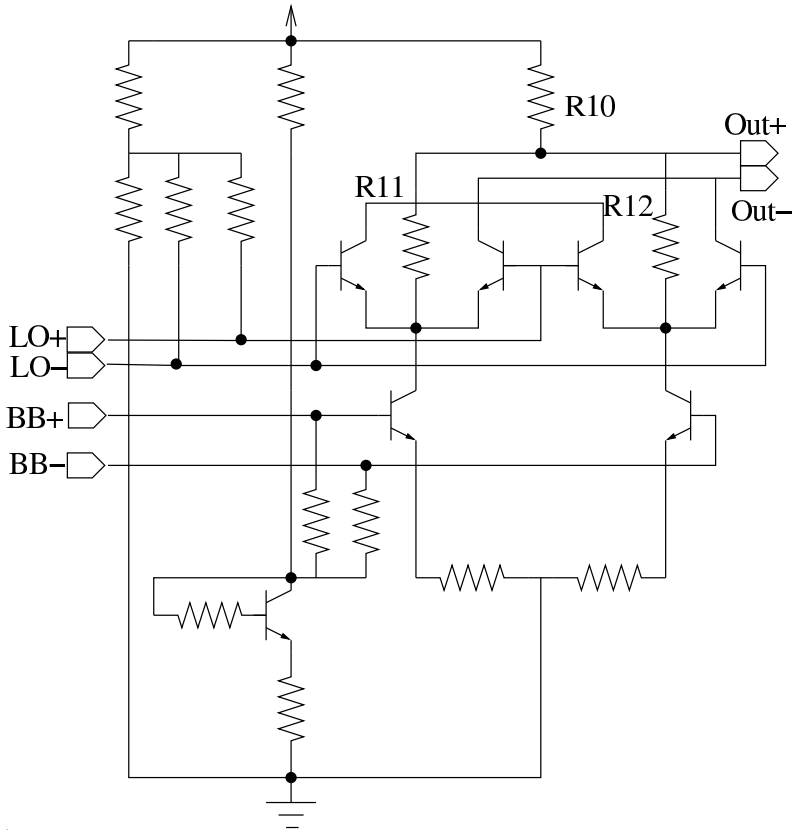


Figure 5.2: Class AB Gilbert mixer with dc blocks and current bypass resistors R10-R12 [40].

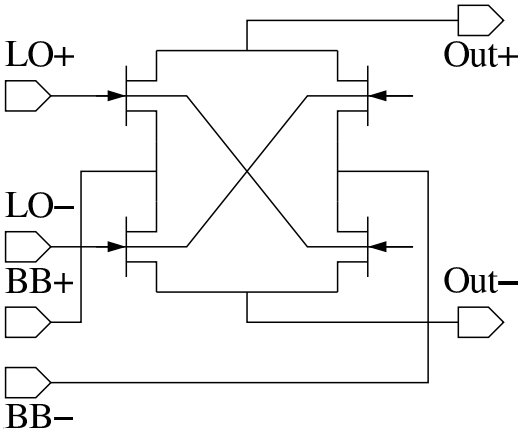


Figure 5.3: MESFET ringmixer [43].

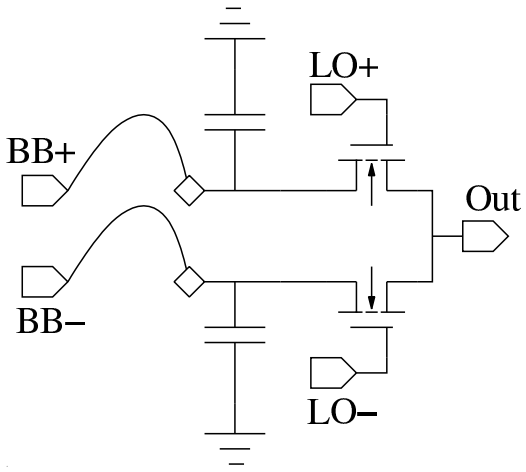


Figure 5.4: Resistive current-mode potentiometric mixer [42].

5.2 Integrated up-conversion mixers

The following subsections will discuss the up-conversion mixers used in the tabulated reference quadrature modulators, an approach that admittedly leaves some good research work on the subject of up-conversion mixers untouched. However, the choice of the topologies can be justified by the time span of a decade covered by the IQ modulators in Table 2.1, as these represent the best efforts that have been published on good broadband performance. In other words, it is probable that some of the more complicated mixer topologies fail under circumstances where two such mixers should match perfectly, as in a quadrature modulator.

5.2.1 Gilbert mixers

Three of the eight reference modulators use the Gilbert mixer or a variant thereof. Two of the three Gilbert mixer modulators [46, 45] use the basic three-stacked-transistor Gilbert configuration, whereas the mixer in Fig. 5.2 [40] uses a two-stacked-transistor variant of the Gilbert mixer, which replaces the current source transistor with a parallel biasing transistor Q1 and its associated resistors R5-R9. The differential pair input stage was thus replaced with two common-emitter amplifiers for better linearity [87] and for increased headroom. To complement this, the technique of current bypass resistors [89] was utilized so as to provide an increased dynamic range. The bypass resistors R10-R12 allow higher current dissipation in the signal input stage Q2-Q3 than in the switching quad Q4-Q7. Decreased current means that the switching quad devices can be made smaller for improved frequency response and for lower LO power requirements. The mixer was also designed to implement a small conversion loss, so as not to drive the following stage into compression too early. Combined, the presented techniques give the mixer a high reported P_{1dB}=3.5 V_{pp}. However, the BB input dc connection was severed for this performance, so the reported mixer was designed for IF applications.

5.2.2 Resistive mixers

Two resistive mixers are used in the reference modulators; one is a GaAs MESFET implementation of the ringmixer [43], while the other is a current mode passive mixer [42].

The ringmixer implementation in Fig. 5.3 uses unbiased, cold FETs to eliminate 1/f-noise up-conversion, and its given linearity around 1000 MHz is good with 3RD-rej performance at better than -50 dBc. The cited linearity was recorded with a respectable output level at -6 dBm, but an off-chip balun is required for this performance. A drawback with this mixing scheme is the hard switching required, which results in increased power dissipation in the LO chain. For example, the quadrature modulator in [43] uses four cascaded differential stages with a synthetic inductor in each chain to drive each mixer with its LO signal, and this translates to 250 mA of current dissipation. Yet, despite the amount of LO amplification used, this type of mixer is always lossy. Another concern with this technique is its symmetry requirements, which are hard to meet with the three baluns or differential amplifiers needed to drive the mixer; this has in fact been labeled as virtually impossible at higher frequencies in [90].

In contrast, the current-mode mixer in Fig. 5.4 uses only two unbiased MOSFETs per mixer. An important feature of this mixer is the 30 pF capacitors implemented at its BB input ports to make the operation of the device independent of the bonding wire inductances. As a result, performance with a better than -30 dBc spurious and LO tone rejections was recorded with the 0.25 μm CMOS technology used, albeit with a high LO power of 0 dBm. However, the use of this topology was not considered for this work for several reasons, the first of which is the proposed capacitors at mixer BB inputs. A large IC area would have been necessary for such capacitors, and it is not at all clear how a wideband BB input could be constructed with

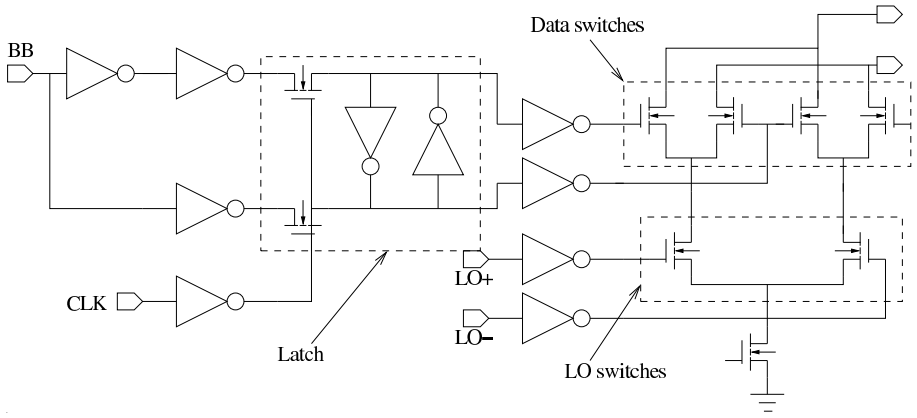


Figure 5.5: The direct digital-to-RF conversion cell [10].

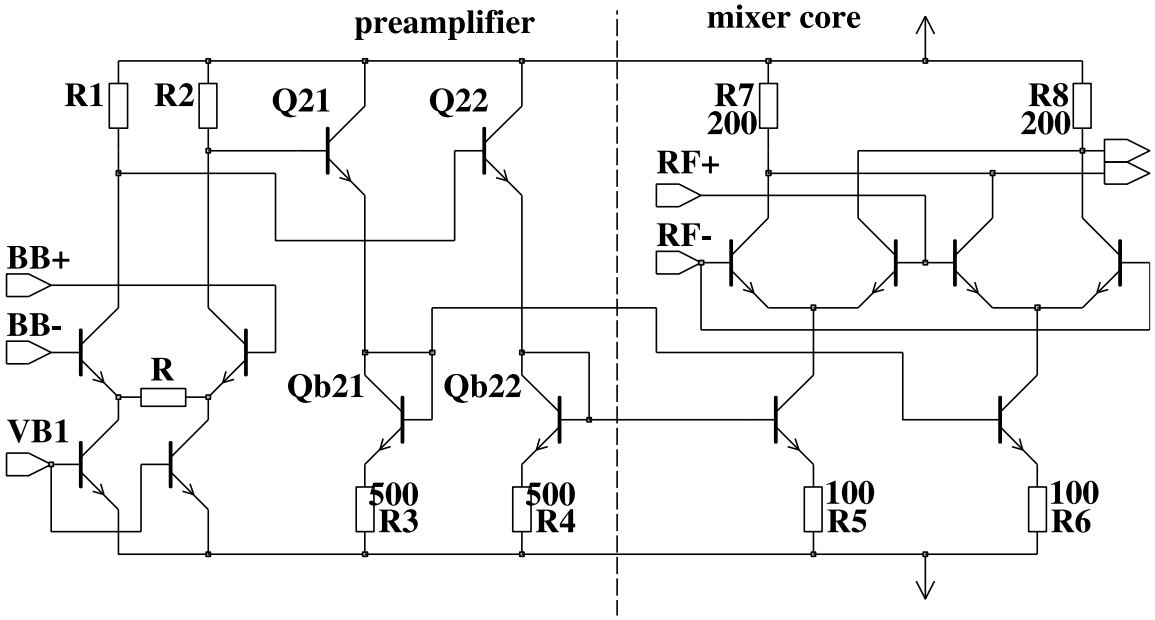


Figure 5.6: An implementation of the mixer proposed by Tsukahara et al. in 1996.

this approach. This is a particularly important point for the suggested goal of multimode radio use, which demands a flat frequency response. A final concern is circuit noise, as potentiometric mixers are extremely noisy, and the suggested use of this current-mode variant is with a synthetic inductor loaded buffer.

5.2.3 Digital-to-RF mixer

The direct digital-to-RF mixer proposed in [10, 91] consists of 8 parallel single-bit conversion cells like the one shown in Fig. 5.5. Individual conversion cells combine to drive a shared current to voltage converting load, which is possibly followed by an RF filter, to perform 8-bit DA conversion directly to the transmitted frequencies. Beneficially, this topology eliminates the analog baseband interface, so there should be no offset induced LO leakage, and the SINC effect (sin(x)/x) can be utilized to attenuate spurious image components at the circuit output. The sin(x)/x notch placement calls for diligent clock frequency planning, but for most applications it does not eliminate the need for filtering at microwave frequencies.

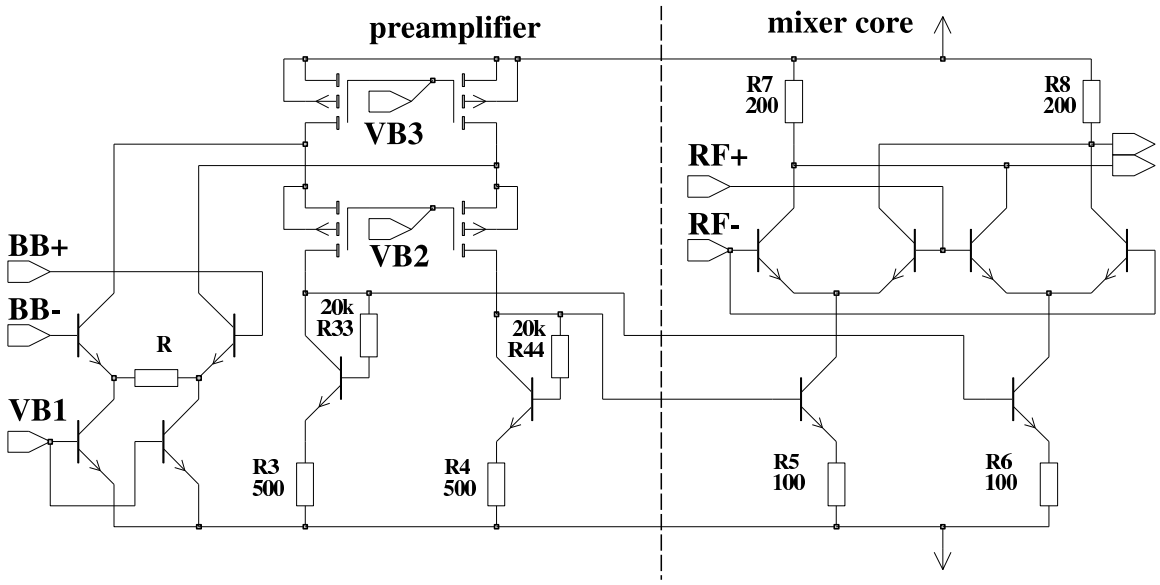


Figure 5.7: A BiCMOS version of the Tsukahara mixer with improved noise characteristics.

Table 5.1: BiCMOS mixer comparison table with large signal simulation results for A_v, 3RD-rej, and Noise.

		[BiCMOS]	[currfold_I]	[currfold_II]	[Gilbert]
A_v	[dB]	0.6	-0.3	0.1	0.5
3RD-rej	[dBc]	-65	-65	-42	-56
Noise	[nV_{RMS}]	58	82	82	8
V_{LO} @900 MHz	[mV_p]		125		
V_{BB} @1 MHz	[mV_p]		100		
A_{PREAMP}	[dB]	2.1	1.2	1.7	–
BW_{PREAMP}	[MHz]	340	1300	2700	–
I_{mixer_core}	[mA]	3.9	3.6	3.9	3.7
I_{DD}	[mA]	6.2	5.8	6	4.7
V_{DD}	[V]		2		3
tech.			0.8 μm BiCMOS		

5.3 The realized 0.8 μm BiCMOS mixer

To implement a direct-conversion quadrature modulator with dc-connected BB inputs and with a well-defined bias, Tsukahara et al. proposed in 1996 the use of a pre-amplifer to drive the two-stacked-transistor Gilbert mixer core with signal and dc bias, a topology which was dubbed the *current-folded mixer* in [44]. An implementation of this 2 V 2 GHz mixer is shown in Fig. 5.6, and its operating point is obviously well defined. Its output voltage is given by:

$$v_{OUT} = \frac{v_{BB}}{\pi}\frac{R_7}{R_5}\frac{2R_1}{R} \tag{5.5}$$

However, large signal simulations with a 2 V supply using the bipolar transistors from the 0.8 μm BiCMOS with an f_T=12 GHz implied that the *current-folded mixer* topology has an unacceptable amount of excess noise as compared to the bare mixer core. To correct this, the 0.8 μm BiCMOS topology in Fig. 5.7 was proposed [24], the idea being that the current limiting resistors $R_{33,44}$ might help to reduce noise and that the use of such resistors, together with the use of external bias sources, might help to increase mixer gain. After analysis, the effect of the current-limiting resistors $R_{33,44}$ on the impedance seen at diode-connected NPN collectors has been analyzed and it can be approximated with:

$$r_{eff} = R_3 + \frac{R_{33} + r_\pi}{\beta} \tag{5.6}$$

, where r_π and β are the bipolar transistor input resistance and current gain, respectively. Using the defined effective resistance value r_{eff} the output voltage is given as:

$$v_{OUT} = \frac{v_{BB}}{\pi}\frac{R_7}{R_5}\frac{2r_{eff.}}{R} \tag{5.7}$$

The tested design examples of the mixers in Figs. 5.6-5.7 have similar mixer cores, with identical currents. Mixer core emitter areas were set to 30 μm$\times$ 0.8 μm and the degeneration $R_{5,6}$ and load resistors $R_{7,8}$ to 100 $\Omega$and 200 Ω, respectively. The preamplifiers have identical input pairs. The degenerating resistors R have been set to 1 kΩ and input pair currents to 580 μA with bipolar areas set to two emitter stripes of 30 μm$\times$ 0.8 μm.

The PMOS values are unique to the BiCMOS mixer in Fig. 5.7 as well as are the 20 kΩcurrent-limiting resistors $R_{33,44}$: the PMOS pair connected to the positive supply rail has a width-to-length (WL) ratio of 400 μm$\times$ 2 μm, which is two times higher than the WL ratio the PMOS pair connected to output at 80 μm$\times$ 0.8 μm has. The difference in PMOS WL ratios provides currents for both the input pair and the output stage. The eF-stage bipolar areas are 3 μm$\times$ 0.8 μm.

The current-folded mixer in Fig. 5.6 has been characterized with two different element value sets to illustrate the trade-offs available for the designer. The design examples differ in:

1. preamplifier resistor values are set to R=1 kΩ, and $R_{1,2}$=750 Ω; $Q_{21,22}$ emitter areas are set to three stripes of 15 μm$\times$ 0.8 μm and $Q_{b21,b22}$ emitter areas to six stripes of 15 μm$\times$ 0.8 μm. The example is named `currfold_I`;

2. preamplifier resistor values are set to: R=$R_{1,2}$=450 Ω; $Q_{21,22}$ emitter areas are set to $3/0.8\mu$ and $Q_{b21,b22}$ emitter areas to two stripes of 2 μm$\times$ 0.8 μm. The example has been named `currfold_II`.

To validate the claims made for highly linear mixing, a traditional three-stacked transistor Gilbert mixer with an emitter-degenerated baseband input like the one used in the current-folded mixers

was designed and characterized using a 3 V supply. The switching core current I_{mixer_core} has been set to 3.7 mA and baseband input degeneration resistor to 200 Ω in order to produce comparable conversion gain vs. linearity results.

The comparison of the simulated results in Table 5.1 shows that the proposed current-folded mixer version in Fig. 5.7 improves gain (0.9, 0.5, 0.1 dB), and 3RD-rej (0, 23, 9 dB). Most importantly, the BiCMOS mixer shows a 5 dB improvement in noise when compared to both the current-folded mixers (currfold_I and II). This is to be expected, as its preamplifier bandwidth (340 MHz) is a good 5-10 times lower. For most modulator (transmitter) applications a baseband bandwidth of 340 MHz is enough, though. Even wideband CDMA requires a lower bandwidth than 5 MHz. A much more serious flaw that the proposed current limited topology has is its possible β dependency as shown by (5.6). This is forbidding for quadrature modulator applications, which depend on state-of-the-art matching between the two mixers.

Additionally, as the Gilbert cell reference produces 17-20 dB lower noise at its output than is the case with all three current-folded mixers, it is prudent to say that the use of all of the proposed pre-amplifiers increases noise too much. The linearity advantage shown by the reported 3RD-rej values for the pre-amplifier mixers is based on the well-known property of increased linearity that the common-emitter stage has over a similarly biased differential pair [87]. Thus it has been possible to combine the common-emitter stage-driven mixer cores with the use of large linearizing resistors in the preamplifiers to improve mixer linearity in comparison to the Gilbert cell reference.

5.4 The realized 0.8 μm SiGe mixer

The mixer in Fig. 5.8 is a low-voltage version of the (doubly-balanced) Gilbert mixer, with its biasing transistor removed. The resulting class AB mixer linearity is therefore not current-limited [92], and its baseband input of two common-emitter stages always outperforms the linearity performance of a similarly biased [87] differential pair. This bbp/bbm-port voltage biased mixer is usable with a 2.5 V supply, and its simplicity helps to keep simulation times/convergence for large signal system characterization purposes reasonable. To increase the mixer bandwidth two 2.5 nH on-chip inductors are used for the inductive gain peaking [59, 60] of the low-value resistive loads. This approximately doubles the simulated mixer bandwidth to 6.7 GHz, while the circuit dissipates 3.1 mA of current, as shown in Table 5.2. The reported mixer bandwidth extension from 3.1 to 6.7 GHz is an improvement of 116%, which is higher than the maximum 85% extension predicted by the theory [60], but there are two possible explanations for this: 1) the real circuit model used in the simulations is much more complex than the RLC circuit load used for the cited modeling, and 2) bandwidths were tested with a large signal simulation which includes effects that are not modeled by a simple RLC model.

To evaluate the performance of the class AB mixer relative to other available topologies, it was compared to three mixer topologies with different baseband linearizations. The studied circuits are shown in Fig. 5.9 and they all use the same switching quad shown as part of Fig. 5.9(a) and resistive 75 Ω loads. The 75 Ω resistors were used to load the mixers with two goals in mind: 1) the use of such small ohmic loads results in a negligible voltage loss over them, and this helps in keeping the transistors in their active region (or in saturation for CMOS), and 2) circuit outputs are thereby resistively matched to 50 Ω with a simulated return loss of -14 dB at 2.4 GHz. Matched outputs made possible the simulated extraction of P_{OUT} and OP_{1dB} to a 50 Ω load through 10 mH capacitors used as near-ideal dc blocks. Since a 0.35 μm version of the 0.8 μm SiGe process was available at the time of the evaluation, it was decided that the parameters for the newer process would be used for the simulations so as to keep the results up-to-date. The 0.35 μm SiGe process also increased bipolar f_T and f_{MAX} to over 70 GHz from the

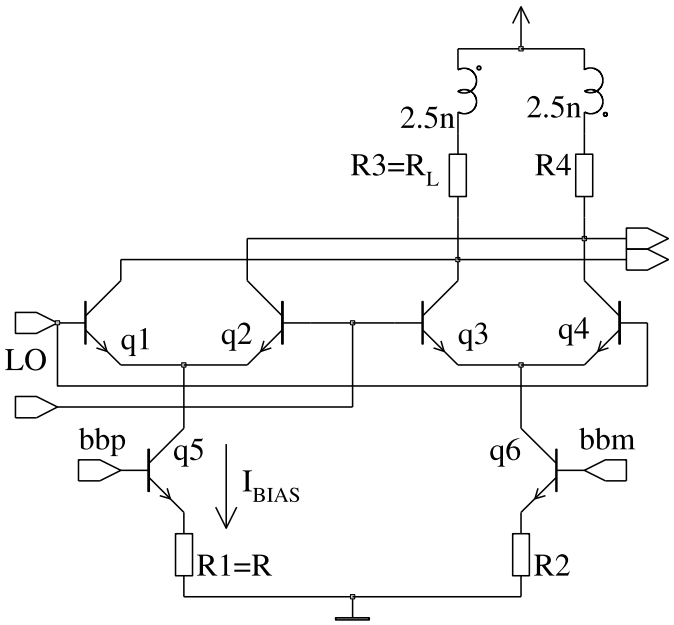


Figure 5.8: Class AB Gilbert mixer without the biasing transistor.

Table 5.2: Simulated characteristics for the mixer in 0.8 μm SiGe with and without gain-peaking.

CL=150 fF		106 Ω	75 Ω+ 2.5 nH
A_v	[dB]	-8	-8
BW_{3dB}	[GHz]	3.1	6.7
OP_{1dB}	[dBV]	-13	-14
P_{1dB}	[dBV]	-5	-5
3RD-rej	[dBc]	-62	-62
N_{+20MHz}	[dBm/Hz]	-159	-161
LO @2.45 GHz	[dBV]	-16	-16
BB @10 MHz	[dBV]	-20	-20
I_{DD}	[mA]	3.1	
V_{DD}	[V]	2.5	

previously reported f_T=35 GHz and f_{MAX}=30 GHz, with corresponding improvements in MOS transistor performance. A large signal RF simulator was used to test circuit characteristics, with the emphasis being on linearity and matching issues. Noise simulations failed, since the models produced floating point errors at the time the simulations were performed in 2004, but available performance has been assessed with reference to the literature. The Monte-Carlo parameters which model variations between circuit devices, the `DEV` parameters, were defined as the ones for the 0.8 μm process in Subsection 3.5.2.

The class AB version of the multitanh doublet shown in Fig. 5.9(b) is a low-voltage modification of the basic topology given in [47], with its two biasing current sources removed. The idea was to study whether a multitanh doublet input stage could be used in a two-stacked transistor configuration as a direct replacement for the two CE stages used in Fig. 5.9(a) (shaded area). The emitter areas and resistor values define a current ratio of 4 between the transistors, although maximally flat g_m would be achieved with a ratio of 3.7. This is an implementation issue, as the transistor models were not scalable, and integer multiples of the modeled transistors had to be used.

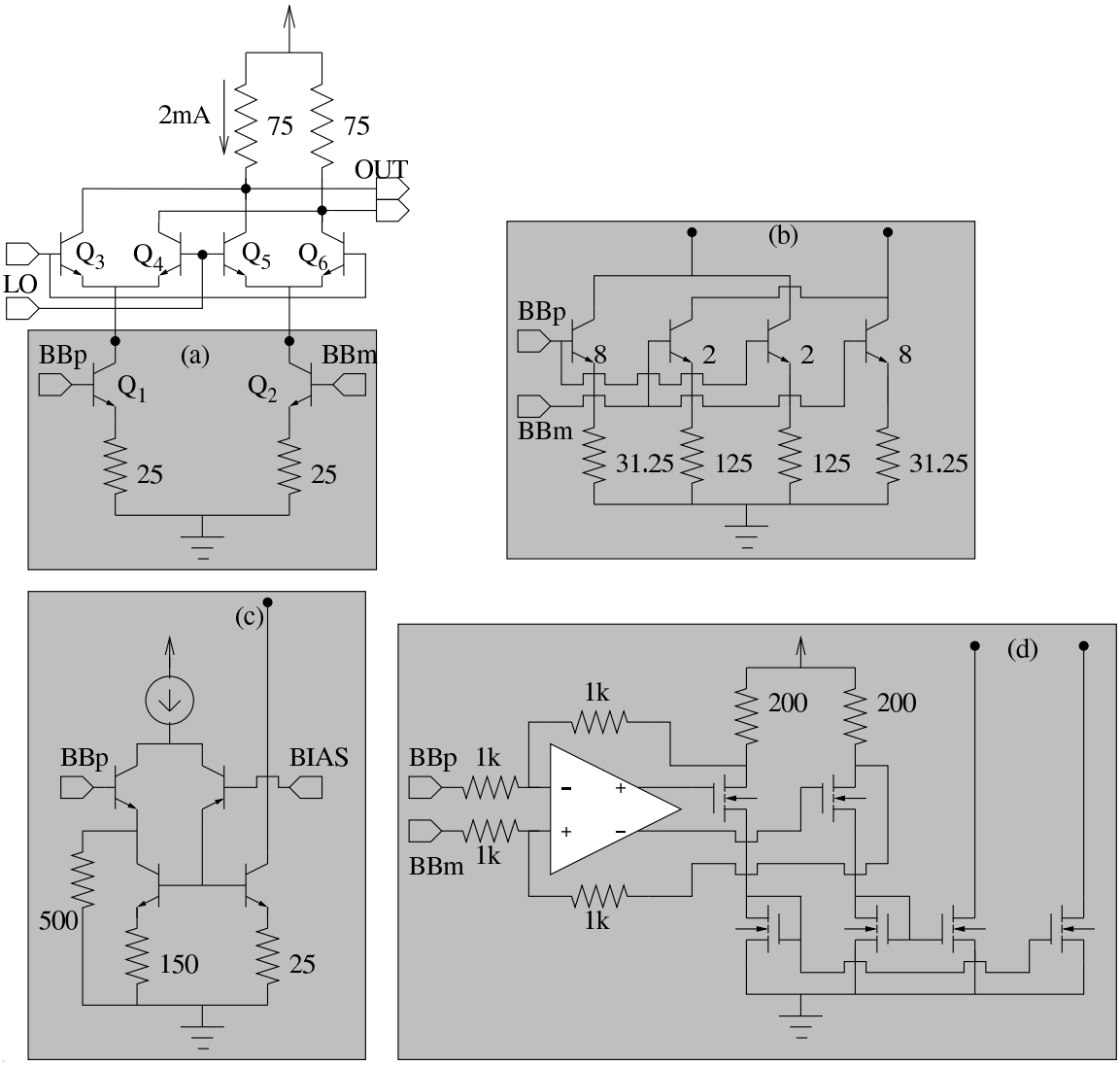


Figure 5.9: Comparison of linearized class AB mixer inputs with (a) resistive, (b) multitanh, (c) current feedback, and (d) opAmp-driven techniques.

Table 5.3: Simulated results for the (a) resistive, (b) multitanh, (c) current feedback, and (d) opAmp mixers.

		(a)	(b)	(c)	(d)
P_{OUT}	[dBm]		-17		
3RD-rej	[dBc]	-31.4	-31.7	-27.4	-36.5
OP_{1dB}	[dBm]	-14.8	-14.8	-15.9	-5
S_{22}	[dB]		-14		
S_{11}	[dB]		-6		
LO@2.4 GHz	[dBm]		-5		
BB@1 MHz	[mv_{RMS}]	110	110	220	100
I_{DD}	[mA]	4	4	4.6	5.4
V_{DD}	[V]		2.5		

The current feedback topology used in the Philips GSM chipset [93] is shown in Fig. 5.9(c), with only one of the two stages used in the tested mixer shown for clarity. Similarly, the implementation details of the current source have been omitted. The originally reported power penalty is 15% with an impressive -3 dBm output power for a 3 mW power dissipation from the 3 V supply. However, as this performance has been reported for the narrowband gsm application using inductive loads, this work aims at defining its usability for broadband applications through comparison of the simulated performance at similar output power and switching quad currents.

Implementation of the opAmp-driven baseband stage [94] is shown in Fig. 5.9(d) with one idealization: the opAmp has not been implemented on a schematic level, but an ideal voltage-controlled voltage source (VCVS) was used instead. This is indicative of a weak point in this concept, as the design time for the opAmp could not be spared for this study. This choice also excludes opAmp power dissipation and noise, plus all practical non-idealities, such as the offset voltage. The non-idealities could necessitate the design of a tuning circuit in quadrature modulator application where good matching of two mixers is essential. Nevertheless, successful quadrature modulator implementations with a very high DR exist [41] which use the opAmp-driven mixer concept.

The simulated results shown in Table 5.3 indicate almost no difference between the resistively linearized class AB (a) and multitanh techniques (b), whereas the current feedback technique (c) has a 3RD-rej performance 4 dB worse than (a). Supporting results have also been extracted in [95], where both the simulated and measured results also indicate that a high noise penalty ensues from the use of the current feedback loop. The linearity performance tabulated for the opAmp-driven mixer is very good, as the reported 3RD-rej performance is 5.1 dB better than that tested for (a). However, these results are not conclusive, since an ideal VCVS was used in (d). In fact, the VCVS precluded the use of the (d) topology in the Monte-Carlo simulations, which were performed in order to study the applicability of the mixers to an IQ modulator application. The mean μ and standard deviations σ of the results obtained in 30 Monte-Carlo runs for the remaining three mixer topologies are shown in Table 5.4, and it is apparent that topology (c) does not perform as well as (a) and (b) would in a quadrature modulator application.

Additionally, in view of the simulated results it is hard to argue for the use of the multitanh doublet, especially as the application of good layout techniques such as the common-centroid configuration might be impossible. The opAmp-driven mixer (d) is the most interesting, but its use involves a good deal of overhead in a design which is solely applicable to up-conversion applications. Furthermore, the uncertainty of the results as a result of the use of an ideal element, the VCVS, is forbidding. Most importantly, the opAmp-driven mixer value should be assessed in comparison to other DR-enhancing topologies such as the one in [89]. However, as this is a field of study in itself, it has not been included in this work. Therefore, the following section will concentrate on a CMOS implementation of the class AB mixer.

5.5 The realized 0.13 μm CMOS mixer

The up-conversion mixer shown in Fig. 5.10 is a CMOS variation of the class AB Gilbert mixer shown in Fig. 5.8. As the circuit was implemented in a bulk digital 0.13 μm CMOS process, a comparison of its simulated performance to the theory will give insight into the RF properties of near-nanometer-scale NMOS transistors. To minimize gate resistance, narrow gate widths (W) of 3 μm were used, and each transistor was designed with 12 fingers for a WL ratio of 180. The high number of gates should improve matching between the transistors [96]. To further improve matching between transistors, a drawn gate length of 0.2 μm was used instead of the 0.13 μm minimum available [97], and this results in larger area transistors as advocated in [63].

Table 5.4: Simulated Monte-Carlo results for an IQ modulator realized using the designed (a) resistive, (b) multitanh, and (c) current feedback mixers.

		(a)		(b)		(c)	
		μ	σ	μ	σ	μ	σ
P_{OUT}	[dBm]	-11.3	0	-11.0	0	-10.7	0
IRR	[dBc]	-57.8	10.3	-56.9	6.3	-47.9	4.7
LO-rej	[dBc]	-46.9	5.2	-48.2	7.4	-33.9	6.7
3RD-rej	[dBc]	-31.6	0.1	-31.2	0.1	-26.7	0.3
2ND-rej	[dBc]	-65.3	6.4	-65.5	4.7	-49.5	5.0

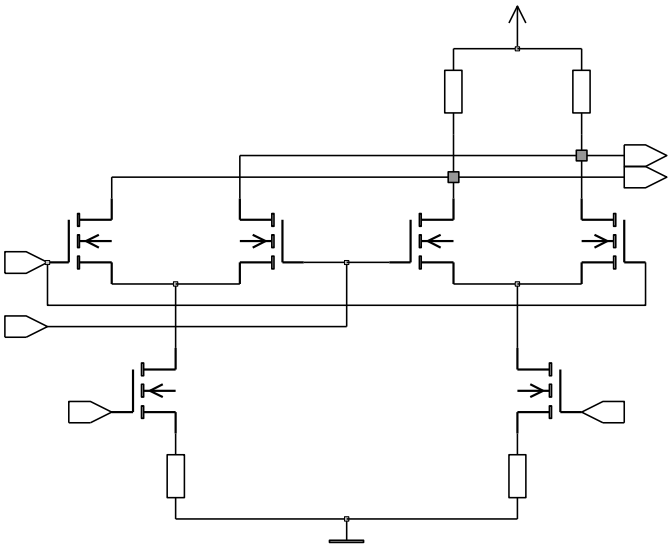


Figure 5.10: CMOS version of the class AB Gilbert mixer.

Table 5.5: Simulated characteristics for the mixer in 0.13 μm digital CMOS.

A_v	[dB]	7
BW_{3dB}	[GHz]	4.6
OP_{1dB}	[dBV]	-4.5
P_{1dB}	[dBV]	-11
3RD-rej	[dBc]	-50
N_{+20MHz}	[nv_{RMS}]	8.8
LO @2.4 GHz	[dBV]	-6
BB @10 MHz	[dBV]	-20
I_{DD}	[mA]	1.7
V_{DD}	[V]	2.2

Non-minimum widths were also used for the designed 24 Ω source-degeneration and 600 Ω load resistors.

The voltage-mode conversion gain A_v can be defined by the application of (5.2) to give:

$$A_v = \frac{2g_m R_L}{\pi} = \frac{2R_L}{\pi R} \tag{5.8}$$

, where g_m is the BB stage transconductance, and R_L and R are the load and linearizing resistors, respectively. Evaluation of the developed equation results in A_v=18 dB, a value which is in disagreement with the simulated value of 8 dB. To refine the model, the BB input stage transconductance was checked, and at 9.5 mS it is not high enough to be replaced by the inverse of the 24 Ω source-degenerating resistor. This is evident from the application of the respective CE stage expression [36] to model the transconductance as:

$$g_m = \frac{g_{m,NMOS}}{1 + g_{m,NMOS}R} \tag{5.9}$$

After the evaluation of (5.9) the BB stage transconductance is reduced to g_m=7.6 mS which corresponds to a 132 Ω degeneration resistor. Accordingly, a conversion gain of A_v=9.3 dB is calculated, but this is still 2.3 dB of the mark. To correct this, the mixer output resistance was checked and, instead of the designed 600 Ω, a value of 415 Ω was simulated at 2.4 GHz. After R_L has been set to 415 Ω, the mixer conversion gain is evaluated at 6.1 dB, which agrees with the simulations to within 1 dB. To exclude parasitics, the output impedance simulation was repeated at 10 kHz, and as this gave a result of 420 Ω it is safe to suspect that the switching quad transistors are responsible for the recorded extra 1.5 dB loss. In fact, each switching quad output node impedance can be estimated at a low 1.53 kΩ, as a parallel connection of two simulated transistors simulated in equilibrium (non-switching). The culprit in this case is the high channel conductance of the short-channel FETs, and the significance of the matter is best understood in the context of down-conversion, where very high impedance loads could normally be used for high gain. In other words, the short-channel CMOS implementation of the switching quad sacrifices some of the insensitivity to load impedances that the Gilbert cell is known for.

Simulated performance at 2.4 GHz is shown in Table 5.5 with the characteristics given in voltage-mode taken differentially. The only exception for this is the noise floor N_{+20MHz}, which was recorded at a 20 MHz offset from the wanted tone single-endedly. Therefore, in order to assess the available DR from the mixer its voltage-mode output and noise characteristics should

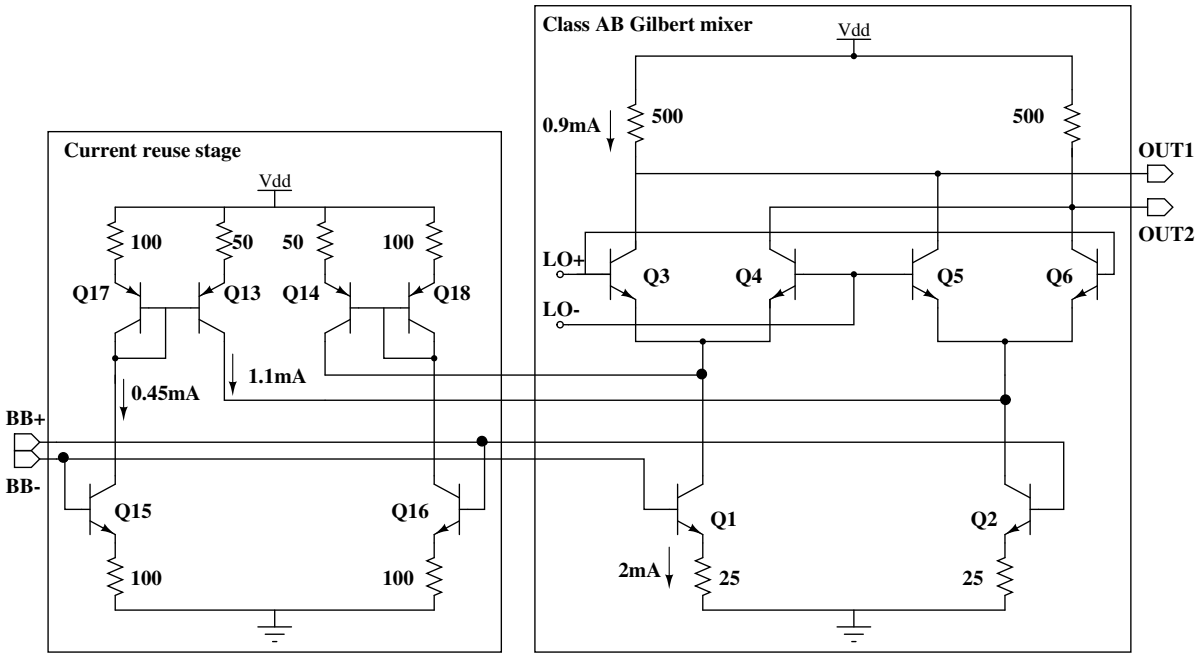


Figure 5.11: Class AB mixer with a current reuse stage.

be converted to dBm:s. To do this -6 dB is added to the tabulated OP_{1dB}, and after comparison of the compression and noise powers using the 415 Ω output impedance established earlier for the mixer, a DR=+148 dB can be recorded. This compares well with the respective SiGe mixer value of +147 dB, which can be calculated from its characteristics as given in Table 5.2.

5.6 The realized 0.4 μm complementary SiGe mixer

Fig. 5.11 shows the current reuse mixer principle: a class AB Gilbert mixer is driven by a folded current reuse stage. This stage is formed of a pair of diode-loaded common-emitter (CE) stages Q15-Q18, which convey the baseband input (BB+/BB-) to the complementary PNP pair Q13-Q14 with a current-mirroring ratio of 2. The use of such scaled-down current-mirroring decreases current dissipation by ca. 1 mA, but produces a simulated drop in the circuit's baseband bandwidth (BW) from 2.5 GHz to 1.5 GHz. However, this is acceptable for up-conversion mixer applications. The out-of-phase PNP collector currents I_{C13} and I_{C14} are then cross-connected and fed in-phase to the input NPN transistor pair Q1-Q2 collectors to double the mixer gain. Since noise simultaneously increases in direct relation to the square root of 2 (for a bipolar transistor: transconductance $g_m \propto I, \text{noise} \propto \sqrt{I}$), circuit signal-to-noise ratio (SNR) is improved by +3 dB.

Unlike previous designs in CMOS [98], the proposed current reuse mixer avoids the use of biasing current source transistors by including the necessary bias as a pre-defined common-mode dc voltage at its signal inputs. Basically, this approach was chosen because a CE stage should possess greater linearity than a similarly biased differential pair [87]. The resulting direct-conversion mixer also supports low supply voltages by redirecting part of the input stage Q1-Q2 current past the mixer switching quad Q3-Q6 and its 500 Ω resistive loads.

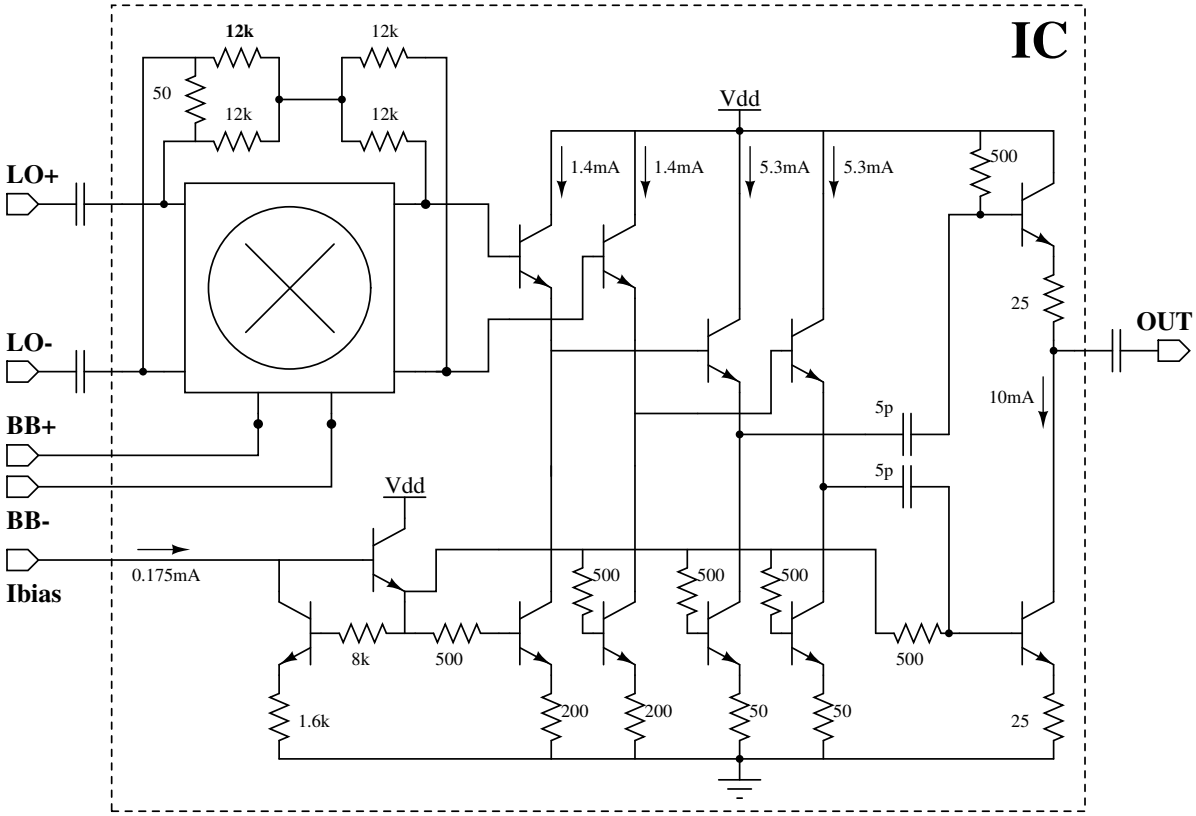


Figure 5.12: A mixer test block with matched LO and OUT ports.

Table 5.6: Comparison of measured mixer characteristics.

		class AB	current re-use
P_{OUT}	dBm	-11	-6
LO-rej	dBc	-31	-42
2ND-rej	dBc	-37	-45
3RD-rej	dBc	-39	-40
OP_{1dB}	dBm	-3	-1
OIP_3	dBm	0	+9
S_{11}	dB	-12	-12
S_{22}	dB	-7	-7
N_{+20MHz}	dBm/Hz	-153	-155
P_{LO}@2GHz	dBm	-8	-8
P_{BB}@10MHz	dBm	-22	-23
I_{DD}	mA	27	29
V_{DD}	V	3.3	3.3

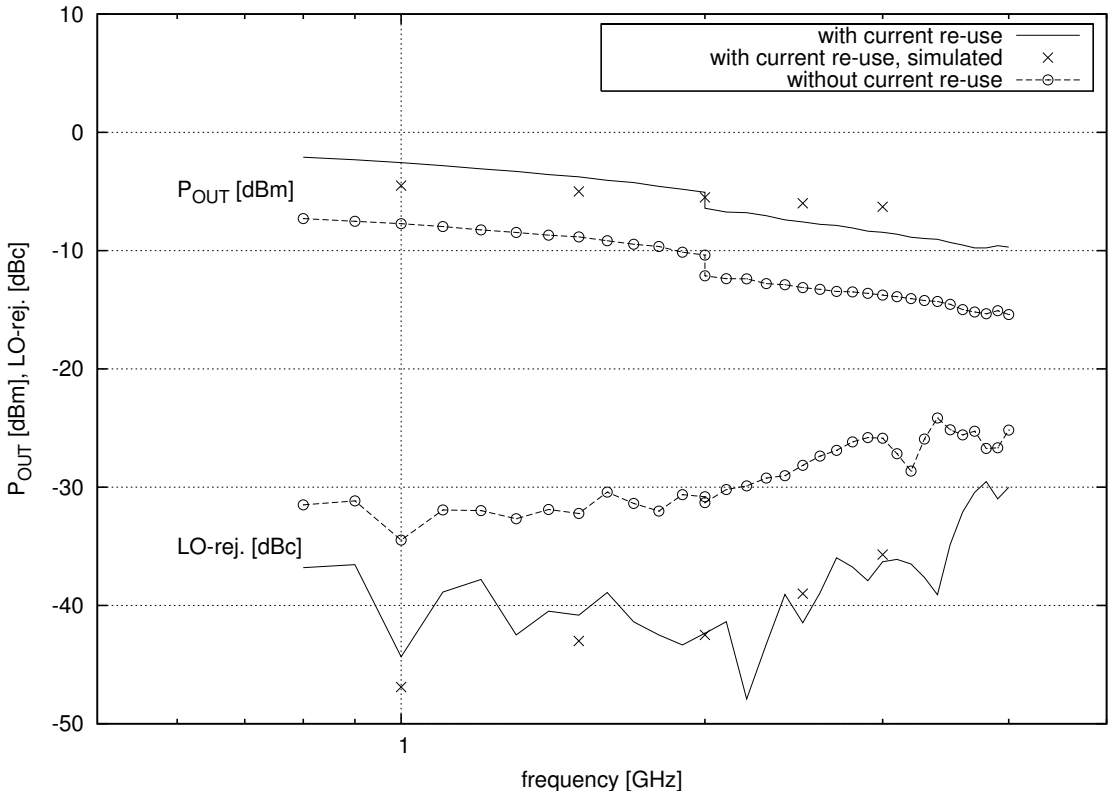


Figure 5.13: Frequency sweep for mixer test blocks up to 4 GHz while using the 3.3 V supply.

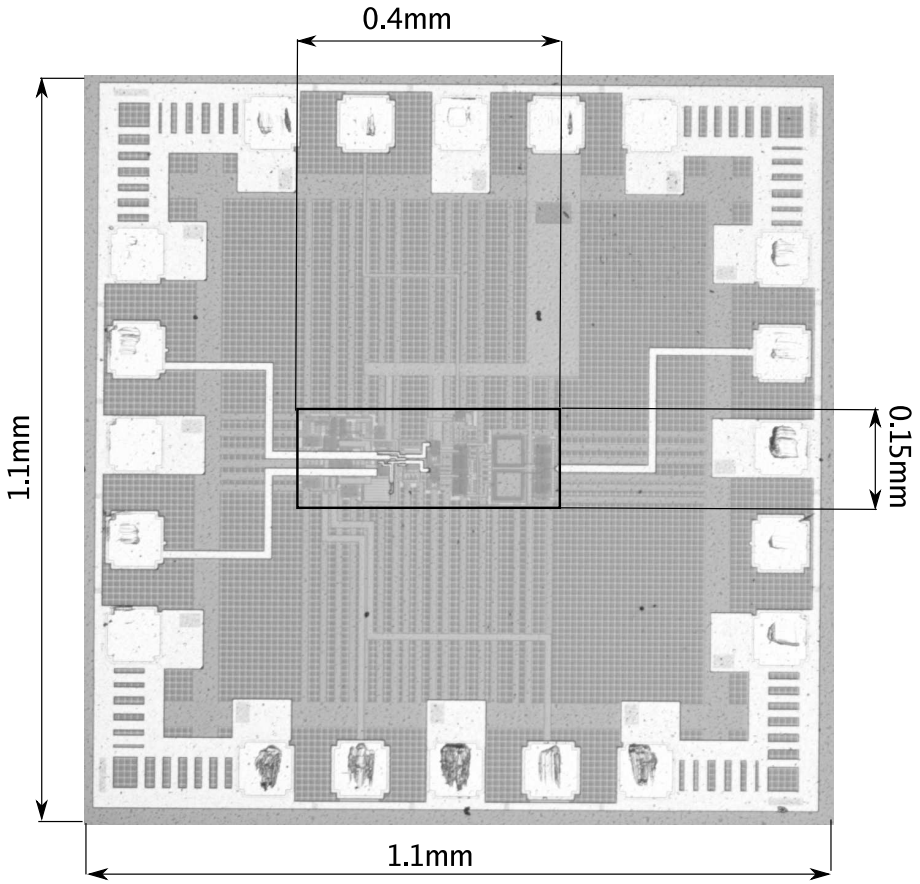


Figure 5.14: Current reuse mixer IC.

5.6.1 Comparison to a class AB Gilbert cell

The realized mixer test block schematic is shown in Fig. 5.12: insertion of the 1.4 mA common-collector (CC) stages increases mixer output BW from 1.5 GHz to 3.1 GHz, whereas the IC area increase is negligible at 25 μm$\times$ 85 μm. Matching of the high-frequency output and LO ports is acceptable, as the totem-pole output stage [41] delivers a measured return loss of S_{22}=-7 dB whereas the resistively matched LO port (LO+/LO-) has a return loss of S_{11}=-12 dB. The LO port dc bias is derived with 12 kΩ resistors, with one pair of resistors sensing, the other delivering common-mode bias for the switching quad.

Two mixer test blocks were realized, one with the proposed *current reuse mixer* shown in Fig. 5.11, the other with the shown *class AB Gilbert mixer* sub-block to act as a reference circuit. A comparison of the measured OP_{1dB} and noise floor (N_{+20MHz}) values in Table 5.6 shows that the proposed mixer has a DR of +154 dB, while the reference circuit achieves a DR of +150 dB. The noise floor has been measured at a 20 MHz offset from the desired tone using an off-chip LNA and a spectrum analyzer. The measured DR results are in good agreement with the predicted +3 dB increase in SNR, despite the fact that the class AB reference mixer had to be measured at -5 dB lower output power (P_{OUT}) in order to obtain a comparably clean spectrum without excessively high distortion-related spurious tones. Allowing for this, the characteristics in Table 5.6 show that the proposed mixer increases second order harmonic (2ND-rej) and LO-RF leakage (LO-rej) attenuations by +8 dB and +11 dB, while third-order harmonic attenuations (3RD-rej) lie both at ca. -40 dBc. The proposed mixer has an output referred third-order intercept point OIP_3 of +9 dBm, which compares well with the corresponding 0 dBm value of the reference mixer. The proposed current reuse mixer draws 29 mA and the reference mixer dissipates 27 mA from the 3.3 V supply for the given performance. A 2 GHz carrier tone (local) at -8 dBm (P_{LO}) and a 10 MHz baseband signal at -22 dBm (P_{BB}) were used for these measurements.

The measured results show that the proposed current reuse mixer is better suited for low-voltage applications, and this point is further justified by Fig. 5.13, where mixer P_{OUT} and LO-rej values have been plotted at 100 MHz steps. A maximum measured increase in LO-rej at +18 dB has thus been shown for the proposed mixer, and the simulated data points match the measured ones well. All results were measured with co-planar waveguide probes to make possible the realization of the prototype and various reference blocks on the same die. The active area of the realized current reuse mixer test block in Fig. 5.14 is 0.4 mm $\times$ 0.15 mm.

An increase in supply voltage from 3.3 to 5 volts made possible a comparison of the mixers at a similar P_{OUT} of 0 dBm, a condition which produced similar spurious responses, i.e. both circuits had an 3RD-rej=-37 dBc. However, the proposed mixer achieved a transmitted DR of +158 dB and a SNR of +154 dB, which are both +3 dB better than the respective values measured for the reference circuit. The proposed mixer test block dissipated 50 mA and the reference mixer used 41 mA for the measured performance with the 2 GHz P_{LO} set at -6 dBm for both circuits.

5.7 Summary

In this chapter up-conversion mixer design issues have been introduced, and the different topologies used in the reference quadrature modulators have been described. The four mixers realized for this work have been analyzed, and the measured results of the proposed current reuse mixer have been compared to a reference class AB Gilbert cell. It has been shown that the use of the proposed mixer current reuse mixer improves SNR by +3 dB in comparison to the reference mixer.

6. Output buffering

Base station transmitters for 3G wireless standards require linear buffer stages to be installed after the IQ-modulator to boost the transmitted signal before the PA in order to produce high power transmissions without unacceptable spectral splatter. This leads to an increased bill of materials (BOM) and to increased power dissipation. To minimize the number of expensive discrete buffers, it is advantageous to maximize the linear output power of the IQ-modulator itself. High linearity is of increased importance because of the variable envelope modulations adopted for high bitrate performance in the emerging wireless standards. One such modulation format is OFDM, which entails an envelope variation with a peak-to-average ratio (PAR) of 8-13 dB. The transmitted noise should also be kept as low as possible, since it defines the smallest possible signal which can be transmitted.

The up-converted signal from the quadrature modulator is actually buffered in most applications, not only in base stations, with a buffer amplifier/PA-driver on-chip, with the aim being to magnify the signal so as to ease PA specifications. Therefore, this chapter first considers theories of cascaded stage linearity and noise [99, 100, 28], then reviews the buffers used in the tabulated reference modulators shown in Table 2.1, and finally studies three buffer stages realized for this work.

6.1 Buffer specifications

A direct-conversion quadrature modulator output buffer isolates the modulator from the PA in order to prevent pulling of the VCO, and it should match circuit output to 50 Ω in the operating band. Its dynamic properties include high linearity and low excess noise, and it should possess a high common-mode rejection ratio (CMRR) to improve LO-rej. Quite often the output buffer also performs differential-to-single-ended conversion, either with active circuits or with integrated transformers, e.g. four of the eight reference quadrature modulators shown in Table 2.1

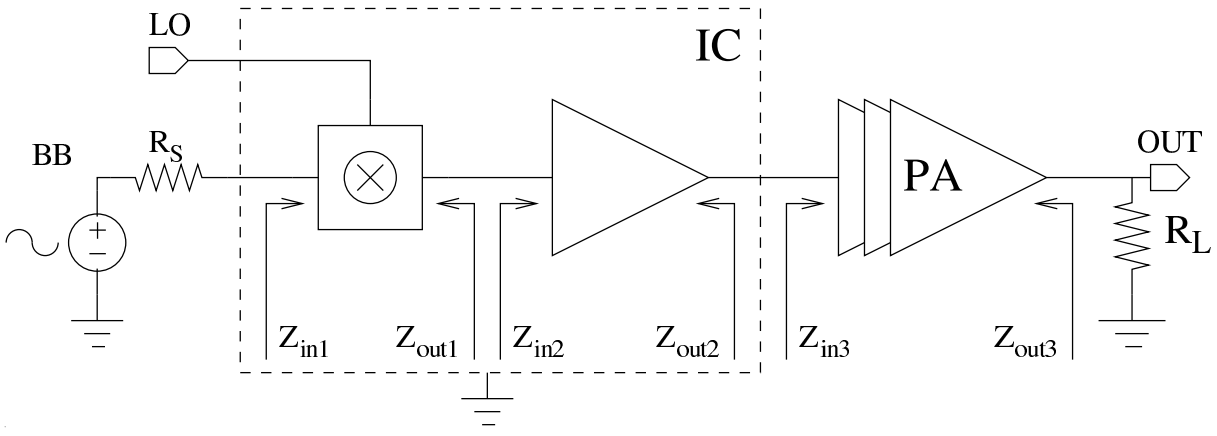


Figure 6.1: Block diagram of direct-conversion quadrature modulator application.

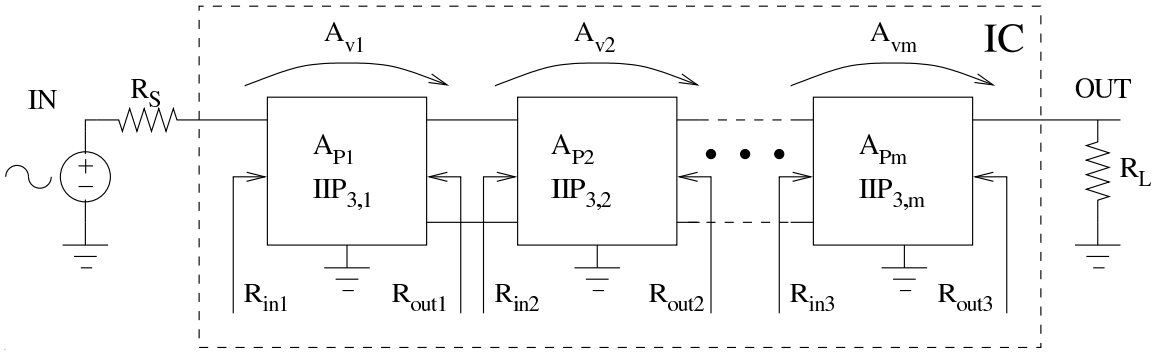


Figure 6.2: Block diagram for a general cascade of m stages with voltage-mode labeling.

have such a functionality integrated in their respective PA drivers, and hence their buffers have been termed as *Integrated buffers*. Correspondingly, the buffers for the remaining four reference modulators, which use off-chip transformers, have been collected under the label of *XFMR buffers*.

The linearity and noise requirements are best contemplated with the help of the block diagram in Fig. 6.1, where the mixer symbol represents the quadrature modulator and its output buffer drives an off-chip PA. For calculations the blocks have been labeled 1, 2, and 3, respectively. First, the linearity of the system will be studied, starting with the definition of its input-referred third-order intercept point (IIP_3). After that, the Friis equation for cascaded stage noise figure (NF) definition will be applied to ICs, to be followed by the sections on different buffers used in the reference quadrature modulators.

6.1.1 Linearity

The IIP_3 for the general case of *m* cascaded stages shown in Fig. 6.2 can be defined in voltage-mode, and it is given by:

$$\frac{1}{\mathrm{IIP}_3^2} \approx \frac{1}{\mathrm{IIP}_{3,1}^2} + \frac{A_{v1}^2}{\mathrm{IIP}_{3,2}^2} + \ldots \frac{\left(A_{v1} \cdots A_{v(m-1)}\right)^2}{\mathrm{IIP}_{3,\mathrm{m}}^2} \tag{6.1}$$

Since this work deals with transmitters it is appropriate to manipulate (6.1) into an output-referred version given by:

$$\frac{1}{\mathrm{OIP}_3^2} \approx \frac{1}{\mathrm{OIP}_{3,1}^2 \cdot \left(A_{v2} \cdots A_{vm}\right)^2} + \frac{1}{\mathrm{OIP}_{3,2}^2 \cdot \left(A_{v3} \cdots A_{vm}\right)^2} + \ldots + \frac{1}{\mathrm{OIP}_{3,\mathrm{m}}^2} \tag{6.2}$$

Both output- and input-referred definitions lead to the same conclusion: if the first two stages have any notable gain, then the linearity of the last stage dominates system behavior. The $\approx$ sign has been used to denote the fact, that (6.1) gives a worst-case estimate of IIP_3 [28].

Of special interest is the application of the developed output referred equation (6.2) to the IC block in Fig. 6.1, i.e. to study what (realistic) conditions should be fulfilled for optimal linearity performance, as described by OIP_3. To accomplish this (6.2) is solved for two stages *m=2* to give:

$$\mathrm{OIP}_3 = A_{v2} \cdot \sqrt{\frac{1}{\frac{1}{\mathrm{OIP}_{3,1}^2} + \frac{1}{\mathrm{IIP}_{3,2}^2}}} \tag{6.3}$$

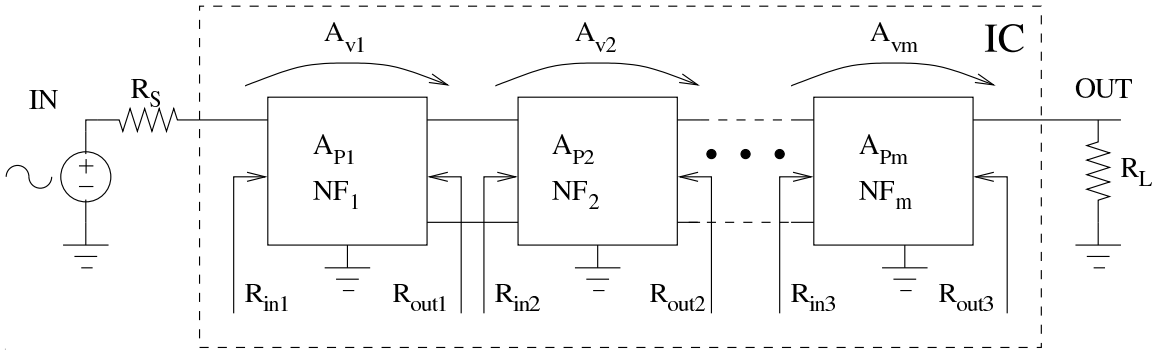


Figure 6.3: Block diagram for redefinition of the Friis equation for IC-applications.

6.1.2 Noise

Although the optimization of noise performance does not dominate output buffer design as much as it does LNA design, it is still important to add as little excess noise to the transmitted signal as possible. The noise factor (F) defines the corruption of the input signal by circuit block excess noise, and it can be defined as:

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = \frac{1}{A_P} \cdot \frac{N_{out}}{N_{in}} \tag{6.4}$$

To avoid confusion, it should be noted that the noise figure is defined as:

$$NF = 10\log_{10}(F) \tag{6.5}$$

The well-known Friis equation was derived for the analysis of noise propagation in a cascade of discrete circuits with matched inputs and outputs, and it ties system noise properties to individual block noise factors and their available gains A_P, as in:

$$NF = NF_1 + \frac{NF_2 - 1}{A_{P1}} + \cdots + \frac{NF_m - 1}{A_{P1} \cdots A_{P(m-1)}} \tag{6.6}$$

However, the Friis equation is not directly applicable to the direct-conversion quadrature modulator case in Fig. 6.1, since it does not have matched inputs and outputs, at least not in its IC block. To correct this the generalized block diagram in Fig. 6.3 depicts a system with unmatched circuit blocks, and redefining (6.5) to take into account the effect differing impedances have on circuit noise performance gives an IC version of the Friis equation as:

$$\begin{aligned} NF =& NF_1 + \frac{NF_2 - 1}{\left(\xi_{0,1}A_{v1}\right)^2} + \cdots + \frac{NF_m - 1}{\left(\xi_{0,1}A_{v1} \cdots \xi_{m-2,m-1}A_{v(m-1)}\right)^2} \\ &, \; where \; \xi_{m-2,m-1} = \frac{Z_{in,(m-1)}}{Z_{in,(m-1)} + Z_{out,(m-2)}} \end{aligned} \tag{6.7}$$

This version of the Friis equation holds [100] if individual block noise factors have been tested with source impedances which are close enough for the realized impedances in the cascade. If this is the case, each block will deliver nominal F performance. However, this is a real problem in the application of (6.7), since F is almost always measured and simulated in a 50 Ωenvironment.

6.2 Integrated buffers

Three of the eight reference quadrature modulators in Table 2.1 use buffers with a single-ended output, whereas five units use differential outputs combined with off-chip transformers. There

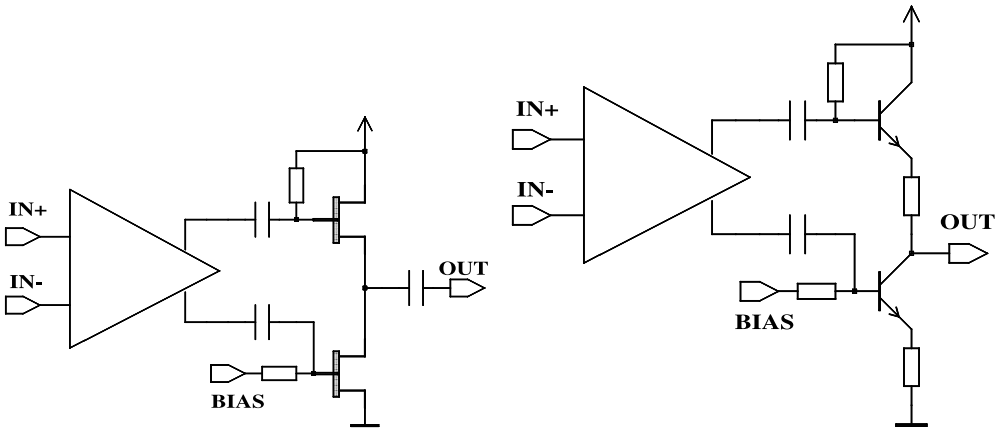


Figure 6.4: Two buffers using totem-pole output stages include a) a source-follower/common-source GaAs MESFET, and b) an emitter-follower/common-emitter bipolar output stage.

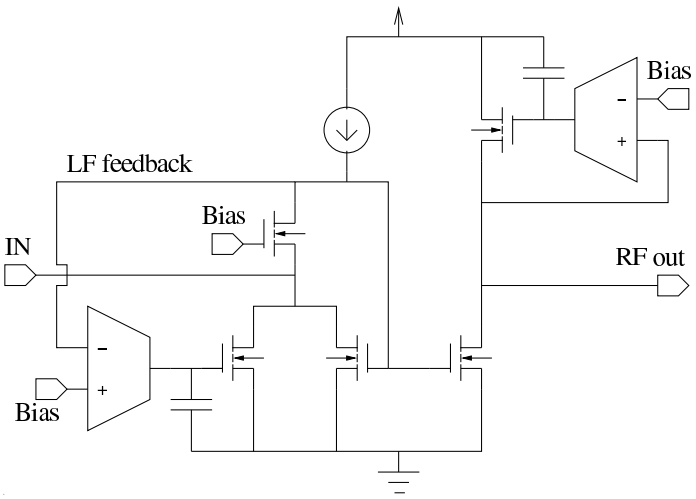


Figure 6.5: The current-mode single-ended buffer [42].

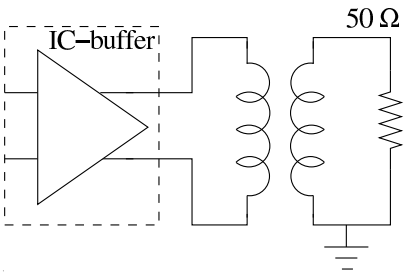


Figure 6.6: Transformer conversion of a differential output to drive a 50 Ω load.

are pros and cons to each of these approaches, but good common-mode rejection is particularly important in order to have good LO-rej performance and for increased suppression of even-order spurious products. The following sections will be used to discuss the published properties of each of the buffers.

6.2.1 Balun buffers

The totem-pole buffers in Fig. 6.4 both perform differential-to-single-ended conversion by means of the combination of an in- and an out-of-phase stage. The quadrature modulator in [46] uses a source follower (in-phase) and a common-source (out-of-phase) stage in Fig. 6.4(a) for an output return loss S_{22} of -15 dB or better over the whole operating frequency range 0.7-3 GHz. A differential amplifier has been inserted before the output stage to increase circuit CMRR and thereby its LO and even-order spurious rejections. Thus the reported LO-rej stays below -40 dBc. The totem-pole buffer [41] in Fig. 6.4(b) has an output stage which is much like a copy of the source follower/common-source buffer in Fig. 6.4(a), the only difference being that it is implemented with bipolar transistors and matched to 50 Ω with a low-value resistor at its

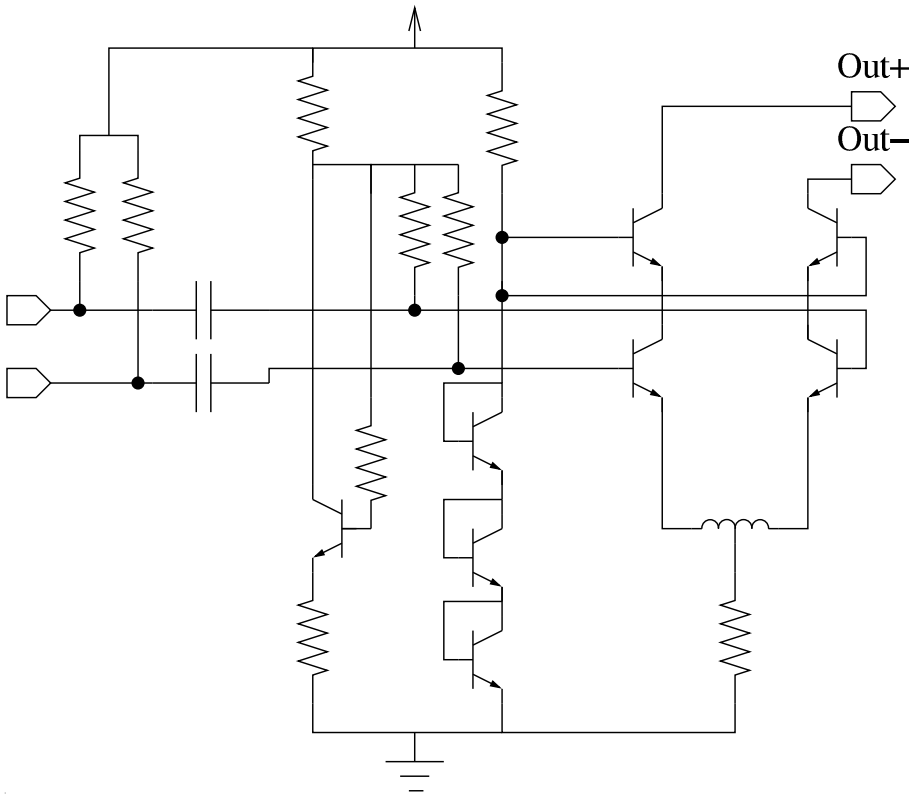


Figure 6.7: Open cascode differential pair buffering example [40].

output. Two emitter-followers are used to drive the output stage for extended bandwidth and high linearity. The realized resistively matched buffer is broadband with a reported minimum OP_{1dB}=-2 dBm over the whole operating frequency range 0.8-2.7 GHz.

6.2.2 Single-ended buffers

The single-ended current-mode output buffer in Fig. 6.5 mirrors input current to output which has been loaded with a regulated PMOS transistor synthetic coil. The circuit has been realized in a 0.25 μm CMOS process, and its characteristic features include: very low input impedance at high frequencies; mirroring of input current to output, and use of an active coil at its output. The use of this active circuit enhances the application range of the device, but at the cost of a first-order amplitude roll-off. Such a topology is needed to test the cold MOSFET mixer in [42]. However, the noise penalty involved in the use of active coil topologies has been shown to be excessively high [101], at least in bandpass filtering applications.

6.2.3 Differential buffers

The reference quadrature modulators shown in Table 2.1 make use of an external transformer either by connecting to it directly [45, 10], or by driving it with an integrated buffer as in Fig. 6.6. The integrated buffers used in the references are either resistively loaded differential pairs [44] or open-cascode buffers [43, 40]. The use of an open-cascode buffer is not limited by voltage headroom concerns, since the supply for the output stage can be connected either via external resistors or via a transformer center tap. This has been utilized for the example in Fig. 6.7 by loading it with two external 3 nH pull-up inductors which connect to two 1.3 pF series capacitors to provide a high OP_{1dB} and acceptable matching with an output return loss at better than -10

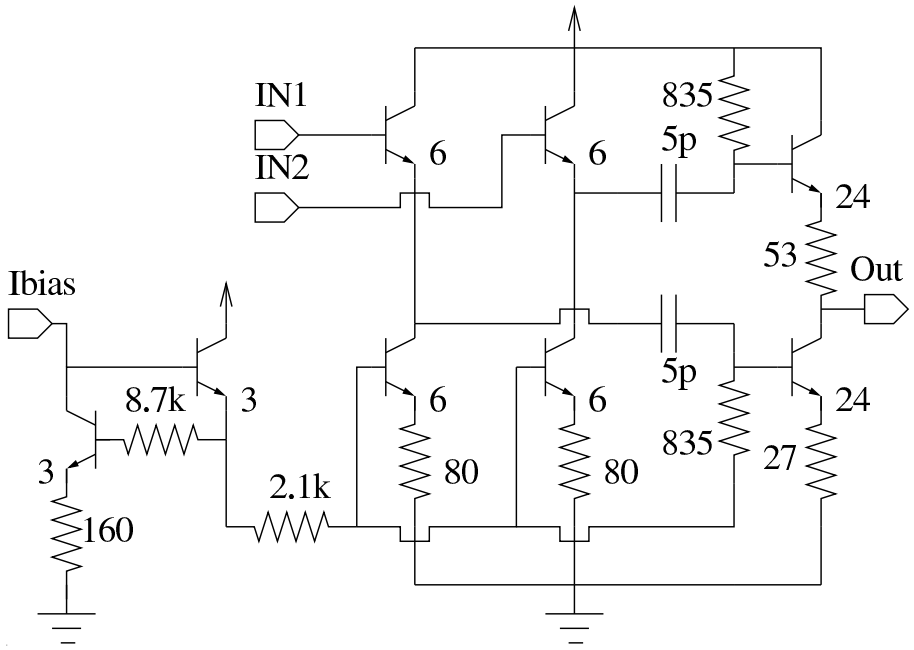


Figure 6.8: Schematic of the realized 0.8 μm SiGe buffer.

Table 6.1: Simulated characteristics for the realized 0.8 μm SiGe buffer.

A_v	[dB]	2
BW	[GHz]	7.3
ϕ	[deg.]	74
S_{22}	[dB]	$<$-20
OP_{1dB}	[dBm]	0
P_{1dB}	[dBV]	-4
3RD-rej	[dBc]	-38
2ND-rej	[dBc]	-31
N_{+20MHz}	[dBm/Hz]	-161
freq.	[GHz]	2.45
I_{DD}	[mA]	9.8
V_{DD}	[V]	2.5

dB over the UMTS downlink band. The matching networks were cascaded with LC lumped element transformers for the measurements. With this setup it is possible to attain a high DR, but the lumped element baluns are only usable for narrow application bands and the BOM is increased by the multiple discretes required.

6.3 The realized 0.8 μm SiGe buffer

The first of the output buffers designed for this work is a totem-pole circuit, and it was used as an output buffer for the 0.75-3.6 GHz direct-conversion quadrature modulator reported in [18]. The 0.8 μm SiGe process has an f_T=35 GHz, high-density poly-poly capacitors, a high-resistivity resistor option, and inductor library elements. The realized buffer is shown in Fig. 6.4(b), and its simulated characteristics in a typical operation point are collected in Table 6.1.

A 0.8 mA biasing current was required for the reported 9.8 mA current dissipation, and 5.6 mA of this current is directed to the output stage, while 1.6 mA is dissipated in each of the

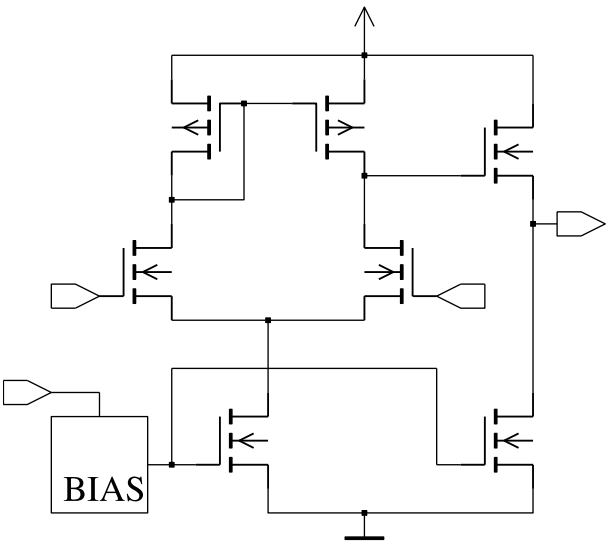


Figure 6.9: Schematic of the realized 0.13 μm CMOS buffer.

Table 6.2: Simulated characteristics for the realized 0.13 μm CMOS buffer.

A_v	[dB]	20
BW	[GHz]	18
ϕ	[deg.]	8
S_{22}	[dB]	< -18
OP_{1dB}	[dBm]	-5
P_{1dB}	[dBV]	-23
3RD-rej	[dBc]	-40
2ND-rej	[dBc]	-30
N_{+20MHz}	[dBm/Hz]	-155
freq.	[GHz]	2.4
I_{DD}	[mA]	6.6
V_{DD}	[V]	2.2

emitter-follower stages driving it. This broadband buffer has a high phase margin of 74° at its unity-gain BW of 7.3 GHz, and since its output return loss S_{22} stays well below 0 dB its stability is not a concern. In fact, comparison to the simulated large signal characteristics shows that the buffer combines good output matching with good linearity, as its simulated OP_{1dB} is 0 dBm at 2.45 GHz, whereas its output return loss stays below -20 dB in the 0.6-6 GHz range. Harmonics rejection and noise performance have been tabulated at a -3 dB power backoff from the 0 dBm compression point, both for the given 2.45 GHz test frequency. The second harmonic rejection (2ND-rej) has been given as a measure of system balance, since ideally its value should be $-\infty$.

The emitter current densities of the buffer have been optimized to values below 280 μA/μm as is seen by a comparison of the given emitter-follower and output stage currents of 1.6 and 5.6 mA to the emitter areas annotated in μm in Fig. 6.4(b). Simulation study confirms the validity of the chosen biasing point, as an increase of bias gave a maximum improvement of +1 dB to the OP_{1dB}. However, the typical biasing point was set at the tabulated lower value to save current and to minimize the risk of failure caused by excessive current densities. If the current densities are kept the same, it is possible to double the circuit area and current dissipation for a +3 dB increase in OP_{1dB}. This is typical class A circuit behavior, and such improvement is obviously limited by the permitted current dissipation, circuit area, and parasitics.

6.4 The realized 0.13 μm CMOS buffer

Since a near-nanometer-level technology was available for the second test circuit realized for this thesis, with f_Ts rising to several dozen gigahertz even for a PMOS device, it was decided to study whether a current-mirror loaded differential pair could be used as an output buffer for the modulator. Possible benefits include good common-mode harmonic rejection and high voltage-mode gain, but caution is needed as its input stage Miller capacitance might be too high. The high gain of the buffer (second stage) should contribute towards a higher OIP_3 as predicted by (6.3), but this is limited by compression of individual cascaded devices. However, part of the buffer gain could be traded for higher linearity, if needed, and optimized with mixer linearity design. As simulations predicted that the quadrature modulator could be buffered with such an

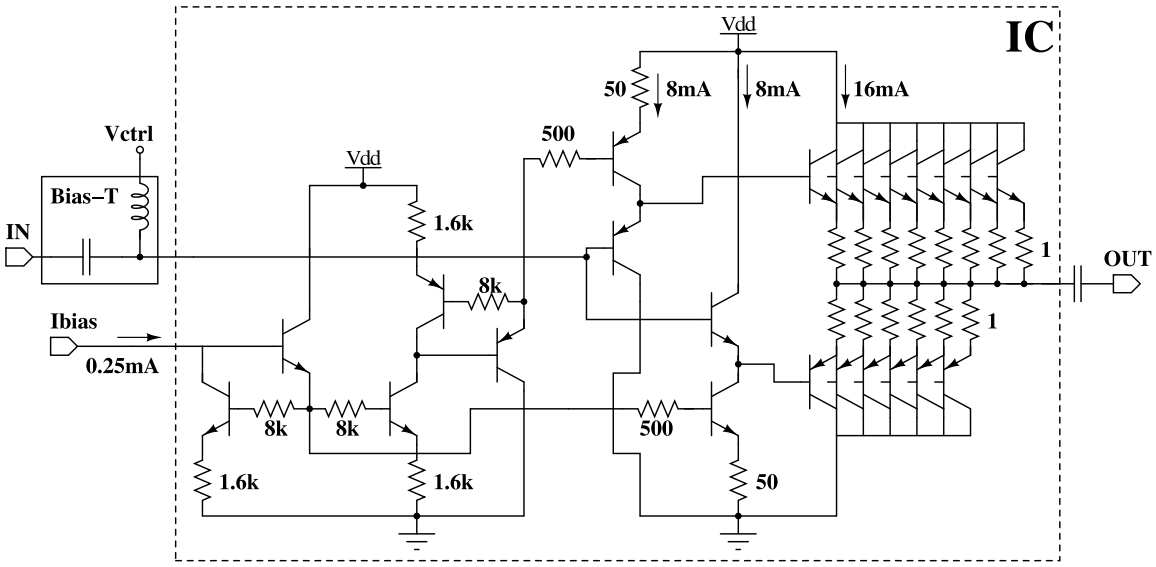


Figure 6.10: Microwave push-pull with ballasting resistors shown.

amplifier without excessive decrease in the available bandwidth, the differential pair output was buffered with a source-follower to realize the buffer shown in Fig. 6.9.

The simulated characteristics shown in Table 6.2 give the buffer voltage-mode GBW as 180 GHz, which is impressive since only 6.6 mA is dissipated from the 2.2 V supply used. As in [88], the source-follower output buffer gives a good output match, as the simulated output return loss is better than -18 dB in the 0.6-6 GHz band. The very low phase margin of 8°, however, is also as expected for a HF/VHF amplifier [96] with an uncompensated frequency response. This low phase margin often indicates possible stability problems, but since harmonic balance stability analysis predicted stable performance with the buffer, it was decided to implement and test the buffer.

Large signal simulations were performed with the circuit driving a 50 Ω load through an ideal dc block. From the tabulated results it is evident that whereas the spurious tone rejection performance of the CMOS buffer (2ND-rej, 3RD-rej) is comparable to that of the SiGe buffer, it is inferior in compression point ($\mathrm{OP_{1dB}}$) and noise ($\mathrm{N_{+20MHz}}$) performance. A +4 dB increase in $\mathrm{OP_{1dB}}$ is easily obtained by the insertion of small, e.g. 24 Ω input stage source-degeneration resistors, and by a simultaneous increase in the output stage area and currents by a factor of $1.5 - 3\times$. For example, a doubling of the source-follower increases the output stage current from 3.6 to 7.3 mA, while stability and an acceptable biasing point are maintained. Combined with a 24 Ω degeneration resistor value, these measures produce the compression point characteristics: $\mathrm{OP_{1dB}}$=-1.4 dBm and $\mathrm{P_{1dB}}$=-19 dBV. Further linearity improvement is prevented by the low 2.2 V supply voltage.

The noise floor characteristics $\mathrm{N_{+20MHz}}$ stands for noise delivered to the 50 Ω noiseless load at a 20 MHz distance from the 2.4 GHz test signal as simulated over a bandwidth of one Hertz. Improvement of the $\mathrm{N_{+20MHz}}$ characteristics shown in Table 6.2 is not possible with the listed scaling approach for linearity improvement, and its impact on system performance remains to be evaluated in the light of the realized buffer DR. The realized DR could in fact be improved if it were possible to safely increase $\mathrm{V_{DD}}$ to e.g. 2.5 V without breaking the narrow linewidth transistors. With a 2.5 V supply, $\mathrm{OP_{1dB}}$=+2.6 dBm and $\mathrm{N_{+20MHz}}$=-152 dBm/Hz could be obtained as based on simulations with 74 Ω input stage source-degeneration resistors and $3\times$ the nominal emitter-follower output stage. This would more than double buffer DR ($\mathrm{OP_{1dB}}$-$\mathrm{N_{+20MHz}}$), from the nominal +150 dB to +154 dB.

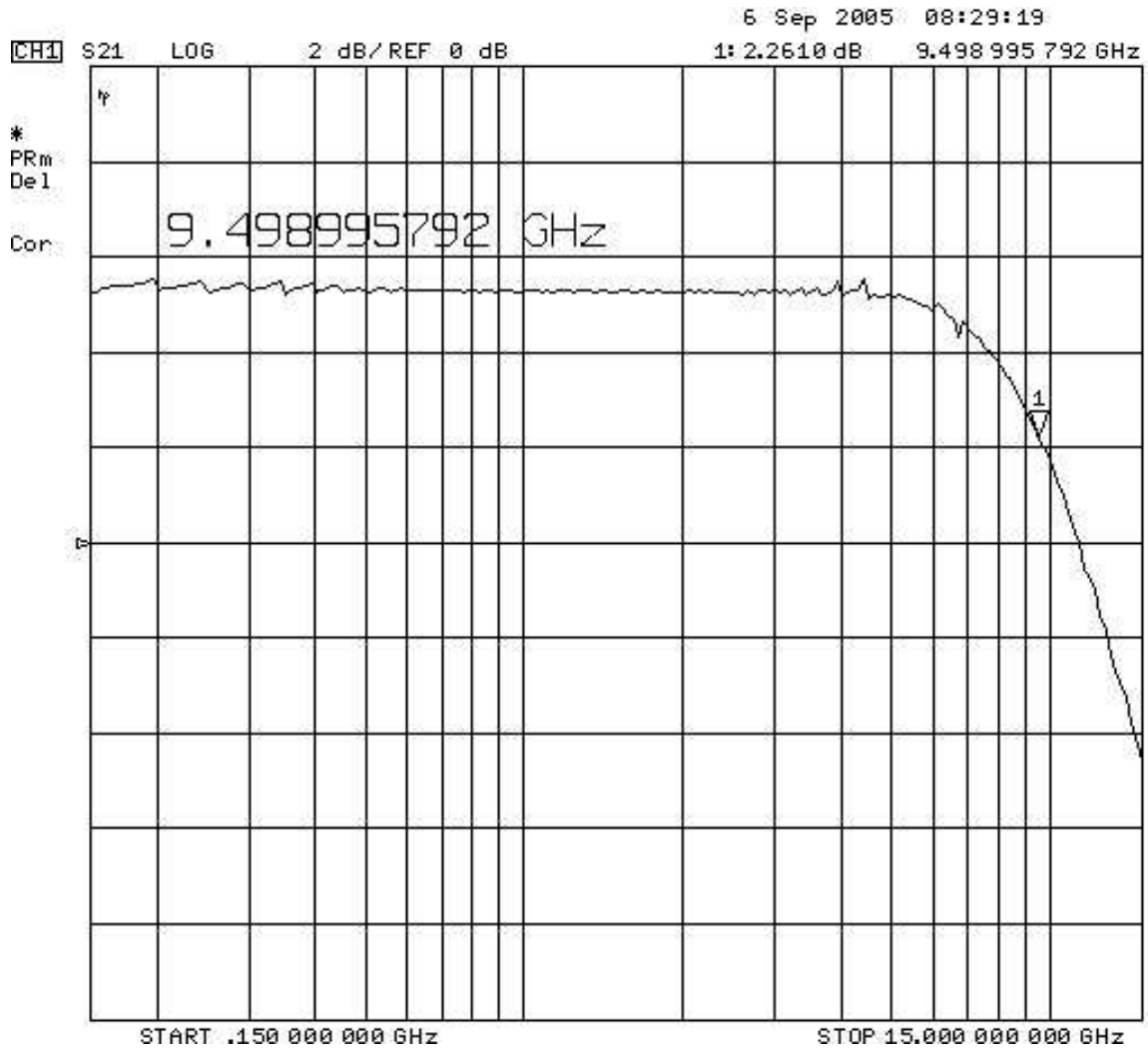


Figure 6.11: Measured push pull stage insertion gain S_{21} at 33 mA/5 V_{DD} nominal operating point.

Table 6.3: Comparison of push-pull to a cascaded CC-stage.

		CC-CC*	Push-pull*	Push-pull
A	dB	5	6	6
BW_{3dB}	GHz	15	11	9.5
P_{OUT}	dBm	0	0	0
2ND-rej	dBc	-36	-48	-48
3RD-rej	dBc	-42	-57	-54
OP_{1dB}	dBm	+7	+11	+9
OIP_3	dBm	-	-	+22
NF	dB	4	4	5
I_{DD}	mA	32	33	33
V_{DD}	V	5	5	5

** simulated results*

6.5 The realized 0.4 μm complementary SiGe buffer

The 0.4 μm complementary SiGe technology can be used to extend the bandwidth of an emitter-follower push-pull stage from VHF to microwave frequencies with a high current drive capability similar to its predecessor [102]. However, because of the insulating SOI substrate, there is a risk of thermal run-off. To prevent this, each output stage emitter stripe of the designed push-pull in Fig. 6.10 has been ballasted with a single 1 Ω metal path resistor.

The measured insertion gain S_{21} of the push-pull stage at the chosen nominal biasing point of 33 mA from a 5 V supply is shown in Fig. 6.11 with a BW of 9.5 GHz. Other measured data at a 2 GHz signal frequency include: OP_{1dB}=+9 dBm, OIP3=+22 dBm and NF=5 dB, whereas the second and third harmonic products lie at -48 dBc and -54 dBc in relation to the chosen nominal 0 dBm output power. These values reveal that good linearity and noise performance have been achieved without coils, since typically this level of performance requires the use of a distributed amplifier with a multitude of integrated coils, which increases the IC-area to 4-80 times that of the push-pull stage. In fact, the 0.11 mm $\times$ 0.24 mm active area prototype contains two push-pull stages and their shared biasing. A single push-pull measures 0.11 mm $\times$ 0.1 mm. The small IC area and high linearity (OIP3=+22 dBm) of the push-pull stage suggest it has potential for use in broadband high-output-power ICs.

The measured push-pull data match simulated values reasonably well at the same operating point, with exact matches on S_{21}=6 dB, P_{OUT}=0 dBm, and 2ND-rej=-48 dBc; the remaining differences can be listed with simulated values in parentheses as: BW=9.5(11) GHz, 2ND-rej=-54(-57) dBc, OP_{1dB}=+9(+11) dBm, and NF=5(4) dB. Therefore simulated values can be used to compare the proposed push-pull buffer to a cascade of two CC-stages at a similar biasing point and P_{OUT}. A comparison of the simulated results predicts a +12 dB improvement in harmonics attenuation for the push-pull stage at the 2 GHz test frequency. This improvement in linearity is confirmed by the predicted increase in OP_{1dB} of +4 dB for the push-pull stage, and it is due to the increased current drive capability of the implemented complementary circuitry. The penalty for this increase in linearity is a simulated 4 GHz drop in BW when the push-pull BW of 11 GHz is compared to the CC-reference BW of 15 GHz.

To test for possible thermal run-off, a pair of close-lying push-pull stages was biased at almost twice the nominal current of 33 mA to dissipate 300 mW each from the 5 V supply: as a result a gain stability of $\pm$0.1 dB was measured during a period of 18 h, with no traces of thermal run-off. Since a corresponding 12 h current dissipation measurement set I_{DD} at 59.8$\pm$0.3 mA, it is safe to conclude that thermal run-off can be prevented by ballasting.

6.6 Summary

The quality of quadrature modulator output buffering has a deciding role in determining the BOM in transmitter applications, since with a super-linear stage very high output powers could be produced and this would lead to a decreased number of, or to a complete elimination of expensive discrete PA drivers. Alas, super-linear performance is elusive, and, on the basis of the best performing samples, also V_{DD} limited.

7. Broadband quadrature modulators

Results on the realized direct-conversion quadrature modulators will be given in this chapter, with comparison to the other quadrature modulators shown in Table 2.1. The first section contains brief summaries of the reference direct-conversion quadrature modulators, and it is followed by separate sections on the realized SiGe and CMOS quadrature modulators. The chapter concludes with a comparison of the reported characteristics.

7.1 Integrated direct-conversion quadrature modulators

Since this work has concentrated on the quality of LO quadrature signaling, this approach forms a natural classification of the circuits shown in Table 2.1, although other criteria could easily be found, e.g. only two out of the ten tabulated IQ modulators have been tested with integrated baluns: one of these is the 0.8 μm SiGe prototype described in this work; the other has been reported in a journal paper by Bóveda et al. [46]. Nevertheless, the following subsections elaborate on RC-CR, polyphase, and div-by-2 quadrature modulators.

7.1.1 Modulators with tunable RC-CR quadrature generation

The four quadrature modulators falling into this category have varied reported performances, with IRR values ranging from -30 to -40 dBc, while operating bandwidths range from one octave to a variation of over two octaves in output frequencies. The earliest of the included papers is the journal paper already mentioned from 1993 by Bóveda et al. [46], which reports an IRR of -40 dBc in a two-octave bandwidth from 0.7 to 3.0 GHz. A notable feature of the reported modulator is that it is fully integrated with LO and output baluns, but the circuit utilizes off-chip tuning for the reported performance. Thus the use of its broadband performance for multi-mode radios would require the development of an automated control co-circuit, which would add to the cost of the system.

The two journal papers reported in 1996 both use the basic RC-CR loop for quadrature generation, and complement it with limiter amplifiers and/or off-chip tuning to attain a mediocre IRR performance. The journal paper by Tsukahara et al. [44] achieves an IRR of -35 dBc in a bandwidth of over one octave from 0.8 to 2.0 GHz. The most notable feature of this paper is that it points out limitations of the basic Gilbert mixer under low supply voltage conditions, and proposes the use of a separate amplifier to drive a two-stacked transistor mixer core with dc bias and signaling. This approach makes possible the use of a 2 V supply voltage, but the use of such a pre-amplifier biased mixer increases noise and creates a very difficult gain-linearity tradeoff situation for the designer.

In contrast, the journal paper by Otaka et al. [45] achieves an IRR of -30 dBc in a one-octave bandwidth from 1.2 to 2.3 GHz. The most notable feature of this paper is its analysis of limiter amplifier operation and the proposed use of an integerated coil in its LO input buffer. However, the reported IRR and operating bandwidth suggest that this approach is limited, possibly as a result of AM-PM distortion introduced in LO quadrature signaling by the limiter amplifiers.

Although the data available on the IQ modulator reported in 1997 by Teetzel [43] are not complete in the sense that they report an IRR of -60 dBc at a single frequency of 884 MHz, whereas its reported operating bandwidth ranges well over a decade, from 250 to 4000 MHz, this work has been included because of its unique LO quadrature generator, which utilizes feedback correction of the RC-CR generated IQ-signaling. The combination of feedback circuitry with off-chip tuning results in an extremely robust performance under temperature variations. Feedback enables this circuit to withstand element value variations to such an extent that its intended application is for use in a general-purpose test-signal generator. The reported -6 dBm nominal output power is also quite high, but achieving this requires the use of a discrete passive balun and high current dissipation of 250 mA from a -6 V source.

7.1.2 Modulators with PP quadrature generation

The three quadrature modulators falling into this category have varied reported performances, with IRR values ranging from -28 to -35 dBc, while operating bandwidths range from over one octave to over two octaves. Such characteristics have already been reported for the RC-CR realizations, but PP filtering can be used to get such a performance without tuning. The earliest of the papers included is a conference paper from the year 1998 by Borremans et al. [42], which reports an IRR of -35 dBc in a two-octave bandwidth from 0.6 to 3.0 GHz. This performance is as expected for a 3-stage PP filter over such an operating band. A notable feature of this paper is its very good LO-rej performance, which results in reported LO leakage values of -45 dBm up to 3 GHz; this performance has been attributed to its single-ended current mode buffer, which was loaded with a synthetic inductor. However, synthetic inductors are noisy, the required LO power is quite high at +6 dBm, and the proposed LC resonator BB interface is cumbersome for a broadband BB input realization.

The two remaining conference papers report IQ modulators intended for basestation applications with an emphasis on maximized TDR. The importance of these papers is increased by the fact that they actually promote commercial direct-conversion quadrature modulators in the marketplace, and thus they represent true state-of-the-art performance. The conference paper by Sam et al. from the year 2001 [41] reports a TDR of 157 dB at 2 GHz; this notable TDR was achieved through the use of a current feedback opAmp-driven mixer. In the microwave signal path, the LO is input differentially to be converted into quadrature signaling by a cascade of two two-stage PP filters for an IRR performance of -28 dBc in a bandwidth of almost two octaves, from 0.8 to 2.7 GHz. An off-chip surface mount transformer was used for the differential-to-single-ended conversion of the LO signaling. With a totem-pole output buffer the circuit has a single output matched to 50 Ω, and an OP_{1dB} of -1 dBm at the 2 GHz test frequency. To summarize, this paper presents solid performance with a high TDR and mediocre IRR. An in-house complementary bipolar process with an insulating substrate and a high 5 V supply with 65 mA current dissipation was required for the cited performance.

The conference paper by Karthaus et al. from the year 2004 [40] achieves a TDR of 161 dB and an IRR of -34 dBc in a two-octave bandwidth, from 0.7 to 2.7 GHz. A three-stage PP filter was utilized for this performance. The most notable feature of this quadrature modulator is its mixer, which was given a two-stacked-transistor configuration with no dc connection, i.e. this device is actually an intermediate-frequencies (IF) quadrature modulator. Combined with the current bypass resistors feeding current past the mixer switching quad, these techniques make possible the optimization of the mixer operating point for increased TDR. Two open-collector cascode amplifiers were used to drive an off-chip lumped element transformer for a best reported performance of OP_{1dB}=+14.3 dBm. However, the performance was reported for a setup optimized for the UMTS downlink frequency range operation at ca. 2 GHz. Additionally,

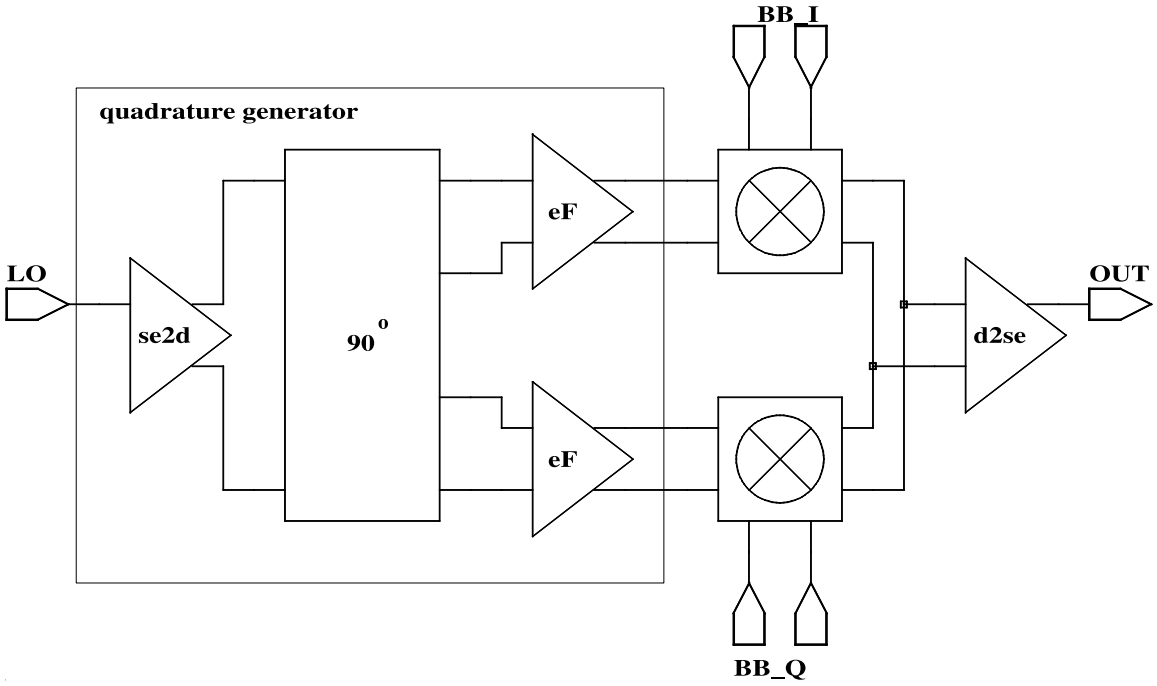


Figure 7.1: Block diagram of the 0.8 μm SiGe direct-conversion quadrature modulator.

the inductive degeneration used in the mixers makes the reported results susceptible to changes in frequency.

7.1.3 Modulators with div-by-2 quadrature generation

The conference paper by Eloranta et al. from the year 2005 is the only reported broadband direct-conversion quadrature modulator with a div-by-2 LO quadrature generator, and this is probably due to the technique's well-known dependence on a perfectly bi-phased 50/50 clock signal, which is difficult to produce at microwave frequencies. Nevertheless, although the div-by-2 circuit has been listed as the performance-limiting factor, the reported digital up-converter achieves an IRR of -39 dBc with a variation in output frequency of over a decade, 0.1 to 2.6 GHz. The elimination of offsets which arise from mismatches in the analog baseband has also helped to produce an impressive LO-rej of -43.5 dBc over the reported operating band, but two off-chip baluns were required for this performance, one for LO, the other for output. However, this approach suffers from various drawbacks, which are missing in the traditional baseband interface of a DA, low-pass filter, and an analog mixer cascade. These drawbacks include a high noise floor and dependence on the availability of a modern CMOS technology; at a fundamental level the circuit utilizes the sinc effect through high oversampling ratios, and this precludes some of the wider band signaling applications, e.g. at an oversampling ratio of 100, the MB-OFDM approach for UWB would need a baseband capable of operating at 25.6 GHz.

7.2 The realized 0.8 μm SiGe quadrature modulator

This modulator circuit was built to test a completely integrated microwave signal path and the limitations imposed on available performance without the use of external transformers. The schematic of the realized IQ modulator in Fig. 7.1 combines the LO balun, quadrature generator, mixer, and output buffer circuits from Sections 3.5, 4.5, 5.4, and 6.3.

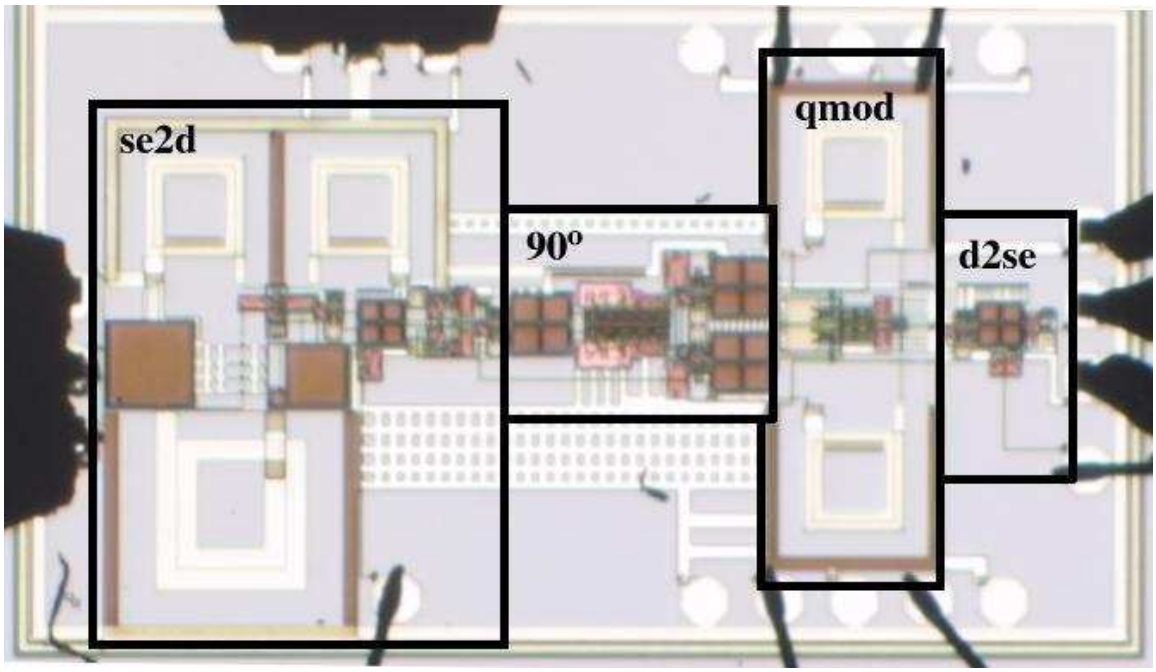


Figure 7.2: Micrograph of the SiGe direct-conversion quadrature modulator, showing blocks (left to right): quadrature-generator (*se2d, 90°*), mixers (*qmod*), and differential-to-single-ended buffer *d2se*.

7.2.1 Measurement setup

The 0.8 μm SiGe prototype measurement setup includes a combination of wafer probing and use of a PCB. RF-signals (LO, output), single supply, and ground were probed to IC; baseband signals (I/Q) and bias currents were directly bonded to the PCB and its SMA connectors. This kind of mixed measurement setup was necessary because of the large number of input/output pins, which made probing-only measurements impossible. The advantage of co-planar wafer probes in this case lies in their extremely low inductive parasitics, as they add a mere 20 pH inductance to signal paths. For the frequency range of interest, 0-6 GHz, this corresponds to an ideal short for all practical purposes. A micrograph of the measured chip with the wafer probes in place is shown in Fig. 7.2. The rectangular die form resulted from the desire to keep the high-frequency signal path as straight as possible. The die area of the direct-conversion quadrature modulator shown in Fig. 7.2 measures 2.2 mm $\times$ 1.3 mm (pads included).

7.2.2 Experimental Results

Table 7.1 collects the measurement results at two LO frequencies (1 GHz and 2.4 GHz) with biasing points at 96 mW and 115 mW, respectively. The extra 19 mW at 2.4 GHz was dissipated in the LO signal buffering se2d block to compensate for the gain roll-off at 2.4 GHz. All the results were obtained at room temperature (ca. 25 °C), and they include measurement setup losses, which are roughly 1.5 dB for the high-frequency output. Only the scattering parameter (S_{11}, S_{22}) measurements were made with a measurement setup calibrated for the 40 GHz co-planar waveguide probes. The measured quadrature modulator output matching is very good, with reported S_{22} values at -22 dB, while LO signal input matching is not this perfect, with an S_{11} value of -5 dB at 1 GHz. However, LO matching correctly improves towards higher frequencies, giving an S_{11} value of -8 dB at 2.4 GHz. Tabulated data have been collected with the desired channel set at LO+BB (1001, 2401) MHz, and channel images at LO-BB (999, 2399)

Table 7.1: Measured results of the 0.8 μm SiGe quadrature modulator.

		@1 GHz	**@2.4 GHz**
P_{OUT}	[dBm]	-13.9	-16.4
IRR	[dBc]	-72	-50
LO-rej	[dBc]	-35	-30
3RD-rej	[dBc]	-37	-37
2ND-rej	[dBc]	-35	-42
OP_{1dB}	[dBm]	-10	-14
OIP_3	[dBm]	-1	–
N_{+20MHz}	[dBm/Hz]	–	-136
S_{11}	[dB]	-5	-8
S_{22}	[dB]	-22	-27
LO	[dBm]	-14.5@1 GHz	-14.5@2.4 GHz
BB	[V_{RMS}]	0.5@1 MHz	0.5@1 MHz
I_{DD}	[mA]	38.5	46
V_{DD}	[V]	2.5	2.5
P_{DD}	[mW]	96	115

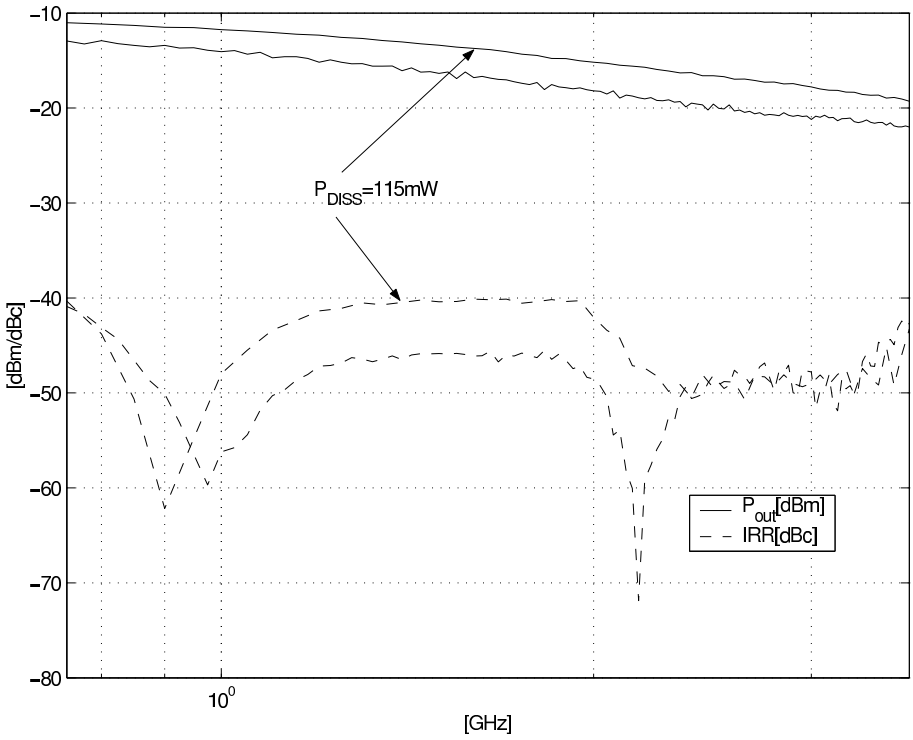


Figure 7.3: Measured (P_{OUT}) and image-rejection ratio (IRR) values.

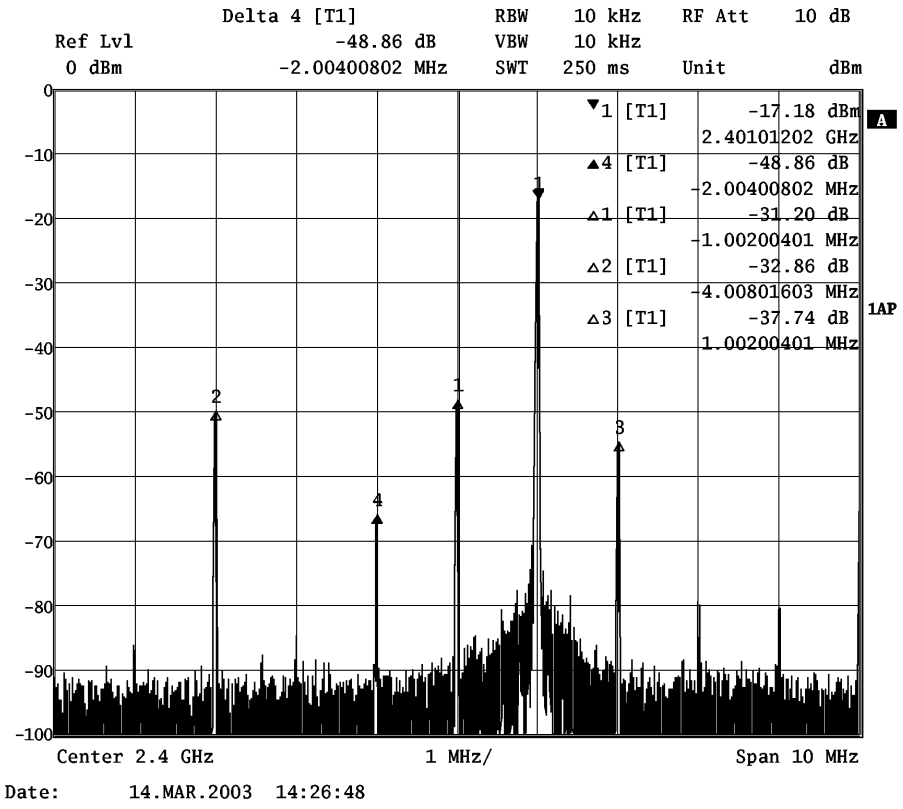


Figure 7.4: Measured spectrum at 2.4 GHz with a 2 V supply.

MHz. The measured output powers (P_{OUT}) are better than -16 dBm with good image-rejection ratios (IRR) at -50 dBc or better; for a broadband quadrature modulator this is one of the best reported, especially considering the circuit's low current dissipation (I_{DISS}).

Higher power dissipation could be used for improved linearity, while the currently reported output -1 dB compression (OP_{1dB}=-10 dBm) and third-order intercept points (OIP_3=-1 dBm) confirm robust circuit performance with the near 10 dB difference. For the determination of third (3RD: LO-3BB) and second (2ND: LO+2BB) harmonics rejection characterics, spurious signals at the highest power levels were selected. Reported 2ND rejection and LO leakage suppression (CRR) values, both at -35 dBc, confirm that the integrated baluns (se2d, d2se) operate satisfactorily. In fact, the use of a very low LO signal level at -14.5 dBm is possible because of the high gain of the LO buffering se2d block. Frequency sweep results (P_{OUT}, IRR) for the two biasing points (96 mW and 115 mW) in Table 7.1 are shown in Fig. 7.3. The depicted results show good broadband performance with measured IRR values at better than -40 dBc in the range 0.75-3.6 GHz. These results were measured with the bias and signaling shown in Table 7.1, with no tuning applied. This, in combination with the large number of measured data points at 25 MHz steps (96 mW, 50 MHz steps for the 115 mW-case), gives a concise view of the performance of this quadrature modulator as a single-sideband transmitter. To demonstrate the low-voltage performance of the proposed quadrature modulator, a spectrum measured while dissipating 90 mW for a 2 V supply is repeated in Fig. 7.4. Only a slight deteriation in performance can be detected in comparison to the corresponding values reported in Table 7.1. Output signal and image rejection are practically the same, with a 1 dB difference, and LO leakage is still acceptable at -48 dBm.

The findings indicate, that despite the long 0.8 μm channel lengths used, broadband operation has been achieved. Partly this was possible through the use of integrated coils, which double the

mixer bandwidths without adding to the power dissipation or noise. The resulting output power variation is quite small, as it stays within 8 dB over the two-octave output frequency variation of 0.75-3.6 GHz.

7.3 The realized 0.13 μm CMOS quadrature modulator

This modulator circuit was built to test a switchable parallel quadrature generator and the extension of its use to microwave frequencies. The schematic of the realized IQ modulator in Fig. 7.5 combines the LO balun, quadrature generator, mixer, and output buffer circuits from Sections 3.6, 4.6, 5.5, and 6.4.

7.3.1 Measurement setup

The IC was realized in a 0.13 μm CMOS-technology with standard low-resistivity substrate, and it has an active area of 0.8 mm $\times$ 0.5 mm, which is only a fraction of the total test chip area of 1.6 mm $\times$ 1.6 mm. These details, however, are practically indistinguishable from the micrograph in Fig. 7.6, as the chip surface displays a reflective mirror surface; this feature is attributable to the chemical mechanical polishing (CMP) which is used in modern CMOS processes to planarize multilevel metallizations and dielectric layers [103, 104].

As mentioned in Section 4.6, the 0.13 μm CMOS direct-conversion quadrature modulator was re-measured for this work using a re-wrapped test setup with much smaller bonding wire parasitics. Special attention was paid to the elimination of supply and ground inductances, as these limit the performance available from the LO buffering stage. From the IC micrograph in Fig. 7.6 it can be estimated that the realized V_{DD} and ground wire lengths are now ca. 0.6-0.9 mm, respectively. This estimate does not include wire curvature, but its effect on the realized wire lengths should be negligible with the short bonding distances used. Using a shared approximate for V_{DD} and ground wire lengths of 0.74 mm, and with 2 to 4 parallel wires, the realized supply and ground wire inductances should now be 0.37 and 0.19 nH, respectively. A previous attempt to produce such small parasitic inductances by connecting 5-6 bonding wires in parallel failed, since the resulting short 100 μm distances between, what were, at that time longer wires of ca. 1.5 mm gave rise to strong mutual inductance effects [105] that counteracted parallelization. Thus the new test setup moved the solder points closer to the IC and used fewer wires so as to keep sensitive interwire distances to a minimum of 300-400 μm.

Fig. 7.7 proves the effectiveness of the changes made to the test setup, since the measured LO-rej values are clearly better at any frequency higher than 1.4 GHz. Below 1.4 GHz the OLD, i.e. previous, measurement board seemingly performs better, but that can be explained by the higher signal amplitude previously used. At higher frequencies, however, the redesigned test setup was driven at comparable amplitudes, which makes the benefits of decreased bond wire inductances obvious. Of particular significance is the fact that the integrated LO buffer now works much better and improves signal balance at much higher frequencies. The improvement of ca. 10 dB shown in the NEW LO-rej values at 2.88 GHz marks the replacement of the off-chip coil-transmission line hybrid transformer with a bulky SMA-connected 2-4 GHz balun. Such SMA-connected baluns could not be used with the prior test setup because of the high bonding wire parasitics.

Noise measurements differ from other measurements, which were all made in an SSB configuration with BB signaling from a 14-bit IQ generator capable of 100 MS/s with two differential outputs. For the noise measurements the synthesizer was used to develop dc bias for the mixer BB inputs; only LO signaling was applied and the noise power densities (dBm/Hz) were measured using a spectrum analyzer. To properly separate device noise from the spectrum analyzer

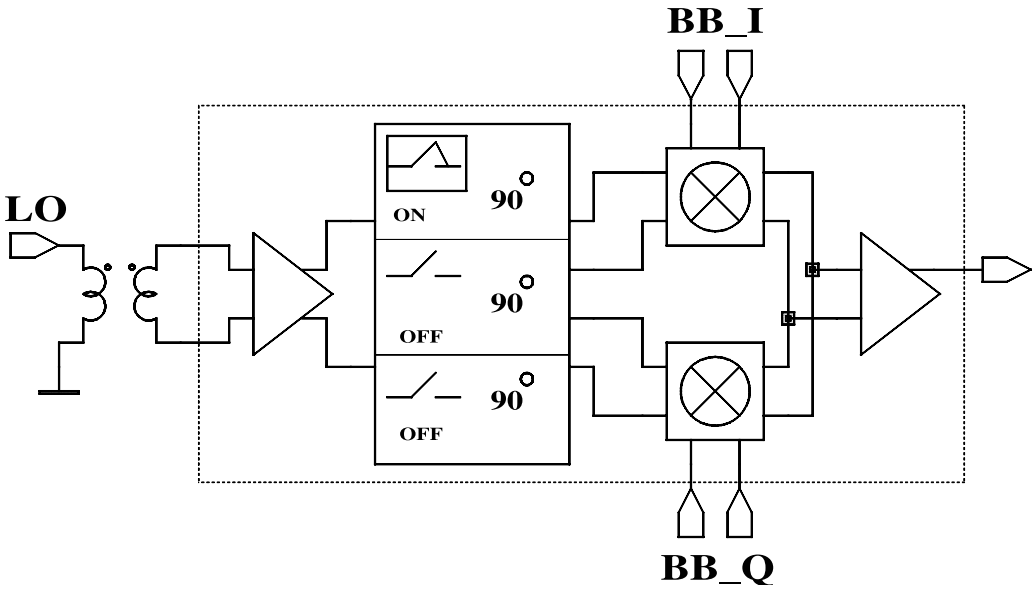


Figure 7.5: Block diagram of the 0.13 μm CMOS direct-conversion quadrature modulator.

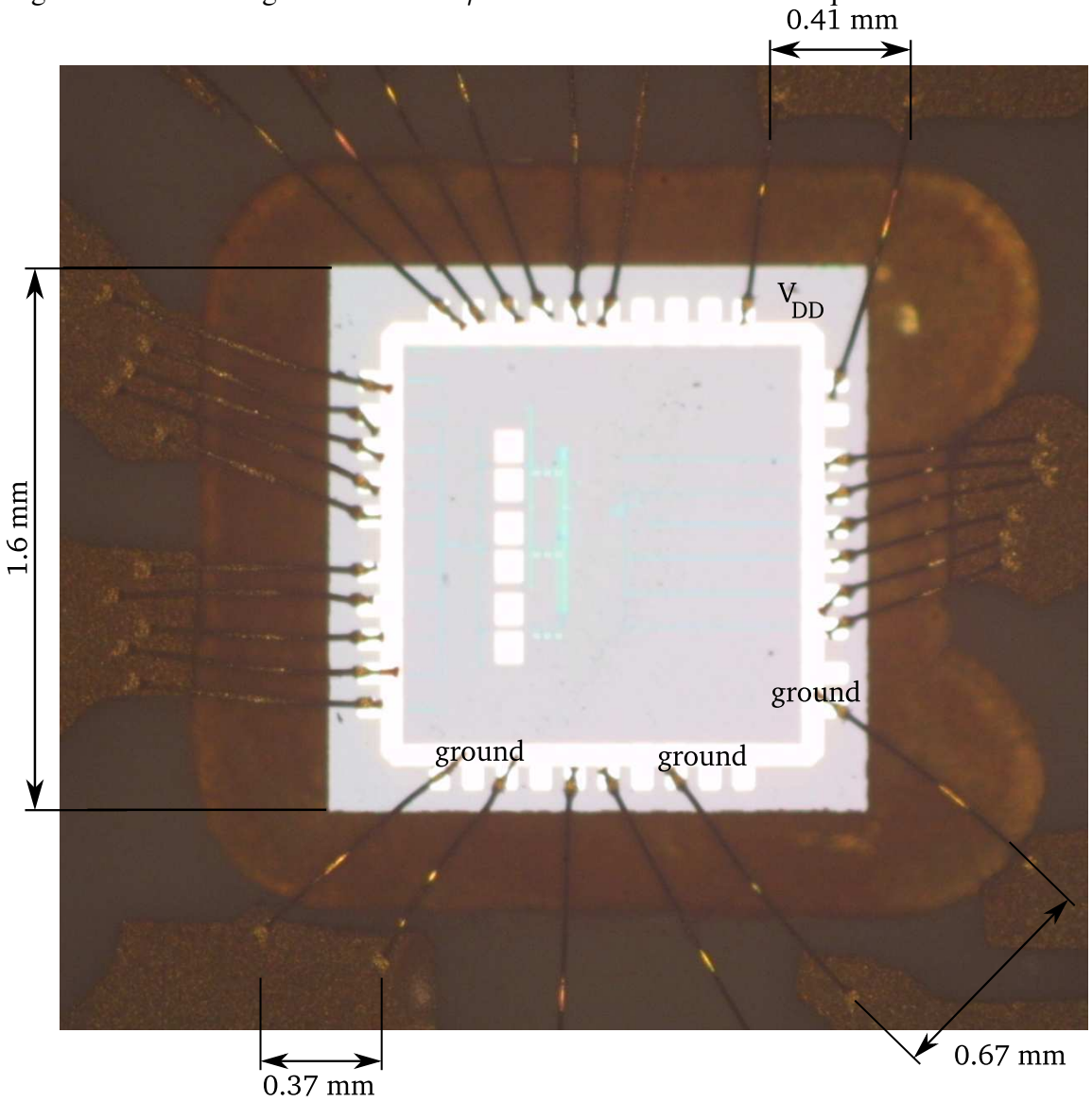


Figure 7.6: Micrograph showing the 0.13 μm CMOS IC wire-bonded to the measurement PCB.

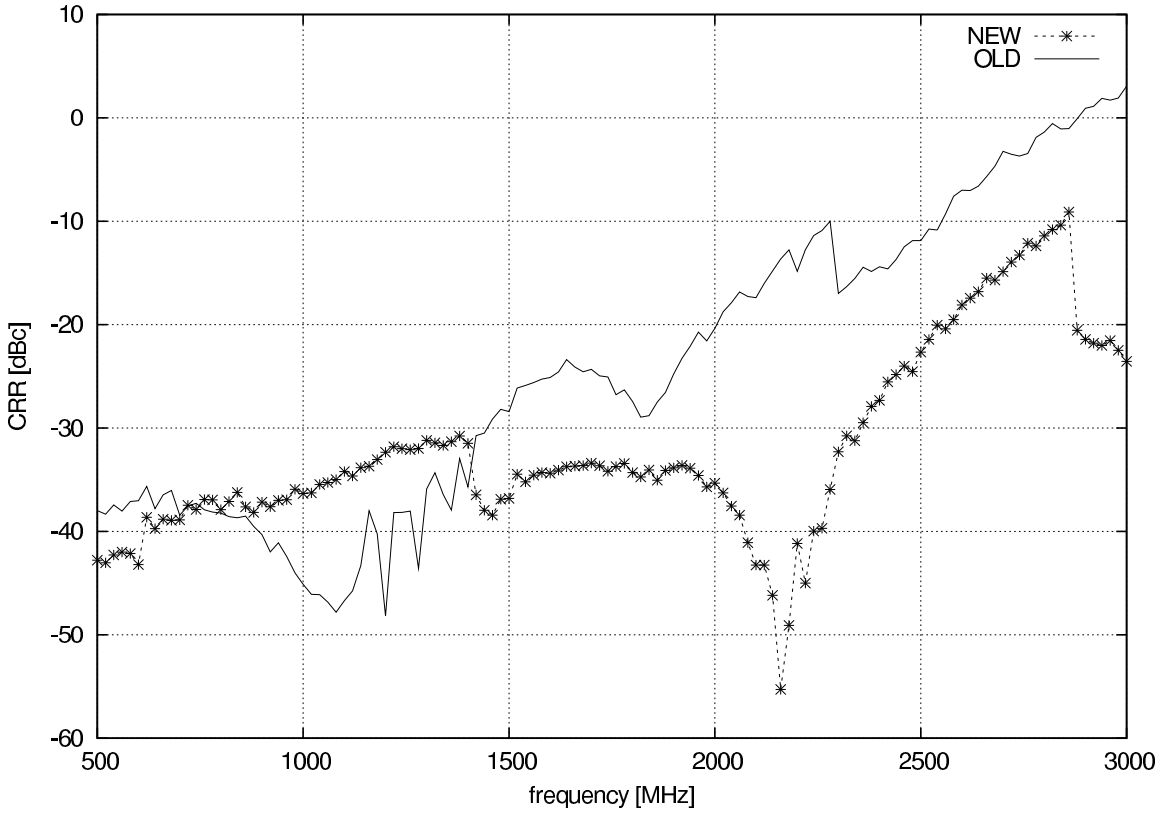


Figure 7.7: LO-rej values measured using the redesigned (NEW) and previously used (OLD) measurement setups.

noise floor, an off-chip LNA should be used to buffer device noise to the spectrum analyzer. With such a setup the output noise power is given by:

$$Ni = No - G - NF \tag{7.1}$$

where Ni stands for the noise at the LNA input, i.e. at the device-under-test (DUT) output, No is the measured noise, G is the LNA gain, and NF is its noise figure. All the terms are in dB as defined over the same bandwidth.

7.3.2 Experimental Results

To verify the switched polyphase quadrature generation technique, the output SSB spectra were measured using each of the three realized PP filters (I/II/III). The measured spectra were recorded in 20 MHz steps with a preset quiescent point, and no post-tuning or calibration was applied. The resulting output, image, and 3^{RD} harmonic powers are shown in Fig. 7.8. The depicted image values correspond to an IRR performance better than -37 dBc in 0.56-4.76 GHz, while in popular wireless application frequency bands (0.8-1, 1.8-2, and 2.4 GHz) substantially better IRR performance was measured at -46, -41, and -49 dBc, respectively. A low -6 dBm LO signal was used for all measurements, whereas BB signaling amplitude was increased from 150 $\mathrm{mv_{RMS}}$ (I) to 300 $\mathrm{mv_{RMS}}$ (III) to partly equalize circuit output power over the operating range. In Fig. 7.9 a measured spectrum at LO=1960 MHz is shown to complement the given frequency sweep plots in Fig. 7.7, and Fig. 7.8. The spurious ripples at $\pm 7\mathrm{MHz}$ offset from the carrier can be attributed to the BB IQ synthesizer.

Quiescent points and signaling for three popular wireless application frequencies, together with measured characteristics, are collected in Table 7.2. As can be seen from the given $\mathrm{P_{OUT}}$

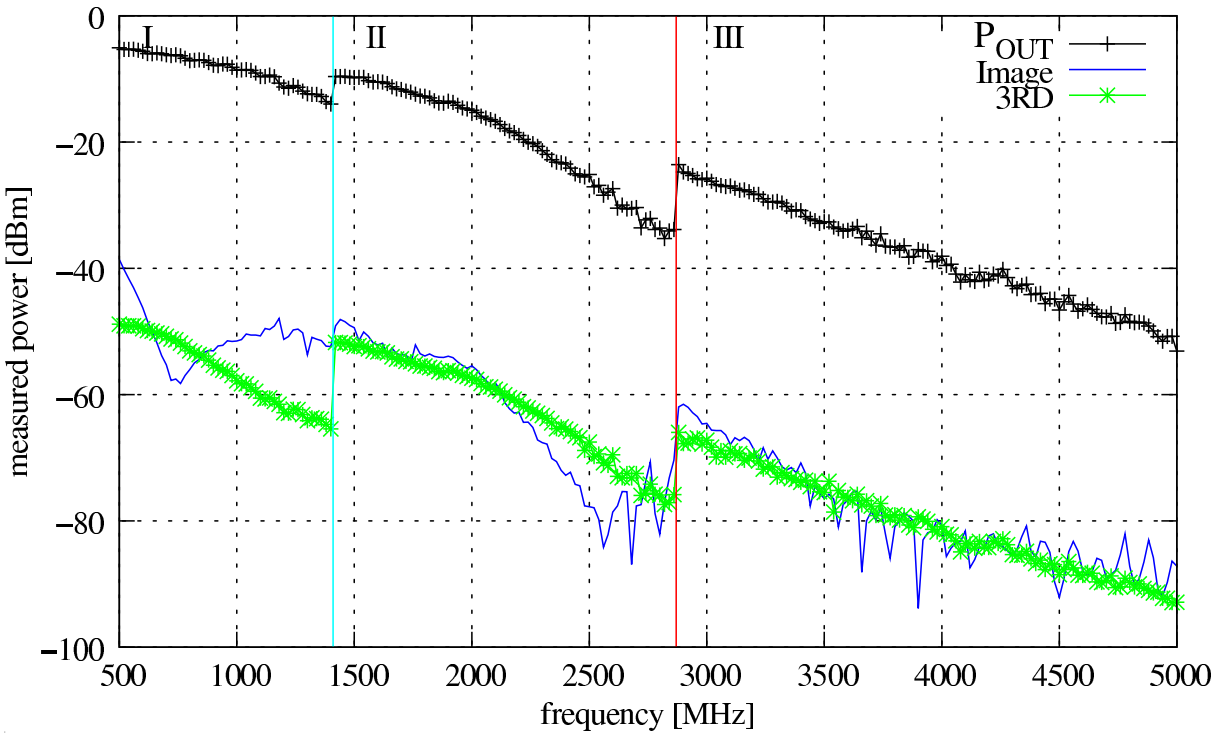


Figure 7.8: Measured output, image, and 3RD spurious powers.

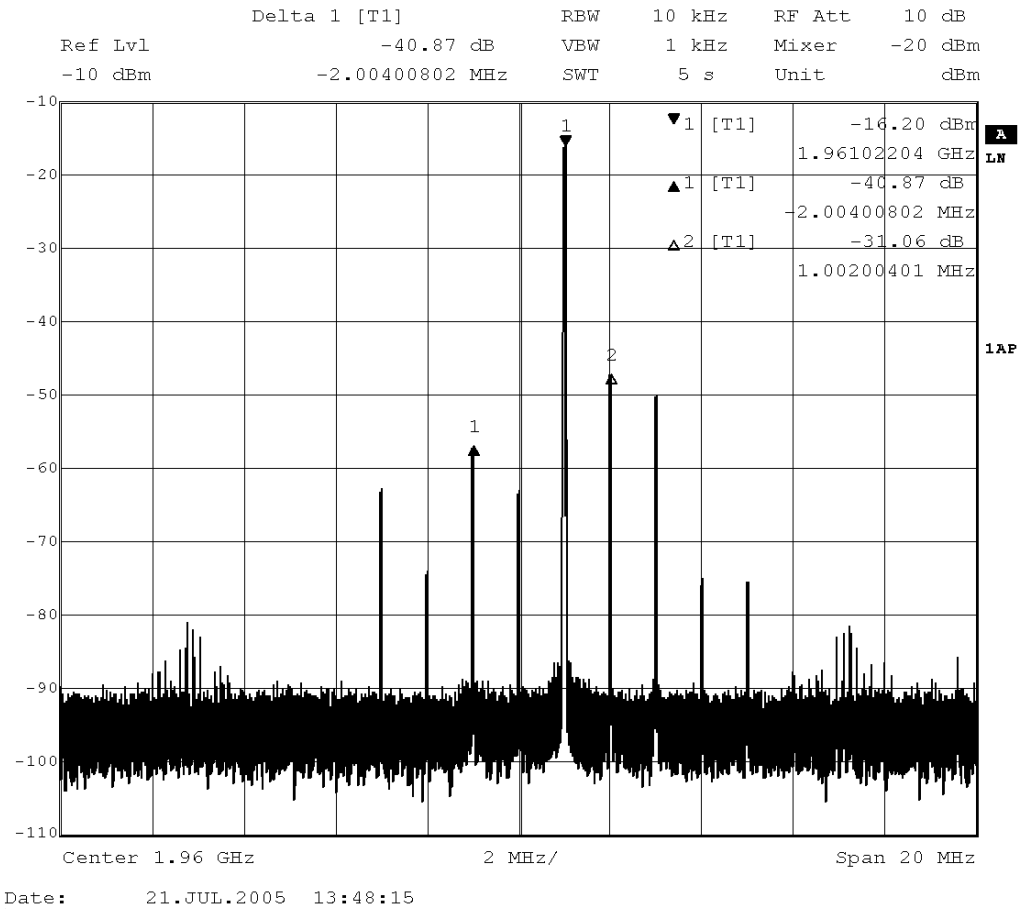


Figure 7.9: Measured SSB spectrum at LO=1.96 GHz.

Table 7.2: Measured results at LO frequencies: 884 MHz, 1960 MHz, and 2400 MHz.

		I @0.884	**II** @1.96	**III** @2.4
P_{OUT}	[dBm]	-7	-15	-23
IRR	[dBc]	-46	-41	-49
LO-rej	[dBc]	-38	-35	-27
3RD-rej	[dBc]	-45	-31	-30
2ND-rej	[dBc]	-41	-29	-27
OP_{1dB}	[dBm]	-9	-15	-22
OIP_3	[dBm]	-2	-5	-13
S_{22}	[dB]	-7	-4	-5
S_{11}	[dB]	-14	-14	-7
N_{+20MHz}	[dBm/Hz]	-139	-150	-156
$N_{+190MHz}$	[dBm/Hz]	-148	-155	-158
LO	[dBm]		-6	
BB@1MHz	[V_{RMS}]	0.15	0.25	0.3
I_{DD}	[mA]		29	
V_{DD}	[V]		2.2	

and OP_{1dB} values, the characteristics were measured with the modulator circuit in saturation. Reason for this error is the fact that OP_{1dB} values were calculated after the data had been measured, and the situation was discovered at that point. Individual spectra were were not rich enough in harmonics to give a warning of the situation during measurements. However, as measurements of typical performance should be made with at least a 3 dB backup from the circuit OP_{1dB}, an additional set of measurements will be taken later. A re-comparison of the measured spectrum in Fig. 7.9 to the tabulated 1960 MHz data suggests that a power backoff might yield improved spurious rejection results, since the spectrum was taken at a -2 dB lower input signal amplitude than the tabulated results. As it is, the extracted data are still adequate to demonstrate the switchable parallel polyphase filtering.

The tabulated LO frequencies at 884 MHz, 1.96 GHz, and 2.4 GHz represent the GSM, UMTS, and WLAN standard frequencies, respectively, and all the measurement data given include cabling and SMA connector losses at approximately 1-2 dB per RF connection. A comparison of the recorded N_{floor} values with the given output return losses S_{22} indicates that the noise results include a mismatch-induced uncertainty, which is realized if the test LNA is not able to produce its nominal measured performance. This error source has been deemed negligible, since an off-chip instrumentation LNA was used. However, to start to correct the situation, the number of bonding wires used at the circuit output should be optimized, and possibly verified with an electro-magnetic simulator.

7.4 Benchmark

Measurement results for the broadband quadrature modulators in Table 2.1 are collected in Table 7.3 and in Table 7.4. The data have been made as comparable as possible, but in judg-

Table 7.3: Comparison of broadband direct-conversion quadrature modulators published in 2005-2001.

		[10]	[16]$^{\mathrm{ThisWork}}$	[40]	[18]$^{\mathrm{ThisWork}}$	[41]
P_{OUT}	[dBm]	-10	-15	-3	-19	-5
IRR	[dBc]	-39	-41	-34	-40	-28
LO-leakage	[dBm]	-60	-35	-34	-44	-33
spurious	[dBc]	NA	-29	NA	-30	NA
LO-range	[GHz]	0.1-2.6	0.56-4.76 GHz	0.7-2.7	0.75-3.6	0.8-2.7
LO-power	[dBm]	NA	-6	0	-14.5	-2
I_{DD}	[mA]	50	29	122	46	65
V_{DD}	[V]	1.2	2.2	5	2.5	2.7-5.5
Technology		0.13μm CMOS	0.13μm CMOS	SiGe f_T=50GHz	0.8μm SiGe f_T=37GHz	Si-BJT
IC size	[mm $\times$ mm]	0.7	0.8$\times$0.5	NA	2.2$\times$1.3	NA
IQ		div-by-2	swtchd PP	3-stg. PP	5-stg. PP	2xPP
XFMR		LO/OUT	LO	LO/OUT	–	LO
published		2005	2004	2004	2003	2001

Table 7.4: Comparison of broadband direct-conversion quadrature modulators published in 1998-1993.

		[42]	[43]	[44]	[45]	[46]
P_{OUT}	[dBm]	-10	-6	-22	-18	-25
IRR	[dBc]	-35	-60@884MHz	-35	-30	-40
LO-leakage	[dBm]	-45	NA	-40	-32dBc	-40
spurious	[dBc]	-32	-40	-40	NA	-40
LO-range	[GHz]	0.6-3.0	0.25-4.0	0.8-2.0	1.2-2.3	0.7-3.0
LO-power	[dBm]	+6	NA	0	-15	NA
I_{DD}	[mA]	58	250	34	37	75
V_{DD}	[V]	1.5	-6	2	2.7	8
Technology		0.25μm CMOS	0.4μm GaAs			
f_T=26GHz	Si-BJT f_T=18GHz	Si-BJT f_T=15GHz	0.5μm GaAs			
IC size	[mm×mm]	2	1.6×1.1	2.4×0.68	2.49×2.14	2.2×2.4
LO IQ		3-stg. PP	RC-CR	tuned RC-CR	RC-CR+limitters	tuned RC-CR
XFMR		LO	OUT	LO/OUT	LO/OUT	–
published		1998	1997	1996	1996	1993

ing spurious performance it is a good practice to compare the given output powers in such a way that typically a 1 dB increase in P_{OUT} gives a 3 dB increase in 3RD-order distortion. Except for IRR performance, the data given for [40] are really only valid for the UMTS downlink range, and the spurious performance reported for [18] represents circuit 3RD-rej performance. The TDR reported for [40] is unparalleled at 161 dB, with equally unparalleled I_{DD}=122 mA, and yet the broadband approach in [41] can almost match this with a TDR of 157 dB.

The SiGe prototype realized for this work achieves a very good IRR performance of better than -40 dBc over two octaves, whereas its P_{OUT} stays within 8 dB despite the rather long minimum channel lengths of 0.8 μm in the process used. No tuning or post-fabrication calibration have been applied as the reported broadband performance was verified by sweeping the LO source at set, small steps of 25 or 50 MHz. Of particular importance is the fact that the required single-ended-to-differential and differential-to-single-ended conversions for LO and output signals, respectively, are done on-chip with integrated baluns, and no expensive off-chip discretes are needed.

As for [40], the data given for the realized CMOS prototype [16] are given for the UMTS downlink range, with the exception of IRR. This has been done, as P_{OUT} deteriorates faster than what its expected single-pole response would do. There are several reasons for this, and a new test IC should be made to correct this deficiency. However, even as it is, the prototype results indicate that the proposed concept of parallel switchable PP filters is a working one: IRR=-37 dBc in 0.56-4.76 GHz was measured using all three of the realized selectable PP filters to an advantage.

8. Conclusions

The direct-conversion quadrature modulator is the transmitter type most amenable to complete integration; it is conceptually simple and it can be used for both constant and variable envelope modulations. Its use as a linear transmitter for variable envelope modulations is quite challenging, however, and as a response to these challenges different alternative transmitters, such as polar radio, have recently started to emerge. Nevertheless, as the best currently commercially available IQ modulators output a DR of +167 dB at lower microwave frequencies, it is not at all clear whether a universal replacement for the quadrature modulator will be available in the near future. Additionally, as many of the papers on emerging radios list an IQ modulator sub-block, its careful analysis is well justified.

This work has evolved as a response to such questions. A thorough theoretical analysis of quadrature modulator operation has been done, and as a result of this work a previously defined linear direct-conversion quadrature modulator model has been extended to include nonlinearities up to third-order. Analysis of this model using sinusoidal excitations has yielded results which have implications on control circuit design, definition of the available DR, and EVM. The developed model indicates clearly the significance of each non-ideality, as the individually named coefficients make it possible to trace this information. To make this part of the work more concrete, model coefficients were specified for an IRR=-40 dBc IQ modulator example, and the developed expressions for characteristics such as SSB performance, $\mathrm{OP}_{1\mathrm{dB}}$, and transmitted DR were evaluated with these. Later error-vector-magnitude analysis with the developed model established a lower bound which does not depend on distortion-related phenomena, in this otherwise system nonlinearity dependend characteristic.

The theoretical proof of the well-known property of improving signal balance that cascaded differential pairs exhibit was done only to satisfy the need to formalize things as practical design experience supported this well-known property of such devices but theory on it was found lacking. As a practical result one of the most accurate integrated baluns ever published operating up to 3.7 GHz was designed during this phase of the work. However, later implementation in CMOS revealed that such balun techniques are strongly dependent on bonding wire parasitics, and that their effect on LO phase noise performance needs to be carefully evaluated. Withal, the developed SiGe balun was the key component in the realization of a completely integrated IQ modulator in a 0.8 μm SiGe technology, which has a measured IRR performance better than -40 dBc in 0.75-3.6 GHz, without tuning ciruitry or post-fabrication calibration. This is so far a best published broadband result for such a device, but other characteristics such as output power would need further work to boost the significance of the result.

Operation without tuning circuitry in support of the software defined radio idea has been one of the goals of this work, and the first-ever realization of parallel switchable polyphase filters for microwave quadrature generation was designed in that spirit. During this thesis, the proposed switchable quadrature generator has been shown to be a functioning technique with reported IRR performance at or better than -37 dBc in 0.56-4.76 GHz. Comparison to existing brodband quadrature generation techniques has produced an improved div-by-2 topology, which could be

used to an advantage in low-voltage conditions. However, no recommendation can be made on its behalf as the div-by-2 circuit was not implemented and needs experimental work.

Finally, a complementary mixer has been shown to yield a +3 dB improvement in TDR when it is compared to a similarly biased conventional prototype. The extension of the compound emitter-follower, or the bipolar push-pull stage, to microwave frequencies has been shown to be possible with proven thermal stability, and with improved harmonics suppression as compared to a similarly biased emitter-follower.

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