PUBLICATION B

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Wafer Scale Packaging of MEMS by Using Plasma-Activated Wafer Bonding

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Plasma-assisted direct bonding has been investigated for wafer scale encapsulation of microelectromechanical systems (MEMS). Direct bonding requires smooth and flat wafer surfaces, which is seldom the case after fabrication of MEMS devices. Therefore, we have used polished chemical vapor deposited oxide as an intermediate bonding layer. The oxide layer is polished prior to bonding the MEMS wafer to cap silicon wafer. The bonding is carried out with plasma-assisted direct wafer bonding at a low temperature ($<300°C$). Two different methods to form electrical contacts to the encapsulated device are presented. In the first method trenches are etched on the surface of the cap wafer before the bonding. During the bonding the trenches are aligned to the contact pads of the device wafer. After bonding the cap wafer is thinned down with grinding until the path to the contact pads is opened. In the second method one or both of the wafers are thinned down to around 100 μm after bonding. The electrical path to contact pads is formed using V-groove sawing, metal sputtering, and lithography. To test the viability of the developed methods for MEMS encapsulation, we have sealed polysilicon resonator structures at a wafer level.
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The wafer scale packaging process is needed for several reasons in microelectromechanical (MEMS) applications. The packaging cost for MEMS may contribute up to 90% of the total device costs. Wafer scale packaging reduces these costs significantly and may also result in system miniaturization. Moreover, microsystems often contain delicate surface structures which have to be protected from the outside world. Sensor surfaces can be sensitive to particles and chemical contaminants. MEMS devices may also need vacuum or controlled atmosphere for their operation. Typical packaging and assembly tools (such as dicing, solder flux, pick, and place) are not usually compatible with delicate mechanical structures. One way to seal the devices at a wafer level is to bond another wafer to the MEMS wafer. The encapsulation of the devices can take place right after the micromechanical structures are released inside the clean room. The encapsulated (0-level packaged) MEMS wafer can be handled more or less like a normal integrated circuit (IC) wafer.

Various methods for 0-level wafer scale packaging of devices have been reported. Glass frit sealing and anodic bonding are probably the most common methods in 0-level packaging. Both of these methods, however, require relatively high temperatures (400–600°C) and also the required bonding rim around the active device blows up chip size dramatically. This is particularly pronounced in the cases where the chip size is small. Glass frit sealing and anodic bonding involve harmful metals (Pb, Na) that hinder their use in many applications requiring complementary metal-oxide semiconductor (CMOS) compatibility. Agilent uses gold seal bonding to encapsulate their film bulk acoustic resonator (FBAR) devices.[1] Covalent bonding of wafers has also been reported as a wafer scale packaging method.[2]

We have studied the wafer scale packaging of MEMS devices by using a plasma-activation-based, low-temperature direct bonding process.[3] In this method a silicon wafer and an oxidized silicon wafer are exposed to short plasma treatment. Then the wafer surfaces are brought into contact and annealed at 100–300°C. Plasma-assisted bonding has the benefits of low process temperature, inherent cleanliness, high throughput, and also the bonding areas can be small. The main drawback of the method is that in order to achieve good bonding the surfaces have to be very flat and smooth (surface microroughness less than 0.5 nm.). Therefore, we have studied different planarization processes as well as ways to protect the surfaces during subsequent process steps. We also investigated two different methods for forming electrical contacts into the package. To test the feasibility of the developed methods for MEMS packaging, we have encapsulated simple polysilicon resonators.

Experimental

In our experiments 100-mm p-type silicon wafers were used. In the first experiments different conductive paths and pads were fabricated to thermally oxidized device wafers. The conductive layer was made by deposition of molybdenum (sputtering) or in situ boron-doped polysilicon (low-pressure chemical vapor deposition, LPCVD) and subsequent patterning of the conductive layer with standard lithography. The conductive layer was then covered with thick (2-μm) LPCVD-oxide (low-temperature oxide, LTO). The surface steps caused by buried conductive paths were planarized with chemical-mechanical polishing (CMP, Strasbaugh 6DS-SP). For this step special fixed abrasive pads were used. In these pads the abrasive material is fixed into the pad and pH-adjusted water is used to increase the removal rate. A second CMP step was used to smoothen the oxide surface to a level required for fusion bonding. For this conventional oxide final polishing pads and slurry were used.

On some capping wafers we fabricated deep trenches for contact opening. In these cases both sides of the cap wafers were patterned with standard lithography by using Süss mask aligner MA6. Backside alignment marks were needed for aligned bonding. Deep silicon etching was done in a Surface Technology System (STS) inductively coupled plasma chamber (ICP) by using an oxide mask.

The wafers were plasma activated in an STS ICP chamber with 30 s argon plasma treatment. Then the wafer pairs were bonded in Süss MA/BA6 bond aligner. Bonded wafer pairs were heat-treated at 200°C for 2 h to strengthen the bonding. Bond strength was measured from some wafers by using a crack opening method.[4] The thinning of the wafer stack was done with a Strasbaugh 7AF grinding tool. Grinding was also used for contact opening when cap wafers with deeply etched trenches were used. LTO was removed from contact pad surfaces with short hydrofluoric acid (HF) dip. After this the resistance of the buried conductive layer was measured. The above-described process flow is depicted in Fig. 1.

Another way to make the electrical contacts was to saw V-grooves to either one of the wafers. For sawing we used a Loadpoint dicing saw. In these cases molybdenum was sputtered to the sawed grooves to establish electrical contacts with the contact pads. For sputtering we used a Von Ardenne sputter system. This second contact opening process is shown in Fig. 2.

To analyze the surface profile we used Veeco Dektak V200 surface profilometer. Surface roughnesses were measured with a Digital Instruments D3100 atomic force microscope (AFM). The bonding quality and bond alignment accuracy were measured with Sonix

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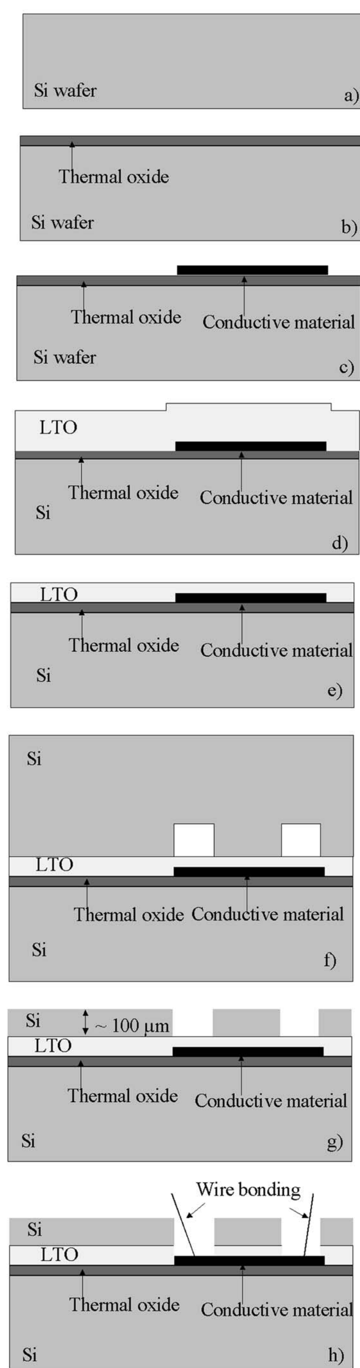

Figure 1. Process flow for buried conductive pads and wires when grinding is used for contact opening: (a) start device silicon wafer, (b) thermal oxidation of the device wafer, (c) deposition and patterning of conductive material (doped polysilicon or molybdenum) on device wafer surface, (d) covering of conductive material with thick LPCVD-oxide layer, (e) oxide surface planarization and smoothening with CMP, (f) aligned bonding of patterned cap wafer to the device wafer, (g) cap wafer thinning and contact hole opening with grinding, and (h) etching of oxide from contact holes and probing or wire bonding.

UHR2000 scanning acoustic microscope (SAM). Scanning electron microscopy (SEM) was used for closer examination of packages from cross-sectional samples.

To test all these process steps in one process flow we fabricated a simple polysilicon resonator and encapsulated it.

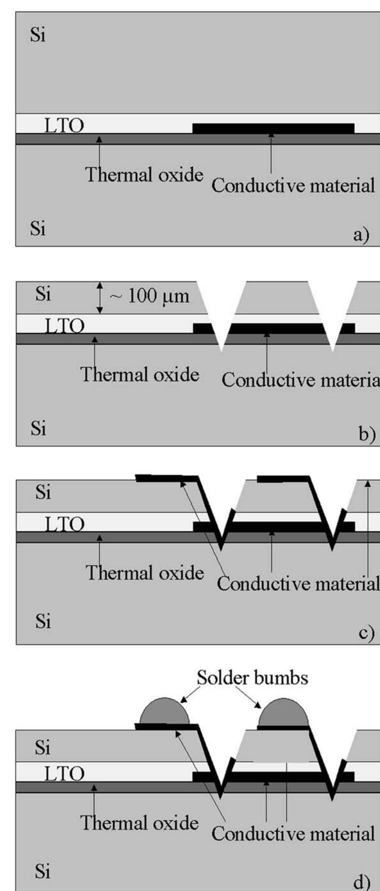

Figure 2. Contact opening by sawing: (a) the device wafer is bonded to the cap wafer, (b) grinding down one of the wafers and sawing of V-grooves, (c) deposition and patterning of molybdenum layer, and (d) growth of solder bumbs.

Results and Discussion

Bonding of LPCVD-oxide differs from bonding of thermal oxide. LPCVD-oxide has to be polished and usually outgassing will take place if bond annealing exceeds oxide growth temperature. The outgassing can be avoided by either using high-temperature annealing prior to bonding or by using a low-temperature bonding process. High-temperature annealing is not usually an acceptable process step because of temperature-sensitive materials or devices on the wafer. Therefore, we have used plasma-activation-based, low-temperature bonding in our process.[3] Figure 3 shows the measured

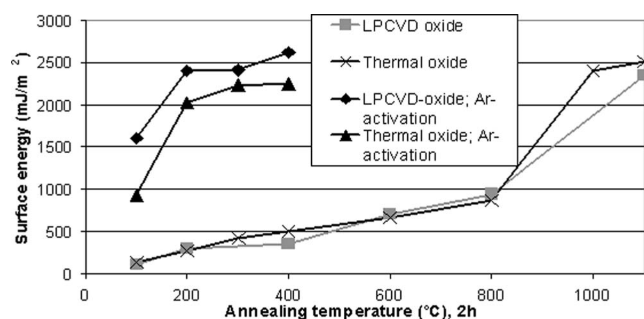

Figure 3. Measured surface energies for thermal oxide to Si and for LPCVD-oxide to Si wafer pairs bonded with and without plasma activation. Bond annealing time was 2 h.

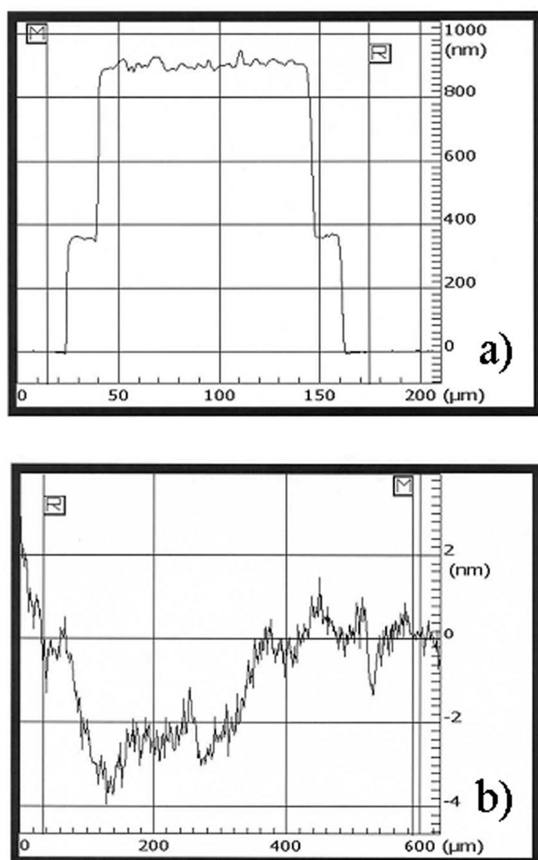

Figure 4. Measured surface profile of the resonator wafer (a) before and (b) after the planarization.

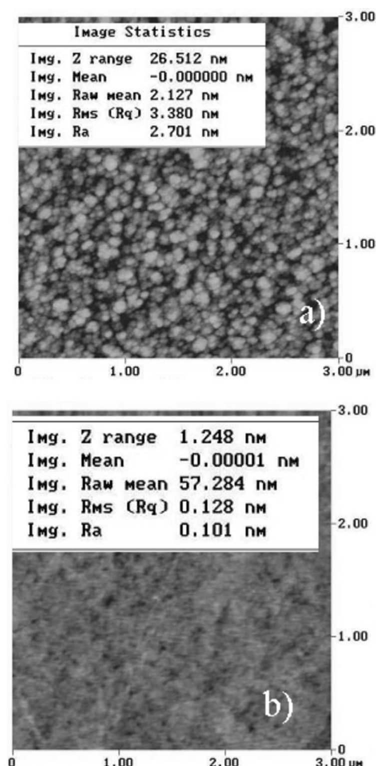

Figure 5. AFM image of resonator wafer (a) before and (b) after CMP steps.

surface energies for low-temperature and high-temperature-bonded LPCVD-oxide and for thermal oxide.

The first tests had patterned conductive layers on top of thermal oxide on the device wafer. When the conductive layers were covered with LPCVD-oxide (LTO), the buried material caused surface steps to the oxide. These steps had to be removed with planarization. Figure 4 shows the profile of the oxide layer on top of buried structure (a) before and (b) after CMP. Before CMP the surface step height was 800–1000 nm. After CMP the step could not be observed with surface profilometry. The total removal needed to planarize 800-nm-thick oxide hills was less than 1000 nm, indicating good planarization capability of our CMP process. Typically oxide planarization processes need removal of oxide layer at least twice the hill height.[5,6] After the first CMP step the surface roughness [root-mean-square (rms)] was reduced from as-grown value of 3.38 nm (Fig. 5a) to 0.273 nm. During the second CMP step, the surface roughness (rms) reduced to 0.128 nm (Fig. 5b).

After the planarization the device wafers were bonded to the cap wafers with trenches using a plasma-assisted bonding process. The bonding was spontaneous and no voids could be observed after annealing of the wafer pairs at 100–300°C (Fig. 6). In Fig. 6 the dark areas represent buried conductive material and white areas trenches on the cap wafer.

We also tested the possibility of removing first the surface steps by lithography and buffered hydrofluoric acid (BHF) etching and then carrying out the polishing process. The problem with this process is usually rounding of the corners of oxide walls or pillars (Fig. 7a and b) during the polishing process. By adjusting the polishing force and slurry flow the rounding effect decreased but could still be noticed (Fig. 7c). However, we managed to develop a CMP process so that even small pillars (~ 50 µm) could be polished without significant edge rounding effect (Fig. 7d) by using fixed abrasive pads. The surface roughness on top of the pillars was reduced from about 3 nm to below 0.3 nm. Figure 8 shows the bonding result of a 200-µm-wide LPCVD-oxide wall pattern bonded to a blank silicon wafer. The polished oxide rim area around the cavities is well bonded and void-free.

We used two different approaches for making the electrical contact to the contact pads between the wafers. The first one was to have deep etched wells on the cap wafer, which were aligned to pad positions during bonding (Fig. 6). When the cap wafer was ground down an access to the contact pad was formed. The electrical probing proved that the electricity flowed well through the buried conductive layer from pad to pad. With large pads and small final cap wafer thickness the final connection can be made with wire bonding, for example. The process is shown in Fig. 1.

Another studied approach for contact formation was to use sawing for contact opening. We used a dicing blade for cutting a

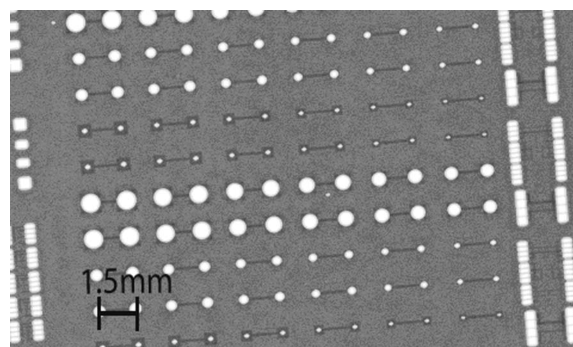

Figure 6. SAM image of wafer with buried conductive structures bonded to a patterned cap wafer. Conductive material is seen in the image as dark areas and cavities are seen as white areas.

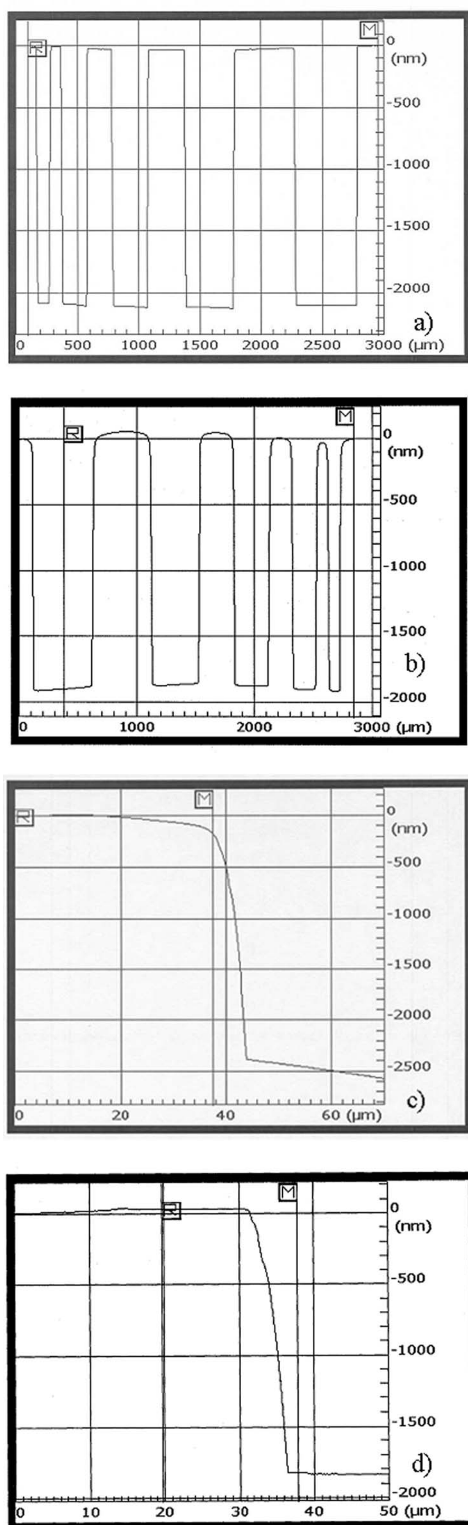

Figure 7. Surface profiles of LPCVD-oxide pillars (a) before CMP, (b) after normal oxide polishing process, (c) after modified oxide polishing (low-force, high-slurry flow), and (d) after the special CMP process.

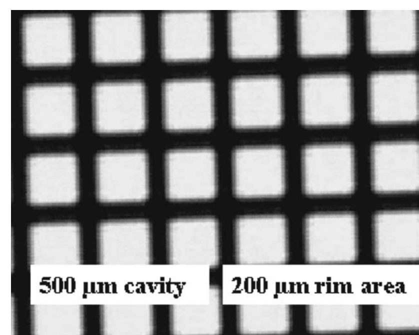

Figure 8. A SAM image of patterned and polished LPCVD oxide bonded to blank silicon wafer.

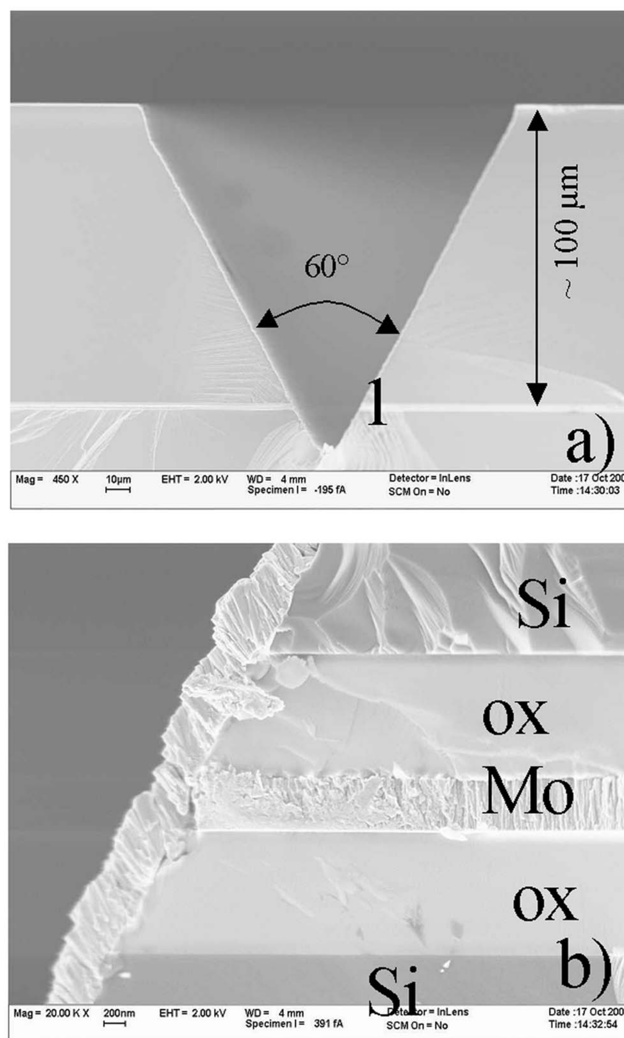

Figure 9. (a) SEM image of a V-groove sawed to the cap wafer. The groove goes about 20 µm into the device wafer. (b) Close-up from point 1 in Fig. 8a. Molybdenum in the V-groove is in contact with molybdenum between the oxide layers.

V-groove through the cap wafer and contact pads (Fig. 9a). The V-groove can also be made from the device wafer side. After sawing a molybdenum layer was sputtered onto the V-grooved surface. The molybdenum made an electrical contact with the buried conductor

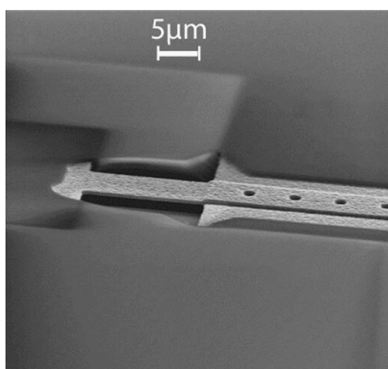

Figure 10. SEM image of released polysilicon resonator.

material, enabling a buried lateral electrical path to be formed (Fig. 9b). Then the molybdenum was patterned so that the only path between the two pads was a line going inside the bonded wafer stack. We found out that the molybdenum can be patterned even inside the groove with standard lithography, if a thick resist mask is used and if the groove is kept relatively shallow (<150 μm). Therefore, it is recommended that the wafer where the grooves are to be placed is thinned before sawing. Afterward the molybdenum is patterned to desired shapes, e.g., solder bumbs can be fabricated on it and used to connect the protected component to the next level package. This process is depicted in Fig. 2. The problem with groove-sawing a contact opening is that first the components and the contact pads have to be placed in the wafer so that sawing of one groove cuts through several pads but does not harm devices or cut-off the connector lines. Both silicon wafers should be high-resistivity wafers to avoid short cutting via Si. Good things with this process are that the cap wafer do not have to be deep-etched on contact pad areas (less lithography and etching, more bonded area) and contacts can be made to either the handle or the cap wafer. Sawing is a cost-effective process compared to, e.g., dry etching, if the pads can be placed in rows.

When probing the electrical properties of these two types of connections, both had resistivity of the same order of magnitude. However, with the sawing process there was sometimes a problem with oxidation of buried molybdenum, which increased the contact resistance between buried Mo and Mo in V-groove significantly. This problem was removed by using short HF-dip and sputtering etching before sputtering Mo to the V-groove. Further investigations are on their way to measure the exact values of resistivity and to test the repeatability of our processes.

One problem with our wafer scale packaging process is that the surfaces to be bonded have to remain really smooth, even though it is sometimes necessary to do several processing steps after the final

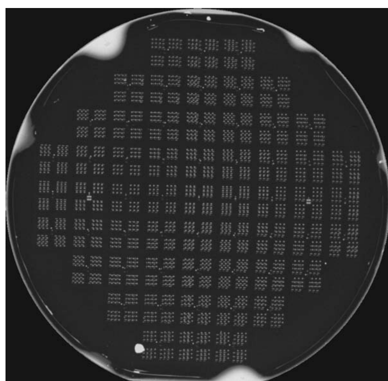

Figure 11. An SAM image of encapsulated resonators.

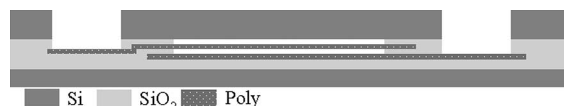

Figure 12. Schematic image of the encapsulated resonator.

polishing steps. Therefore, we tested different materials as protective layers for areas to be bonded. The best result was obtained by using sputtered molybdenum as a protective layer. This layer was resistant to HF during oxide patterning and was later on easily removed with mild SC-1 cleaning (H_2O_2:NH_3:H_2O). The surface roughness of the protected areas remained the same as before processing. If buffered hydrofluoric acid (BHF) is used for oxide etching, a good protective layer is standard photoresist.

Both protective layers were tested on resonator packaging. A simple polysilicon resonator was covered with LPCVD-oxide. After oxide planarization and smoothening the areas to be bonded were protected with molybdenum or photoresist, depending on if HF or BHF was used for release etching. The critical step after release etching is drying. If normal drying is used the resonator structures break or stick due to surface tension of the liquids. Therefore we used supercritical carbon dioxide drying. An SEM image of a released resonator is presented in Fig. 10. After the release etching the protective layer was removed and the device wafer and the cap wafer were plasma activated and bonded together. An SAM image of a bonded wafer pair is presented in Fig. 11. The bonding result was good, although wafer pairs had some voids due to particles. The cap wafer was subsequently thinned down to open the contacts to resonator pads. A schematic image of the final package is shown in Fig. 12. The resonator properties were not optimized, because the goal was just to test the packaging concept with an actual device structure.

Conclusions

In our experiments we have shown that plasma-assisted direct bonding is a usable method for wafer scale MEMS packaging, if care is taken in surface preparation and protection. Covering of the device with LPCVD oxide and using it as an intermediate bonding layer was found to be a viable method for encapsulation. By using a special CMP polishing process, surface steps can be removed and surface roughness reduces to a level required for fusion bonding. If device fabrication steps are needed after CMP, the roughening of the surface has to be prevented with a protective layer.

We have also tested two different methods to fabricate electrical contacts to the package. Both methods, opening of pre-etched trenches on the cap wafer by grinding as well as a V-groove sawing method, facilitated an electrical path from the encapsulated device to the outside world.

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References

1. F. Geefay, U.S. Pat. 6,836,013 (2004).
2. G. Fountain, Q.-Y. Tong, P. Enquist, and R. Markunas, U.S. Pat. 6,822,326 (2004).
3. T. Suni, K. Henttinen, I. Suni, and J. Mäkinen, *J. Electrochem. Soc.*, **149**, G348 (2002).
4. Q.-Y. Tong and U. Gösele, *Semiconductor Wafer Bonding*, p. 25, John Wiley & Sons, New York (1999).
5. D. C. Hermes, T. Heuser, E. J. van der Wouden, J. G. E. Gardeniers, and A. van den Berg, *Workshop on Wafer Bonding for MEMS Technologies*, Book of Abstracts, pp. 37-38, Halle, Germany (2004).
6. C. Jia and M. Wiemer, *Presentation at Workshop on Wafer Bonding for MEMS Technologies*, Oct 11, 2005, Halle, Germany.