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Journal of The Electrochemical Society, Vol. 153, No. 4, (2006), pp. G299–G303.
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Journal of The Electrochemical Society, **153** (4) G299-G303 (2006)
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Silicon-on-Insulator Wafers with Buried Cavities

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Direct bonding and mechanical thinning of pre-etched silicon wafers have been studied for the fabrication of silicon-on-insulator (SOI) wafers with buried cavities. The thin Si diaphragm over the cavity is deflected downward during the grinding and polishing, as the thinning is carried out without supporting the diaphragm. The deflection causes thickness variation for the Si diaphragm that can also be observed as a hill on the wafer surface after thinning. The results show that the thickness variation of the Si diaphragm increases with increasing cavity size and with decreasing SOI layer thickness. After grinding the measured hill height was about 1.5 μm for a 20-μm-thick Si diaphragm over a 1 × 1 mm cavity. The hill height was reduced to less than 0.5 μm when a small supporting column was placed under the diaphragm. With polishing the hill height was further reduced to <0.1 μm. It appears that mechanical thinning of the bonded wafers with pre-etched cavities is a viable method for various applications.
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Manuscript submitted June 22, 2005; revised manuscript received November 11, 2005. Available electronically February 22, 2006.

In silicon microelectromechanical system (MEMS) technology the prominent techniques currently in use are bulk and surface micromachining. Silicon-on-insulator (SOI) MEMS is a complementary micromachining technology which has several advantages over bulk and surface micromechanics. Nevertheless, it also has some limitations, such as the gap between the released mechanical structure and the substrate cannot be freely adjusted but is limited to the thickness of the buried thermal oxide used as a sacrificial layer. The need for protection of the metal layers during hydrofluoric acid (HF) release etching of the sacrificial oxide may also cause process complications. Bonded substrates with pre-etched cavities would provide freedom to the design of MEMS structures and solve some of the restrictions to the use of SOI for microsystems. It might also be useful in fabrication of 3D structures containing several wafer-bonded layers. After bonding the device/cap wafer can be thinned down mechanically and/or chemically to the desired device layer thickness, resulting a Si diaphragm over the cavity.[1-3] Subsequently, these diaphragms can be released with dry etching, avoiding the problems due to HF etching. In pre-etched SOI wafers the cavity dimensions are well-defined because they are lithographically patterned prior to the bonding. Moreover, the parasitic capacitance between the device layer and the substrate can be decreased far below what is achievable with a buried oxide layer in conventional SOI wafers if deep cavities and small bonding areas are prepared on a wafer. Also, the pressure inside the cavity can be adjusted by using suitable bonding ambient. Overall, pre-etched SOI wafers would be a suitable platform for vertically and horizontally moving structures in various applications, such as capacitive inertial sensors, pressure sensors, microphones, and microfludic devices. Bonding of patterned wafers enables double-side processing of the SOI layer and in principal, a wafer with pre-etched cavities would be transparent to complementary metal oxide semiconductor (CMOS) processes.

We have studied direct bonding and mechanical thinning of patterned Si wafers for the fabrication of thick-film SOI wafers with pre-etched cavities. The viability of grinding and chemical mechanical polishing (CMP) for silicon diaphragm fabrication has been investigated. The main objective of the work is to gain design rules for the buried cavities and mechanical thinning.

Experimental

A typical process flow for pre-etched SOI wafers is depicted in Fig. 1. The process is basically similar to a standard thick-film SOI wafer manufacturing process that is based on direct wafer bonding and mechanical thinning of the device layer. The difference is the fabrication of cavities on the handle wafer or the device wafer or even both prior to the bonding. In addition to the processing tools found in a typical wafer-manufacturing factory, some lithography equipment is needed. At the beginning of the process the cavities are prepared on a handle wafer using standard wet or dry etching techniques. Next, the etched handle wafer is bonded to another wafer, and subsequently the Si diaphragms are thinned with surface grinding and polishing (CMP).

In this work, ⟨100⟩-oriented 100-mm, p-type Si wafers were used for prepatterned SOI fabrication. The handle wafers were thermally oxidized either before or after the cavity etching. Wells with various sizes and shapes were formed on the handle wafers using standard lithography and wet and/or dry etching. The wells were etched to thermal oxide and/or to silicon. Thermal oxide was etched in buffered hydrofluoric acid (BHF) at room temperature. Wet etching of silicon was carried out in tetramethylammonium hydroxide (TMAH) at 80°C, and inductively coupled plasma (ICP) etching was used for the dry etching of silicon. Oxide and/or photoresist masking layers were used during the etching of silicon cavities. In some cases the cavity wafers were reoxidized in order to form oxide layer on the bottom and walls of the cavity (cavity oxidation). This reoxidation step was carried out after the oxide mask layer was removed with HF.

After cavity fabrication and buried oxide formation the handle wafers were bonded to the cap wafers with direct bonding. The bonding (wafer contacting) was carried out in vacuum (pressure $<10^{-2}$ mbar) or in air with commercially available wafer bonder (EVG801). Subsequently, the wafer pairs were annealed at 1100°C to increase the bonding strength. After bonding the cap wafer was thinned down by grinding and CMP. The grinding was conducted on a Strasbaugh model 7AF wafer backgrinder using a diamond cup coarse and fine wheels. The used fine grinding wheels were no. 2000 mesh (ca. diamond size 3–6 μm) or finer resin bonded diamond wheels. The grinding process was not optimized for cavity wafers, but a process that yielded a smooth surface and a thin subsurface damage layer was applied. This kind of processes is typically used in SOI wafer manufacturing, because short polishing process and a good wafer uniformity can be obtained. The polishing was carried out with a commercial CMP tool (Strasbaugh 6DS-SP) using standard polishing pads and slurries for silicon.

The bonding quality was evaluated with scanning acoustic microscopy (SAM), cross-sectional scanning electron microscopy (SEM) samples, and HF etching (50% HF, 10 min) of the buried oxide.[4] Prior to the bonding some of the cavity wafers were studied with atomic force microscopy (AFM) to see how the cavity preparation influences the surface roughness. In addition, the profiles of the cavity edges were investigated with SEM and surface profilom-

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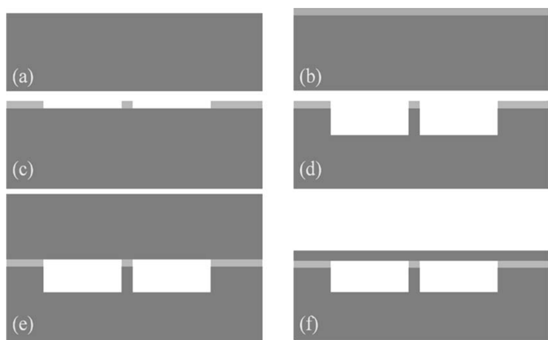

Figure 1. A typical process flow for SOI substrates with pre-etched cavities starts with a silicon handle wafer (a), which is thermally oxidized (b). The next step is patterning and etching of oxide (c) and silicon (d). After cavity formation the handle wafer is bonded to the cap wafer (e). Subsequent process steps are grinding and polishing down to a required Si diaphragm thickness (f).

etry (Veeco Dektak V-200). After thinning of the bonded wafer pairs the deflection and thickness of the Si diaphragms were measured with surface profilometry and SEM, respectively.

Results

In Fig. 2 SAM images of patterned bonded wafer pairs with square cavities are shown. Prior to the bonding the cavities were formed on thermally oxidized handle wafers using BHF etching. The width of cavity and pitch were varied on different wafers to change the overall bonded fraction. For wafers with large bonded areas the bonding occurred as expected. However, SAM measurements taken after air bonding and annealing at 1100°C showed voids at the bonded interface when the bonding area was small as compared to the total wafer surface area. For example, when the cavity width was 500 μm and the pitch 555 μm (bonded rim area 55 μm), corresponding to a cavity fraction of over 80%, wafer bonding in air resulted in a large void while wafers bonded in vacuum showed no voids. Voids with same size and shape were found from all similarly prepared air bonded samples, only location of the void varied. We assume that this is due to the pressure increase in the cavity during the high-temperature annealing. If the bonding area is sufficiently small, the pressure in shallow (in this case 2 μm) cavities may lead to the formation of voids. The wafer pairs with smaller cavity fractions, that is larger bonding area, had no voids irrespective of the bonding ambient.

The bond strength of patterned bonded wafers was measured by using the HF etching method.[4] In this test the buried oxide of the SOI wafer is etched with 50% HF for 10 min and the etched distance of the buried oxide is measured from the bonded interface with cross-sectional SEM. The etch rate has a relation with the bond strength: a faster etch rate means a weaker bond, as has been found for the bonded unpatterned wafer pairs.[4] After annealing of the patterned bonded wafer pairs at 1100°C the etched distance of buried oxide was 15–18 μm in vacuum-bonded samples, whereas an etched distance of 25–30 μm was measured for air-bonded samples. The result suggests that bonding in vacuum yields somewhat higher bond strength than air bonding.

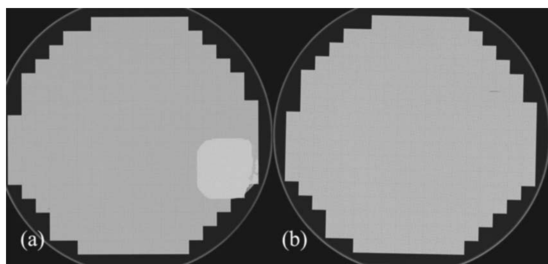

Figure 2. SAM images of prepatterned, bonded wafer pairs with 0.5 × 0.5 mm cavities. The width of the bonding rim area around the cavities is 55 μm. The bonding was carried out in either air (a) or in vacuum (b).

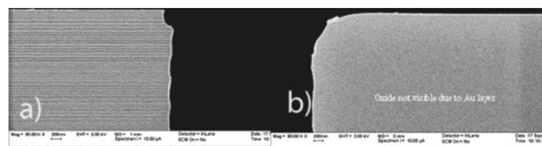

Figure 3. Cross-sectional SEM images of edges of the plasma etched Si cavities before (a) and after (b) thermal oxidation. The oxide layer (thickness 500 nm) is not visible in Fig. 3b, because a thin gold layer was evaporated on the sample for better image quality.

In some cases it would be desirable to cover the walls and bottom of the cavities with oxide layer. This can be accomplished by thermal oxidation, which is carried out after cavity formation. However, thermal oxidation of etched wafers may cause poor bonding because of pattern-dependent oxidation rate. Figure 3 presents SEM images of edges of the cavities before and after thermal oxidation. It is well documented that convex and concave corners on Si cause oxide thinning.[5] This stress-dependent oxidation causes rounding of the etched cavity corner (Fig. 3b). Surface profilometry revealed that the oxide surface is also slightly elevated near the edge of the cavity (Fig. 4). The height and width of this elevated area (bump) are typically 5–20 nm and a few micrometers, respectively. According to Tong and Gösele,[3] the gap closing can occur at the bonded interface if the condition $h < 3.5(R\gamma/E')^{1/2}$ is fulfilled, where h is height of the bump, R is the lateral extension of the gap, γ is surface energy at room temperature (0.1 J/m^2 for oxide–silicon bonding), and $E' = E/(1 - \nu^2)$, where E and ν are Young's modulus and the Poisson ratio, respectively. Based on this equation, the gap closing should not occur with typical bump dimensions. However, we could not detect any unbonded area with SAM measurements. This might be due to insufficient resolution of SAM. In order to study the bonding quality of oxidized cavity wafers, we thinned down the bonded handle wafers with oxidized cavities using backgrinding and anisotropic plasma etching. The thinning was continued until the etched cavities were reached. Figure 5 shows an SEM image of a etched column located inside the cavity after removing the handle wafer. Because the column survived the grinding and etching processes, it appears that at least the center area of the column is bonded to the handle wafer regardless of stress effects at the cavity edge. Anyway, the stress effects in oxidation have to be taken into account when one is performing thermal oxidation for cavity structures prior to the bonding.

To study the relation between the lateral dimension of the cavity, SOI layer thickness, and thickness variation of the Si diaphragms over the cavities, we ground and polished bonded wafers with pre-etched cavities of various size. After thinning the total thickness variation, convexity or concavity of Si diaphragms were measured. Figure 6 presents the measured total thickness variation of Si diaphragms as a function of average SOI-layer thickness for the various cavity sizes. The values were obtained from rectangular cavities. The length of the cavities was 10 mm and the width varied from 250 to 750 μm. It appears that the thickness variation of the Si diaphragm over the cavity increases with increasing lateral dimension of the cavity and with decreasing SOI layer thickness. The thickness of the Si diaphragm is largest at the center of the cavity and decreases toward the edge of the cavity. The result is similar to the data, which have been published by Prochaska et al.[1] With surface profilometry this thickness variation can also be observed as a hill on the Si film over the cavity (Fig. 7). The magnitude of hill height

Figure 4. Surface profilometry on the edges of TMAH-etched Si cavities which were thermally wet oxidized at 1050°C after cavity formation. The thicknesses of the oxide layer are (a) 100, (b) 400, (c) 1000, and (d) 2000 nm.

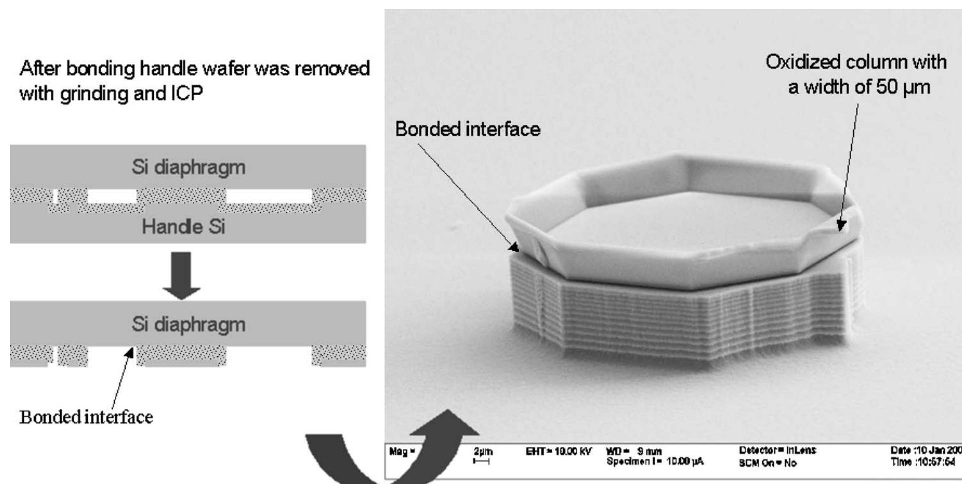

Figure 5. SEM image of an oxidized bonded column inside the cavity after removing the handle wafer with grinding and plasma etching. The width of the column is 50 μm.

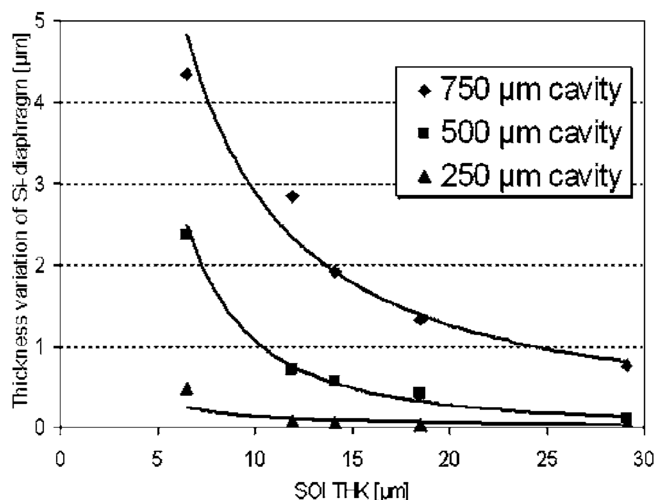

Figure 6. Measured thickness variation (TTV) for thinned (grinding + CMP) Si diaphragms as a function of average SOI-layer thickness for various cavity sizes. The cavities were etched on SiO_2/Si with BHF and ICP plasma etching. The length of the cavities are 10 mm, and the cavity depth is 50 μm. The widths for the cavities are 250, 500, and 750 μm. The wafer pairs were bonded in vacuum.

depends on the thickness of the diaphragm and its location on the wafer. Larger hill height was observed for the cavities at the wafer edges than at the wafer center. Concave bending was measured for a 6-μm SOI film over a cavity with a width of 500 μm. This is caused by the pressure difference between the inside and outside of the cavity that deflects the diaphragm downward.

It appears that the grinding and polishing forces bend the Si diaphragm downward during the thinning process, leading to nonuniform Si membrane thickness. The bending occurs due to increasing flexibility of Si film toward the center of film (cavity) and because of lack of support under the film. The thickness variation and integrity of the Si diaphragm can be improved by using support structures under the silicon diaphragm. Figure 8 depicts the influence of support structures on the surface profile of the Si diaphragm after grinding. All profiles were convex, because the vacuum inside the cavities was not able to deflect the membranes with the used cavity dimensions. For an unsupported cavity the hill height was about 1.5 μm after grinding with a SOI layer thickness of 20 μm. Figure 8 indicates that if a center support column is placed under the silicon diaphragm the hill height is about four times lower than the values observed for unsupported diaphragms. As the wafers were polished the measured hill heights were less than 0.1 μm for SOI thicknesses over 20 μm. Figure 9 presents 3D surface profiles of 2 × 2 mm cavities with a simple column support and four column supports inside the cavity. The measurements were carried out after grinding the diaphragms to a thickness of 23 μm. The measured hill height was about 1.9 μm for the diaphragm with four 50-μm column supports and about 0.6 μm for the diaphragm with a 800-μm

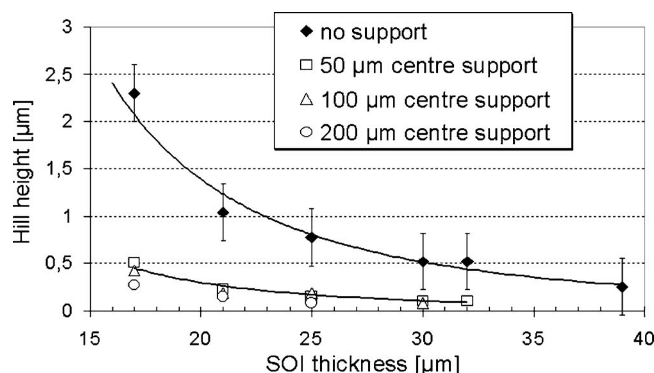

Figure 8. Measured hill heights for the Si diaphragms over 1 × 1 mm cavities with and without support columns. The depths of cavities were around 5 μm. No CMP was carried out, but the values were measured after grinding. The support square columns were located at the center of the cavity. The sizes for the columns were 50, 100, and 200 μm. The wafer pairs were bonded in vacuum.

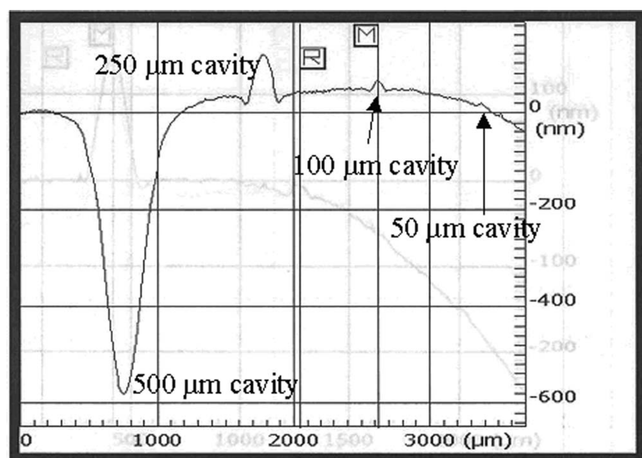

Figure 7. Surface profilometry on thinned (grinding + CMP) Si diaphragms over similar rectangular cavities as in Fig. 6. Scanning direction is perpendicular to the long side of the cavity. The thickness of the SOI layer is about 6 μm. The measured deflections are −600, 80, and 30 nm for 500, 250, and 100 μm diaphragms, respectively. The wafer pairs were bonded in vacuum.

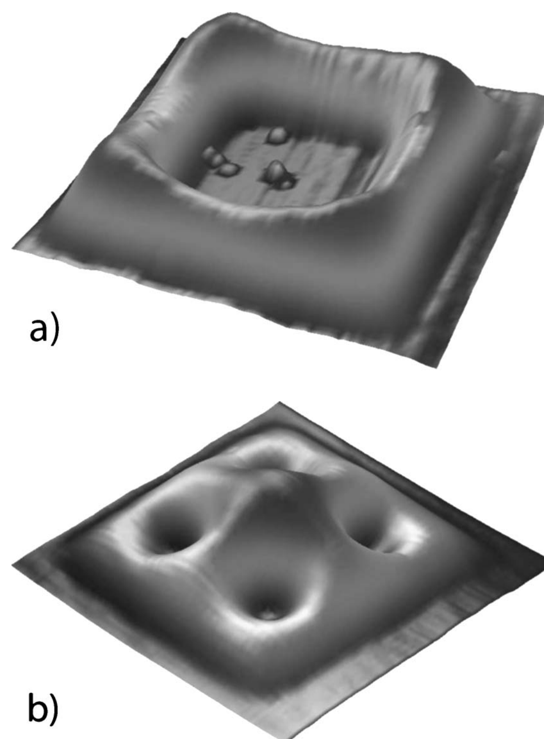

Figure 9. Measured 3D surface profiles of ground Si film over a 2 × 2 mm cavity with a 800-μm center column (a) and with four 50-μm columns under the diaphragm (b). The thickness of the SOI layer is 23 μm. The measured maximum hill heights are 0.6 and 1.9 μm for (a) and (b), respectively.

center column support. This suggests that the hill height and the thickness variation of the silicon diaphragms are largely determined by the dimensions of the unsupported film area.

Conclusions

Mechanical thinning of pre-etched and bonded silicon wafers is a viable method for fabrication of SOI substrates with buried cavities. SOI with pre-etched cavities may solve some of the problems inherent to conventional SOI MEMS technology. The grinding and CMP induce forces on the Si diaphragms over the etched cavities during the thinning of the bonded wafer pairs with cavities. This leads to thickness variation and hill formation on the surface of a Si diaphragm. The hill height was found to decrease during the polishing process. The integrity of the diaphragm can be significantly improved with various support structures. The results suggest that grinding and polishing can be utilized in buried cavity fabrication for various MEMS applications.

Acknowledgments

The authors thank the Finnish Funding Agency for Technology and Innovation (Tekes).

VTT assisted in meeting the publication costs of this article.

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