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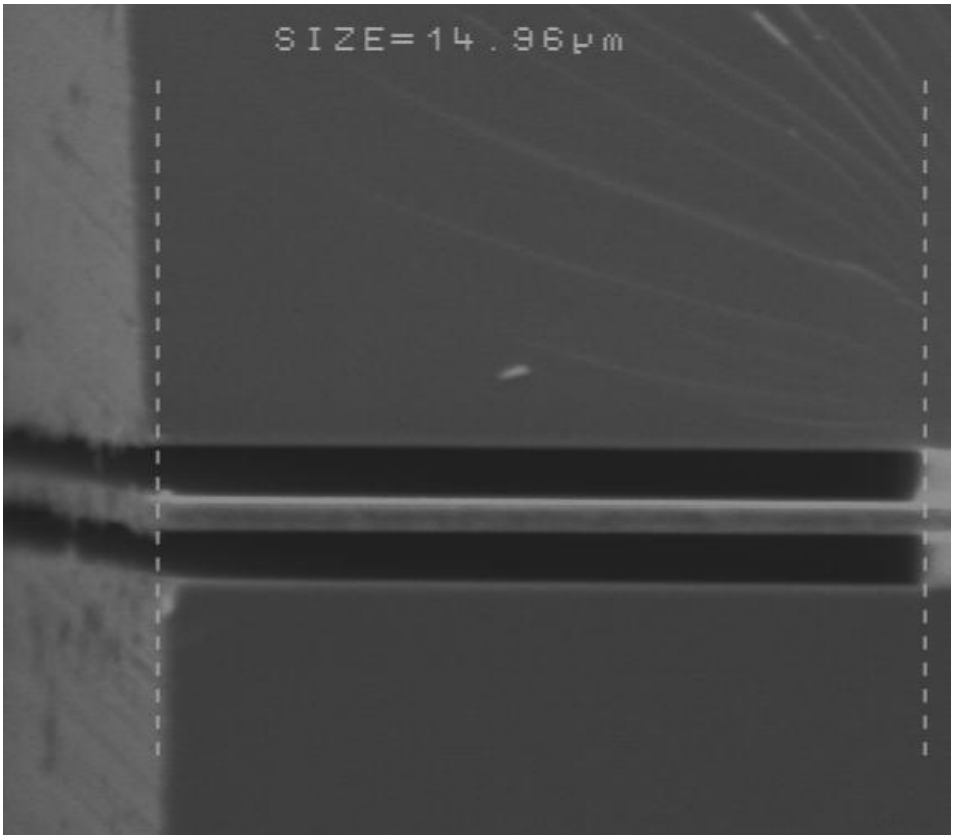

Tommi Suni

Direct wafer bonding for MEMS and microelectronics

VTT PUBLICATIONS 609

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Tommi Suni

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Keywords direct wafer bonding, MEMS, microelectronics, microelectromechanical systems, SOI, silicon-on-insulator, integrated circuits, bond strength measurement, heterogeneous integration, pre-processed SOI fabrication, wafer-scale packaging, plasma activation

Abstract

Direct wafer bonding is a method for fabricating advanced substrates for microelectromechanical systems (MEMS) and integrated circuits (IC). The most typical example of such an advanced substrate is the silicon-on-insulator (SOI) wafer. SOI wafers offer many advantages over conventional silicon wafers. In IC technology, the switching speed of circuits fabricated on SOI is increased by 20-50% compared to circuits fabricated on a bulk Si wafer. The required operation voltage is lower in ICs on SOI than in ICs on a bulk silicon wafer, which decreases power consumption and chip heating. In the MEMS industry, the buried oxide layer works as a good sacrificial layer during release etching of diaphragms, beams etc. and offers an excellent etch stop layer for silicon etching. Direct wafer bonding can also be used in the fabrication of more complex structures than SOI. The wafers to be bonded can be of different materials, can contain patterns, and may have multiple layers or ready-made devices.

This thesis reports on studies of direct wafer bonding and its use in various applications. Different bonding processes used in microelectronics are briefly described. The main focus of this thesis is on the plasma activation-based low temperature bonding process, and on the control of bond strength by surface preparation.

A novel method for bond strength measurement is introduced. This method, based on buried oxide etching, is presented and compared with other methods used in evaluating bond quality.

This thesis also contains results on research of different applications requiring direct wafer bonding. Heterogeneous integration, pre-processed SOI fabrication, and wafer scale packaging are the main application topics.

Suni, Tommi. Direct wafer bonding for MEMS and microelectronics [Puolijohdekiekkojen suoraliittäminen mikroelektroniikan ja mikromekaniikan sovellutuksissa]. Espoo 2006. VTT Publications 609. 89 s. + liitt. 34 s.

Avainsanat direct wafer bonding, MEMS, microelectronics, microelectromechanical systems, SOI, silicon-on-insulator, integrated circuits, bond strength measurement, heterogeneous integration, pre-processed SOI fabrication, wafer-scale packaging, plasma activation

Tiivistelmä

Puolijohdekiekkojen suoraliittäminen on menetelmä valmistaa kehittyneitä alustoja mikroelektromekaanisille systeemeille (MEMS) ja integroiduille piireille. Yleisin tämänlainen kehittyneempi alusta on SOI-kiekko, jossa kantajakiekon ja varsinaisen komponenttipiikerroksen välissä on eristävä oksidikerros. Verrattuna tavallisiin piikiekkoihin SOI-kiekot tarjoavat useita parannuksia. Integroitujen piirien tapauksessa kytkentänopeus on SOI:lla 20–50 % nopeampi, käyttöjännite matalampi ja energian kulutus pienempi. MEMS-teknologiassa haudattu oksidi toimii uhrautuvana kerroksena kalvojen ja palkkien vapautusetsauksessa ja myös pysäytyskerroksena piin syövyttämisessä. Suoraliittämistä voidaan käyttää myös monimutkaisempien rakenteiden kuin SOI-kiekkojen valmistamiseen. Liitettävät kiekot voivat olla eri materiaaleista, kuvioituja tai sisältää valmiita komponentteja.

Tässä väitöskirjassa keskitytään pääasiassa korkean ja matalan lämpötilan suoraliittämiseen sekä liitoslujuuden kontrollointiin pintoja karhentamalla. Kirjassa esitellään lyhyesti myös muut kiekkoliitostekniikat.

Väitöskirjassa raportoidaan myös uusi menetelmä mitata liitoslujuus kahden kiekon välillä. Menetelmä perustuu haudatun oksidin märkäsyövyttämiseen ja sitä verrataan myös muihin raportoituihin liitoslujuuden mittausmenetelmiin.

Tämä väitöskirja sisältää myös tuloksia suoraliittämisen käyttämisestä muutamiin erilaisiin sovellutuksiin, kuten kiekkotason paketointiin, heterogeeniseen integrointiin ja esiprosessoitujen SOI-kiekkojen valmistukseen.

Preface

This work has been carried out at VTT Microelectronics. I would like to thank first my co-workers at VTT for their help and support. Especially I would like to thank Kimmo Henttinen and Hannu Luoto for their assistance in the experimental work as well as in writing the articles. I would also like to thank my advisor Dr. Jari Mäkinen and my supervisor Prof. Ari Lehto for their guidance during final writing process. Thanks also to Dr. Jukka Lahtinen and Dr. Anke Sanz-Velasco for pre-examining the thesis and for Prof. Nathan Cheung for agreeing to be my opponent in the public defence of the thesis.

A lot of people have also been helping me and pushing me forward during all these years of studying making the writing of this thesis possible, so special thanks to: Äiti, T. Fält, E. Valovirta, J. Niemistö, T. Kaskiala, R. Jansson, K. Kaskiala, V. Sompa, J. Ylikerälä, J. Repo, A. Hirvonen, I. Suni, M. Kulawski, S. S. Lau, T. Penttinen, T. Tuominen, O. Alanen, A. Laukkanen, A. Saaristo, T. Tulkki, T. Karila, S. Mustala, S. Nurmi and also to my father and to my brothers.

Espoo, July 2006

Tommi Suni

Contents

List of abbreviations and terms

AFM	Atomic force microscope
APCVD	Atmospheric pressure chemical vapour deposition
BOX	Buried oxide
Cap wafer	Also known as device wafer. Top wafer in SOI wafer, thinned to desired SOI thickness
CMP	Chemical-mechanical polishing/planarization
CTE	Coefficient of thermal expansion
Device wafer	See cap wafer
DIW	Deionized water
DSP	Double side polished (wafer)
FBAR	Film bulk acoustic resonator
GaAs	Gallium arsenide
Handle wafer	Bottom wafer in SOI, the wafer that is usually not thinned
IC	Integrated circuit
InP	Indium phosphite
IR	Infrared
LPCVD	Low pressure chemical vapour deposition
MEMS	Microelectromechanical system
NIR	Near infrared
OH	Hydroxyl

PECVD	Plasma enhanced chemical vapour deposition
RMS	Root mean square
SAM	Scanning acoustic microscope
SC-1	Standard cleaning 1, also known as RCA-1. Typical cleaning bath for silicon wafers which removes particles and makes the surface hydrophilic.
SEM	Scanning electron microscope
SIMOX	Separation by oxygen implantation, one way to fabricate SOI
Si-OH	Silanol
Smart Cut™	Hydrogen implantation based method to make thin silicon layers
SOG	Silicon-on-glass
SOI	Silicon-on-insulator
SOQ	Silicon-on-quartz
SOS	Silicon-on-sapphire
sSOI	Strained silicon-on-insulator
SSP	Single side polished (wafer)
TTV	Total thickness variation
UHV	Ultra-high vacuum
Void	Discontinuation on the bonded interface

List of publications

This work is based on the following papers (Publications **A–F**), referred to in the text by the relevant letter in bold:

List of appended publications:

A. T. Suni, K. Henttinen, I. Suni, and J. Mäkinen. Effects of plasma activation on hydrophilic bonding of Si and SiO_2. Journal of the Electrochemical Society, Vol. 149, No. 6, (2002), pp. G348–351.

B. T. Suni, K. Henttinen, A. Lipsanen, J. Dekker, H. Luoto, and M. Kulawski. Wafer scale packaging of MEMS by using plasma-activated wafer bonding. Journal of the Electrochemical Society, Vol. 153, No. 1, (2006), pp. G78–82.

C. T. Suni, K. Henttinen, J. Dekker, H. Luoto, M. Kulawski, J. Mäkinen, and R. Mutikainen. SOI wafers with buried cavities. Journal of the Electrochemical Society, Vol. 153, No. 4, (2006), pp. G299–G303.

D. T. Suni, J. Kiihamäki, K. Henttinen, I. Suni, and J. Mäkinen. Characterization of bonded interface by HF etching method. In Semiconductor Wafer Bonding: Science, Technology and Applications VII, edited by C. Hunt, H. Baumgart, S. Bengtsson, T. Abe, Electrochemical Society, pp. 70–75, 2003.

E. K. Henttinen, T. Suni, A. Nurmela, M. Kulawski, and I. Suni. Mechanical delamination for the materials integration. In Semiconductor Wafer Bonding: Science, Technology and Applications VII, edited by C. Hunt, H. Baumgart, S. Bengtsson, T. Abe, Electrochemical Society, pp. 359–367, 2003.

F. K. Henttinen, T. Suni, A. Nurmela, H. Luoto, I. Suni, V.-M. Airaksinen, S. Karirinne, M. Cai, and S. S. Lau. Transfer of thin Si layers by cold and thermal ion cutting. Journal of Material Science: Materials in Electronics, 14, (2003), pp. 299–303.

Author's contribution

In **Publication A**, the author planned the experimental work together with co-authors, performed the experimental work and wrote the manuscript with the help of the co-authors.

In **Publication B**, the author planned and performed the experimental work together with the co-authors and wrote the manuscript with their help.

In **Publication C**, the author planned and performed the experimental work together with the co-authors and wrote the manuscript with K. Henttinen.

In **Publication D**, the author planned and performed the experimental work and wrote the manuscript, taking into account comments by the co-authors.

In **Publication E**, the author planned the experimental work together with K. Henttinen and performed the experimental work together with other authors. The manuscript was written with K. Henttinen, taking into account comments by the other co-authors.

Publication F is a joint paper together with researchers from VTT, Okmetic Oyj, Tampere University of Technology and the University of California, San Diego. The main experimental work was planned and performed at VTT by the author and K. Henttinen. The manuscript was written by K. Henttinen and the author with the help of the other co-authors.

1. Introduction

Direct wafer bonding means joining two surfaces without intermediate adhesives or external force. If the surfaces are flat and clean, wafers bond together when brought into contact. The initial bond strength is usually weak. Therefore, a subsequent annealing step is generally carried out to strengthen the bond.

Direct bonding was first reported by Sir Isaac Newton in the 17th century. He observed a black spot surrounded by "Newton's rings" when a flat and a convex optical surface were brought into contact. [1]

Currently direct wafer bonding has many applications in the microelectronics industry. It is used to fabricate substrates for modern integrated circuits (SOI, SOG, SOS, sSOI), to stack many processed layers (3D-integration) and as a method to encapsulate MEMS devices. These different applications require usually more than just a typical silicon wafer bonding process (wafer contacting and annealing at 1100°C). Bonding of processed wafers or wafers with a large difference in thermal expansion coefficients requires a low-temperature bonding process. Surface preparation may also be required before wafer contacting, the most typical process steps being plasma activation, chemical cleaning and chemical-mechanical polishing.

1.1 Objectives of this thesis

The main objectives of this thesis were first to study low temperature direct bonding, then to develop bonding processes suitable for various applications, such as fabrication of silicon-on-glass (SOG), silicon-on-sapphire (SOS), and silicon-on-insulator substrates with buried cavities, as well as for wafer scale packaging of MEMS components. This study also introduces a bond strength measuring technique based on the etching of buried oxide with hydrofluoric acid. This method is suitable for evaluating the bond strength easily from ready-made SOI, diced samples and from small bonded areas, which are difficult or impossible to measure with the crack opening method. This thesis focuses on bonding of silicon, but the same requirements apply to bonding of other semiconductor materials as well: surfaces have to be flat, smooth and clean.

1.2 Summary of appended papers

This thesis includes six publications on the topic of wafer bonding.

Publication A reports on the influence of plasma activation on wafer bonding and lists measured bond strengths for different bonding process combinations.

Publication B describes two different methods for encapsulating MEMS devices at wafer level utilizing plasma activated wafer bonding.

Publication C reports some design rules for fabrication of pre-processed SOI wafers for MEMS applications.

Publication D describes a method for measuring the bond strength of samples where the crack opening method cannot be used. Characterization of the bond strength by measurement of the buried oxide etch rate is, for example, applicable to small chips, silicon-to-glass and silicon-to-quartz bondings, which are difficult or impossible to measure with conventional methods.

Publication E presents a method for controlling the bond strength between two wafers. Good bond strength control creates possibilities to fabricate substrates that would be difficult or impossible to achieve with conventional methods (e.g. single crystalline silicon-on-sapphire)

Publication F describes a cold-cut process for fabrication of thin film SOI and SOG wafers. It also describes the influence of boron doping and crystal orientation on surface energy of the implanted layer after various annealing temperatures, setting the requirements for the bonding process.

2. Bonding

Bonding in general means the joining of two pieces of the same or a different material together. Bonding can be divided into three categories: bonding with a conducting interlayer, with an insulating interlayer, or without an intermediate layer. All of these categories are used extensively in the microelectronics industry. The bonding methods and their advantages and drawbacks are listed in Table 1. In this thesis, the focus is on hydrophilic direct bonding and low temperature direct bonding. Direct bonding means that there is no intermediate layer between the wafers, and the wafer surfaces bond spontaneously.

Table 1. Bonding techniques used in microelectronics.

Techniques	Advantages	Drawbacks
Bonding without interlayer	Hermetic	Flat surface required
Anodic	strong bond	high-voltage, bond time, sodium glass
Direct	strong bond	high-T, very flat surface required
Low-T direct	low-T	very flat surface required
Metallic Interlayer	Hermetic, non-flat surface ok	specific metals required
Eutectic	strong bond	flat surface required
Thermocompression	non-flat surface ok	high forces
Solder	self-aligning	solder flow possible
Insulating Interlayer	non-flat surface ok	varies
Glass frit	hermetic, common in MEMS	large area, medium to high-T
Adhesive	versatile	non-hermetic

2.1 Direct bonding (high temperature)

Direct bonding or fusion bonding generally means any joining of two materials without an intermediate layer or external force. In principle, most materials bond

together if their surfaces are flat, smooth and clean. The principle of this method is simple: two flat, clean and smooth wafer surfaces are brought into contact and form a weak bonding based on physical forces. The physical forces can be van der Waals forces, capillary forces or electrostatic forces [2]. The wafer pair is then annealed at high temperature (in the case of hydrophilic Si at >1000°C) and the physical forces are converted to chemical bonds. A typical process flow for wafer bonding is presented in Figure 1. In the case of silicon, high temperature bonding falls into two categories: hydrophilic bonding, in which the bonded surfaces are silicon dioxide, and hydrophobic bonding, in which the surfaces are silicon.

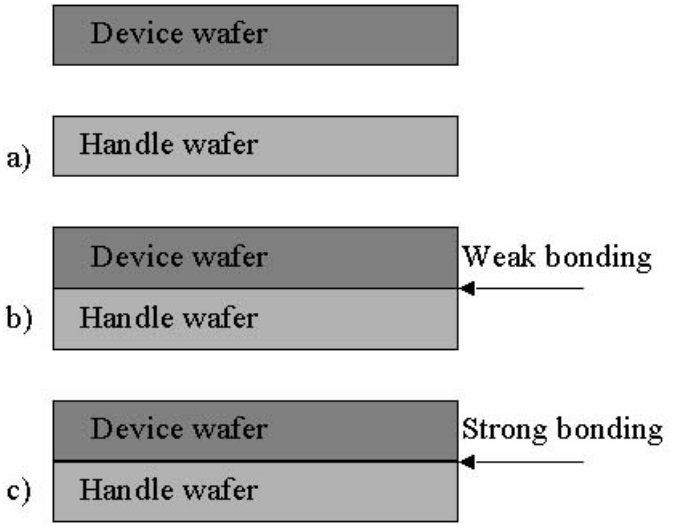

Figure 1. a) Surface preparations (e.g. cleaning, polishing, surface activation) b) Wafer contacting c) Annealing.

2.1.1 Hydrophilic high temperature bonding of silicon

Hydrophilic high temperature bonding is used commercially, for example, in SOI wafer manufacturing. The typical annealing temperature is ~1100°C. In hydrophilic bonding of silicon, the silicon wafer surface is covered with an oxide layer. The oxide can be a thin native oxide, thermally grown oxide or deposited oxide. The surface contains Si-O-Si and Si-OH bonds. It is the amount of Si-OH (silanol) groups on the surface that determines the hydrophilicity of the surface

due to polarization of the hydroxyl (OH) groups. The hydrophilicity of the surface can be enhanced with various methods, of which most popular is warm SC-1 (1:1:5 NH_3:H_2O_2:H_2O solution).

The reaction between two hydrophilic silicon surfaces during bonding is depicted in Figure 2. At the initial state after establishing contact between the wafers, water molecules form a "bridge" between the surfaces (Figure 2a). During annealing these water molecules diffuse out from the interface, dissolve into the surrounding material or react with surfaces increasing the number of silanol groups on the surface. Once these water molecules are removed, a bond is formed between silanol groups (Figure 2b). During further annealing, opposing silanol groups react according to reaction 1.

$$Si\text{-}OH + Si\text{-}OH = Si\text{-}O\text{-}Si + H_2O \quad (1)$$

During this reaction between silanol groups, more water molecules are released and Si-O-Si bonding is formed (Figure 2c).

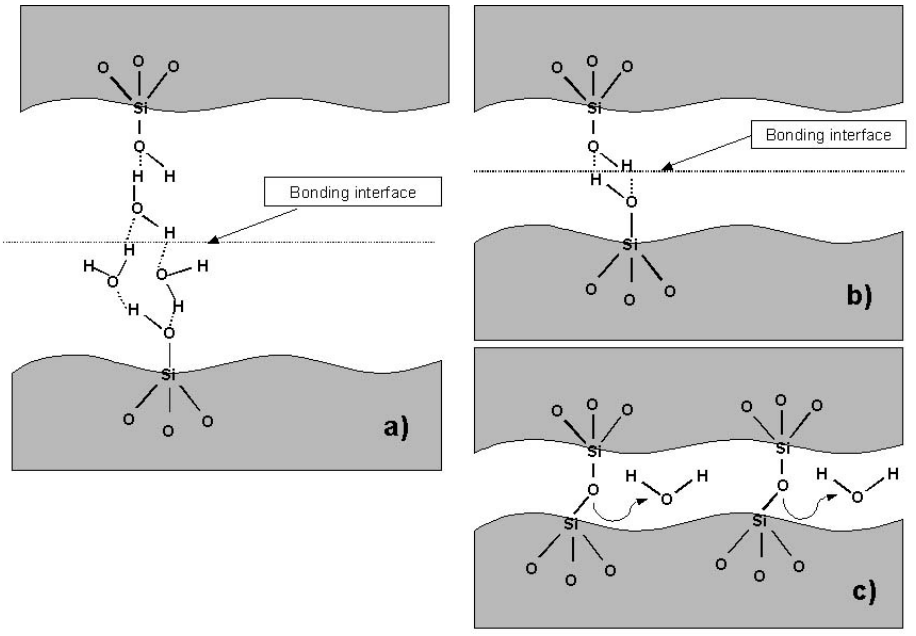

Figure 2. a) Bonding via intermediate water molecules, b) Bonding between two OH groups by van der Waals forces, and c) Formation of Si-O-Si bonds [2].

The water molecules diffuse into the silicon dioxide on the surfaces. If the water reaches the silicon, it reacts with it to form silicon dioxide and hydrogen.

$$Si + 2\ H_2O = SiO_2 + 2\ H_2 \qquad (2)$$

The remaining hydrogen does not react with silicon and may cause problems in the form of trapped gas, which is detectable with an IR camera or scanning acoustic microscopy (SAM) as voids (Figure 3). However, hydrogen has a high solubility into SiO_2 and by having an oxide layer of thickness > 50 nm on at least one wafer surface, hydrogen-induced voids can be avoided. The required amount of oxide on the surfaces for completely dissolving the hydrogen depends on the amount of water present at the interface. It can be enhanced by changing the hydrophilicity of the surfaces with different surface preparations and by using different bonding atmospheres.

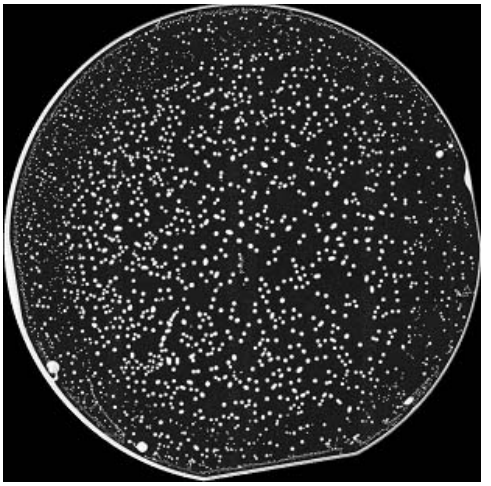

Figure 3. Hydrogen-induced voids in a bonded wafer pair. Both wafer surfaces had only ~2 nm thick native oxide, which cannot accommodate all of the hydrogen formed during the process.

2.1.2 Hydrophobic high temperature bonding of silicon

Hydrophobic bonding is a method for replacing epitaxial growth in some applications during fabrication of Si wafers with variously doped Si layers. For example, p-n junctions can be fabricated by bonding p-doped Si to an n-doped Si

wafer. It is also used to fabricate compliant substrates by twist bonding. In hydrophobic Si bonding, silicon is directly joined to another silicon wafer without an intermediate oxide.

In hydrophobic bonding, the wafers to be bonded have a bare silicon surface, which is either hydrogen and fluorine terminated or in some cases has dangling bonds on the surface. A hydrogen and fluorine terminated surface results from hydrofluoric acid etching, which is a standard process for removing silicon dioxide. The hydrophobic surface is quickly contaminated with hydrocarbons, therefore the wafers should be quickly contacted or stored in a vacuum after removal of the silicon dioxide layer [3].

The bonding process is illustrated in Figure 4. At first the HF molecules form a bridge between two silicon surfaces. At temperatures from 150°C-300°C, the HF molecules are rearranged and additional bonds are formed. During annealing at 300°C–700°C, hydrogen desorbs from the surfaces and Si-Si bonds are formed according to reaction 3 [2].

$$Si\text{-}H + Si\text{-}H = Si\text{-}Si + H_2 \qquad (3)$$

During annealing at >700°C, surface diffusion of silicon takes place and closes the microgaps between the surfaces [2]. The problem with the bonding process is again the presence of hydrogen at the bonded interface, which may cause voids.

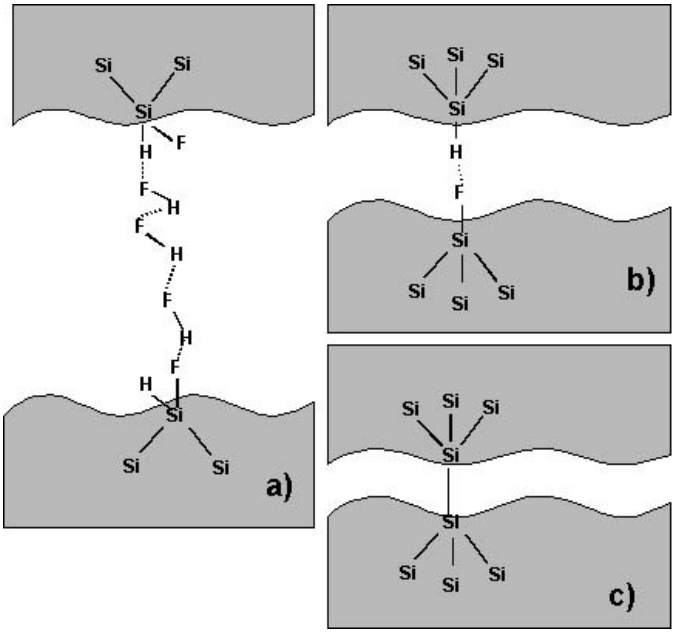

Figure 4. a) Bonding via HF molecules, b) Bonding via H & F atoms with van der Waals forces, c) Si-Si bonding formed after high-temperature annealing [2].

2.2 Low-temperature direct bonding

A low-temperature bonding process may be needed if the wafers are pre-processed, contain temperature-sensitive materials or components, or have different thermal expansion coefficients. The most common methods used for low-temperature hydrophilic direct wafer bonding are based on plasma activation [**Publication A**, 4, 5, 6, 7]. In these methods the wafer surface or surfaces is/are activated with short plasma treatment prior to wafer contacting. Numerous plasma processes have been reported for bond strengthening. The most often reported plasma gases are argon, nitrogen and oxygen. Sometimes it is advantageous to have a short wet cleaning step between activation and bonding [**Publication A**]. After this, a strong bonding is achieved at low temperatures (<400°C); even room-temperature processes have been reported [4, 5].

Different chemical activation methods have also been published [3, 2], but their effectiveness is not as good as plasma activation.

Low temperature hydrophobic wafer bonding is mainly done using ultra-high vacuum bonding [8, 9]. Other reported methods involve fabrication of an amorphous silicon layer by arsenic implantation, B_2H_6 or argon plasma treatment or sputter deposition [10].

2.2.1 Plasma activation based low-temperature bonding

The bond-strengthening influence of short plasma activation is clear and has been reported in numerous articles [**Publication A**, 4, 6, 5, 7]. However, the mechanism behind this effect is still unclear. This chapter gives an overview of the theories presented in the literature. The final answer may not be just one effect of the plasma but a combination of many.

During plasma treatment, many processes take place simultaneously. The plasma contains charged and neutral particles. The charged particles can be ionized atoms or molecules and electrons. These particles can react chemically with the wafer surface. During plasma processes a bias voltage is usually applied. This induces bombardment of the particles on the wafer surface, creating a sputtering effect. During plasma processes, UV radiation is also formed and it can have an effect on the chemistry of the wafer surface by breaking Si-O and Si-H bonds [11].

It has been reported by Farrens et al. that the oxide layer thickness on silicon wafer increases by 1–1.5 nm during oxygen plasma exposure. They believe that this oxide layer contains free radical ions from the plasma, which enhance the bond strength at low temperatures by increasing the atomic mobility of reacting species at the interface. [5]

The plasma has also been found to create highly hydrophilic surfaces. Reiche et al. have measured contact angles of below 2° between water droplet and wafer surfaces after plasma exposure. This behaviour has been found to last for several days. [7]

The influence of plasma exposure on the surface roughness has been reported by many research groups [7, 12, 13]. The data is controversial because some results show roughening [7] and some smoothening [12, 13] of the surface. In

Publication A, short Ar plasma treatments (30 s) showed no roughening or smoothening effects on Si, but prolonged (10 min) treatment increased the surface roughness slightly from ~1 Å RMS to about 2 Å RMS.

Charging of the wafer surface is also said to be the reason for higher bond energies for plasma-activated samples [5]. During plasma exposure the surface becomes charged due to implantation of the ions, ionization of the oxide and breakage of the bonds on the wafer surface, creating dangling bonds [14]. Charging of the oxide leads to electric fields which may affect the general chemical properties of the oxide and also the ion transport [15].

The intermediate water has to be removed before SiOH groups can react and form Si-O-Si bonds (Figure 2). This is assumed to take place by oxygen reacting with silicon while hydrogen dissolves into the oxide. If one of the oxides is thin, the water can reach the silicon and form silicon dioxide, even at low temperature. With thick oxides, the diffusion length for water to reach the silicon is longer, which is assumed to be the reason for weaker bond strength between SiO_2-SiO_2 surfaces than between Si-SiO_2 surfaces [**Publication A**]. It is suggested that the plasma increases the kinetics of water removal from the bonded interface [**Publication A**, 16, 13]. This is considered to take place due to a porous oxide layer formed by the plasma [**Publication A**, 13, 16]. The porosity of the layer is suggested by the increased oxide etch rate in SC-1 solution [**Publication A**, 13], by a higher etch rate during buried oxide etching with HF [**Publication D**] and by X-ray reflectivity at the bonded interface [13].

2.2.2 Ultra-high vacuum low-temperature hydrophobic bonding

Ultra-high vacuum (UHV) bonding has been reported as a method for making room-temperature hydrophobic bonding [9, 8]. First the wafer pair is bonded in the same way as in hydrophobic bonding (SC-1, HF dip, wafer contacting) but no annealing is done after wafer contacting. The bonding is done at this state only to protect the surfaces during transportation to the UHV chamber. After the wafers are placed in the UHV chamber and the base pressure is reached (10^{-10} mbar), the wafers are separated. By using an elevated temperature of 450°C the hydrogen termination is removed and the surface contains only reactive dangling bonds. The wafers are cooled to room temperature and bonded in the UHV

atmosphere. The measured bonding energy is close to the bond strength of the bulk silicon [8].

2.3 Bonding of chemical vapour deposited (CVD) oxides

Usually in SOI structures the buried oxide is thermally grown prior to bonding. Typically, deposition temperatures of CVD oxides are lower (150°C–500°C) than thermal oxidation temperatures (>800°C). Therefore, the CVD oxide layers can be grown on surfaces that contain temperature sensitive devices. Also, the growth rate is faster and the CVD process is not self-limiting like thermal oxidation (thickest thermal oxides < 3 μm). CVD SiO_2 can also be grown on non-silicon materials and therefore used as an intermediate bonding layer for heterogeneous integration. However, the CVD oxides also have some drawbacks compared to thermally grown oxide. The thickness uniformity is inferior and the as-deposited oxide surface is usually too rough for direct bonding. Electrical and physical properties are also inferior to thermal oxides.

Possible applications for bonding of CVD oxides are SOI wafers with thick buried oxides, bonding of pre-processed wafers (for e.g. encapsulation purposes), and bonding of non-silicon materials.

To study the suitability of CVD oxides for direct bonding, high and low temperature bonding tests were performed with plasma-enhanced chemical vapour deposited (PECVD) and low-pressure chemical vapour deposited (LPCVD) silicon dioxide layers. The bonding processes were carried out in vacuum. In the low temperature bonding process the wafer surfaces were activated with 30s oxygen plasma treatment followed with short SC-1 dip before bringing the surfaces into contact [**Publication A**]. The deposition temperatures were 425°C for LPCVD oxide and 300°C for PECVD oxide. For comparison, some wafers with thermally grown wet oxide were also bonded.

The CVD oxide surface roughness was first measured with AFM. The as-deposited PECVD oxide had a surface roughness of ~1 nm RMS and the as-deposited LPCVD oxide a surface roughness of ~3 nm RMS (Figure 5). From the SAM image (Figure 7a) of as-grown PECVD oxide bonded to the silicon wafer pair, it can be seen that the surface roughness is too high for direct

bonding. The as-deposited LPCVD oxide did not bond at all. Therefore, the wafers with CVD oxide went through a short oxide polishing step on the chemical-mechanical polishing (CMP) tool. After polishing, the measured surface roughness was below 2 Å RMS (Figure 6), enabling void-free bonding (Figure 7b).

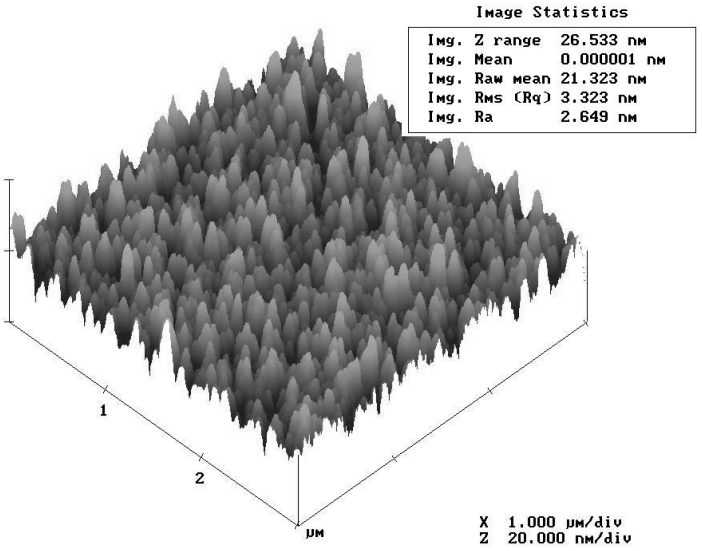

Figure 5. AFM image of as-deposited LPCVD oxide.

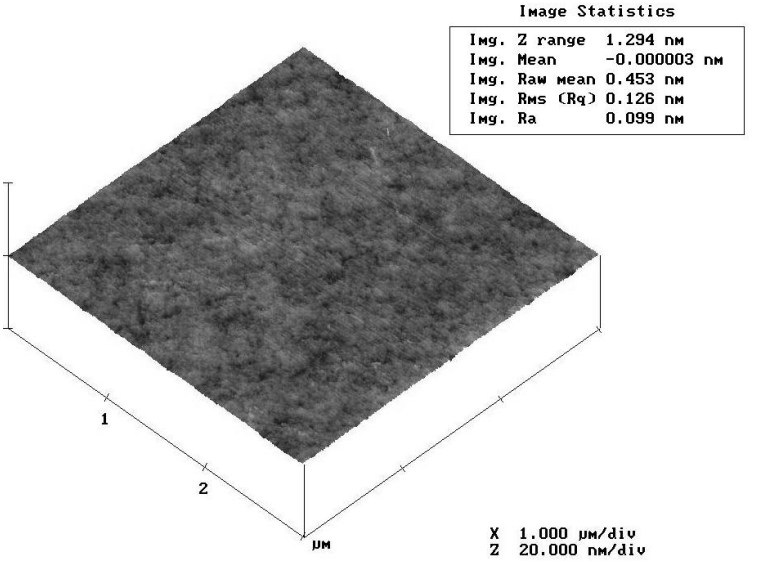

Figure 6. AFM image of polished LPCVD oxide surface.

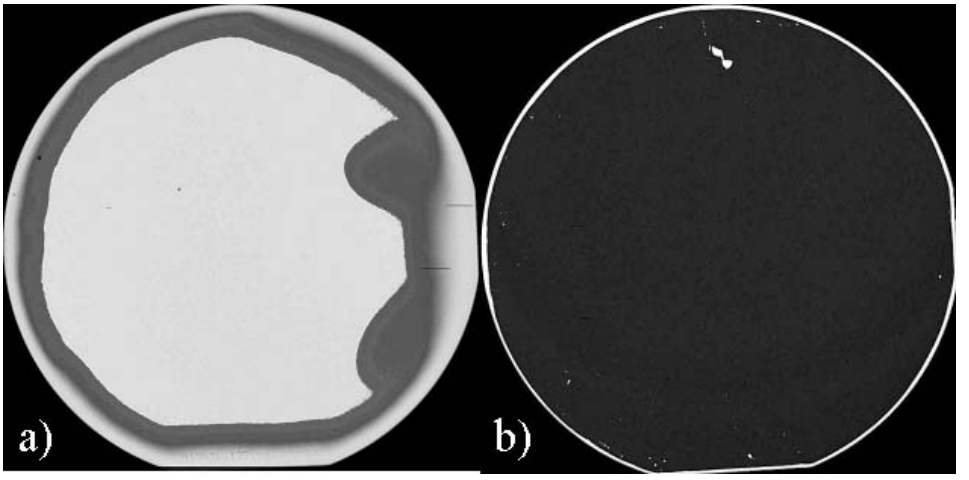

Figure 7. SAM images of a) as-deposited PECVD oxide bonded to Si wafer pair b) CMPd PECVD oxide bonded to Si wafer pair.

During bond annealing it was found that impurity outgassing takes place as the annealing temperature exceeds the deposition temperature. For example, PECVD oxide deposited at 300°C and bonded to the silicon wafer looks almost void-free in SAM after bond annealing has been carried out at 200°C (Figure 7b). When the same wafer is further annealed at 400°C, voids start to appear

(Figure 8a) and after annealing at 600°C the wafers are almost completely debonded (Figure 8b). Similar results were found with LPCVD oxide layers. When using an annealing step (2h, 1000°C) prior to bonding to outgas the impurities, no voids appear during bond annealing at temperatures between 100°C and 1100°C (Figure 9).

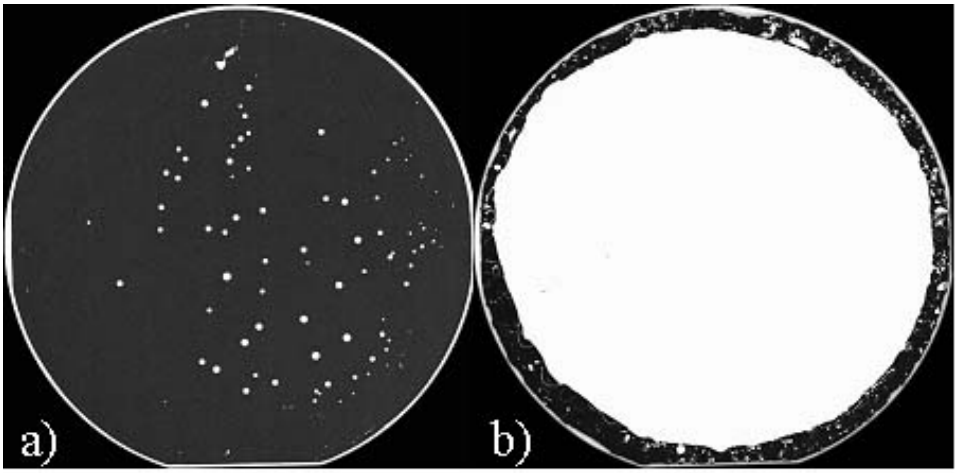

Figure 8. SAM images of Si-PECVD oxide wafer pair after annealing at a) 400°C b) 600°C for 2 h.

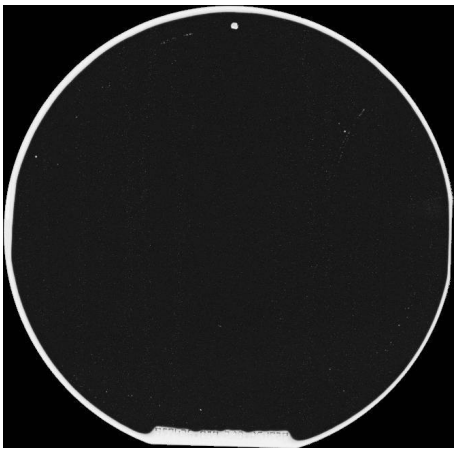

Figure 9. SAM image of Si-PECVD oxide wafer pair after annealing at 1100°C for 2h. PECVD oxide was pre-annealed before bonding at 1000°C for 2h.

Bond strength measurements were also carried out using the crack-opening method. Surface energies for different oxide-silicon wafer pairs are shown for non-activated samples in Figure 10. The CVD oxides were annealed at 1000°C prior to bonding to avoid impurity outgassing and debonding at high bond annealing temperatures. The figure shows that the strongest bonds are obtained for PECVD oxide/Si wafer pairs. It is possible that the PECVD oxide layer is more porous than LPCVD and thermal oxides. Porosity of the oxide makes it easier for bonding reaction products to exit the bonded interface. Ellipsometric film composition measurements also showed that the PECVD oxide contains excess silicon. This may also be the reason for stronger bonds, reducing the diffusion distance for the interfacial water to find silicon to react with.

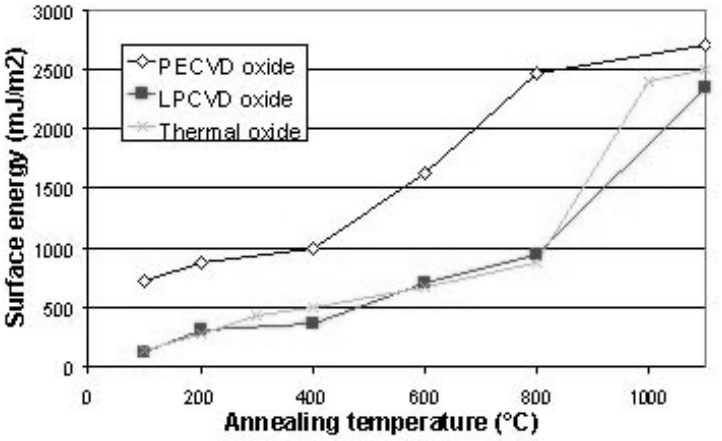

Figure 10. Bond strength as a function of annealing temperature for different Si-oxide wafer pairs bonded without plasma activation.

Figure 11 shows the surface energies for oxygen plasma activated samples. Oxygen plasma activation enables strong bonding already at a low temperature [**Publication A**]. All wafer pairs reached a surface energy of >2000 mJ/m^2 at 200°C, independent of the used oxide.

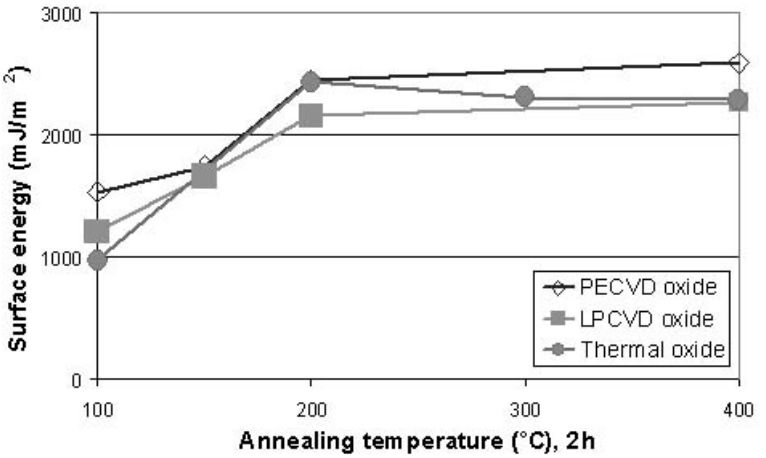

Figure 11. Measured bond strengths for plasma activated and bonded samples as a function of annealing temperature. Annealing time 2h.

2.4 Bonding of chemical vapour deposited silicon

Chemical vapour deposited polysilicon is sometimes used in MEMS applications. If polysilicon is used as the surface layer on the silicon wafer, the encapsulation is typically carried out by anodic bonding, which is not as sensitive to surface roughness as direct bonding. However, in some applications, it would be desirable to use direct bonding of polysilicon.

The first experiments were done with amorphous-like LPCVD silicon. In the as-deposited state on the oxide surface, the amorphous silicon had a surface roughness of 3–12 Å RMS. This surface roughness is not good enough for bonding, but in the amorphous state the silicon polishing with CMP was easy and required only removal of ~50 nm of silicon to achieve a surface roughness of ~1 Å RMS. The bonding was carried out in a vacuum and subsequent annealing was 2h at 1100°C, which not only strengthens the bond but also crystallizes the amorphous silicon into polycrystalline form. Measured bond strengths were high and no crystallization originating voids could be detected with SAM. The problem is the low deposition rate of amorphous films (~4 nm/min).

Tests have also been carried out on polishing and bonding of atmospheric pressure chemical vapour deposited (APCVD) and low-pressure chemical

vapour deposited (LPCVD) polysilicon films. With CVD polysilicon films, the problem is high as-deposited roughness of the films, which may be up to 10% of the final thickness. This means that during the polishing process the removal has to be much higher than with amorphous silicon. Another problem is that the chemistry of CMP attacks grain boundaries more than other areas, also causing problems in the polishing process. The advantage of growing in the polysilicon state is the increased growth rate compared to amorphous state deposition (40 nm/min with LPCVD, 4 μm/min with APCVD). The polishing process is carried out in two steps: the first step planarizes the surface (surface roughness ~12 Å RMS) and the second step smoothens the surface to the level required for bonding (~3 Å RMS). After polishing, the polysilicon surface was successfully bonded to the oxidized silicon wafer. [17]

2.5 Anodic bonding

Anodic bonding is a common method used in MEMS technology for device packaging. It was first introduced by Wallis and Pommerantz in 1969, after Pommerantz found that by applying an electric field a bond between metal foil and glass could be achieved at lower temperature than with conventional thermal bonding [18]. In anodic bonding, glass wafers can be joined to silicon wafers at low or moderate temperatures (300–450°C) and by applying a high DC voltage to the wafer pair (500–1000V) [19]. The most common glasses used for anodic bonding are Pyrex 7740 and Schott 8330, which are sodium borosilicate glasses having a coefficient of thermal expansion (CTE) close to the CTE of silicon. Sodium ions are needed for anodic bonding to take place, and matched CTEs help to maintain low stress on the bonded stack.

In anodic bonding the glass wafer is brought into contact with the silicon wafer and an external electrostatic field is applied at elevated temperature. Mobile sodium ions move towards the electrode, leaving a negatively-charged region into glass wafer, and electrostatic forces pull the silicon and glass tightly together. Next an electrochemical reaction takes place and covalent bonds are formed between the glass and silicon. Anodic bonding is less sensitive to surface roughness than direct bonding, but it requires that one of the wafers is alkali glass. It also requires high voltage and moderate temperatures.

2.6 Adhesive and polymer bonding

Adhesive bonding, as the name suggests, means that an intermediate adhesive layer is used to form bonding between two different materials. Adhesive bonding requires only low temperature annealing, if any. The bonding process is also cheap and requirements for surface smoothness are low. The disadvantages of these materials are long-term instability, a limited temperature range for their use, and the fact that they are not hermetic. However, the adhesive bonding is commonly used in applications where hermeticity is not needed. In some cases the bond hermeticity is obtained afterwards by using an additional metallization step [20]. Typical adhesives are different photoresists, polyimides and benzocyclobutane (BCB). [21, 22, 23]

2.7 Metallic bonding

Metallic bonding uses an intermediate metal layer between the wafers. It includes thermocompression, solder and eutectic bonding. In thermocompression bonding, two metallic surfaces are joined using high pressure and intermediate or low temperatures. For example, gold-gold thermocompression bonding is used by Avago Technologies to seal their film bulk acoustic resonator (FBAR) devices [24]. Bonding is formed by pressing together two wafers with gold pads at high pressure (~80 Mpa) at elevated temperature (~350°C).

In solder bonding, the solder balls are fabricated first by electroplating on one of the wafers, then the solder balls are brought into contact with contact pads on another wafer. The bonding is finished with low-temperature solder reflow. [25] The reflow process can also be carried out selectively using a laser [26]. Typical solders used in metallic bonding are SnPb and SnAg [20].

In eutectic bonding, typical metal systems are AuSi, AlGe and AuSn [20]. In the eutectic bonding carried out by Kim et al. [27], the cap wafer was covered with Cr-Au-Sn-Au layers and the handle wafer with Cr-Au layers. In the cap wafer the intermetallic reaction between Sn and Au had already occurred on the Sn-Au interface. As the bonding temperature was raised towards 250°C, the tin layer melted first and dissolved the thin $AuSn_4$ intermetallic layer. This molten Sn layer then came into contact with the thin Au layer on the handle wafer and

dissolved it. Upon cooling, the joint solidified and was expected to consist of a β-Sn matrix with $AuSn_4$ grains. [27]

Metallic bonding provides a hermetic seal at relatively low temperatures (200-400°C). Metallic bonding, however, has limitations regarding wafer topography and it is difficult to use it as a wafer-level bonding process.

2.8 Glass frit bonding

In glass frit bonding a glass paste layer is used as the bonding medium. It usually consists of finely ground (grain size less than 15 μm) lead or lead silicate glass and organic binder [28]. With inorganic additives the glass paste's CTE can be adjusted to match that of silicon. The glass paste is first deposited on the handle or the cap wafer, usually by screen-printing. After deposition the organic solvent is removed and the glass is sintered by drying and heating the sample. Then the cap wafer is placed on top of the handle wafer, the glass layer is melted at the process temperature, and the wafer pair is bonded under thermo-compression. The temperature needed is above the softening temperature of the glass used, usually still below 450°C. The advantages of the method are insensitivity to surface roughness, usability with most materials, and cheap price. The disadvantages are incompatibility with IC technology (due to Pb) and the requirement for a wide bonding rim (>200 μm).

3. Methods for evaluating bonding quality

The bonding quality is usually considered to consist of two parts: the bond strength and the amount of voids. In some applications these two quality factors are the only information needed, but in some applications it is also important to know e.g. the electrical properties of the interface and the etch rate of the buried oxide. This chapter looks at different bond quality measurements.

3.1 Methods to estimate the bondability of wafers

Especially with processed wafers, it is important to investigate the surface quality before bonding. This makes it possible to predict whether or not bonding is possible. The most important tools for this are profilometers to investigate the planarity of the wafer, and atomic force microscopy (AFM) for surface roughness measurements. Sometimes it is also important to use a particle detector to find process steps that may induce void-causing particles to the surface.

3.1.1 Atomic force microscopy (AFM)

The surface roughness of wafers is usually measured with an atomic force microscope (AFM) in tapping mode. The operating principle of the AFM is shown in Figure 12. In tapping mode, a silicon tip barely touches, or ”taps”, the surface. The system vibrates a cantilever near its resonant frequency at an amplitude of a few to tens of nanometers. Then it detects changes in the resonant frequency or vibration amplitude as the tip nears the sample surface. The changes in amplitude are measured with a laser beam, reflecting from the cantilever to a detector. The resonant frequency of the cantilever varies as the square root of its spring constant. In turn, the spring constant of the cantilever varies with the force gradient experienced by the cantilever. Finally, the force gradient changes with tip-to-sample separation. Therefore, changes in the resonant frequency of the cantilever can be used to measure sample topography. [29]

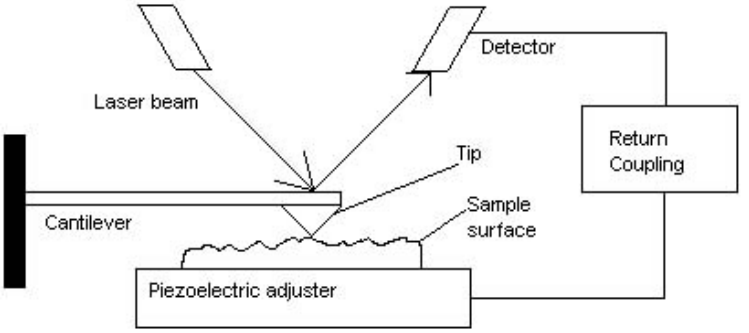

Figure 12. Operating principle of the atomic force microscope (AFM). A sharp silicon tip taps the surface and the amplitude of the oscillation is measured with a laser beam. Return coupling adjusts the height of the cantilever to keep the amplitude constant. [29]

3.1.2 Surface profilometry

Surface profilometry is of two types: contact and non-contact. The principle of contact profilometry is quite similar to AFM: a needle moves along the surface and its height is detected. The difference is that AFM usually scans areas of a few μm^2 and heights in the nanometre range whereas the profilometer's typical scan length is a few centimetres and the measured step heights are tens of micrometres.

Non-contact surface profilometry is based on optical interferometry. The interferometer splits a source beam of light into two different beams, one of which is reflected against the sample and another against a reference mirror. The two beams are then recombined and a CCD camera records the interference phenomena. Based on the interferogram the computer can calculate the distance between the sample and the objective. [30] The optical profilometry image of a cavity in a Si wafer is shown in Figure 13.

Figure 13. Optical profilometry image of an etched cavity on a Si wafer.

3.1.3 Particle detection

Particle detection on the wafer surface is usually done with methods based on light scattering. The surface is scanned with a high-intensity light spot and the light is scattered by defects (particles, scratches etc.). The scattered light is collected by a photodetector and a map is formed of the scanned surface showing locations and sizes of particles and other defects on the wafer surface.

3.2 Bond strength measurements

An important parameter that should be known in bonded wafer pairs is the amount of adhesion or the bond strength. This is because the bond strength may have a critical influence on the process steps (mechanical thinning, patterning, etching etc.) that the substrate undergoes.

3.2.1 The crack opening method

The most common method for measuring bond strength is the crack opening method [31]. A blade is inserted between two wafers, creating a crack between them. The crack length is then measured and in the case of identical wafers the bond strength can be calculated from

$$\gamma = \frac{3Ed^3 t_b^{\,2}}{32L^4} \tag{4}$$

where E is Young's modulus, t_b is the thickness of the blade, d is the thickness of the wafers and L is the length of the crack.

However, this method has its limitations. It is not suitable for measuring fragile wafers, because they tend to break during measurement. To insert the blade into the bonded surface, the bonded wafers have to be rounded at the edges. This is usually the case with two bonded silicon wafers, but it limits bond strength measurements to the areas near the edge of the wafer. It is also an inaccurate measurement, because the crack length in Equation 4 is to the power of 4 and the crack length also depends on the surrounding atmosphere. Some changes in crack length can also take place due to the force and speed with which the blade is inserted. To make the method more accurate, an automated blade insertion tool is suggested together with an environmental protective chamber [32]. Despite these drawbacks, it is the most popular method because it is cheap, simple and does not require wafer patterning.

3.2.2 Pulling test (or tensile test)

In the pulling test, as the name suggests, the bonded samples are pulled apart and the required force is measured. This method was first used for bonded silicon wafers by Abe et al. [33]. Both sides of the wafer pair are glued to the pulling rods in the test apparatus and force is applied. The force is increased until the wafers are separated. The operating principle is depicted in Figure 14.

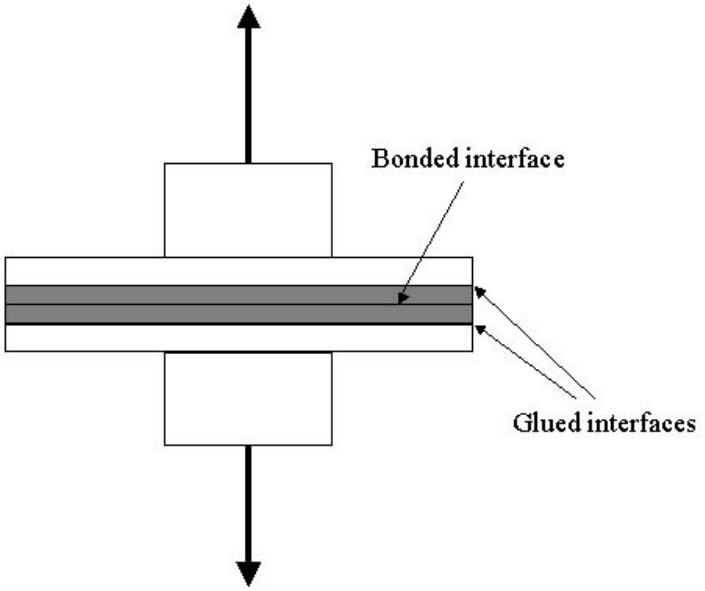

Figure 14. Set-up for the pulling test.

The pulling test is a useful method for measuring bond strength from small samples and it can be used to form bond strength maps for the wafers. The drawbacks are a more complex apparatus than in the crack opening method, and a problem with strong bonds or fragile samples in that the fracture does not occur at the bonded interface. The pulling rods should be placed into the centre of the sample and the pull axis should be perpendicular to the sample surface. Even small misalignment in the set-up may have a drastic influence on the results. Gluing is time consuming and may be the part that breaks first in the pulling test [32].

3.2.3 Blister test

The blister test has also been suggested as a method for measuring bond strength. In this test, one of the bonded wafers contains a hole and the hydrostatic oil pressure is applied through the hole until debonding takes place (Figure 15). The pressure required for debonding to occur is measured. With this pressure, the surface energy of the bonded interface can be determined from Equation 5. [2]

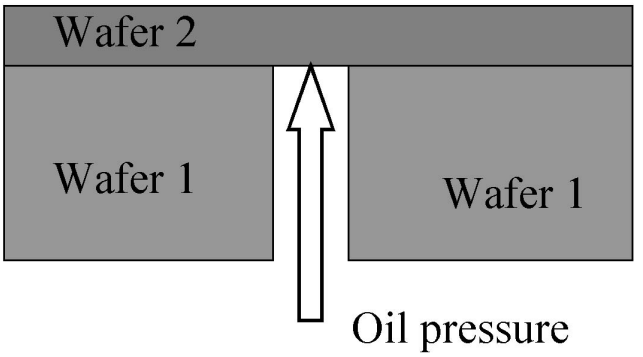

Figure 15. Set-up for the blistering test. Oil pressure on the hole is increased until debonding occurs.

$$\gamma = \frac{0.088 P_f^2 a^2}{E t_w^3} \tag{5}$$

where a is the hole radius, E is Young's modulus for the top wafer, P_f is the pressure required for debonding and t_w is the top wafer's thickness.

3.2.4 HF etching test

This bond strength measurement method is based on buried silicon dioxide etching in hydrofluoric acid (HF). It is described in more detail in **Publication D**. It has been found that the HF etch rate is dependent on the bonded interface quality. In this method the sample is dipped into 50% hydrofluoric acid for 10 minutes and the etched distance is measured with scanning electron microscopy from cross-sectional samples. A cross-sectional SEM image of strong bonding is shown in Figure 16. The etch rate at the bonded interface is close to the etch rate at the thermal oxide growth interface, which seen from the vertical oxide wall. At a weak interface (Figure 17), the profile of the oxide wall is less vertical due to a faster etch rate at the bonded interface.

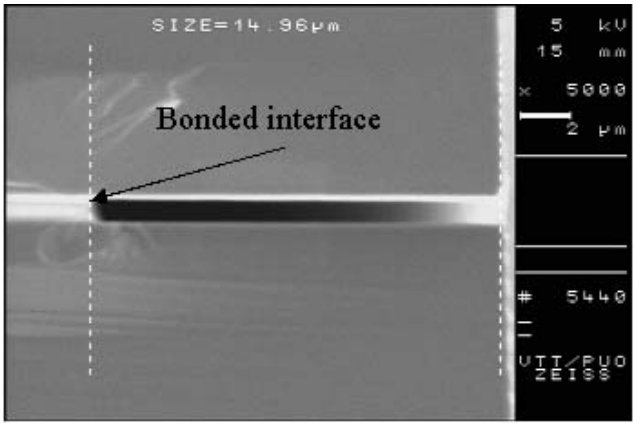

Figure 16. SEM image of buried oxide etched for 10 min in 50% HF. The etch rate of ~1.5 µm/min, and an equal etch rate on the bonded interface and the oxide growth interface indicate strong bonding.

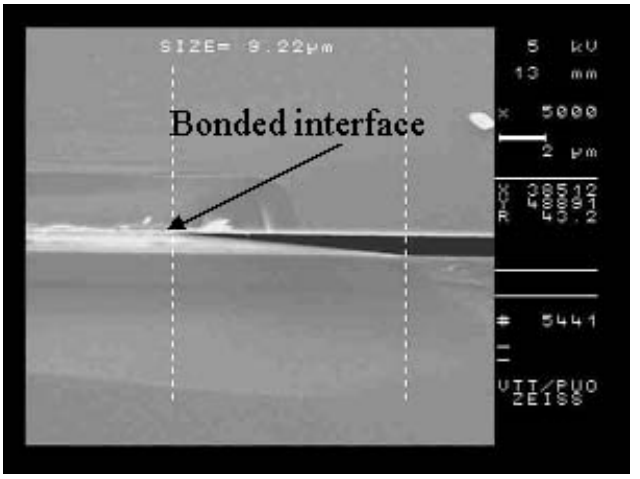

Figure 17. SEM image of buried oxide etched for 10 min in 50% HF. The higher etch rate at the bonded interface and the long total etched distance (~200 µm, not seen in the picture) indicate weak bonding.

For high temperature bonding of hydrophilic silicon wafers, the relation between bond strength and etch rate is logarithmic, as seen in the results plotted in Figure 18 [**Publication D**]. With plasma-activated samples the correlation is not as easy, because plasma creates a porous oxide layer. This porous layer has a higher etch rate than normal thermally-grown silicon dioxide, which makes the correlation more difficult.

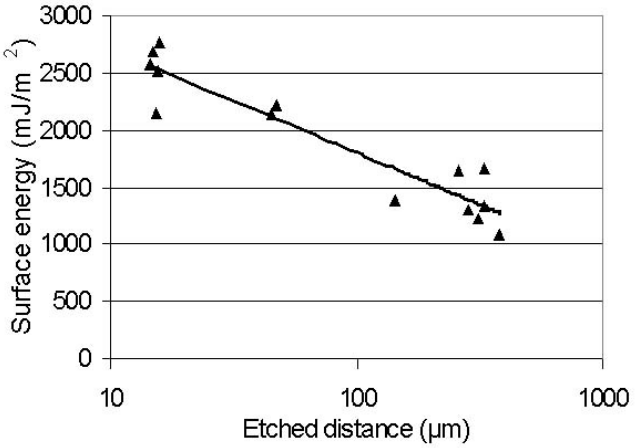

Figure 18. Relationship between etched distance of buried oxide during 10 min 50% HF etching and measured surface energy for high temperature bonded samples.

The etching method is a good method for certain samples that cannot be measured with the crack-opening method. Such samples are fragile, like quartz and glass wafers, ready-made SOI and diced samples.

The HF etching method also gives a good idea of the bond strength across the whole wafer area. The SOI layer is first patterned with standard lithography, and holes through the SOI layer are formed with ICP etching. Next the SOI wafer is dipped in 50% HF for 10 minutes, rinsed in DI water and dried. With relatively thin SOI layers (< 15 µm) and not highly boron-doped samples, the etched distance can be measured with an optical microscope attached to a near infrared (NIR) or infrared (IR) camera. By having "through-SOI" holes over the whole wafer area, the etched distance is easily measured from different locations, and variations are easily detected. A near-IR microscopic image (20x magnification) of the HF etched oxide front is shown in Figure 19.

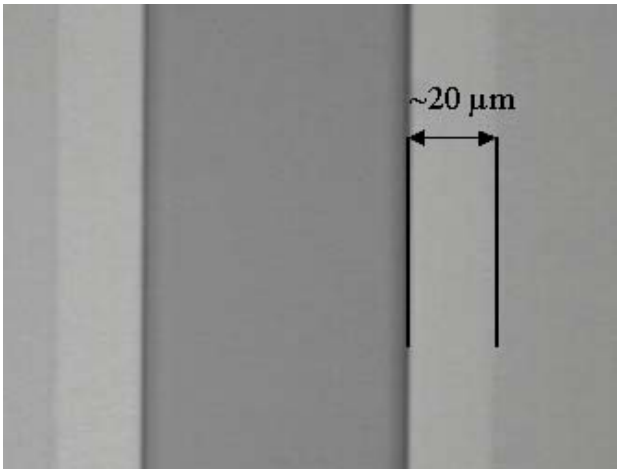

Figure 19. Near-IR image of buried oxide-etched sample. The darker area in the middle is where the SOI layer has been removed with ICP etching; the lightest areas represent the areas on which the BOX has been etched.

3.2.5 Chevron test

The chevron test is nowadays also a popular method for measuring the bond strength. It was first introduced by Rayleigh as early as 1936. It was first used for direct bonded wafers by Hoshi and Ogino in 1989 [32]. In recent years, Dr. Bagdahn's group at the Fraunhofer Institute in Halle, Germany, has been active in further developing the method, which they call the micro-chevron or MC test [34, 35].

In this method one of the wafers has chevron-shaped patterns on the surface before bonding, and it is bonded to an unpatterned wafer (Figure 20a). Pulling studs are then glued to the sample and a pulling force normal to the bond is introduced (Figure 20b). The force is slowly increased and a crack is formed starting from the tip of the chevron. While the crack propagates, the width of the crack increases according to the shape of the chevron. As the crack reaches its critical length, the crack's growth becomes unstable and instantly causes a fracture in the sample. The crack length depends only on the loading conditions and the specimen geometry, therefore the critical load for fracture to take place is the only thing needed to calculate the toughness of the bonded structure. [32]

This method is considered to be the most accurate measurement method for determining the bond strength. The measurement of maximum force is more accurate than measuring the crack length. The method is also suitable for measuring high bond strengths, because the fracture starts at the bonded interface at the chevron tip due to a high stress concentration [32]. Usually small chevron shapes are located all over the bonded area, so with the chevron test, bond strength maps can also be determined. Small chevrons can also be used on wafers containing actual devices to confirm the quality of the bonding. The only problems are the necessity for wafer patterning before bonding and gluing during loading, both of which are time-consuming.

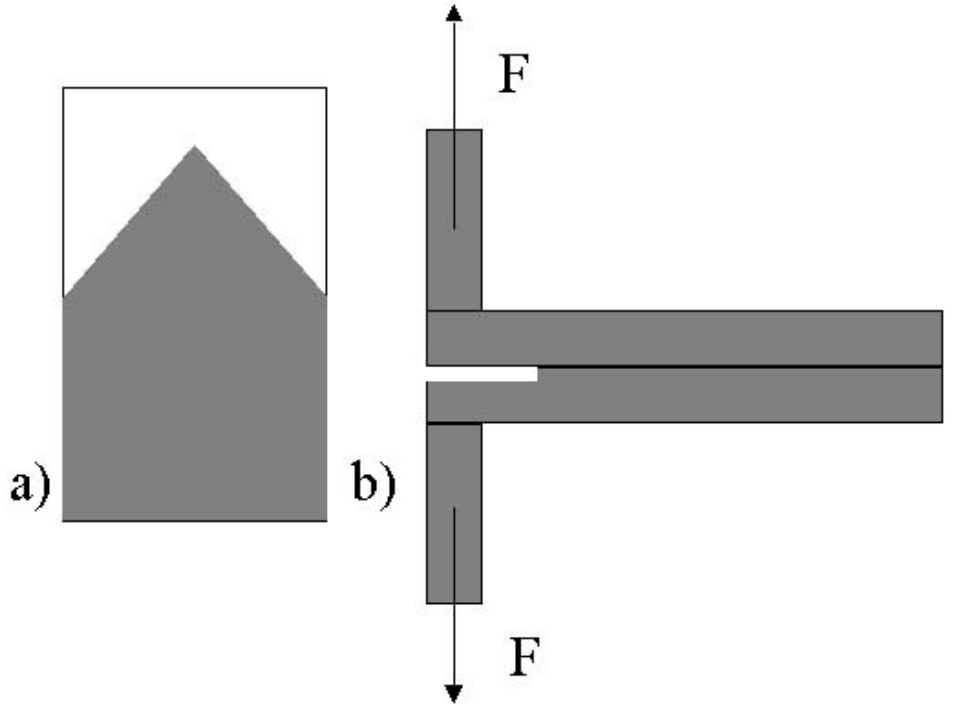

Figure 20. Set-up for micro-chevron test. a) Handle wafer with chevron shape bonded to a cap wafer b) Cross-section of the same sample with two pulling studs connected to the end with an unbonded area.

3.3 Void detection

Another important quality factor of the bonded interface is the amount of discontinuations of the bonded interface, so called “voids”. These voids may be caused by particles, chemical contaminants, poor surface quality or trapped gas. There are different methods for void detection. Optical inspection can be used in cases where at least one of the wafers is transparent to light (quartz, glass, sapphire). In the case of silicon wafers, typically the first inspection is done with an infrared (IR) camera before annealing. A final, more detailed inspection is usually done after final annealing. For this, the most widely used method is scanning acoustic microscopy.

3.3.1 Optical inspection

For instant investigation of the bonding quality, optical transmission is the most popular method. Areas that are not in contact form Newton’s rings due to the interference of light reflected on internal surfaces. The shape of the rings shows the shape of the delamination, and light and dark rings enable determination of the distance between unbonded surfaces [36].

If at least one of the bonded wafers is transparent (e.g. glass, quartz, sapphire), voids can be observed with the naked eye. For cases with two silicon wafers, IR light and an IR camera are required. Heavily doped silicon, however, is not transparent to IR light and therefore IR transmission is not suitable for wafer pairs with at least one highly doped counterpart. Figure 21 shows an IR image of a bonded 4’’ silicon wafer pair having one large and a couple of smaller voids.

The method is popular because it is fast and non-destructive. It can be used instantly after wafer contacting, so no annealing is needed before inspection. However, it is unable to detect all voids. To detect a void with IR, the surfaces must be at least one fourth of the wavelength apart and the lateral resolution is typically limited to about 1 mm. [37] Nowadays there are commercially available scanning IR tools that use light scattering over inhomogeneities. For example, Phoseon Technology [38] promises a resolution of ~5 µm.

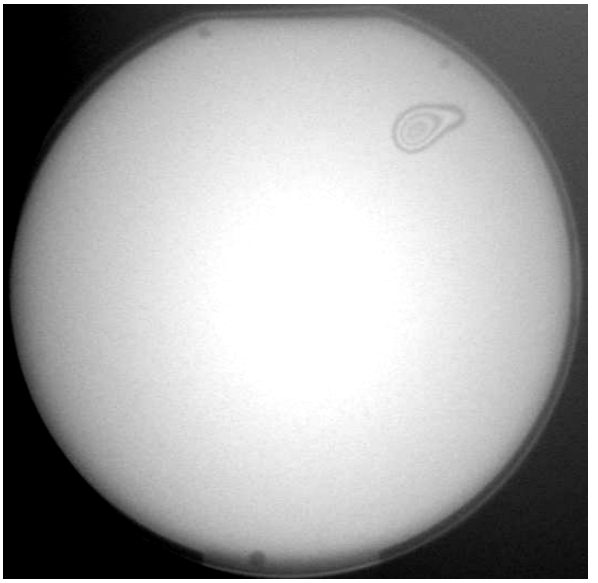

Figure 21. IR image of bonded 4'' wafer pair. At top right is a large void surrounded by Newton's rings.

3.3.2 Scanning acoustic microscopy (SAM)

Scanning acoustic microscopy is also used for void detection. It works like a sonar, sending an acoustic signal and measuring the time it takes to reflect back to the detector. The intermediate material between the sample and the emitter-receiver is water. The acoustic signal reflects back if the media it travels through changes. Interpreting the signal in the case of two bonded wafers is fairly easy. The microscope shows a signal graph in which the x-axis represents the time of delay from the transducer to the receiver, and the y-axis represents the strength of the reflection. From this graph it is easy to distinguish the reflections coming from the front and back surface of the bonded wafer pair. If there is also a reflection originating between the front and back surface reflections, it is usually caused by an interfacial void (in some cases e.g. thick buried oxide causes reflection, but it is typically weaker than the signal coming from a void).

In wafer bonding the SAM is typically used in C-mode. In C-mode, the SAM-image is formed from the reflections coming from a depth set by the user. The theoretical maximum resolution of SAM is 0.5 µm [39], but this requires high

frequency and a really thin sample. The typical scan resolution for full-wafer scans is ~100 µm to limit the scan time to a few minutes. The SAM image of patterned 30 nm oxide bonded to a blank silicon wafer is shown in Figure 22. The white areas represent reflection and therefore also unbonded areas. For comparison, an IR image of the same wafer pair is presented in Figure 23. In the IR image only the largest, particle-induced voids can be detected. The drawback of acoustic microscopy compared to IR inspection is the necessity to do bond annealing before measurement in order to avoid debonding of the wafers when exposed to water. Another drawback is throughput; IR inspection takes only a couple of seconds, whereas SAM C-scan inspection of a 4'' wafer takes a couple of minutes.

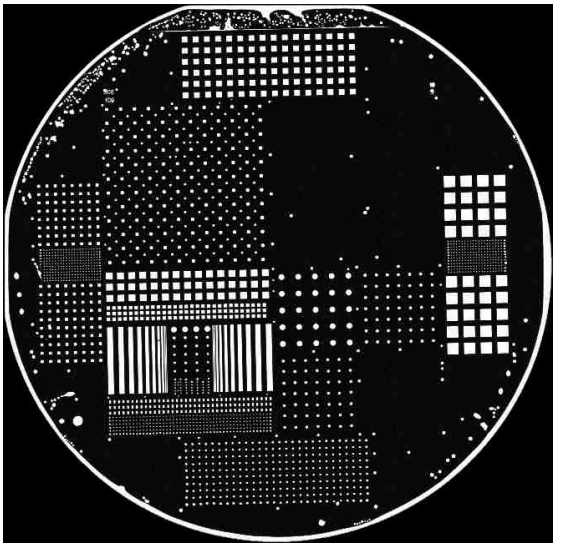

Figure 22. SAM image of a bonded wafer pair showing patterns on a handle wafer's 30 nm thick oxide layer.

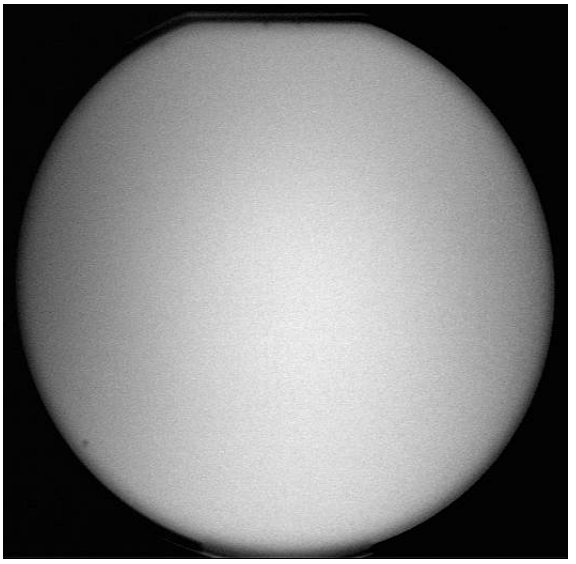

Figure 23. IR image of the same wafer as in Figure 22. 30 nm high patterns are too small to be detected by IR transmission.

4. Applications of Wafer Bonding

Wafer bonding is becoming an increasingly common method in IC- and MEMS manufacturing. It is no longer limited to substrate manufacturing, but is also used as a method to fabricate 3D MEMS devices [40], 3D integration of layers containing different devices [41], and device encapsulation [42]. However, the most common application for wafer bonding is still the fabrication of silicon-on-insulator (SOI) substrates. Direct bonding is also used for bonding of more exotic materials than silicon, such as GaAs, InP, glass, quartz, sapphire etc. Basically any material with a smooth enough surface (< 1 nm RMS) can be directly bonded.

4.1 Silicon-on-Insulator (SOI)

Silicon-on-insulator wafers consist of a silicon handle wafer, an oxide layer and a silicon device layer (SOI layer) (Figure 24). SOI wafers are basically divided into two categories: thin film SOI (device layer thickness a few nm – 2 μm) and thick film SOI (5 μm – 200 μm). Thin film SOI is mainly used in IC fabrication and thick film SOI is more for MEMS purposes. The thinning methods for these two thickness areas are quite different. However, the bonding process is quite similar.

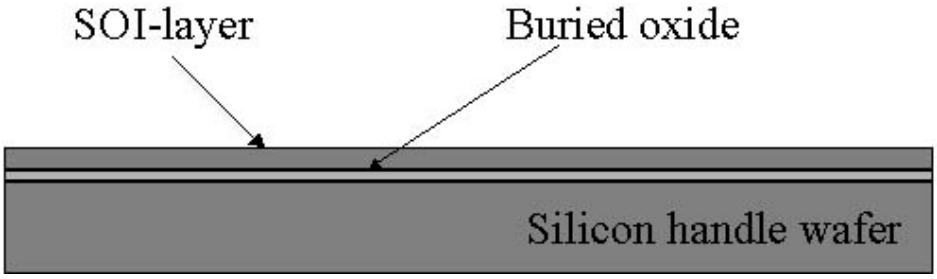

Figure 24. Typical SOI wafer. The buried oxide thickness is usually 50 nm – 3 μm and the SOI layer thickness 50 nm – 150 μm.

4.1.1 Thin film SOI

Thin SOI wafers are mostly made using ion implantation. An old method was to implant oxygen to a certain depth into the silicon wafer and then induce an oxidation process inside the silicon wafer by annealing. The process was called separation by implanted oxygen (SIMOX). However, this process had problems with implantation-induced dislocations [2] and it was also very expensive. Because of these problems, SIMOX has been commonly replaced with wafer bonding-based fabrication methods.

The most common method for thin SOI fabrication is Smart Cut™. In this method the device wafer is implanted with hydrogen before bonding. Bruel found that implanted hydrogen forms blisters (Figure 25) during annealing. [43]

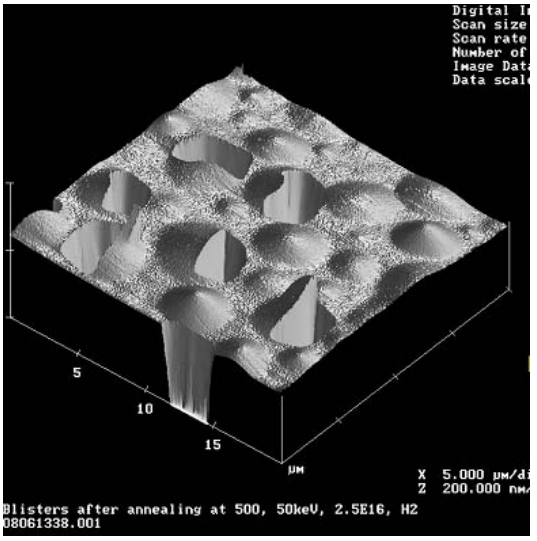

Figure 25. Exploded blisters after annealing hydrogen implanted silicon at 500°C (Picture courtesy of Kimmo Henttinen, VTT).

If another wafer is bonded to the implanted wafer, the blisters cannot "explode" but form lateral "platelets". These platelets grow in size with increasing annealing temperature. The crack is formed at the far end of the implantation damage [44, 45]. The splitting temperature is influenced by the hydrogen concentration and it can be reduced by implanting a dose of boron [**Publication F,** 46]. Boron is assumed to trap hydrogen, increasing local hydrogen

concentration and thus lowering the temperature required for blister or platelet formation [47].

It is also possible to use mechanical instead of thermal splitting. In this case the bond strength at the bonded interface should be higher than the strength in the implanted region. Figure 26 shows the development of surface energies for a plasma-activated and bonded interface and for an implanted region as a function of the annealing temperature [**Publication F**].

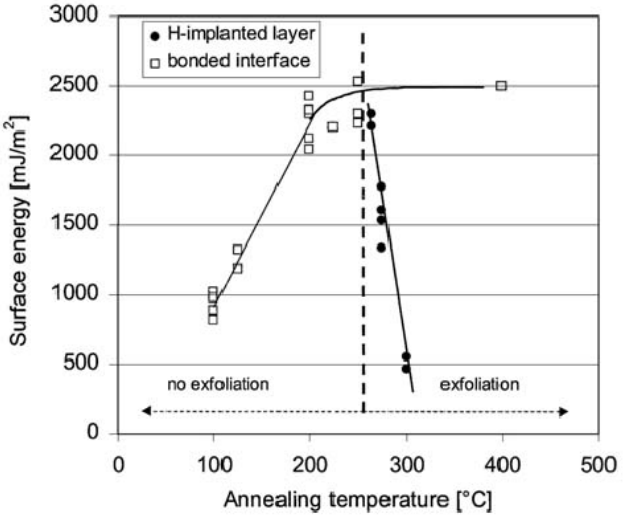

Figure 26. Measured surface energies for the bonded interface and for the H-implanted region as a function of annealing temperature. Annealing time was 2 h.

Mechanical splitting is induced by inserting a razor blade between the wafers. The wafer pair is separated from the weaker interface, so achieving high bonding energies already at low temperatures is necessary for demanding applications. One such case is silicon-on-quartz, where the annealing temperature is limited because of a great difference in the coefficients of thermal expansion (CTE) [48]. In this example, the use of boron had to be avoided, because the final application was in thin film transistors, and boron implantation changes the electrical properties of the silicon layer. Therefore, a process was applied that involves high-dose hydrogen implantation, plasma activation-based low temperature bonding and mechanical exfoliation. [48]

After splitting, the surface roughness is 5–10 nm RMS and therefore the surface should be polished before device fabrication. The device wafer can be polished and recycled over and over in the process. If the layer needs to be thinned down further, this can be done using thermal oxidation and oxide etching without loosing thickness uniformity. The process is depicted in Figure 27. The Smart Cut™ process patent is owned by SOITEC. They fabricate thin film SOI with various thicknesses (50 nm – 100 µm) on wafer sizes up to 300 mm.

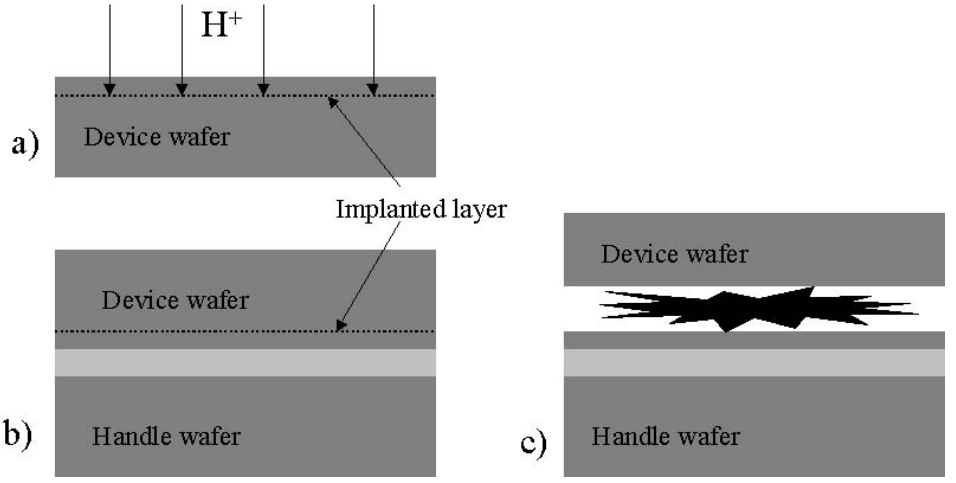

Figure 27. Smart Cut™-process: a) The device wafer is implanted with hydrogen b) The device wafer is bonded to an oxidized handle wafer, c) Thermal annealing strengthens the bond and induces splitting in the implanted region.

Canon have their own method for fabricating thin film SOI. They grow a porous layer of silicon on the device wafer using a special process, on top of which it is possible to grow epitaxially single crystalline silicon. Once the epitaxial layer is polished, it is bonded to the handle wafer and the layer can be released from the weakest region, which in this case is the porous layer. Their mechanical release process is based on a water jet. [49]

Thin SOI wafers provide many advantages for IC fabrication. The switching speed of circuits fabricated on SOI is increased by 20–50% compared to circuits fabricated on a bulk Si wafer. The required operation voltage is lower in ICs on SOI than in ICs on a bulk silicon wafer, which decreases power consumption and chip heating. The circuit packaging density is also increased due to simplification of the lateral and vertical isolation structures.

4.1.2 Thick film SOI

Thick film SOI is replacing conventional Si wafers as the start substrate for microelectromechanical systems (MEMS). The advantage of SOI substrates is that the buried oxide layer can be used as sacrificial layer, and by etching it different types of diaphragms, films and beams can be released.

Thick film SOI wafers are made by bonding, grinding and polishing. Before grinding, the edges of the bonded stack are usually ground to avoid edge chipping. The reason for edge chipping is the unbonded area near the edge due to the edge roundness of the bonded wafers. Grinding is usually done in two steps; the first is coarse grinding to remove most of the material, the second is fine grinding (10–25 µm removal) to reduce the depth of the grind lines and reduce the sub-surface damage.

A CMP or etching step is used to remove sub-surface damage. The damage layer causes stress to the SOI film and therefore, if not removed, may cause breakage of the MEMS device. CMP is also used to remove the grind lines and create a smooth surface. The CMP causes thickness variation and thus silicon removal with CMP should be minimized.

4.1.3 Intermediate SOI (device layer thickness 2–5 µm)

SOI wafers with thicknesses between 2 and 5 µm are difficult to find, because conventional thinning methods used in thick SOI fabrication cause large procentual thickness variation (0.5 µm TTV is 10% variation for 5 µm SOI layer, 25% for 2 µm SOI layer). Therefore, these layers with intermediate thicknesses are mainly made using either etching thick film SOI with etch stop layers or by growing epitaxially more silicon on thin film SOI.

4.1.4 Strained silicon-on-insulator (sSOI)

Carrier mobility can be improved by having the device layer silicon under tensile stress. [50]. This improves the performance of CMOS circuits fabricated on strained silicon. This improvement can be combined with the advantages of

SOI (e.g. reduced junction capacitance) by fabricating strained silicon-on-insulator (sSOI) substrates.

The strain in silicon is typically introduced by epitaxially growing silicon on a material with a larger lattice constant, such as SiGe. sSOI is usually fabricated by first fabricating a SiGe-on-insulator (SGOI) substrate. Three different methods have been reported for SGOI fabrication: SIMOX, Ge-condensation and wafer bonding and thinning [51].

In SIMOX the buried oxide is fabricated by implanting oxygen ions into the substrate, and during subsequent high temperature annealing the implanted oxygen reacts with silicon and forms a buried SiO_2 layer. However, this method is only applicable with low Ge concentrations due to thermal instability of SiGe at elevated temperatures [51]. Since the strain-induced hole mobility is expected to continue to improve up to about 30% Ge concentrations, other approaches for SGOI preparation have been developed.

One method for fabricating SGOI substrates with a higher Ge concentration than obtained with SIMOX is the Ge condensation method. Here a low Ge concentration SiGe layer is grown on SOI. When SiGe is exposed to an oxidant, a mixed oxide of SiO_2 and GeO_2 is formed. At high temperatures, the GeO_2 formation is replaced by SiO_2 formation and the Ge concentration at the SiGe layer increases, as shown in Figure 28. The oxidation temperature must be kept below the melting point of SiGe alloy. [51]

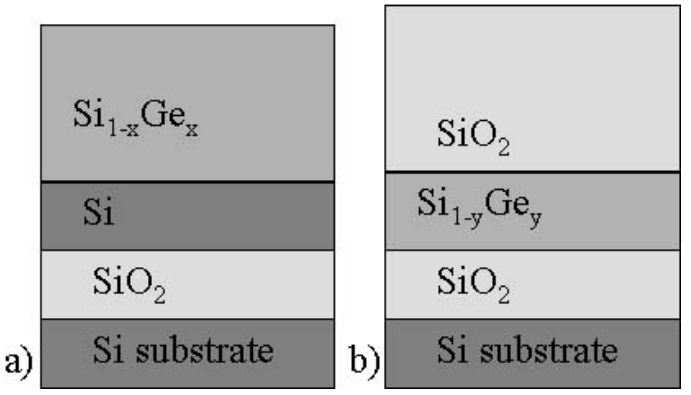

Figure 28. a) Low Ge content SiGe on SOI, x<0.1 b) At high temperature oxidation SiO_2 is formed and Ge diffuses into the underlying SiGe, increasing its Ge content, y>x [51].

A third approach to SGOI fabrication is to use wafer bonding combined with a thinning method. In this case the strain-relaxed SiGe layer is grown on a silicon wafer by ultra high vacuum chemical vapour deposition (UHVCVD). The SiGe epilayer is then polished and bonded to an oxidized silicon wafer. Thinning methods are similar to conventional SOI fabrication, including etch back (using SiGe-layer as an etch stop), grinding and polishing as well as ion-implantation based methods.

Once the SGOI substrate is ready, a thin silicon layer is grown on top of it. The silicon is strained due to a larger lattice constant of SiGe. One possible process flow for the fabrication of strained Si-on-SiGe-on-insulator with wafer bonding and ion-cut is depicted in Figure 29 [50].

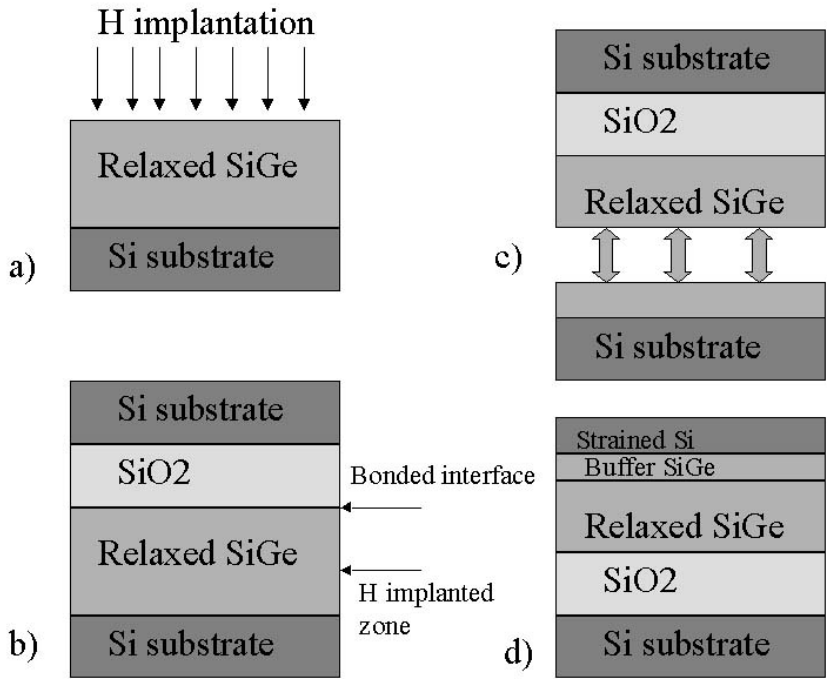

Figure 29. a)The SiGe-on-Si wafer is implanted with hydrogen b) The wafer is bonded to the oxidized Si wafer c) Thermal ion-cut enables SiGe layer transfer from the SiGe-on-Si wafer to the oxidized Si wafer, resulting in an SiGe-on-insulator structure d) Growth of thin Si layer on SGOI substrate. Si is strained due to a lattice mismatch between Si and SiGe. [50]

Having sSOI substrates with a buried SiGe layer, however, poses several challenges to further processing steps. The SiGe-strained Si stack is difficult to make below a thickness of 30 nm. Presence of SiGe layer alters the dopant diffusion and changes the contact metallurgy reactions. Ge may also diffuse into the sSOI layer. Therefore, it would be advantageous to have sSOI wafers without buried SiGe-layer.

Langdo et al. have fabricated SiGe-free sSOI substrates by wafer bonding and layer transfer [52]. They first fabricated a substrate containing a strained Si layer on SiGe-on-Si substrate (Figure 30a). They then implanted hydrogen through the strained Si layer (54 nm thick) into a $Si_{0.68}Ge_{0.32}$ layer to a depth of ~350 nm below the strained Si. Next the wafer was bonded to the oxidized silicon wafer and annealed to strengthen the bond and induce hydrogen splitting (Figure 30b).

The $Si_{0.68}Ge_{0.32}$ layer film was then removed by a combination of low temperature steam oxidation and dilute HF etching. The final result was SiGe-free strained silicon on the insulator structure (Figure 30c). [52]

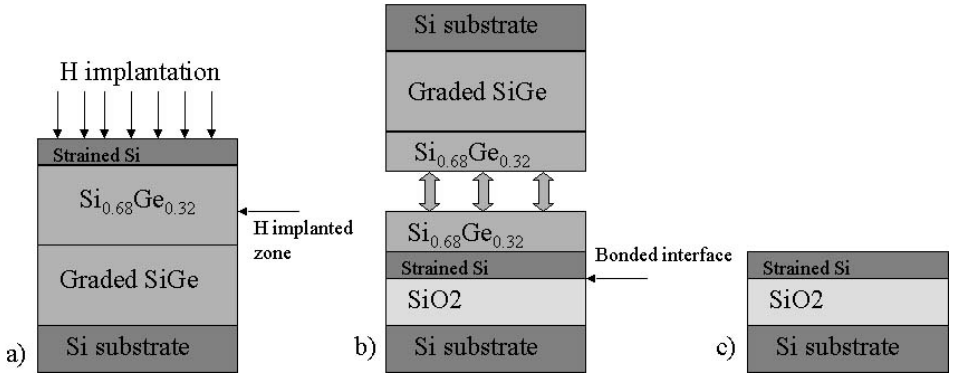

Figure 30. Fabrication process for SiGe-free strained Si substrates. a) The SiGe layer is hydrogen implanted through the strained Si layer b) Si on the SiGe-on-Si substrate is bonded to the oxidized silicon wafer and thermal ion-cut is used to transfer the strained silicon layer and part of the SiGe layer c) The SiGe layer is removed by steam oxidation and dilute HF etching. [52]

4.1.5 Cavity SOI

In order to allow greater freedom in MEMS designing, there is increasing interest in SOI wafers with buried structures (cavities, different support structures). A fabrication process for such wafers is presented in **Publication C**. Fabrication of the pre-patterned SOI wafers requires cavity fabrication on one or both of the wafers before bonding. During cavity fabrication, special care should be taken to keep the surfaces smooth and particle free. It should be emphasized that there are a wide range of different MEMS devices. Different MEMS devices place different demands on pre-patterned SOI wafers concerning cavity location (top, bottom or on both wafers), oxide location (top, bottom, both, on cavity), cavity shape and size, possible support structures (number, shape, size, locations), cavity atmosphere etc. Therefore, the fabrication process for pre-processed SOI also depends on the device. One approach to cavity-SOI fabrication is presented in Figure 31.

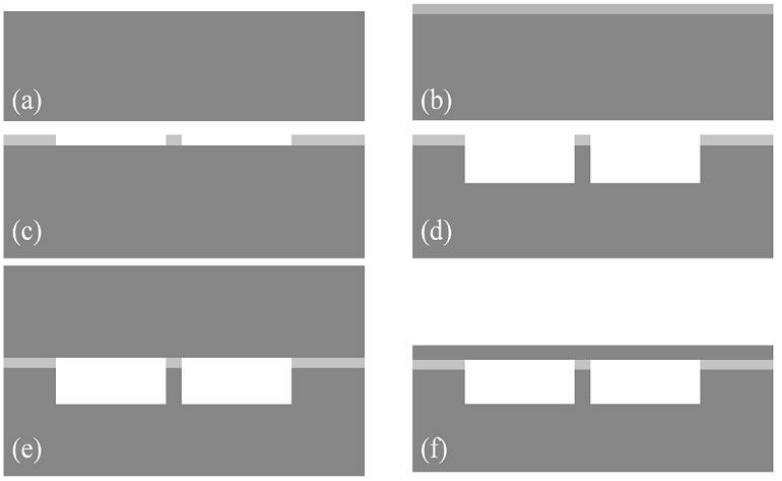

Figure 31. Fabrication process for cavity SOI a) Silicon handle wafer b) Thermal oxidation c) Patterning of the oxide d) Deep silicon etching e) Bonding of the cap wafer f) Thinning of the cap wafer.

After cavity fabrication and possible cleaning steps, the cap wafer and handle wafer are bonded. In most cases the bonding result has been good, but with a large cavity fraction (small bonded area compared to total wafer area) and air as a bonding atmosphere, large voids could be detected with SAM (Figure 32). When either a larger bonded area or vacuum atmosphere was used, no such void problem was detected (Figure 33).

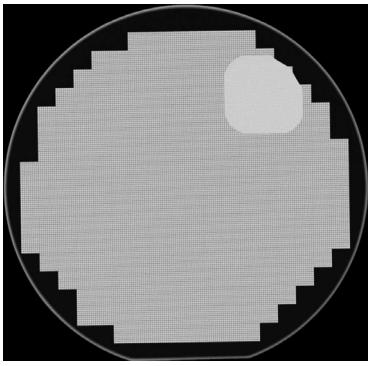

Figure 32. SAM image of air-bonded wafer pair with a cavity fraction of ~80% (500 µm wide square cavity surrounded by 55 µm wide bonding rim).

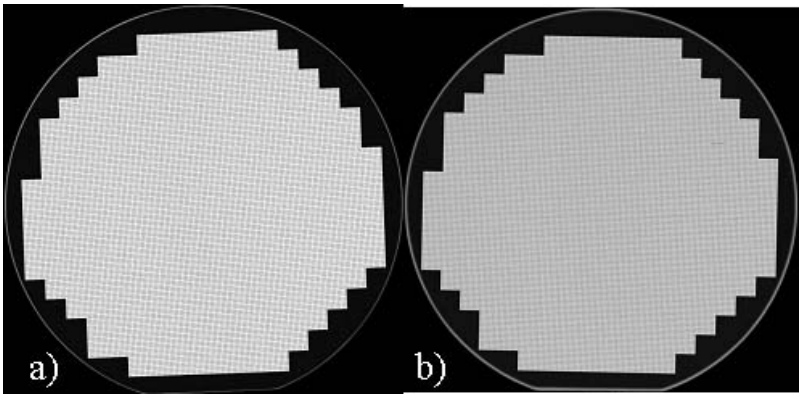

Figure 33. a) SAM image of air-bonded wafer pair with a cavity fraction of ~36% (100 µm wide square cavity surrounded by 55 µm wide bonding rim). b) Vacuum-bonded wafer pair with a cavity fraction of ~80% (500 µm wide square cavity surrounded by 55 µm wide bonding rim).

Vacuum bonding resulted in slightly higher bond strength than air bonding [**Publication C**]. Tests were also performed to study whether small areas can be properly bonded by bonding handle wafers with cavities and small support pillars into the cap wafer and then removing the handle wafer. SEM investigation showed that 100 µm wide pillars were still standing on the cap wafer after handle wafer removal (Figure 34). This means that the support pillar is properly bonded to the cap wafer. Even support pillars with 20 x 20 μm^2 area were found to be well bonded.

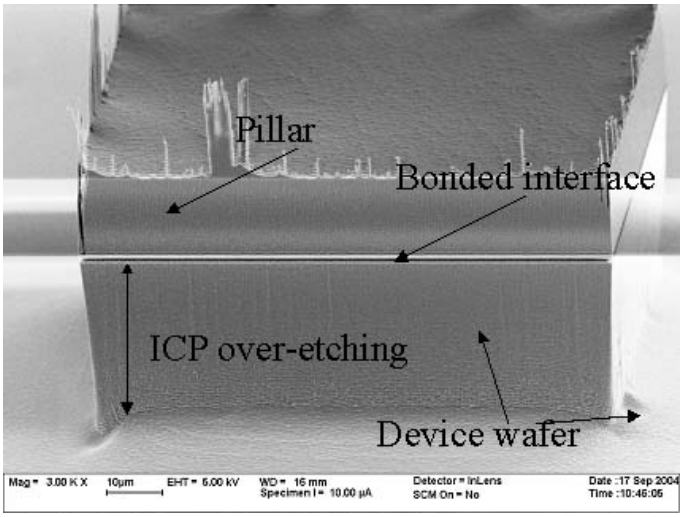

Figure 34. SEM image of 100 µm x 100 µm pillar bonded to the device wafer. The handle wafer is removed with ICP etching.

In cavity SOI wafers, the location of the oxide varies depending on the final application. The oxidation can be done on the cap wafer, the handle wafer before patterning, and the handle wafer after patterning. The first process is straightforward, as the cap wafer is unpatterned and the oxide surface is flat and smooth after thermal oxidation. In the second process care should be taken to avoid roughening of the oxide during cavity fabrication by having a protective layer on top of it, e.g. photoresist. However, in some applications it is desirable to have oxide as well on the bottom of the cavity. The thermal oxidation rate is different in convex and concave corners than on flat surfaces. The oxide profile was measured in the area next to the cavity after cavity fabrication and thermal oxidation with a Veeco Dektak surface profilometer. On these wafers small oxide bumps were detected (width 1–5 µm, height 5–15 nm) next to the cavity (Figure 35). However, these bumps did not cause voids large enough to be detected with SAM or SEM. [**Publication C**]

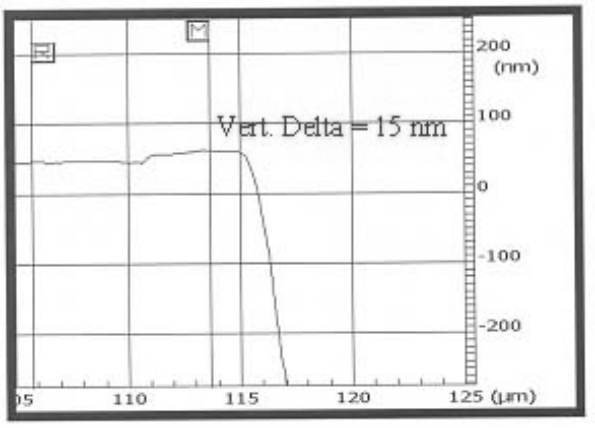

Figure 35. Dektak surface profilometer image of oxide shape next to the cavity.

The next step in cavity SOI fabrication is mechanical thinning. The thinning procedure consists of two grinding and one polishing step. The forces present in the grinding and polishing processes press the film in unsupported areas (areas above the cavities) downwards, causing variation in the SOI film thickness [**Publication C**].

After thinning, the device structure can be defined and released using lithography and ICP etching. Figure 36 shows a MEMS delay line fabricated on a cavity SOI wafer.

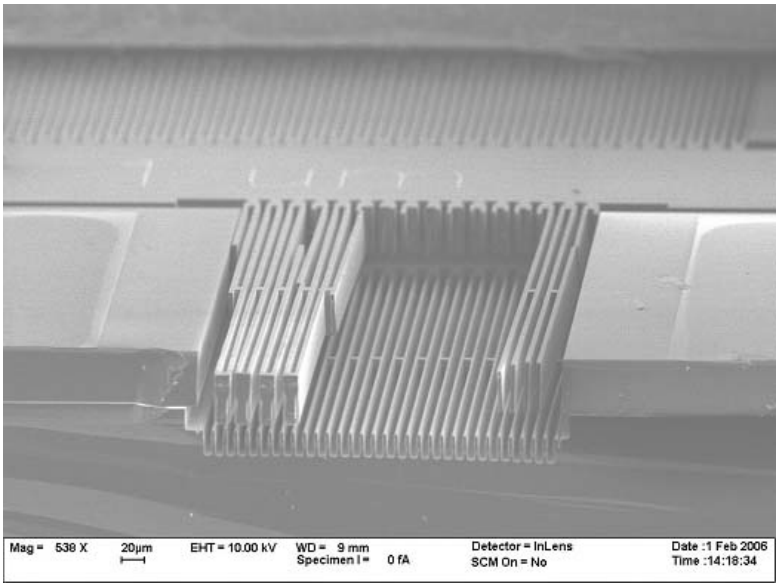

Figure 36. SEM image of a delay line fabricated on cavity SOI wafer. (Picture courtesy of James Dekker, VTT.)

4.1.6 Multi-layer SOI

Some applications may require substrates with more buried layers than just an insulating oxide layer. For example, in some cases it is advantageous to have a buried conductive layer inside the oxide. A boron-implanted polysilicon layer is one such option. In the process (presented in Figure 37) the cap wafer and the handle wafer are thermally oxidized. The silicon layer is then deposited on the handle wafer using LPCVD. The silicon is deposited in the amorphous state, because polishing of amorphous silicon to the surface roughness required for direct bonding is much easier than polishing of polycrystalline silicon. The amorphous silicon is then ion implanted with boron and polished with a short CMP step (removal ~50 nm). It was decided to carry out ion implantation before CMP, as boron implantation was found to roughen the polished surface from ~1 Å RMS to about ~2.5 Å RMS. The wafers were bonded and annealed at 1100°C for 2 hours.

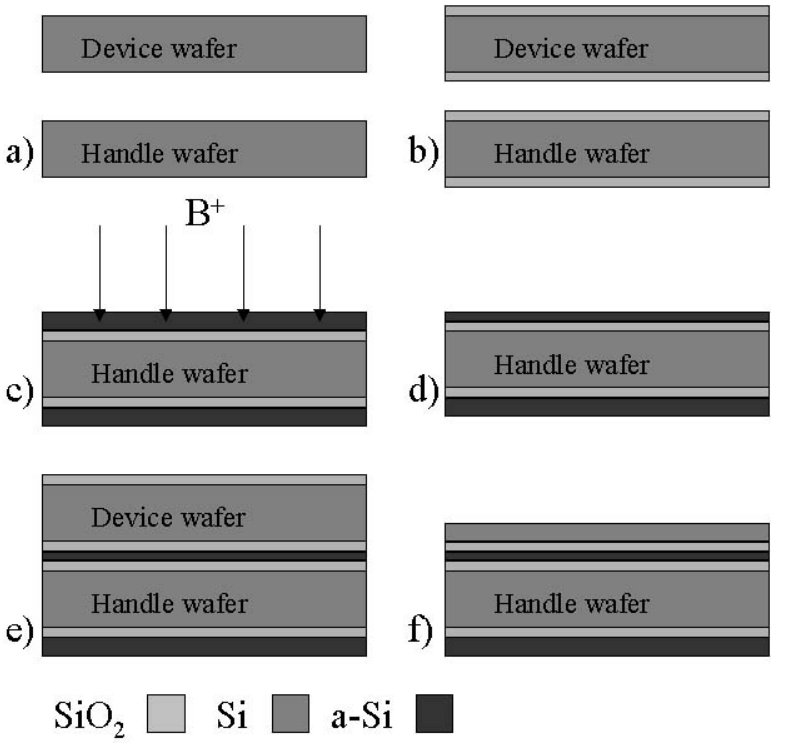

Figure 37. a) Start wafers are standard silicon wafers b) The wafers are thermally oxidized c) The amorphous silicon layer is deposited on the handle wafer with LPCVD and the silicon layer is boron-implanted d) The prime side a-Si is polished with CMP e) The handle wafer is bonded to the device wafer and high-temperature annealing (1100°C) converts a-Si to polycrystalline Si f) The device wafer is thinned to the desired SOI thickness.

Despite the silicon turning from the amorphous state to the polycrystalline state during high temperature annealing, no voids were detected at the bonded interface (Figure 38). The bond strength was also excellent, as can be seen from the SEM image in Figure 39, which shows a polysilicon beam after buried oxide etching of 10 minutes in 50% HF. The etch rate of ~1.5 µm/minute at the bonded interface equals strong bonding (**Publication D**).

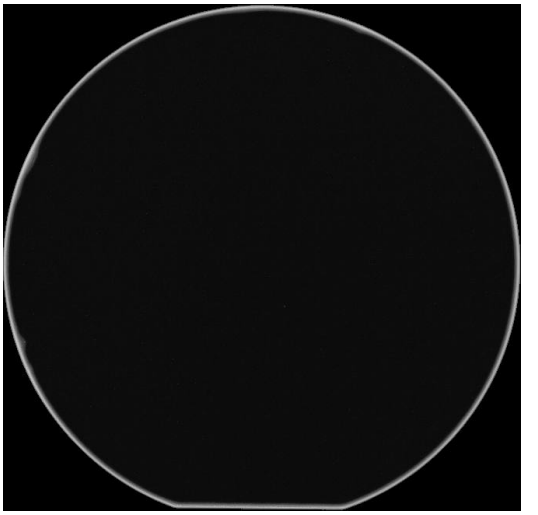

Figure 38. SAM image of a bonded Si-ox-aSi-ox-Si stack.

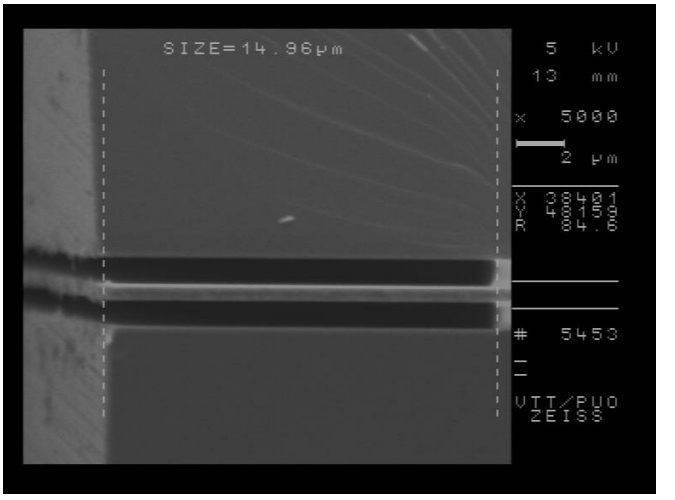

Figure 39. SEM image of a polysilicon beam after buried oxide etching (10 min, 50% HF). The etch rate of both oxides is equal and ~1.5 µm/min, which indicates strong bonding.

4.2 Heterogeneous integration

Heterogeneous integration means the joining of wafers of different materials. Various materials, such as GaAs, InP, Quartz, Glass, Sapphire, SiC, and GaN have been successfully bonded. In such bonding, the same requirements for smooth and clean surfaces apply, but there are further restrictions in the bonding process. In the bonding of dissimilar materials, there is usually a difference in the coefficients of thermal expansion (CTE), which causes stresses during bond annealing. Therefore, the annealing temperatures are usually limited to lower regions than in silicon-to-silicon bonding. Sometimes polishing of the material to be bonded is too difficult or expensive (e.g. SiC is difficult to polish) and an intermediate layer is needed. A good option is then to use a material with known properties and bonding behaviour. Therefore, most common intermediate layers used in direct bonding are polished CVD-SiO_2-layers.

An example of a difficult CTE mismatch is silicon-on-sapphire (SOS) wafers. When bonding silicon to sapphire, the annealing temperature should be kept below 150°C to avoid cracking of the silicon wafer. This causes problems, for example, when trying to make thin film SOS wafers. Low annealing temperature restricts the use of Smart Cut™ after the final bonding. For this purpose a temporary wafer bonding has been developed. In this method the device layer is first fabricated on a temporary handle wafer and then transferred to the final substrate. This method requires controlling of the bond strength during both bonding steps to keep the first bonded interface weaker than the second interface. If the difference between the bond strengths is large enough, the layer can be mechanically transferred from one handle wafer to another. The required steps for this method are shown in Figure 40. The methods for controlling the bond strength are explained in more detail in Chapter 5 and **Publication E**.

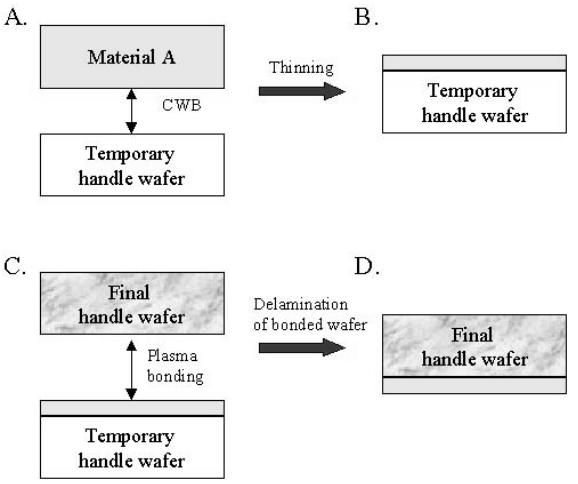

Figure 40. Principle of temporary wafer bonding for high CTE-mismatched materials integration a) Bonding of desired thin film material to temporary handle wafer b) Thinning of the material with ion-cut or mechanical thinning and polishing to make the surface smooth enough for direct bonding c) Low-temperature bonding of the layer to the final handle wafer d) Delamination at the interface between the thin film and temporary handle wafer.

4.2.1 Compliant substrates

Nowadays heteroepitaxy is a common method for fabricating substrates for electronic and optoelectronic purposes. If the layers have the same lattice constant as the substrate, or if the thickness of the layers is kept below their critical thickness, no defects are formed during growth. If the critical thickness is exceeded, the epitaxial layers relax plastically by forming dislocations at the interface. Lattice and thermal mismatches are the main causes of defect formation [53]. These dislocations cause deterioration of the optical and electrical properties of the structure, therefore the amount of dislocations should be minimized. However, this has proved difficult with standard epitaxy. This problem can be avoided by using a compliant substrate. This kind of substrate should accommodate the misfit by deforming elastically or plastically in a zone localized near its top surface, right below the heteroepitaxial layer [54]. The idea of elastic relief was first introduced by Lo [55]. According to his hypothesis, the template as a whole can shrink or expand by slipping along the weak interface.

Several authors have rejected the hypothesis; a more reasonable one is plastic relief of the epitaxial film [56]. In plastic relief the film relaxes by slipping on its crystallographic slip planes, where the slip direction is oblique to the film plane. It may also be that relaxation occurs due to climbing of dislocations instead of slip. However, the final answer regarding the theory behind compliant substrates is still under debate.

There are various methods for fabricating compliant substrates and some of them require wafer bonding. To have an efficient compliant substrate, some criteria should be fulfilled: the layer on which the epitaxy is performed should be as thin as possible, the layer should remain flat and planar and if it is supported, the layer should be free to glide and supporting media should be soft [57].

The first compliant substrates were free-standing thin films, actually GaAs membranes supported at several points (Figure 41a) [58]. However, warping of the film due to stress induced by the deposited epilayer is a serious problem and the method is no longer in use. Another reported freestanding film structure has an InGaAs membrane standing on a central pedestal [59]. However, this structure is fragile and the surfaces are not planar.

Compliant layers when implementing the SOI technique have also been reported (Figure 41b) [60]. In this method the oxide layer is supposed to behave as a viscous layer and a frictionless interface. During epitaxial growth the viscous layer flows, allowing the misfit strain to decrease [61]. As an example of such a compliant substrate, Hansen et al. have reported $In_{0.40}Ga_{0.60}As$ growth on a 10 nm GaAs template on borosilicate glass on a GaAs mechanical host [62]. The viscous intermediate material can also be something else than glass oxide, for example indium.

The most popular option for compliant substrate fabrication has been the use of a twist-bonded layer (Figure 41c). In this method a thin layer of material is transferred to a mechanical host of the same material, but introducing a large twist angle between them. This method was first presented by Ejeckam et al. [63]. The layer is thinned down using either Smart Cut™ [43] or an etch-stop layer and etch-back [63, 54]. The twist-bonded substrate is considered to have a weak boundary due to a network of screw dislocations, which can accommodate the slip resulting from growth of a mismatched layer [53].

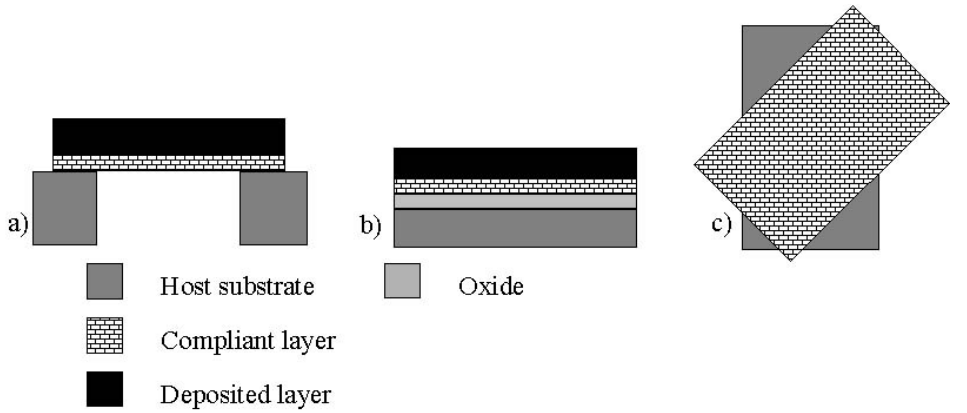

Figure 41. Different compliant substrates a) Free-standing thin film, e.g. GaAs membrane b) Compliant layer on viscous glass c) Twist-bonded layer.

With these different types of compliant substrates, the quality of heteroepitaxially grown layers has increased significantly. Compared with layers grown on ordinary substrates, the density of threatening dislocations has decreased significantly, the relaxation is less or comparable, and the layer thickness is no longer limited to the critical thickness but to a much higher thickness value [57]. While the use of heteroepitaxially grown layers on electrical and optoelectrical applications is increasing, the development of compliant substrates will remain a hot topic in substrate development research.

4.3 Wafer scale packaging

Packaging of MEMS devices is required for various reasons. The sensors are usually delicate components, the operation of which may be sensitive to particles or chemical contaminants. They may also require a specific operation atmosphere (vacuum, inert gas, certain pressure) to function as planned. The encapsulation process should be also cost effective, because nowadays packaging costs can contribute up to 90% of the total device costs. To reduce these costs, the packaging should be done at wafer level, enabling encapsulation of multiple devices on a single run. This can significantly reduce the packaging cost per chip.

Wafer-scale packaging is not a new approach in the MEMS industry. The most common methods are anodic bonding and glass frit bonding. These methods, however, have limitations such as high temperature (400–600°C) and a large bonding area. These processes also involve metals that are not compatible with ICs sometimes required with the MEMS device. Agilent uses gold seal bonding to encapsulate their devices [24] and Ziptronics uses covalent bonding for wafer-scale encapsulation [42].

Publication B examines methods for direct bonding of a silicon wafer to another silicon wafer containing MEMS devices at low temperature. To achieve strong bonding at low temperatures, plasma activation of wafer surfaces is used before contacting the wafers. The advantages of the plasma-activation based process over glass frit and anodic bonding are a lower process temperature, high throughput, IC compatibility and the possibility to have a small bonding rim. The problem with this method is that the areas to be bonded have to be very smooth and flat, which is usually not the case with processed wafers. Therefore, the device wafer usually needs planarization and/or polishing before direct bonding can take place.

There are three principal steps in the encapsulation of MEMS devices with direct bonding: Planarization and polishing (including surface protection during further processing), bonding itself, and fabrication of electrical contacts into the package.

4.3.1 Planarization and polishing

To make the handle wafer bondable, it needs to be planar and smooth in the areas to be bonded. For this purpose three different approaches were tested: a) covering of the whole handle wafer with thick CVD-oxide, followed by global planarization and smoothening (Figure 42); b) planarization, polishing and protection of the areas to be bonded before actual device fabrication (Figure 43); c) covering of the whole handle wafer with CVD oxide, removal of the oxide from the top of the device and polishing of the elevated oxide areas (Figure 44).

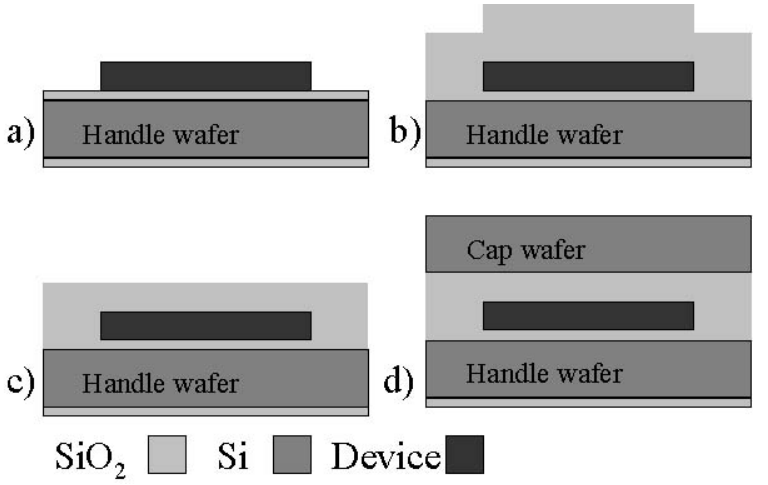

Figure 42. a) Device fabrication on oxidized wafer b) Covering of the device with CVD oxide c) Planarization and polishing d) Bonding of cap wafer.

The first proposed method can be done with conventional oxide polishing processes, but it requires a large amount of extra oxide polishing before the step, caused by the buried device, is planarized. Typically the required removal is about twice the height of the hill. By using polishing pads with fixed abrasives, the main part of the removal takes place at the elevated areas and the 800 nm high surface step can be planarized by removing less than 1000 nm of oxide [**Publication B**].

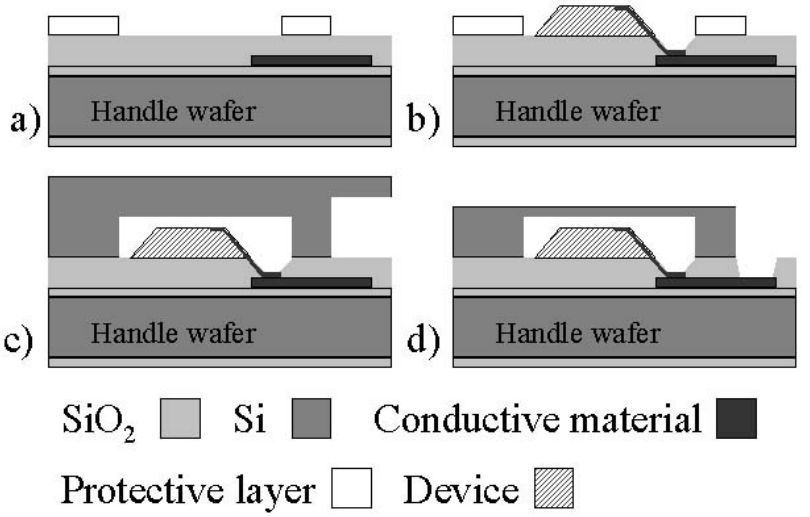

Figure 43. a) Fabrication of conductive path on thermally oxidized Si, CVD oxide deposition, planarization and polishing and deposition and patterning of protective layer b) Device fabrication and contact fabrication from device to conductive path c) Removal of protective layer and aligned bonding to patterned cap wafer d) Thinning of cap wafer for contact opening.

In the second proposed method, the surface of the oxide layer is polished before device fabrication. The areas to be bonded can be polished with a conventional oxide polishing step. The difficult part in this method is to protect the oxide surface during device fabrication so that no roughening of the oxide takes place. The protective layer should also be selectively removable from the top of the oxide. Molybdenum is a good protective layer, for example during release etching with HF, and it can be selectively removed from the oxide surface with mild SC-1 cleaning (NH_3:H_2O_2:H_2O solution). If buffered HF is used for release etching, then also standard photoresists can be used for surface protection. The resist can be removed with various solvents and developers without roughening the oxide surface. With complex devices this method is difficult or impossible to use, because it is hard to find a protective material that could withstand all the various process steps and still be easily removable from the oxide surface afterwards.

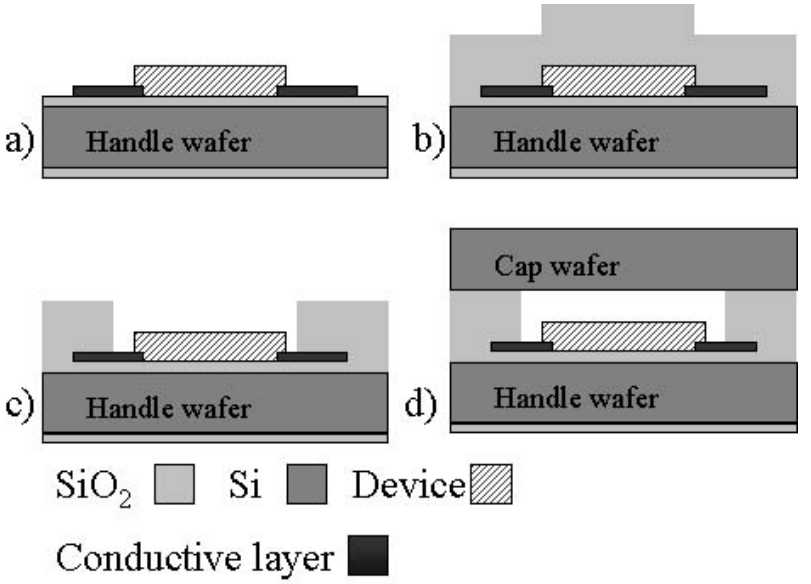

Figure 44. a) Device and conductive path fabrication b) Covering of the device with CVD oxide c) Oxide etching from top of the device and polishing of elevated oxide areas d) Bonding to cap wafer.

The third option is to fabricate the device first, cover it with CVD oxide, remove it from the top of the device, and then polish the areas to be bonded. With typical polishing processes the problem is rounding of the corners of the oxide "walls", which especially with a narrow bonding rim areas drastically reduce the area to be bonded (Figure 45b&c). By again implementing the fixed abrasive polishing process, the elevated oxide areas can be polished without detectable edge rounding (Figure 45d).

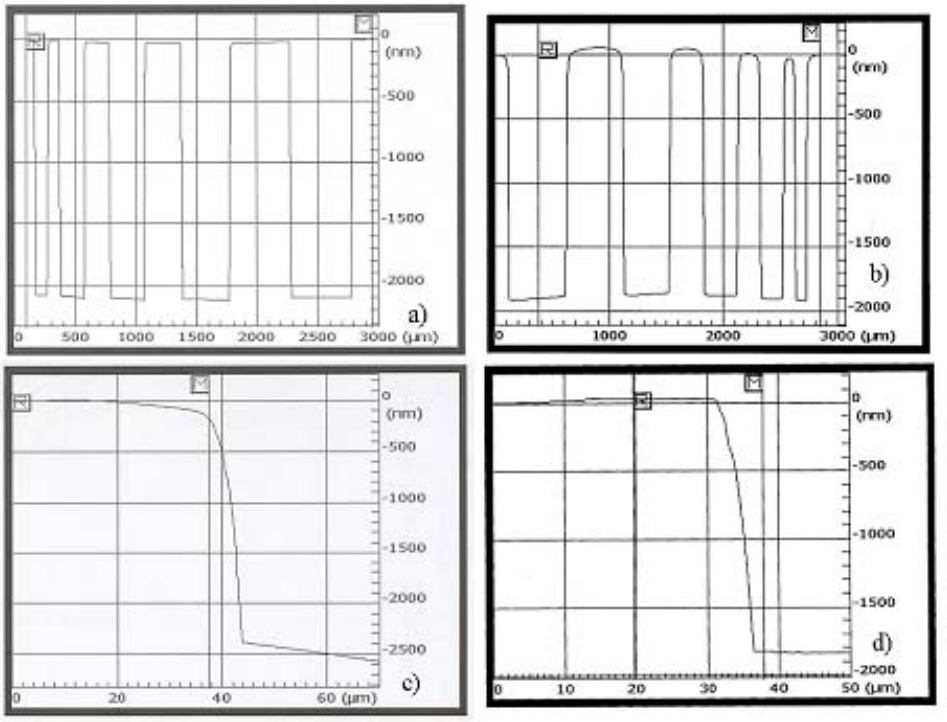

Figure 45. Surface profiles of elevated oxide areas a) After patterning b) After conventional oxide polishing process c) Oxide pillar profile after conventional oxide CMP d) Oxide pillar profile after fixed abrasive polishing process.

The encapsulation process needs to be decided upon already when designing the MEMS and its fabrication process.

4.3.2 Direct bonding of MEMS wafer

Direct bonding of wafers containing MEMS devices must in most cases be carried out at low temperature. The temperature of 1100°C needed for the high-temperature bonding process is too high for possible metallizations and other temperature sensitive parts, and also causes outgassing (and void formation) from the CVD oxides. Therefore, plasma activation should be used for both wafer surfaces to achieve strong bonding already at 200°C. In cases where the cap wafer is patterned, aligned bonding should be used.

The main thing to remember in direct bonding of wafers containing MEMS is the same as with any other direct bonding processes: the areas to be bonded must be smooth and clean. Therefore, it is important to highlight again the need for good CMP processes and the importance of having particle-free processes.

4.3.3 Fabrication of electrical contacts

In **Publication B** two different methods for fabrication of electrical contacts are presented. The first possibility is to use a patterned cap wafer which contains wells for contact opening. The wells are aligned during bonding above the contact pads, and during cap wafer thinning the wells are opened and a path to the contact pads is created (Figure 43). The encapsulated device can then be contacted to the next level, for example by wire bonding (Figure 46).

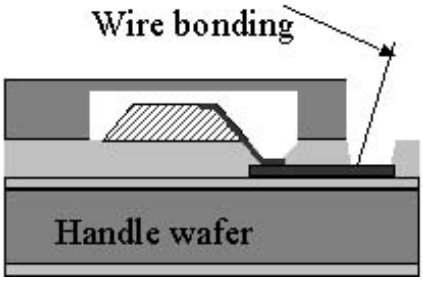

Figure 46. Contact fabrication with wire bonding for encapsulated device, continuation of the process presented in Figure 43.

The second approach is to use a dicing saw for the contact opening. The bonded cap wafer is first thinned down to <100 µm thickness. Next the v-shaped dicing blade is used to cut through the remaining handle wafer, slightly penetrating the contact pads. After this, a layer of conductive material, e.g. molybdenum, is deposited onto the v-groove and patterned (Figure 47). Then, for example, solder bumps can be grown on top of the cap wafer to make the final contacts to the next level.

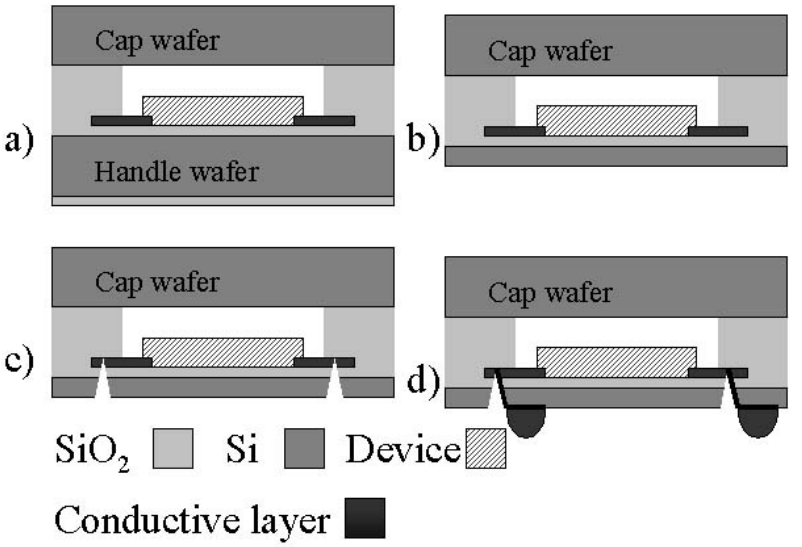

Figure 47. Contact fabrication with an encapsulated device, continuation of the process presented in Figure 44. a) Encapsulated device b) Thinning of the handle wafer c) V-groove sawing through the handle wafer and contact pads d) Conductive material deposition into the groove, patterning and solder bumping.

5. Temporary wafer bonding

Temporary wafer bonding means bonding of wafers to a temporary substrate so that they can easily be released afterwards. The principle of the method is presented in Figure 48 and explained in more detail in **Publication E**. The main principle of the method is that the crack propagates on the weakest interface. Therefore, if the bonding between the temporary holder wafer and the thin film is weaker than between the thin film and the final handle wafer, the film can be transferred to the final substrate. In practice, the difference should be significant (> 500 mJ/m^2) to avoid "jumping" of the crack from one interface to another.

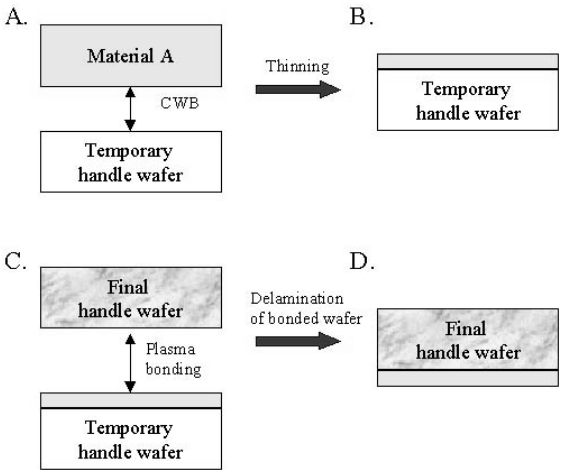

Figure 48. Principle of temporary wafer bonding a) Bonding of the desired thin film material to the temporary handle wafer b) Thinning of the material with ion-cut or mechanical thinning, and polishing to make the surface smooth enough for direct bonding c) Low-temperature bonding of the layer to the final handle wafer d) Delamination at the interface between the thin film and the temporary handle wafer.

The use of a temporary handle wafer is advantageous in many cases, such as wafer thinning and heterogeneous integration. For example, the quality of ion-cut silicon-on-glass (SOG) layers can be improved by removing ion implantation induced crystalline damage from the silicon film with high temperature annealing (at >1000°C). However, the glass substrate cannot withstand temperatures over 600°C and annealing before bonding is out of the question

because of the blistering effect. Therefore, the annealing should be done while the thin film is on a temporary handle (Si) wafer.

Temporary wafer bonding is also a usable method in fabrication of silicon-on-sapphire (SOS) wafers. Coefficients of thermal expansion (CTE) vary between silicon and sapphire so that the bonded silicon-sapphire wafer pair starts to break at temperatures over 150°C. However, the ion-cut requires annealing temperatures of ~200°C even if boron implantation and mechanical delamination are used [46]. The SOS wafer can be fabricated by first bonding the implanted silicon wafer to the oxidized silicon wafer without plasma activation, then doing a thermal ion-cut at 500°C. The transferred Si-layer is then polished to reduce the surface roughness from a split roughness of ~3 nm RMS to ~1 Å RMS. On a sapphire wafer, the PECVD oxide layer should be deposited to avoid void formation during bonding. PECVD oxide should also be polished to enable direct bonding. After ion-cut annealing, the bond strength of the temporary bonding is <1000 mJ/m^2. By using plasma activation on both surfaces and long annealing at 120°C, bonding between the sapphire and silicon layer could be made much stronger than the temporary bonding. After mechanical delamination, the surface roughness of the transferred layer was ~1 Å RMS, which is close to the surface roughness of the donor wafer at the start of the process. A thin film SOS wafer is shown in Figure 49.

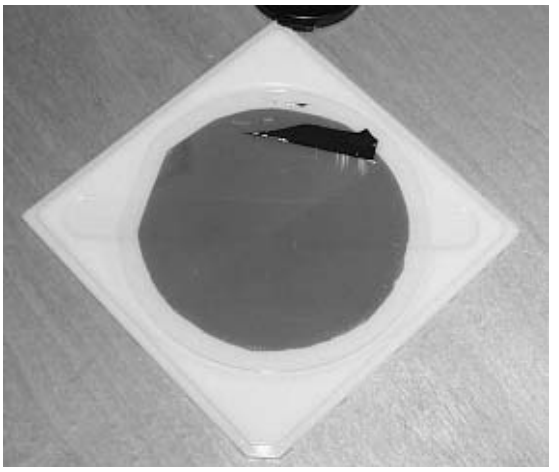

Figure 49. Picture of thin Si layer on a sapphire wafer.

The third application would be the fabrication of cavity SOI wafers (Figure 50). As mentioned in chapter 4.5.1, mechanical thinning induces thickness variation in diaphragms above cavities. Therefore, it would be advantageous (especially with thin diaphragm thicknesses) to do the thinning while the SOI layer is on the temporary substrate. Once the SOI layer is thinned to desired thickness, it is bonded to the patterned wafer and the temporary handle is removed by debonding.

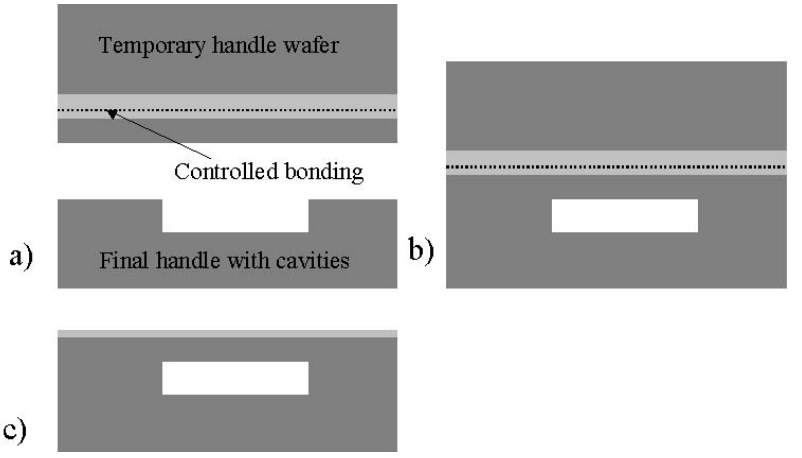

Figure 50. Temporary wafer bonding for cavity SOI fabrication a) Fabrication of SOI wafer with weak bonded interface b) Bonding of temporary SOI wafer to cavity wafer c) Mechanical delamination for removal of the temporary handle.

With this method it is also possible to carry out double side processing on the SOI layer. In this case one side of the SOI layer is processed while it is bonded to the temporary substrate. After bonding and debonding, another side of the SOI layer can also be processed. It is also possible to stack many processed SOI layers on the same handle wafer. [**Publication E**, 64]

5.1 Temporary wafer bonding using impurity outgassing of CVD oxides

Impurity outgassing of CVD oxides can be used for temporary wafer bonding. As mentioned in the chapter on bonding of CVD oxides, trapped impurities start to outgas when the bond annealing temperature exceeds the film deposition

temperature. Use of this behaviour in temporary wafer bonding was tested by bonding a PECVD oxide layer to a silicon wafer using plasma activation and annealing at 200°C. After this bonding procedure, the bond is strong. Then the cap silicon wafer was thinned down to a thickness of 20 µm by grinding and polishing. After polishing, the surface roughness of the SOI layer was low enough to enable good bonding. This SOI wafer was then bonded to a thermally oxidized wafer with plasma activation and the wafer stack was annealed at 500°C. At this temperature, the first made bonded interface weakens due to impurity outgassing (Figure 8b) while the second interface gets stronger. After annealing, a razor blade was inserted between the wafers and the crack propagated on the weaker PECVD oxide / silicon interface. After complete separation the 20 µm SOI layer was successfully transferred to another substrate. The new SOI wafer had some residual PECVD oxide on the surface due to crack propagation partly inside the CVD oxide layer. After short a HF dip the oxide residues were removed and the silicon surface was found to be smooth (~1Å RMS).

5.2 Temporary wafer bonding using surface roughening

The requirements for spontaneous direct bonding to take place are smooth and clean surfaces. The surface roughness limit is ~1 nm RMS and usually the silicon and oxide surfaces have a surface roughness of 1–2 Å RMS. **Publication E** describes how increasing the surface roughness within the limits of spontaneous bonding affects the bond strength. Similar results have been published by Moriceau et al. [64]

The optimal target would be to have a controlled surface energy (of 700–1200 mJ/m^2) for a temporarily bonded wafer pair after annealing at temperatures ranging from 200°C to 1100°C. This would enable thermal ion-cut at low temperatures and removal of the ion-implantation induced crystalline damage with high temperature annealing before moving the thin film to the final substrate. If the bond strength is below 500 mJ/m^2 at the thermal ion-cut temperature, instead of a thermal cut blistering and debonding will occur.

The experiments focused mainly on roughening of thermally grown oxide with plasma etching. After several tests, the best process for roughening the oxide

surface was found to be 30s CHF_3 plasma etching, which resulted in a surface roughness of ~8 Å RMS (Figure 51).

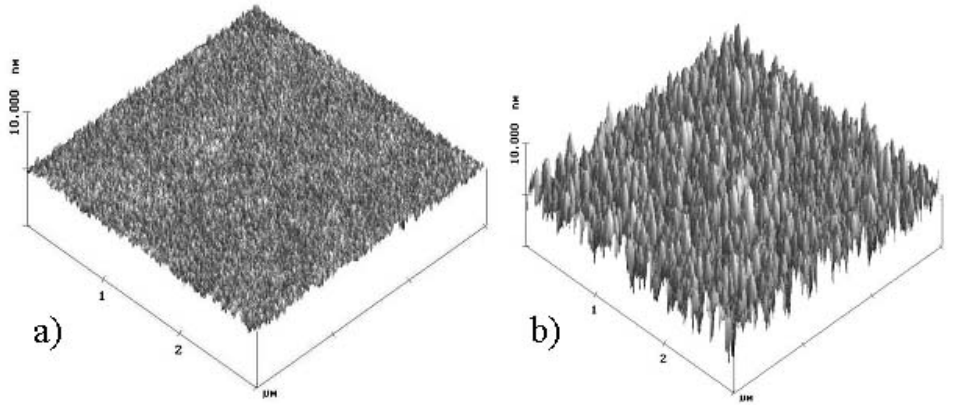

Figure 51. AFM images of a) as grown thermal oxide (RMS ~2 Å) and b) roughened thermal oxide (RMS ~8 Å).

Figure 52 presents measured surface energies for roughened and bonded SiO_2 wafers after annealing at different temperatures. Roughening of surfaces has a clear influence on the bonding energy and the bond strength remains at a level still debondable after annealing at 1100°C. However, with roughened surfaces the bond strength at temperatures < 500°C is not sufficient for thermal ion-cut.

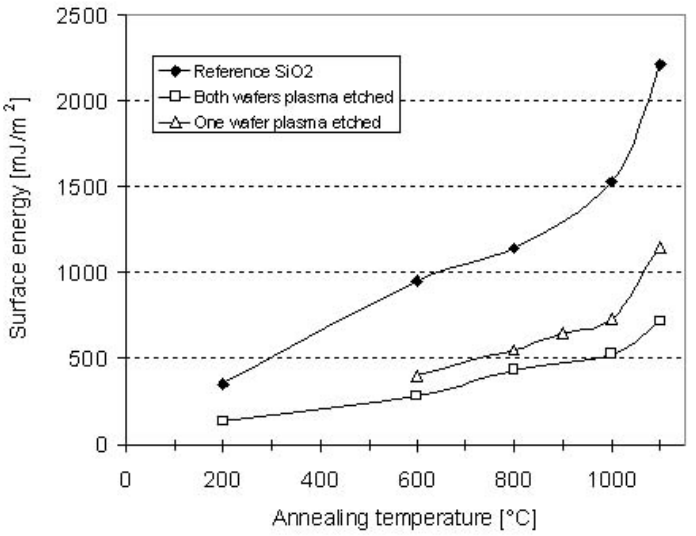

Figure 52. Bond strength as a function of annealing temperature for oxide-oxide wafer pairs with and without surface roughening. Annealing time was 2 h.

To improve bond strength at low annealing temperatures, plasma activation was combined with surface roughening. The plasma activation of the roughened surface seemed to remove the influence of the roughening somewhat, and the bond strength at high temperatures was similar or higher to that in reference samples (Figure 53). By plasma-activating one wafer and roughening the other, the desired results were obtained enabling ion-cut at 400°C (bond strength ~500 mJ/m^2) and debonding after high temperature annealing (~1200 mJ/m^2).

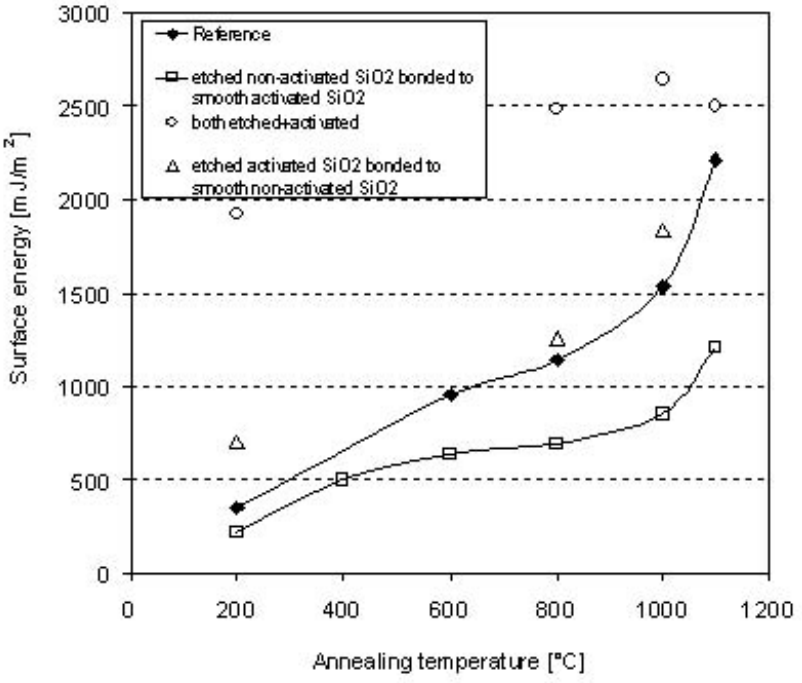

Figure 53. Measured bond strengths for oxide-oxide wafer pairs as a function of annealing temperature after different roughening and plasma activation procedures. Annealing time was 2 h.

6. Summary

The purpose of this work was to study silicon direct bonding processes and evaluate the influence of different pre-bonding treatments on the bond quality. The main focus was on studying the effect of plasma activation before bonding on the bond strength. The influence of other pre-bonding treatments such as chemical-mechanical polishing (CMP), lithographical surface patterning and surface roughening was studied while developing bonding processes for various applications. These applications included heterogeneous integration for fabrication of silicon-on-glass (SOG) and silicon-on-sapphire (SOS) substrates, bonding of patterned wafers for fabrication of SOI substrates with buried cavities, and bonding of wafers with MEMS devices for wafer scale packaging.

The plasma-activation based bonding process reduces the required annealing temperature to achieve strong silicon to thermal oxide bonding from 1100°C to <200°C. Plasma is assumed to create a porous layer on the oxide surface, which helps the water diffuse out from the bonded interface at low temperature. The plasma activation effect can be lost by excess SC-1 cleaning after activation.

The plasma activation-based bonding process has been found to be a suitable method for MEMS encapsulation at wafer level. Covering the wafer with LPCVD oxide and using it as an intermediate bonding layer was found to be a viable method for encapsulation. Suitable CMP processes were found for LPCVD oxide planarization and polishing. By using a protective layer above areas to be bonded during further processing, surface roughening could be avoided. Two methods were developed for fabrication of electrical contacts in the package. Contact pad opening by grinding or sawing enables electrical contact to the package without losing the hermeticity of the package.

Patterning, bonding and mechanical thinning is a viable method for fabricating SOI wafers with buried cavities. Such new substrates enable fabrication of MEMS components difficult or impossible to fabricate on conventional Si or SOI wafers.

Bond strength is usually measured with the crack opening method or a chevron test. The former requires a place for blade insertion, and is therefore unsuitable for thinned or diced samples. It also has problems measuring high bond strengths

or fragile samples due to sample breakage during measurement. The latter method is accurate but requires pre-patterning before bonding and is therefore time-consuming. The HF etching test was found to be a suitable method for measuring bond strength from ready-made SOI, small samples or small bonded areas. In the method the buried oxide is etched in HF and the etched distance is measured. In direct bonding of hydrophilic silicon, the bond strength was found to be logarithmically dependent on the bond strength. The etched distance can be measured by cross-sectional SEM or IR microscopy.

The mechanical exfoliation of hydrogen implantation and bonded Si is a suitable method for fabrication of thin film silicon-on-insulator and silicon-on-glass substrates. In mechanical exfoliation the crack propagates on the weakest interface, therefore it is necessary to achieve a high bond strength at low temperature by using plasma activation. With this method the mechanical transfer of hydrogen-implanted Si is possible after annealing at 200°C. The strength of the implanted layer is dependent not only on the hydrogen dose, but also on crystalline orientation and boron doping. High boron doping (implantation dose of 3e15 cm^{-2}) combined with hydrogen implantation was found to decrease the required annealing temperature for mechanical exfoliation of about 80°C compared to a sample with hydrogen implantation only.

Controlling of the bond strength is possible with different surface preparations. By slightly increasing the surface roughness of wafers to be bonded, the bond strength can be limited to a level that is still mechanically debondable after high temperature annealing (1100°C). For example, the crystalline damage due to hydrogen implantation in ion-cut Si layers could be removed by high temperature annealing on temporary substrate before transferring the Si film onto a temperature-sensitive final substrate.

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Direct wafer bonding for MEMS and microelectronics

Abstract

Direct wafer bonding is a method for fabricating advanced substrates for microelectromechanical systems (MEMS) and integrated circuits (IC). The most typical example of such an advanced substrate is the silicon-on-insulator (SOI) wafer. SOI wafers offer many advantages over conventional silicon wafers. In IC technology, the switching speed of circuits fabricated on SOI is increased by 20-50% compared to circuits fabricated on a bulk Si wafer. The required operation voltage is lower in ICs on SOI than in ICs on a bulk silicon wafer, which decreases power consumption and chip heating. In the MEMS industry, the buried oxide layer works as a good sacrificial layer during release etching of diaphragms, beams etc. and offers an excellent etch stop layer for silicon etching. Direct wafer bonding can also be used in the fabrication of more complex structures than SOI. The wafers to be bonded can be of different materials, can contain patterns, and may have multiple layers or ready-made devices.

This thesis reports on studies of direct wafer bonding and its use in various applications. Different bonding processes used in microelectronics are briefly described. The main focus of this thesis is on the plasma activation-based low temperature bonding process, and on the control of bond strength by surface preparation.

A novel method for bond strength measurement is introduced. This method, based on buried oxide etching, is presented and compared with other methods used in evaluating bond quality.

This thesis also contains results on research of different applications requiring direct wafer bonding. Heterogeneous integration, pre-processed SOI fabrication, and wafer scale packaging are the main application topics.

Keywords

direct wafer bonding, MEMS, microelectronics, microelectromechanical systems, SOI, silicon-on-insulator, integrated circuits, bond strength measurement, heterogeneous integration, pre-processed SOI fabrication, wafer-scale packaging, plasma activation

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Suni, Tommi

Nimeke

Puolijohdekiekkojen suoraliittäminen mikroelektroniikan ja mikromekaniikan sovellutuksissa

Tiivistelmä

Puolijohdekiekkojen suoraliittäminen on menetelmä valmistaa kehittyneitä alustoja mikroelektromekaanisille systeemeille (MEMS) ja integroiduille piireille. Yleisin tämänlainen kehittyneempi alusta on SOI-kiekko, jossa kantajakiekon ja varsinaisen komponenttipiikerroksen välissä on eristävä oksidikerros. Verrattuna tavallisiin piikiekkoihin SOI-kiekot tarjoavat useita parannuksia. Integroitujen piirien tapauksessa kytkentänopeus on SOI:lla 20–50 % nopeampi, käyttöjännite matalampi ja energian kulutus pienempi. MEMS-teknologiassa haudattu oksidi toimii uhrautuvana kerroksena kalvojen ja palkkien vapautusetsauksessa ja myös pysäytys-kerroksena piin syövyttämisessä. Suoraliittämistä voidaan käyttää myös monimutkaisempien rakenteiden kuin SOI-kiekkojen valmistamiseen. Liitettävät kiekot voivat olla eri materiaaleista, kuvioituja tai sisältää valmiita komponentteja.

Tässä väitöskirjassa keskitytään pääasiassa korkean ja matalan lämpötilan suoraliittämiseen sekä liitoslujuuden kontrollointiin pintoja karhentamalla. Kirjassa esitellään lyhyesti myös muut kiekkoliitostekniikat.

Väitöskirjassa raportoidaan myös uusi menetelmä mitata liitoslujuus kahden kiekon välillä. Menetelmä perustuu haudatun oksidin märkäsyövyttämiseen ja sitä verrataan myös muihin raportoituihin liitoslujuuden mittausmenetelmiin.

Tämä väitöskirja sisältää myös tuloksia suoraliittämisen käyttämisestä muutamiin erilaisiin sovellutuksiin, kuten kiekkotason paketointiin, heterogeeniseen integrointiin ja esiprosessoitujen SOI-kiekkojen valmistukseen.

Avainsanat

direct wafer bonding, MEMS, microelectronics, microelectromechanical systems, SOI, silicon-on-insulator, integrated circuits, bond strength measurement, heterogeneous integration, pre-processed SOI fabrication, wafer-scale packaging, plasma activation

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