PAPER A

A Novel CMP Process on Fixed Abrasive Pads for the Manufacturing of Highly Planar Thick Film SOI Substrates

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A novel CMP Process on Fixed Abrasive Pads for the Manufacturing of highly planar thick film SOI Substrates

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ABSTRACT

A new approach using Fixed Abrasive (FA) pads has been undertaken to overcome the problem of non-uniform thick film Silicon-on-Insulator (SOI) wafers after CMP polishing. The theoretical models indicating the advantages of the 2-body system of the fixed abrasive configuration vs. the conventional 3-body system of slurry based polishing have been convincingly demonstrated in practise upon experiments in a wide range of parameters. As a result it is possible to maintain or improve the flatness of wafers after back grinding, while simultaneously removing the sub-surface damage. A surface quality of prime wafers can be reached on the device layer. Capacitive thickness measurement scans and atomic force microscopy (AFM) monitoring confirm the results. A detailed comparison with conventional processing has been carried out to clarify the advantages on bulk silicon wafers. Decoration etching is used to analyse the wafer surface quality in terms of oxide induced stacking faults (OISF). As a result an alternative processing method is proposed for manufacturing thick film SOI substrates with improved uniformity.

INTRODUCTION

The manufacturing of thick film silicon-on-insulator (SOI) substrates requires a significant amount of mechanical treatment. In thin film SOI production the SmartCut™ process leaves an already highly uniform surface, which only requires a small amount of polishing if at all [1]. Processing of thick film SOI however requires extensive grinding and polishing to remove most of the bonded device wafer. Therefore, care has to be taken for the non-uniformity of the thinning processes. While grinding leads to a TTV (Total Thickness Variation) of 0,5 µm on the wafer it leaves a sub-surface damage (SSD) of up to 6 µm deep in the substrate, which has to be removed by subsequent chemical mechanical polishing (CMP). The conventional slurry based processing however often leads to high values of thickness non-uniformity due to the strong bias for rounding the edge of the thick device layer with reduced diameter on top of the handle wafer. Since the specs for SOI-wafers at the time are more and more demanding with TTV values of < 0,5µm at EE (Edge Exclusion) of < 3mm, the conventional processing for highly planar SOI wafers often results in low yields or is not working at all. To overcome this obstacle polishing of ground wafers on so-called fixed abrasive (FA) pads has been investigated in order to improve the CMP process performance and maintain the flatness of the SOI substrate.

EXPERIMENTAL

Polishing was done on a Strasbaugh 6DS-SP Planarizer with 4” wafers ground on a Strasbaugh 7AF backgrinding tool equipped with a #325 coarse wheel and a #2000 fine wheel providing a TTV value of < 0,5 µm. Experimental FA Pads from 3M were used for the polishing. The pads possessed a microreplicated pattern of 200µm wide and 50 µm high posts containing the abrasive material in a resin-like matrix. The density of posts results in a total contact area of around 10% of the entire wafer surface, thus a higher local pressure under the posts on the wafer is achieved. The 3M pads consisted of the fixed abrasive layer stacked on a rigid layer followed by a resilient layer finished by a standard self adhesive for mounting on the polishing platten of the CMP tool. Instead of slurry a lubrication liquid containig DI water with base chemicals for pH value adjustments was applied to the pad during polishing. The time was set to 300s in general but doubled in some cases for long term studies. Starting from a standard parameter set downforce and rotation speed were varied in wide ranges in order to evaluate the potential of the pad. Also the pH-values have been varied under the tests.

THEORY

While under conventional polishing the abrasive particles can reach the complete exposed surface of the wafer, removal occurs both on the elevated and the lower areas. Thus a polishing cycle results in a higher material removal until the entire area is planarized. Also the exact defined edges of the substrate (especially in the caes of the SOI device layer) are attacked by the particles in the slurry film being pressed onto the surface by the bending compressable pad. Removal in conventional CMP thus occurs via the so-called 3 body interaction.

In the case of SlurryFree™ polishing the abrasive particle is bound in the elevated posts of the pad. Thus removal resulting contact is mainly occuring at the elevated areas of the exposed surface. The removal rate ratio between higher and lower areas of the wafer is much higher than in the case of slurry based CMP. A much more effective planarization effect is expected and the overall necessary material removal for complete planarization is minimized. For the fixed abrasive pad removal mechanism one speaks of a 2-body system (See Figure 1).

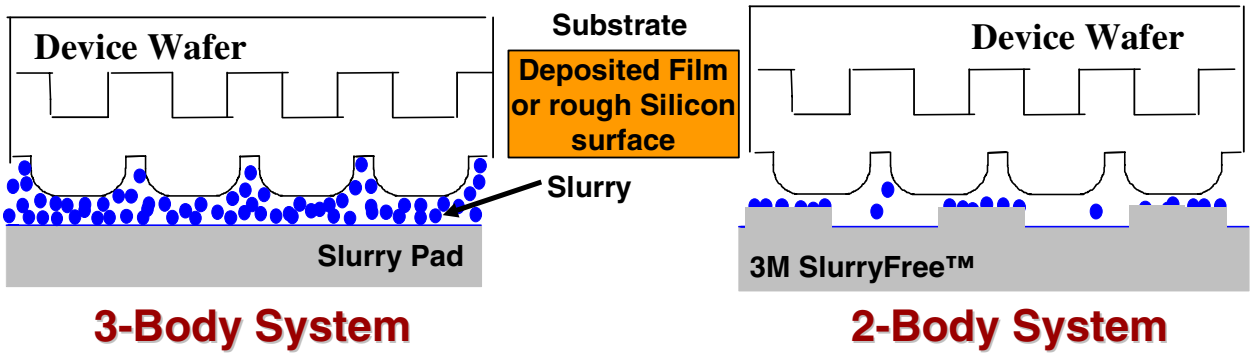

Figure 1. Schematic comparision of the conventional CMP Process and the Fixed Abrasive case

DISCUSSION

First Tests

In figure 2 a summary of various process parameter settings is shown in terms of TTV degeneration (d-TTV) and total removal. As comparison the d-TTV value of 0,76 µm for a conventional CMP step with a 5 µm removal is shown. As one can see the d-TTV value stays well around 0 µm in nearly all parameter settings thus maintaining the superior TTV values of < 0,5µm of the incoming material. However a total removal of 1,3 µm is not exceeded in any case. The calculated removal rate (RR), 0,1-0,2 µm/min is far below the expected 1µm/min of conventional CMP.

Calculating the Non-Uniformity of the removal (NU) however one can see in figure 3 that the achieved values for fixed abrasive polishing are well around 5%. This is a strong improvement compared the reference value of 15% NU in the case of slurry based CMP.

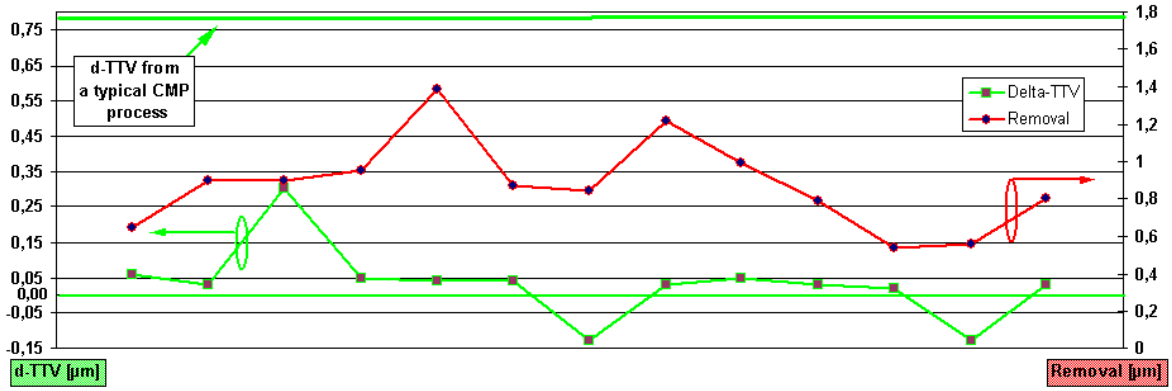

Figure 2. A nearly neutral TTV behavior is visible, while the overall removal is limited

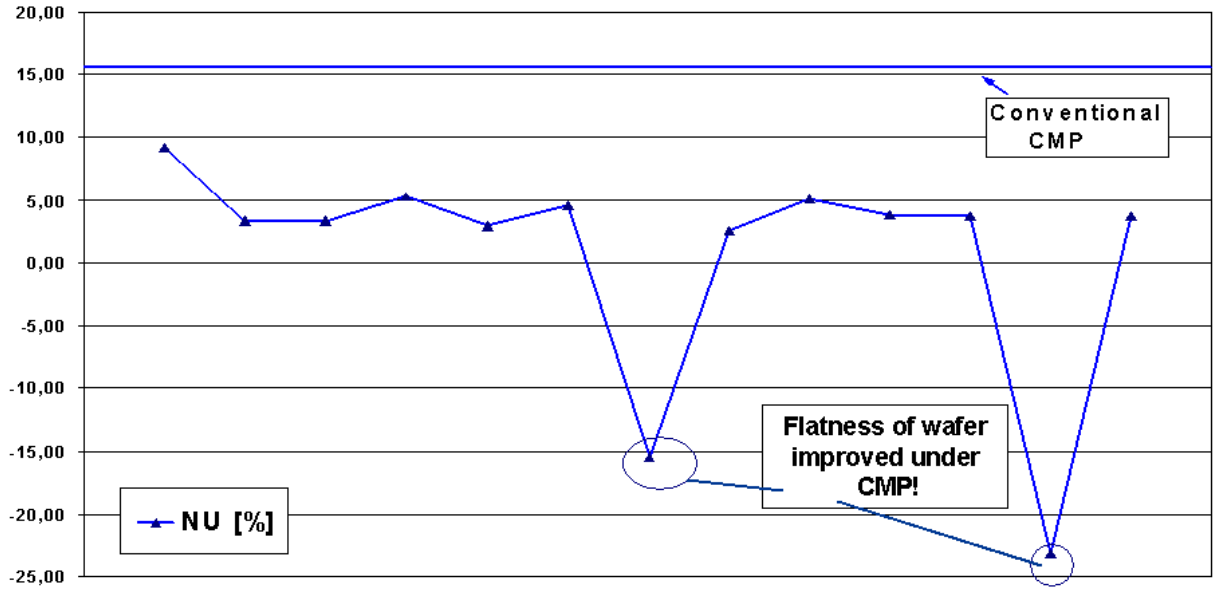

Figure 3. NU of FA pads shows only a third of the value achieved in slurry based CMP

It can be stated that the fixed abrasive technology indeed provides exellent planarization. In terms of TTV degeneration good results are achieved in a wide process window. However the process stopped after the roughness of the surface was eliminated and no further removal could be achieved. In most cases the grindlines were invisible after a 1 µm removal comparing to a minimum of 3 µm in slurry based CMP. For the removal of the deeper laying sub-surface damage (SSD) a "blank-rate" would be needed and also an increase of the achievable RR would be beneficial in order to limit the needed polishing time.

Second Generation fixed abrasive Pads

Further development was leading to set of FA pads, which is providing improvements in the needed areas. Now a total removal of more than 2,5 µm was achieved while the NU of removal was still low varying in between 1,4-9,7% (see Figure 4). The RR could be increased to 0,35 µm/min by increasing the downforce while lowering the pH-value of the applied lubrication liquid. As major factor for the RR optimization the pH-value of the applied lubrication liquid was identified. Splitting the long process steps of 10 min into 5+5 min resulted in pad blunting since smooth wafers could not provide a sufficient re-conditioning of the abrasive posts, while the single step long time polish could maintain a reasonable RR (figure 5). A dull pad however could be recovered by polishing one rough as-ground wafer and then the original RR level was reached again.

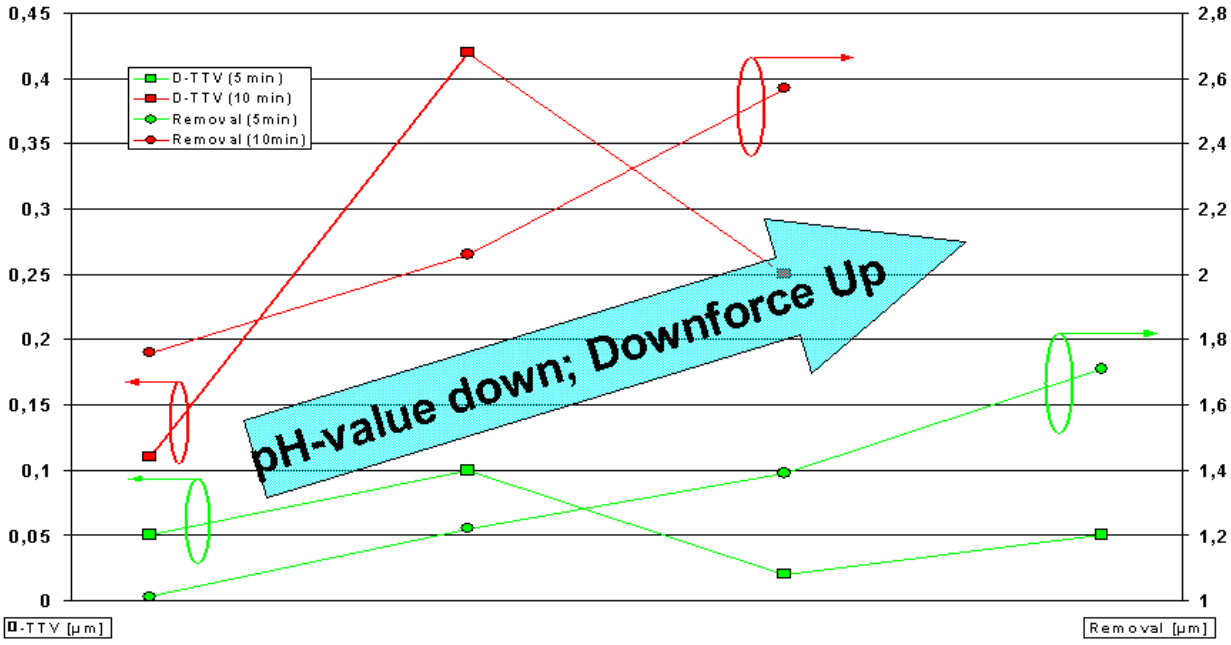

Figure 4. Second generation fixed abrasive pads provide a higher total removal while the d-TTV behavior stays better than in slurry based CMP.

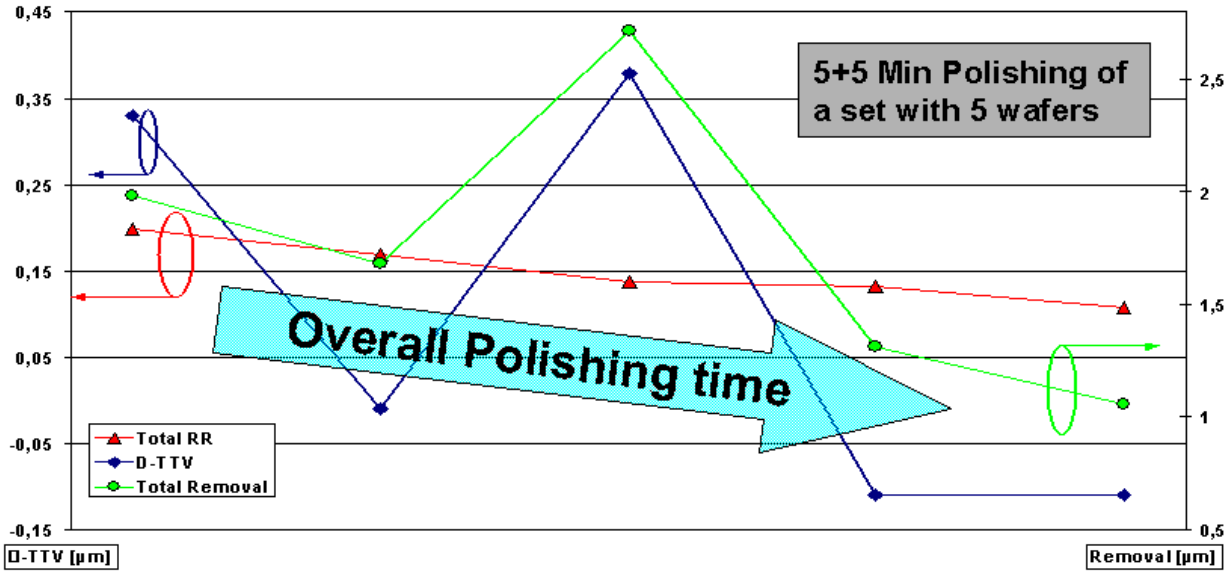

Figure 5. Splitting the process step results in pad blunting but the TTV value is maintained

Surface Quality

The surface quality was analysed by AFM. In figure 6 the as-ground silicon surface is on the left while a FA polished wafer is shown on the right. It can be clearly seen that all grindlines are removed and coming from an rms roughness value of more than 15 nm reaching a superior surface quality with a roughness of below 0,8 nm after only 1 µm removal. This indicates that even the final polishing step for haze removal can be reduced when using FA polishing instead of conventional CMP in the stockremoval process.

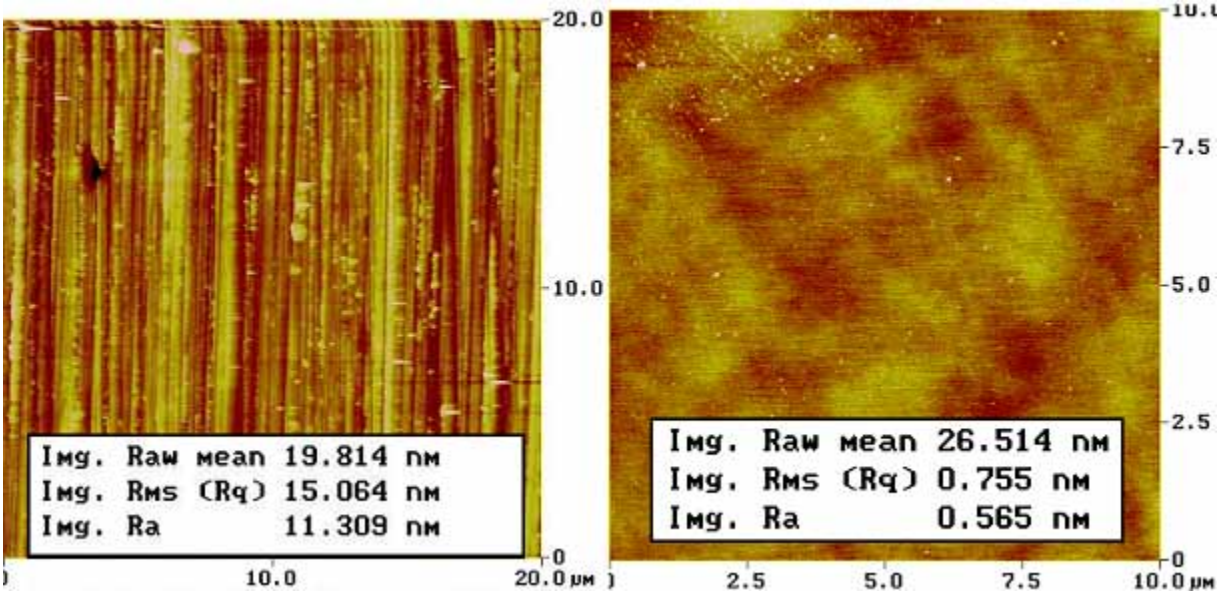

Figure 6. Comparison of AFM scans post grinding and post fixed abrasive polishing. A strong improvement of the roughn ess values is obtained

Improved fine Grinding

While being able to already remove more than 2,5 µm of damaged Silicon with the second gneration FA pads still at least another 3 µm would be needed in order to eliminate all SSD induced by the conventional grinding procedure.

In another test different fine grinding techniques were compared including new grinding wheels. Polishing down stepwise after grinding followed by decoration etching the level of oxide induced stacking faults (OISF) were compared. It could be shown that with advanced fine grinding wheels the reference level of OISF was already reached when removing 3 µm of silicon compared to the standard 6-7 µm in conventional grinding.

This advanced fine grinding enables the reduction of the necessary CMP removal so that further processing with second generation fixed abrasive is feasible.

CONCLUSIONS

With the new approach of using fixed abrasive pads for polishing instead of slurry based CMP for ground silicon wafers it has been shown that strong improvements in terms of TTV degeneration can be achieved. The TTV level of 0,5 µm was maintained in many cases while the surface roughness could be reduced to a level of below 0,8 nm. The second generation fixed abrasive pads also provide the capability of removing more than 2,5 µm with removal rates of up to 0,35 µm/min. In combination with an advanced grinding technology providing a sub-surface damage level of below 3 µm instead of 6-7 µm in conventional grinding the surface can reach prime wafer level in terms of crystal defects. The superior surface quality after the fixed abrasive polish further enables the reduction of the final haze removal polish providing the possibility of even more flat wafers.

With further work a deeper understanding of the overall process shall be gained and after long term tests and stability runs a real alternative process for highly planar thick film SOI substrates can be enabled.

ACKNOWLEDGMENTS

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