PAPER C

Integration of CMP Fixed Abrasive Polishing into the Manufacturing of Thick Film SOI Substrates

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Integration of CMP Fixed Abrasive Polishing into the Manufacturing of Thick Film SOI Substrates

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ABSTRACT

The specification for the total thickness variation (TTV) of the device layers on thick-film silicon on insulator (SOI) wafers tighten for future applications. Therefore, the bulk removal polishing process of current technology after grinding cannot meet the demands in terms of flatness. The currently required amount of material removal for polishing out the induced sub surface damage (SSD) of the grinding is very high. Additionally, slurry-based CMP processes show unsatisfactory grindline and topography removal. This in turn reflects negatively to processing times, throughput and overall flatness performance.

Encouraging early results of FA pad use for silicon and SOI polishing have already been further developed [1]. Low SSD grinding has been introduced to silicon manufacturing [1]. In this work, an integrated manufacturing process sequence is presented. Starting from low SSD grinding of the bonded SOI wafer couple, an optimized FA CMP step is replacing the conventional bulk polishing with reduced removal. The SSD after FA CMP is investigated by oxide induced stacking fault (OISF) method [2] and results are used to adjust the final polishing step of the substrates. The overall process sequence is highly advantageous in terms of performance in TTV and provides a highly competitive and effective method for achieving best possible surface quality with minimized total silicon removal. This method is not only useful for SOI wafers but also in other areas of silicon processing.

INTRODUCTION

When making thick film SOI substrates a significant amount of mechanical treatment on wafers has to be done. Unlike in thin film SOI the device layer of the wafer has to be formed by removing most of the bonded top substrate during grinding and subsequent polishing. Grinding is used to adjust the required thickness, which can vary from 1 µm to more than 100 µm. Grinding leads to very flat wafers, however it leaves not only mechanical abrasion lines, but also introduces a several microns deep layer with crystalline defects [4, 5]. Therefore, subsequent polishing is needed to provide a smooth and defect-free device layer surface. Conventional slurry-based CMP leads to unsatisfactory results in terms of TTV, as the edge of the slightly smaller device layer is rounded under the removal of the damaged layer. As the required polishing amount is increasing, the TTV degenerates. Currently a polishing removal of 5 µm is needed for slurry-based CMP to remove all grindlines and 6 to 8µm is necessary to remove all crystalline damage from standard grinding processes [1].

For achieving flat thick film SOI wafers it is therefore important to minimize the overall CMP removal by reducing the SSD layer and simultaneously optimizing the polishing process for more effective grindline removal. New grinding wheel technology provides wheels, which will induce a shallower SSD layer as has been shown earlier [3]. With the fixed abrasive technology, an appropriate method has been found to avoid edge rounding under polishing and to remove grind lines much more effectively than in conventional CMP [1].

When integrating these new approaches into a manufacturing sequence the resulting surface quality is essential. After stock polishing, only little material is removed by final polishing in order to provide best surface roughness and haze removal. In this study the influence of replacing the conventional grinding and polishing on the overall manufacturing sequence is analysed. Low-SSD grinding and FA CMP are used. The surface quality is analysed after different final polishing times for remaining damage.

EXPERIMENTAL

Polishing was done on a Strasbaugh 6DS-SP Planarizer on 6” bonded and edge-ground wafer couples, which were thinned by a Strasbaugh 7AF back-grinding tool equipped with a #325 coarse wheel by Norton. Prior to polishing also fine grinding was done on #4000 fine wheel from DISCO, providing a reduced sub surface damage (SSD). The resulting TTV was ~0.5µm. Experimental FA Pads from 3M were used for CMP. The micro replicated posts of these pads were about 125µm wide and 50 µm high, containing ceria abrasives in a resin-like matrix. The density of posts resulted in around 10% contact area during processing. Polishing time was set to be 300s, in some cases 360s. The previously optimized parameter set [1] was used in the process. Final polishing was done on commercially available polishing pads with commercially available polishing slurry under different times. The resulting removal was varying between 0.2 and 0.6 µm. A set of wafers was then investigated by OISF method for stacking faults. Wafers were measured by ADE capacitive measurement gauge for thickness and TTV performance.

RESULTS AND DISCUSSION

Thinning of the bonded wafer couples

A set of 15 wafers was ground to a device layer thickness of about 53 µm, leaving 3 µm for subsequent grindline and crystal damage removal by CMP. The achieved average thickness was 52.79 µm with a standard deviation of 0.66% indicating a stable grinding process. Average TTV of the wafers was 0.46 µm providing very flat starting material for the polishing trials.

Fixed Abrasive and final polishing

Ground wafers were then polished by fixed abrasive pad. The removal was set to be about 2.5 µm. A subsequent final polishing step removed another 0.5 µm. Figure 1 shows a typical result after FA polishing step. No edge rounding is visible rather slight centre fast removal behaviour is detected. In Figure 2 a typical result is shown after final polishing. No bigger influence on the flatness is obtained and the overall wafer remains significantly below 1 µm

TTV. Table 1 gives an overview on the performance of the entire wafer set. All wafers are below 1 µm TTV with an average value of 0.78 µm. As can be seen from figures 1 and 2 the edge exclusion used in the measurements is 3 mm. With an edge grinding process removing around 1.7 mm, this results in a SOI layer edge exclusion of 1.3 mm.

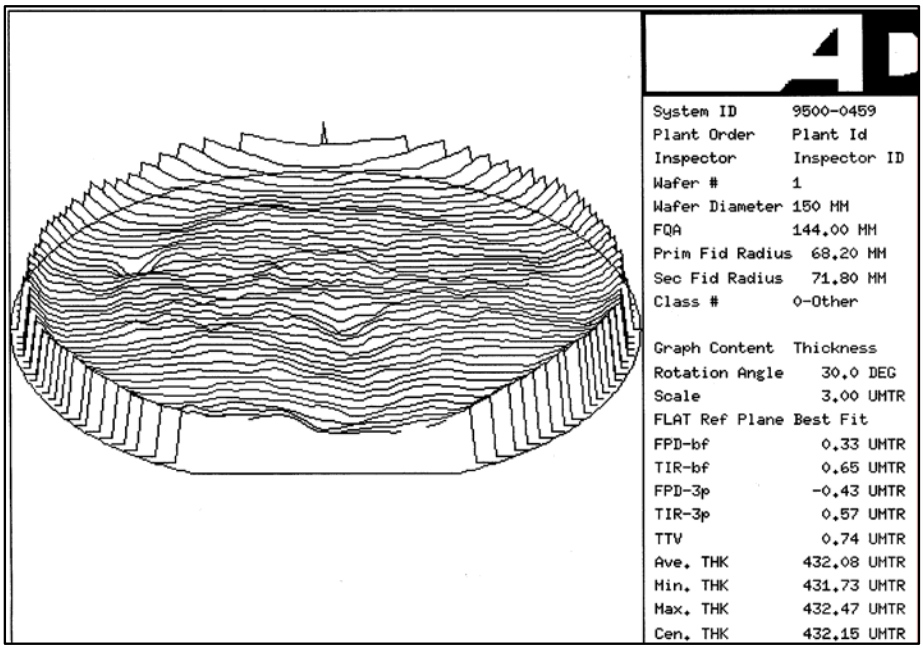

Figure 1: Capacitive thickness scan of the FA polished wafer. No edge rounding is visible. The overall TTV is well below 1 µm

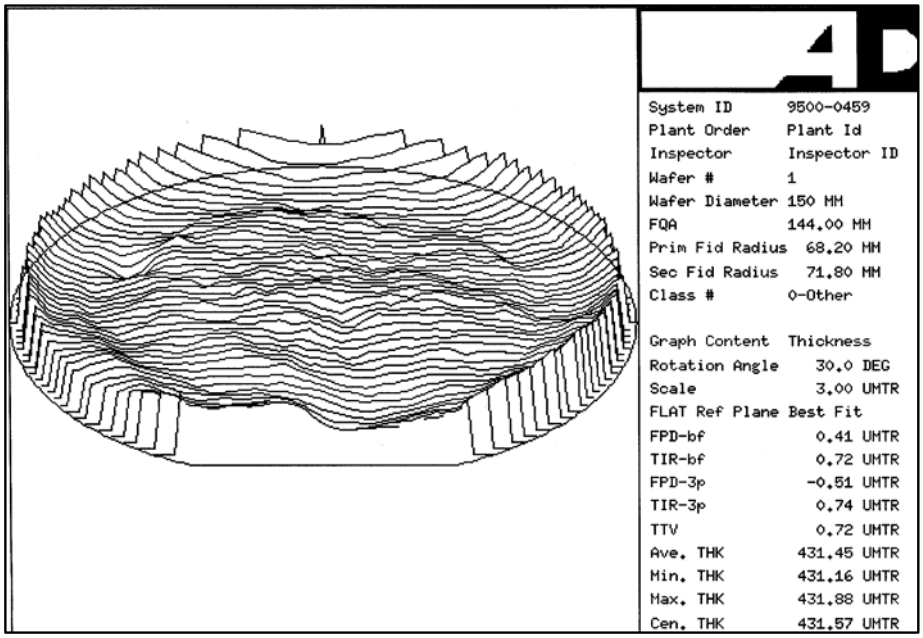

Figure 2: After final polishing and further 0.5 µm removal the wafer is still very flat. The last polishing step does not strongly influence the result.

Table 1: Overview of the performance of the combined grinding and polishing sequence. All wafers are well below 1 µm TTV and the goal thickness of 50 µm is well achieved.

	SOI-layer thickness after grinding:	sd		Thickness after CMP:	TTV after CMP:
1	52.2	0.19		50.05	0.72
2	52.94	0.17		49.95	0.69
3	53.36	0.09		50.03	0.91
4	52.89	0.24		49.39	0.94
5	52.82	0.11		49.46	0.94
6	52.36	0.12		49.48	0.81
7	53	0.2		50.27	0.67
8	53.13	0.13		50.35	0.81
9	52.79	0.18		49.98	0.9
10	52.57	0.2		49.79	0.81
11	53.16	0.2		50.38	0.77
12	53.02	0.16		50.29	0.64
13	52.47	0.09		49.72	0.69
14	52.16	0.19		49.43	0.84
15	52.94	0.12		50.2	0.68
	sd	0.35		0.34	0.10
	av	52.79		49.918	0.788
	sd [%]	0.66		0.68	

Surface damage after FA polishing

A set of wafers was used after FA and final polishing for further surface analysis. As the process involves a rather rigid abrasive containing post rather than a soft polishing cloth, it was expected, that the process might induce defects to the surface. Depending on the depth of those defects an intermediate polishing step would be required to remove the defects before final polishing can take place. This in turn would complicate the integration of FA CMP into any manufacturing sequence. Using a standard final polishing procedure process time was increased stepwise up to 300s, which refers to a typical value. A maximum removal of 0.6 µm was achieved. With the high sensitivity of OISF analysis, all defects should be revealed. Figure 3 shows the result of the OISF analysis involving a diameter scan. After decoration procedure, the wafer is scanned along its diameter and defects are counted by optical inspection. The total count is then processed for comparison.

As expected the FA polishing leads to a high number of defects covering the surface. However, these defects are of very shallow nature. Already after 120s of final polishing, most defects are gone (FA+120s in Figure 3). As the final polishing time is increased towards standard value of 300s and removal of 0.5 µm is reached, the fixed abrasive processed wafers have no significant defect level anymore. For reference two prime quality wafers were analyzed simultaneously, showing (Figure 3) that indeed normal defect density level is achieved after 300s final polishing.

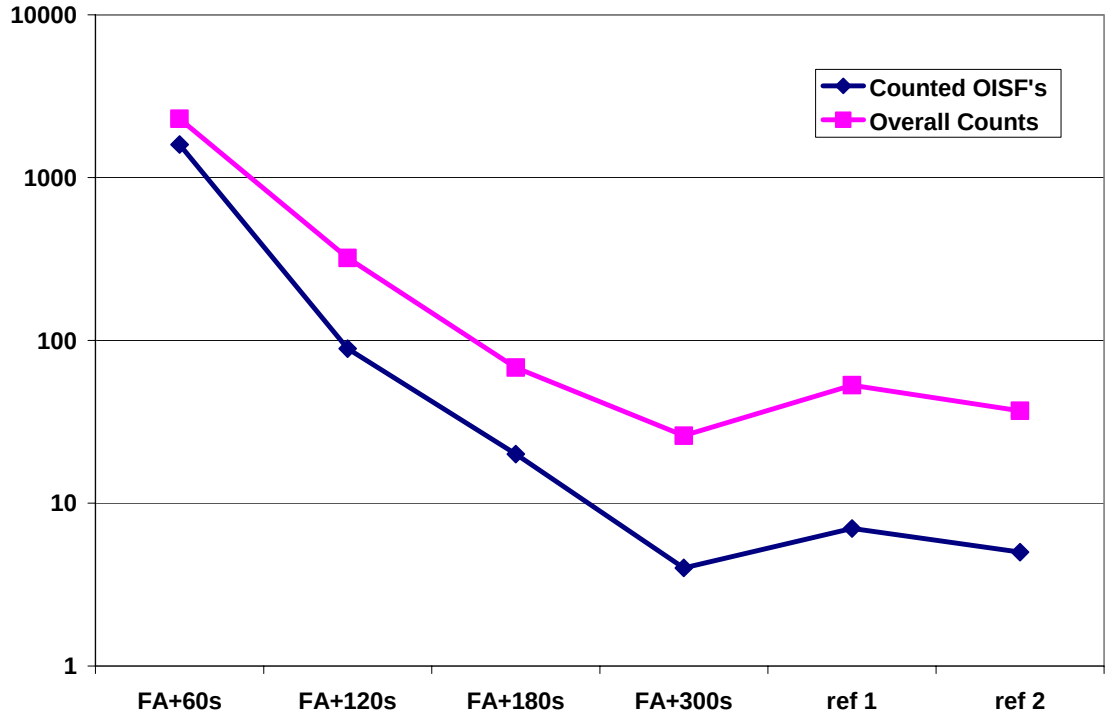

Figure 3: OISF counts on a diameter scan after different final polishing times. The count decreases rapidly with increasing the final polishing time and reaches reference level after 300s referring to 0.5 µm removal.

Process integration

With the above results, it is feasible to compare the standard manufacturing procedure of thick film SOI wafer production with the modified sequence. This is done in Table 2. The advantage of the new process sequence is evident. In best case situation for the typical standard process, the performance is still not as good as the average fixed abrasive and low-SSD grinding sequence and process time or throughput are even or better for the new process.

Table 2: Performance comparison of the new sequence with typical standard manufacturing

THICK FILM SOI:	**STANDARD SEQUENCE**	**LOW-SSD GRINDING AND FIXED ABRASIVE**
Typical required CMP Removal after Grinding	6.5- 8 µm	3- 3.5 µm
Achieved TTV	>1.0- 2.5 µm	0.5- 1.0 µm
Qualified Edge Exclusion (SOI-Layer)	3.0- 4.5 mm	1.5- 2.5 mm
Typical Removal Rate	0.5- 0.8 µm	~0.4 µm
Final Polishing Removal	0.5 µm	0.5 µm

CONCLUSIONS

The fixed abrasive polishing for silicon - especially SOI- has been successfully integrated in feasible industrial manufacturing sequence. Low SSD fine grinding enabled the total required removal after grinding to be reduced to around 3 µm. This corresponds to a reduction of more than 50% of the usual polishing depth. Besides a clearly beneficial behavior in terms of TTV, this also implies a tremendous improvement in throughput for already installed polishing lines in SOI manufacturing. The FA polishing step induced SSD has been identified to be very shallow. The regular final polishing step is able to remove the defects within typical polishing times and no additional polishing step is required. Thus, FA polishing can serve as a full replacement of the standard stock polishing step without any further need of extra processing steps or major modifications elsewhere in the manufacturing process of thick-film SOI substrates. The process can also be utilized in other areas of substrate manufacturing, when a high degree of flatness is required and effective planarization of rough surfaces with good throughput is of importance.

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