V. T. Rangel-Kuoppa and M. Pessa, Inductance deep-level transient spectroscopy for determining temperature-dependent resistance and capacitance of Schottky diodes, Review of Scientific Instruments 74, 4561-4563 (2003).

REVIEW OF SCIENTIFIC INSTRUMENTS VOLUME 74, NUMBER 10 OCTOBER 2003

Inductance deep-level transient spectroscopy for determining temperature-dependent resistance and capacitance of Schottky diodes

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(Received 24 February 2003; accepted 18 July 2003)

We present a modification of the deep-level transient spectroscopy (DLTS) to accurately determine the series resistance and capacitance of a semiconductor Schottky diode. In a DLTS sample, the resistance and capacitance are in series, but when measured by a capacitance meter they appear to be parallel, which causes a significant error in all DLTS parameters. We show theoretically and experimentally that the correct resistance and capacitance can simply be obtained if an inductor is placed in series with the sample. © *2003 American Institute of Physics.*
[DOI: 10.1063/1.1610786]

Deep-level transient spectroscopy (DLTS)[1] is a powerful tool for studies of electrical defects in semiconductors. Because DLTS measures a time-dependent change in the capacitance of a Schottky diode, it is necessary to precisely know the real capacitance. It has been shown[2] that the series capacitance C_S and series resistance R_S of the equivalent circuit of the Schottky diode [Fig. 1(a)] are related to the parallel capacitance C_p and resistance R_P [Fig. 1(b)], as measured by the capacitance meter through

$$C_P = C_S/(1+Q^2), \tag{1}$$

$$R_P = R_S(1+1/Q^2). \tag{2}$$

Here, $Q=\omega R_S C_S$ is the quality factor of the series circuit and ω is the frequency of the capacitance meter. It is usually assumed that R_S is so low that $Q=\omega R_S C_S \ll 1$, hence, $C_P \approx C_S$. However, this assumption is a remarkable simplification and a source of error at low temperatures when interpreting the DLTS data. As we show next, the simplification may yield a 25-fold error in the measurement of the capacitance.

If an additional inductor L_X were placed in series with the sample [Fig. 1(c)], one could prove, *via* an impedance equation, that such a circuit is equivalent to the circuit of Fig. 1(a) on the assumption that the measured series capacitance with an inductor attached in the circuit is C_S' [Fig. 1(d)].

$$C_S' = C_S/(1-\omega^2 L_X C_S). \tag{3}$$

Introducing C_S' of Eq. (3) into Eq. (1), one gets a measured parallel capacitance $C_P'(L_X \neq 0)$:

$$C_P' = C_S(1-\omega^2 L_X C_S)/((1-\omega^2 L_X C_S)^2 + (\omega R_S C_S)^2). \tag{4}$$

It is then straightforward to obtain the correct series capacitance and series resistance of the Schottky diode:

$$C_S = (C_P - C_P' + 2\omega^2 L_X C_P C_P')/((\omega^2 L_X C_P) \times (1+\omega^2 L_X C_P')). \tag{5}$$

$$R_S = ((C_S - C_P)/C_P)^{1/2}/(\omega C_S). \tag{6}$$

C_P and C_P' can be determined by carrying out two separate measurements; namely, a DLTS scan without an inductor to obtain C_P, as read directly from the capacitance meter, and another scan with a series inductor L_X attached in the circuit to yield C_P', also directly read from the capacitance meter.

This inductance-DLTS method can be validated experimentally. Before testing the method with a Schottky contact, a resistance and capacitance circuit in series was studied at room temperature. The resistance and capacitance were measured separately. Two resistance (2274 Ω and 1560 Ω) and one capacitance (497 pF) were used. Then, the capacitance of the circuit in series was measured with the DLTS capacitance meter. A total capacitance of 211 pF and 305 pF were obtained using the two resistances in series, respectively. Finally, two inductances of 1.019 mH and 1.5 mH were added in series and the total capacitance of this circuit was measured. Using Eqs. (5) and (6), the capacitance and resistance

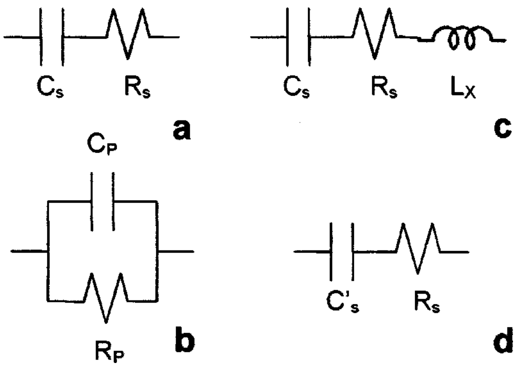

FIG. 1. Series equivalent circuit of the Schottky diode (a), parallel equivalent circuit of the Schottky diode, as seen by the capacitance meter (b), series equivalent circuit of the Schottky diode with an inductor in series (c), and series equivalent circuit of the Schottky diode with a capacitance which accounts for both the Schottky capacitance and the inductance.

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0034-6748/2003/74(10)/4561/3/$20.00

TABLE I. Measured circuit capacitance with inductors of 1.019 mH and 1.5 mH, and calculated resistances and capacitances according to Eqs. (5) and (6). The original capacitance component of the circuit is 497 pF, and the resistance components are (a) 2274 Ω and (b) 1560 Ω, which yield a total circuit capacitance of (a) 211 pF and (b) 305 pF as probed by the capacitance meter.

Series inductance (mH)	Measured circuit capacitance pF		Calculated resistance and capacitance[a]		Calculated resistance and capacitance[b]	
			(Ω)	(pF)	(Ω)	(pF)
1.019	158.9[a]	285.3[b]	2351.22	482.02	1590.67	491.18
1.5	92.3[a]	184.1[b]	2345.83	491.56	1595.12	495.63

[a] For series resistance 2274 Ω.

[b] For series resistance 1560 Ω.

were calculated. The results are shown in Table I. It can be seen that the calculated resistance and capacitance are very similar to their values, within the error limits of 3.27% and 3.018%, respectively. These errors are attributable to capacitances and resistances from the wires and connections. We prepared a Schottky sample for the experiments by depositing gold onto a 2 μm thick *n*-type $Al_{0.4}Ga_{0.6}As$:Si layer, grown on an *n*-type GaAs (100) substrate by molecular-beam epitaxy. The area of the Schottky contact was 2.38×10^{-3} cm^2. On the back side of the substrate, an ohmic contact was made by evaporating a multiple metal layer of 5 nm Ni/5 nm Au/30 nm Ge/100 nm Au, and then annealing the contact for 1 min at 410 °C.

We connected four different inductors in series with the sample with $L_X = 3.413$, 4.543, 6.665, and 8.510 mH to get a set of C_S's in Eq. (5). R_S was corrected for minor internal resistances of the inductors: 16.00, 18.09, 33.00, and 38.14 Ω, respectively. The DLTS scans were performed in the temperature interval from 85 to 470 K. The pulse width was 100 ms and the pulse period was 1s. The reverse bias was -0.7 V and the pulse bias was 0 V.

C_S and R_S obtained from Eqs. (5) and (6) are shown in Fig. 2. Interesting phenomena are observed. First, R_S remains independent of applied L_X in agreement with Eq. (6). Slight variations in R_S at a high temperature are attributable to an inductance effect, due to the ohmic contact.[3] Second, R_S increases, as the temperature is decreased, typical of semiconductors, reaching 20–25 kΩ at 120 K in our case. Consequently, R_S is far from being zero in a temperature interval usually applied in DLTS; in other words, the assumption that C_P is equal to C_S at low temperatures is a crude approximation. Third, C_S remains independent of temperature in a wide range from 150 to 350 K, contrary to the behavior of C_P.

The quality factor Q is shown in Fig. 3. It is temperature dependent and bigger than one when the temperature is between 100 and 160 K. If C_S were considered to be the same as the measured C_P read from the capacitance meter and were not corrected for $Q \neq 0$, an error of an order of 25 in C_P would be occur at 100 K [Eq. (1)]. Although this error becomes less important at higher temperatures, it seriously influences the DLTS parameters of semiconductors, such as InGaAsN,[4] GaNAs,[5] InP,[6] and AlGaAs,[7] all of which exhibit deep levels in the range from 85 to 200 K. The density of deep levels (ρ_{DL}) is strongly affected by this error because ρ_{DL} is inversely proportional to C_P during reverse bias. Finally, the activation energy of a deep level depends upon the temperature position of the peak in a DLTS scan, which is distorted by the presence of high resistance[2] and, as it has been pointed about by Broniatowski *et al.*,[2] the real change in capacitance C_S is a function of Q, and therefore, is a function of C_P, via Eq. (1).

Finally, we discuss the justification of the inductance-DLTS method. A complete Schottky diode model[8] considered here is shown in Fig. 4. It accounts for the capacitance and resistance of the Schottky and ohmic contacts, the packing capacitance C_{CS}, which is zero in our case, and the resistance of the substrate. The majority electron mobility μ_H is about 2800 cm^2/V s for our GaAs substrate having the electron density of 10^{17} cm^{-3} and remains rather constant in the temperature range of interest.[9] Using the length of the

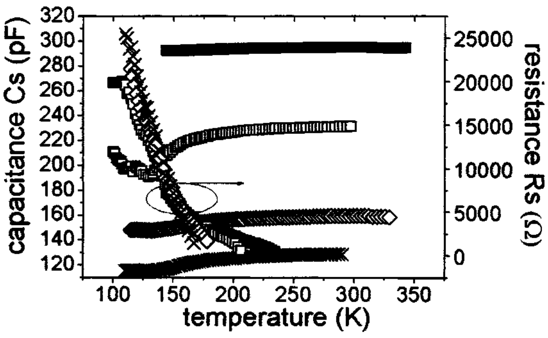

FIG. 2. Series resistance and series capacitance measured for *n*-type $Al_{0.4}Ga_{0.6}As$:Si epitaxial layer on a *n*-type GaAs (100) substrate, with a pulse width of 100 ms and a period width of 1 s, obtained by applying Eqs. (5) and (6). The graphics correspond to the use of the following inductances: (■) 3.413 mH, (□) 4.543 mH, (◇) 6.665 mH, and (×) 8.51 mH.

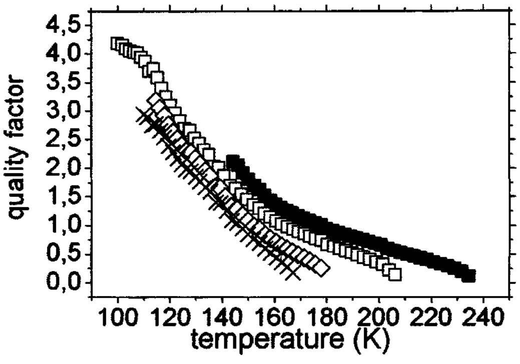

FIG. 3. Quality factor Q obtained for $Al_{0.4}Ga_{0.6}As$:Si with a pulse width of 100 ms and a period width of 1 s. It appears that $Q \neq 0$ over a large temperature range in sharp contrast to what is often assumed, suggesting $C_P \neq C_S$. The graphics correspond to the use of the following inductances: (■) 3.413 mH, (□) 4.543 mH, (◇) 6.665 mH, and (×) 8.51 mH.

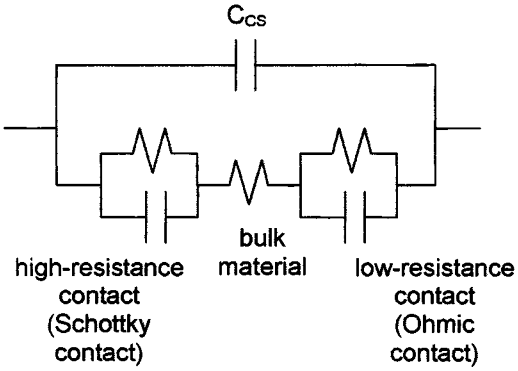

FIG. 4. Equivalent circuit of a total (two-contact) Schottky diode. C_{CS} is the parasitic capacitance of the package, which is zero in the present case.

electron path (350 μm) through the substrate and the area of the Schottky contact (2.38×10^{-3} cm^2), we obtain a negligible substrate resistance of 0.33 Ω. The 2 μm $Al_{0.4}Ga_{0.6}As$:Si epilayer ($\sim10^{17}$ cm^{-3}) has an even smaller resistance. At 120 K, μ_H has a maximum value[10,11] which is about 1000 cm^2/V s, yielding the epilayer resistance of $\sim5\times10^{-3}$ Ω. The ohmic contact resistance is on the order of 10^{-5}–10^{-6} Ω, totally negligible. Therefore, our model is comprised of a high resistance and a capacitance in parallel, which are electrically indistinguishable[8] from the resistance and capacitance in series [Fig. 1(a)]. The series model is preferred because this makes it possible to regard the capacitance and resistance of a DLTS sample directly as those of the Schottky contact.[8]

This work was supported, in part, by the Academy of Finland within the framework of the DIODE Project and by the National Council for Science and Technology (CONACYT) of Mexico, Fellowship 136605.

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