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A Multicarrier GMSK Modulator With On-Chip D/A Converter for Base Stations

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***Abstract*—A multicarrier Gaussian minimum shift keying (GMSK) modulator with a 14-bit on-chip digital-to-analog (D/A) converter is presented. The design contains four GMSK modulators, which generate GMSK modulated carriers at the user-defined center frequencies. In wireless base stations, the modulated transmit signals are usually combined at the RF frequency after power amplification. The multicarrier modulator combines four GMSK modulated signals in the digital domain, thereby eliminating the need for an antenna microwave combiner. A new digital ramp generator and output power-level controller performs both the burst ramping and the dynamic power control in the digital domain. The maximum dynamic performance is obtained by multiplexing two D/A converters with output sampling switches. The digital multicarrier GMSK modulator is designed to fulfill the derived spectrum and phase-error specifications of the GSM 900/1800/1900 base stations for pico-, micro-, and macrocells. The die area of the chip is 26.8 mm^2 in 0.35-μm CMOS (in BiCMOS) technology. Power consumption is 706 mW at 3.3 V with 52 MHz.**

***Index Terms*—Direct digital frequency synthesizer, GMSK modulator, interleaved D/A converter, multicarrier, power control.**

I. Introduction

N CURRENT base-station solutions, the power ramping and output power-level control is performed in the analog domain, as shown in Fig. 1(a), and carrier combining is performed in a lossy RF combiner. Multicarrier transmission with digital carrier combining provides a number of attractive benefits over the current solution. It saves a large number of analog components, many of which require production tuning. Consequently, an expensive and tedious part of the manufacturing can be eliminated. Additionally, there is no need for cavity or hybrid combiners, and the approach enables fast changes in carrier frequency configuration, thereby supporting dynamic channel allocation. However, multicarrier transmission with digital carrier combining necessitates power control to be implemented in the digital domain, as shown in Fig. 1(b). Otherwise, it would not be possible to adjust the relative power of a single carrier with respect to the others. Since an individual carrier in a digital multicarrier signal cannot be filtered in the analog domain, the digital-to-analog (D/A) converter in Fig. 1(b) faces extremely high dynamic-range requirements. The Gaussian minimum shift keying (GMSK) modulation method used in the GSM 900/1800/1900 (referred to subsequently only as GSM) is a constant envelope modulation scheme. As a number of these GMSK carriers are combined to produce a multicarrier signal, the beneficial properties are lost. Because of the strongly varying envelope of the composite signal, very stringent dynamic linearity requirements are imposed on the wide-band D/A converter, upconversion mixers, filters, and power amplifier. The analysis of spurs, harmonics, and noise from the filters, mixers, and power amplifier are beyond of the scope of this paper.

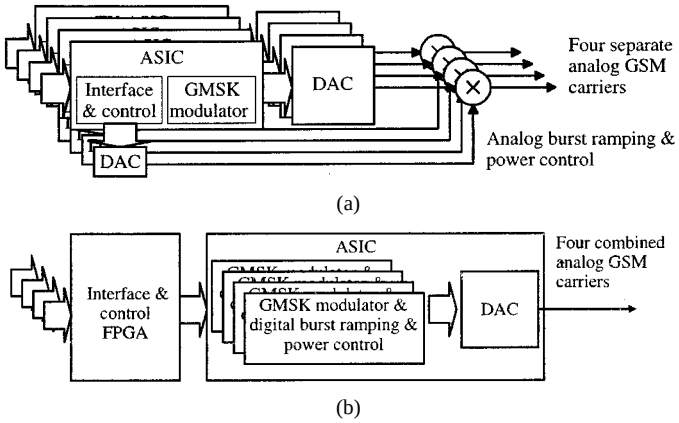

Fig. 1. Two multicarrier modulators. (a) Current base-station solution. (b) Approach in this paper: Multicarrier modulator with digital carrier combining.

The paper is organized as follows. The different multicarrier modulator architectures are introduced in Section II. Section III provides a description of the GMSK modulator, which is the core of this multicarrier modulator. The new ramp generator and output power-level controller is described in Section IV. The on-chip D/A converter is described in Section V. A mixed-signal high-precision monolithic device requires a significant design effort at the physical level, which is the topic of Section VI. Finally, experimental results obtained from the chip are presented in Section VII, followed by a few concluding comments in Section VIII.

II. Multicarrier Modulator Architectures

In the GMSK modulation, the input symbols are filtered by the Gaussian low-pass filter before frequency modulation. The requirements of the multicarrier GMSK modulator are shown in Table I. The multicarrier modulator architecture should be optimal for generation of four GMSK modulated carriers

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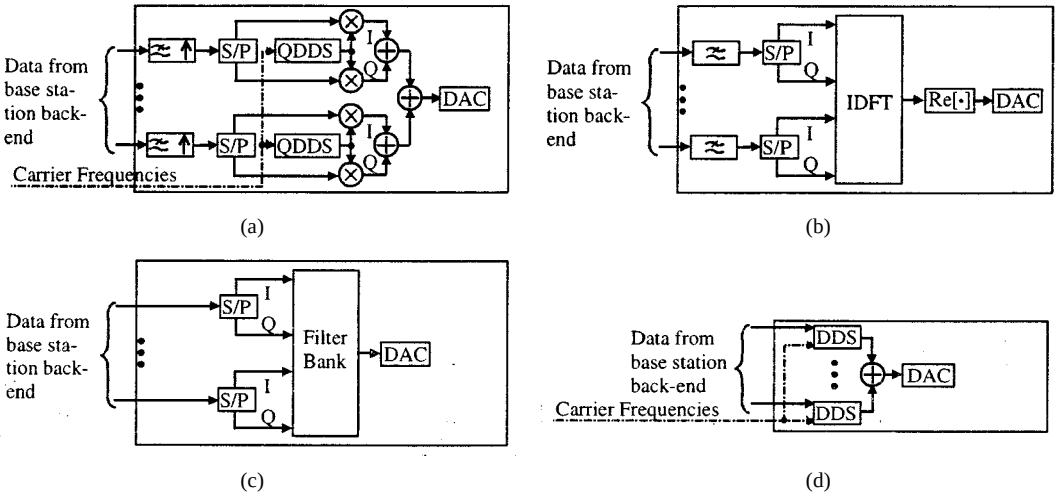

Fig. 2. Multicarrier options. (a) Parallel upconverters. (b) IDFT based. (c) Synthesis filter bank based. (d) Parallel DDSs.

TABLE I
MULTICARRIER GMSK MODULATOR SPECIFICATIONS

Symbol rate	270.833 Kb/s
Frequency error	2 Hz
Hopping frequency	1.733 kHz (GSM burst-by-burst)
System clock frequency	52 MHz
Number of carriers	Four
Carrier spacing	200 kHz
Modulation	GMSK with BT = 0.3
Phase error rms	1.5°
Phase error peak	2.5°
Spurious Free Dynamic Range	-80 dBc
Ramp-up time	14 μs
Ramp-down time	14 μs
Ramp curve type	Raised cosine/sine
Power control range	0 – -32 dB
Power control step	2 dB
Power control fine tuning step	0.25 dB

Some margin has been left between the values in [26] and the values specified in Table I. This margin should take care of the other transmitter stages that might degrade the spectral purity of the signal.

at user-defined frequencies with fine frequency tuning. In Fig. 2, four multicarrier modulator architectures are presented: a bank of parallel quadrature digital upconverters [1]–[6], quadrature upconversion using the inverse discrete Fourier transform (IDFT) [7], pulse-shaping filtering, interpolation and quadrature upconversion using a synthesis filter bank [8]–[14], and a bank of parallel direct digital synthesizers (DDSs) with frequency modulation capabilities. In Fig. 2(a)–(c), it is possible to produce different modulation schemes by means of programming the pulse-shaping filter. In Fig. 2(a), the upconversion to the IF frequency is performed by a quadrature direct digital synthesizer (QDDS), two multipliers, and an adder [15]. The upconversion can be also performed by a coordinate rotation digital computer (CORDIC) algorithm [1], [2]. In Fig. 2(b), the upconversion is carried out by the IDFT block, where the IDFT block is interpreted as a bank of complex modulators in the time domain, each at a different carrier frequency. The carrier frequency resolution depends on the number of points in the IDFT, and, therefore, this approach requires a considerable amount of hardware if a fine carrier frequency tuning and a small number of carriers are needed (see Table I). The hardware cost could be reduced by using two staged approaches, where the fine carrier frequency tuning is achieved by doing fine-grain frequency adjustments in complex baseband with, e.g., the CORDIC approach and then a coarse-grain mixing in the IDFT. In Fig. 2(c), the pulse shaping, interpolation, and upconversion to the IF frequencies are performed by the synthesis filter bank. The synthesis filter banks can be classified into three main types, as described in [10], namely: per-channel approaches [11], multistage techniques [9], [14], and block techniques which include orthogonal transform of the IDFT type [8], [12], [13]. The carrier frequency resolution depends on the number of channels in the synthesis filter bank, and, therefore, this approach requires a considerable amount of hardware if a fine carrier frequency tuning and a small number of carriers are needed (see Table I). In the synthesis filter bank,

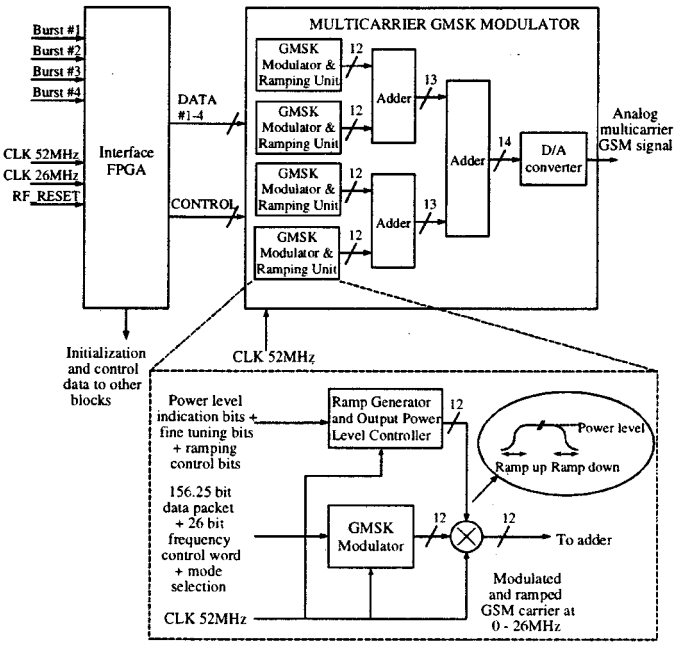

Fig. 3. Multicarrier GMSK modulator.

the carrier frequency resolution can be also improved by doing fine frequency adjustments in complex baseband [14]. The fine carrier frequency resolution could be achieved with low hardware cost in Fig. 2(a) and (d) by programming the QDDS or DDS [16]. The fine carrier frequency resolution gives a high degree of flexibility in IF and RF frequency planning. The GMSK modulation used in the GSM is frequency modulation. The frequency modulation and upconversion could be done directly by the DDS in Fig. 2(d) [16], saving hardware compared with the architectures in Fig. 2(a)–(c). Therefore, the choice was made in favor of the DDS bank architecture with frequency modulation capabilities.

III. GMSK Modulator

The interface field-programmable gate array (FPGA) in Fig. 3 extracts data bits, power-level indications, frequency control words, initialization, and control data from the base-station back-end. The FPGA feeds necessary data and control bits to the multicarrier GMSK modulator. The block diagram of the GMSK modulator is shown in Fig. 4. The system consists of a shift register, counter, frequency trajectory look-up table (LUT), adder/subtractor, phase accumulator, carrier frequency register, phase-to-amplitude converter (conventionally, a sine ROM) and D/A converter. The input data symbols are filtered by the Gaussian low-pass filter [17]. The use of the LUT as a digital filter has been described in [18] and [19]. Incoming data symbols to the frequency trajectories LUT are stored in the shift register (see Fig. 4). The simulation shows that in order to meet modulation spectrum requirements, the impulse response of the Gaussian filter can be truncated to a 2-bit width (three stages in the shift register) [20]. Utilization of the redundancy in the stored waveforms reduces the size of the frequency trajectories LUT to less than a quarter of the original size in the modulator [20].

The output of the adder/subtractor is $N_n = (C_n \pm L_n)$, where C_n is the carrier frequency ($\pm$carrier offset) control word, L_n is the frequency modulation control word (the LUT output), and N_n is the input to the phase accumulator, n being the time index. The phase value of the phase accumulator is $P_n = (N_n + P_{n-1}) \mathrm{mod} 2^j$, where j is the phase accumulator width. The phase accumulator acts as a digital integrator followed by a modulo 2^j operator. The output frequency is

$$f_{\mathrm{out}} = \frac{\Delta P_n}{\Delta T} = \frac{N_n f_{\mathrm{clk}}}{2^j} \tag{1}$$

where f_{clk} is the clock frequency. As the GMSK modulator generates frequencies close to one half of the clock frequency, the first image becomes more difficult to filter. Therefore, the maximum output frequency is limited to approximately 0.33 times the clock frequency. The input to the phase accumulator N_n can only have integer values, therefore, the frequency resolution is found, setting $N_n = 1$, as

$$\Delta f = \frac{f_{\mathrm{clk}}}{2^j}. \tag{2}$$

The frequency resolution will be 0.77 Hz from (2), when f_{clk} is 52 MHz, and j is 26. The frequency resolution is better than the target frequency error specification in Table I.

The number of samples per symbol is 192 ($192 \times 0.270\,833$ MHz $= 52$ MHz) in the frequency trajectories LUT. The burst length is 156.25 bits in GSM systems [21]. A quarter of a guard bit ($= 0.25 \times 192 = 48$ samples) is inserted after each burst, following the eight differentially coded guard bit ones [21]. Therefore, the counter has 48/192 modes in Fig. 4 [20].

The phase accumulator addresses the sine ROM, which converts the phase information into the values of a sine wave. A sine memory compression technique is applied to reduce the size and access time of the sine ROM [22]. The wordlengths of the compressed sine ROM are described in [20]. The multiplier controls the envelope of the digital GMSK modulated IF signal in Fig. 4. The four GMSK modulated signals are combined together in the digital domain, as shown in Fig. 3. Next, the signal is presented to the D/A converter, which develops an analog signal.

IV. Ramp Generator and Output Power-Level Controller

A. Conventional Solutions

Multicarrier transmission with digital carrier combining necessitates power control to be implemented in the digital domain. Otherwise, it would not be possible to adjust the relative power of a single carrier with respect to the others. Therefore, a digital ramp generator and output power-level controller is proposed in Fig. 4.

Conventional methods for implementing the ramp generator and output power controller are to use either a memory or a finite-impulse response (FIR) filter. The clock frequency is high in the digital IF modulators, therefore, the size of the necessary memory is large. Furthermore, the multiplier is needed to set the output power level. Similarly, due to the high clock frequency in the IF modulators, there are many taps in the FIR. Multistage implementations may reduce the number of the taps to some extent.

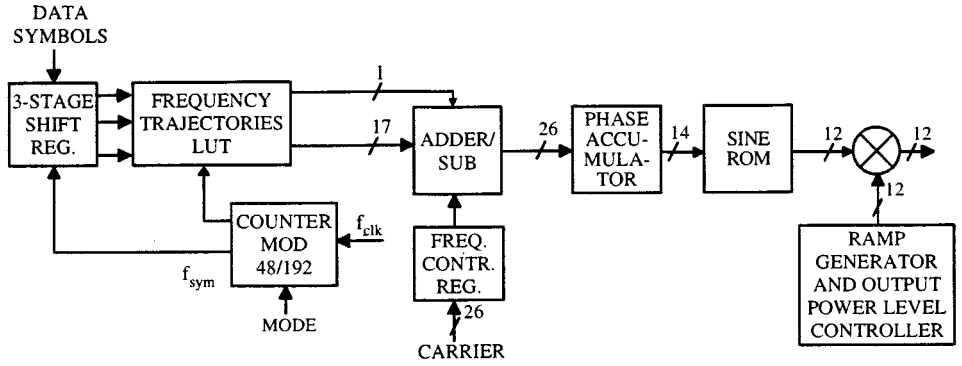

Fig. 4. Details of the single GMSK modulator and ramping unit in the multicarrier GMSK modulator (Fig. 3).

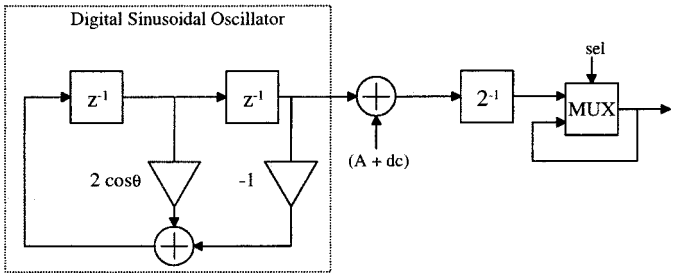

Fig. 5. Ramp generator and output power-level controller.

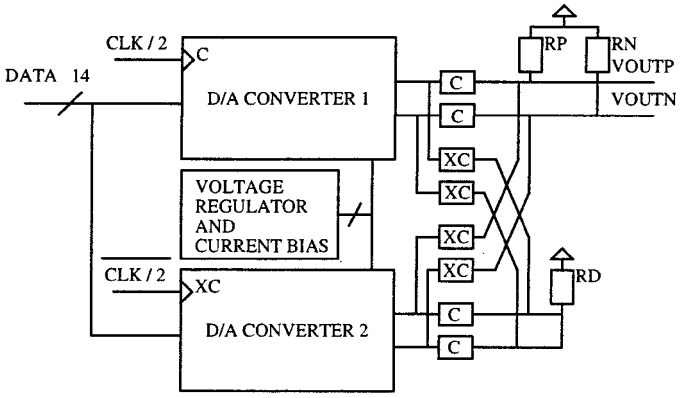

Fig. 6. D/A converter system.

B. New Ramp Generator and Output Power-Level Controller

The power-control range of the proposed design is 0 to −32 dB, where the 0-dB level is the nominal maximum power. The downlink dynamic power control in GSM uses up to 16 power levels with 2-dB separation (30 dB). The additional 2-dB range is introduced to assist the gain stabilization of the transmitter analog parts. Furthermore, a power-control fine-tuning step (0.25 dB) is introduced for this purpose (see Table I). The power level can be changed burst by burst. The digital GMSK modulated IF signal is multiplied by the ramp signal for a smooth rise and fall of the burst in Fig. 4. The power control is realized by scaling the ramp curve, which follows a raised cosine/sine curve. The new ramp generator and output power-level controller is shown in Fig. 5. The output of the ramp generator and output power-level controller is

$$\frac{1}{2}\left((A+\mathrm{dc})+(A-\mathrm{dc})\cos\left(\frac{\pi t}{T_r}+\phi\right)\right) \qquad (3)$$

where dc determines the starting power level before the ramp and the power level after the ramp [20], A is the amplitude of the ramp, t is $[0 \quad T_r]$, and ϕ is phase offset (0 for raised cosine and π for raised sine). It generates the raised sine for power up and the raised cosine for power down. The value A controls the amplitude of the ramp (power level). The cosine term in (3) is implemented by a recursive digital sinusoidal oscillator in Fig. 5. The value A controls the amplitude of the ramp (power level) [20]. During the ramp period the signal sel is low in Fig. 5 and the multiplexer conducts the ramp signal to the multiplier (Fig. 4). After the ramp duration T_r, the signal sel becomes high, the output of the multiplexer is connected to the input of the multiplexer, and the output power level is constant. The number of samples for power ramping up/power ramping down is $728(f_{\mathrm{clk}} \times T_r)$, where f_{clk} is 52 MHz (see Table I) and T_r is 14 μs from Table I. The details and finite wordlength effects of the digital ramp generator and output power-level controller are described in [20].

The D/A converter usually exhibits a fully sample-and-hold output that causes the $\sin x/x$ rolloff function to the spectrum of the converted analog signals. One method for compensating for the $\sin x/x$ rolloff is the use of the inverse $\sin x/x$ filter in the IF frequency [23]. The digital ramp generator and output power-level controller can compensate for this droop, when the bandwidth of the single carrier is narrow. The $\sin x/x$ rolloff is taken into account when the power-level value of the carrier is calculated. There will be a slight slant in the D/A converter frequency response across the channel bandwidth of 200 kHz. It was calculated that with the maximum output carrier frequency and D/A converter clock frequency (see Table I), the output power tilt across the channel bandwidth is 0.04 dB. The effect on the modulator performance can be considered negligible.

V. D/A Converter

The 14-bit D/A converter is based on a segmented current steering architecture. It consists of a 6-bit thermometer-coded most-significant-bit (MSB) segment, a 3-bit thermometer-coded second segment, and a binary-coded 5-bit least-significant-bit (LSB) segment. The dynamic linearity is of utmost importance in this multicarrier IF modulator because of the strongly varying envelope of the composite signal. The static linearity, which is achieved by sizing the current sources

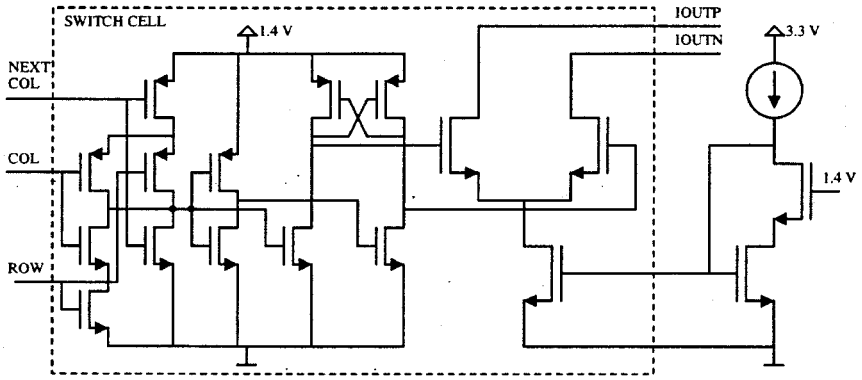

Fig. 7. MSB switch cell of the D/A converter and biasing.

for intrinsic matching [24], is a prerequisite for obtaining a good dynamic linearity. The maximum dynamic performance is achieved by multiplexing two on-chip D/A converters with output sampling switches, which are transmission gates. The D/A converter system, comprising two D/A converters that are sampled sequentially at half the clock rate, is shown in Fig. 6. For the output switches, the current transients are sampled to the external dummy resistor load RD and settled current to the external output resistor loads RP and RN. As the output current is sampled, the need to latch data inside the D/A converters is reduced; the D/A converter structure is simplified and the digital noise coupled to the analog output current is reduced. A high-swing cascode current mirror is used to bias the current source transistors of the D/A converter (Fig. 7). This approach provides a large $V_{\rm GS}$ voltage to the current source transistors, and, thus, improved matching between the current sources, due to the decreased effect of the variation of V_T. A 1.4-V supply voltage is regulated and stabilized internally for the digital parts of the D/A converter and for the high-swing current mirrors. The layout of D/A converters 1 and 2 consists of switch cells, latched thermometer coders, LSB latches, and input registers.

The measured integral nonlinearity (INL) and differential nonlinearity (DNL) are ± 5 and ± 3 LSB, respectively. The INL and DNL were measured at the output of the two interleaved D/A converters and at the outputs of the separate D/A converters. The measurement results indicate that the matching problems inside the D/A converter dominate the static linearity errors, not the matching between the two identical D/A converters. The INL and DNL performance can be improved by using larger devices and $V_{\rm GS}$ in the current sources for better matching [25] and by using a single current-source transistor matrix containing both the interleaved D/A converters. However, the dynamic nonlinearities dominate the output spectrum because of the strongly varying envelope of the composite signal, not the static nonlinearities.

VI. Chip Design Issues

This multicarrier GSMK modulator was synthesized from the very-high-speed integrated circuits hardware description language (VHDL) description using the 0.35-μm CMOS standard cell library. Static timing check and prelayout timing simulations were performed for the netlist, and the chip layout was completed using place and route tools. Finally, based on the parasitic information extracted from the layout, the post-layout delays were back annotated to timing verification. Fig. 8 displays the chip micrograph.

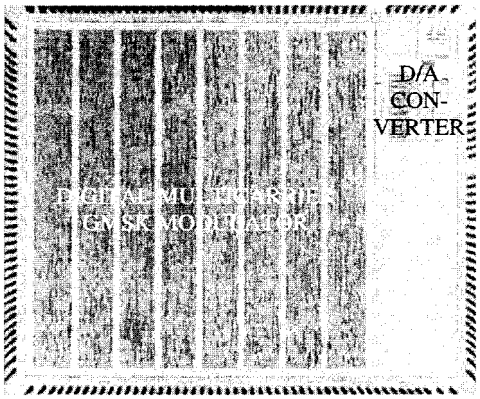

Fig. 8. Chip micrograph.

The multicarrier GMSK modulator is a mixed-signal high-precision monolithic device, which requires a significant design effort at the physical level. The D/A converter is implemented with a differential design, which results in reduced even-order harmonics and provides common-mode rejection to disturbances. In order to minimize the coupling of the switching noise from the digital logic to the analog output, on-chip decoupling capacitors (total capacitance of 2 nF) are used to reduce the ground bounce in the digital part. In the BiCMOS technology used, transistors can be easily isolated in the epi layer, which is an effective way to eliminate substrate coupling. Interference at the on-chip D/A converter output band is reduced, avoiding digital hardware using in-band clock frequencies (frequency planning).

VII. Measurement Results

The spectrum due to the modulation and wide-band noise in the cases of single-carrier and multicarrier transmissions is shown in Fig. 9, where the dashed line shows the spectrum requirements due to the GMSK modulation. Some margin (6 dB) has been left between the most stringent modulation spectrum requirement defined for GSM microcell base stations in [26] and the values specified in Fig. 9 at offsets larger than

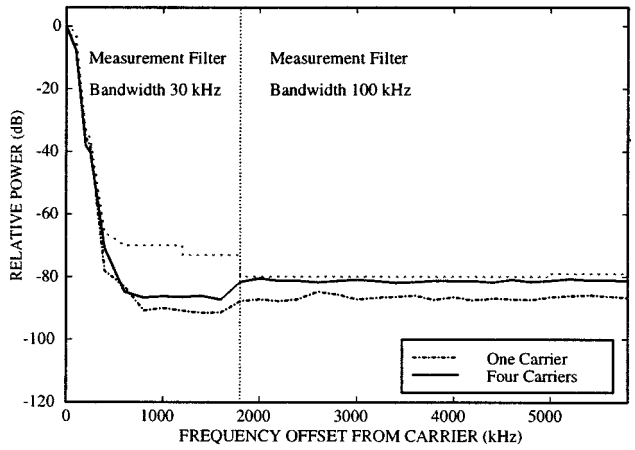

Fig. 9. Measured GSM base-station spectrum due to GMSK modulation (single carrier, multicarrier) in the D/A converter input.

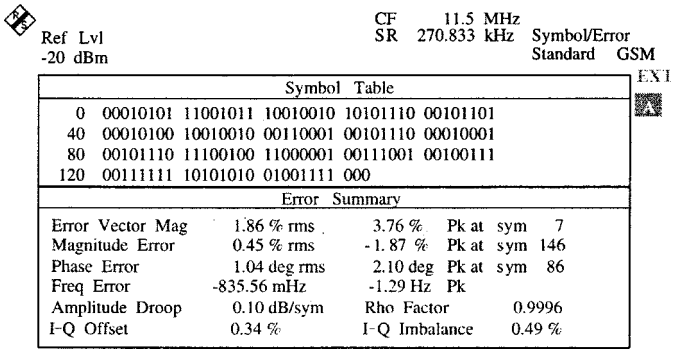

Fig. 10. Measured phase and frequency errors.

1800 kHz. This is because in the case of the multicarrier digital modulator it is not possible to use steep analog bandpass filters [Fig. 1(b)] around each carrier. After the four carriers are combined together in Fig. 3, the power per carrier is not changed, but the noise floor is increased by 6 dB. Therefore, when compared to single-carrier transmission, the noise floor is about 6 dB higher in case of multicarrier transmission in Fig. 9. Increasing the wordlengths of the sine ROM and the multiplier and changing the quantization to be done after the carrier combining could reduce this degradation. In the GMSK IF modulator, most of the errors are generated less by quantization errors in the digital domain and more by the D/A converter analog nonidealities. Hence, the spectral improvement in the digital output would not be visible in the D/A converter IF output. The wordlengths used are sufficient to fulfill the target spectrum requirements due to the modulation, as shown in Fig. 9. The increased wordlengths of the multipliers and sine ROMs would add complexity and enlarge the core area. Therefore, it was decided that the wordlengths shown in Figs. 3 and 4 should be used. The wordlengths were selected from system simulation [16], [20].

The phase-error target is specified to be 1.5° root mean square (rms) with a peak value of 2.5°, and the target frequency error is 2 Hz (see Table I). The measured rms phase error is 1.04° with a maximum peak deviation 2.1°, and a peak frequency error of −1.2 Hz at the D/A converter output (see Fig. 10).

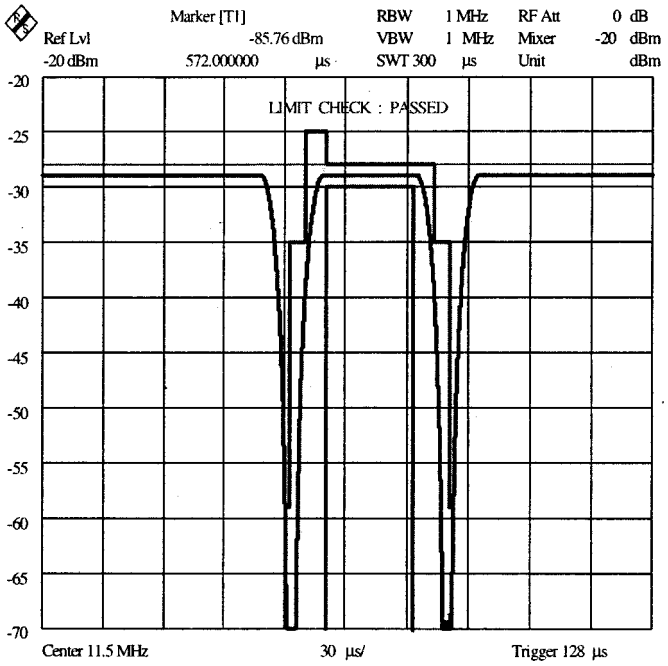

Fig. 11. Measured transmitted power level of the burst versus time. Observe that the middle part of the burst is not shown.

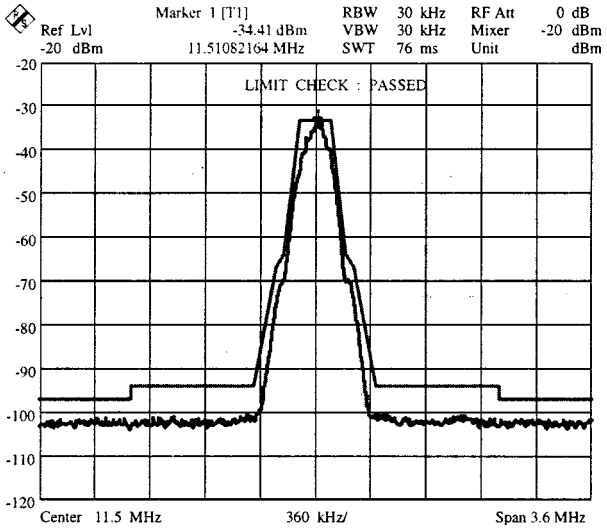

Fig. 12. Measured power spectrum of the modulated carrier.

Fig. 11 shows the measured ramp-up and ramp-down profiles of the transmitted burst, which satisfy the GSM base-station power versus time masks. The allowed power of spurious responses originating from the power ramping before and after the bursts are specified by the switching transient limits. Some margin (3 dB) has been left between the values in [26] and the values specified for this implementation in Table II to take care of the other transmitter stages that might degrade the spectral purity of the signal. The power levels measured at the digital output are well below the limits shown in Table II, while the power levels measured at the D/A converter output cannot conform to the target requirements due to the dynamic range limitations of the D/A converter.

TABLE II
SPECTRUM DUE TO SWITCHING TRANSIENTS (PEAK-HOLD MEASUREMENT, 30 KHZ FILTER BANDWIDTH, REFERENCE $\geq$ 300 kHz WITH ZERO OFFSET)

Offset (kHz)	Maximum Power Limit (dBc)	Measured Maximum Power (dBc) at Digital Output	Measured Maximum Power (dBc) at D/A converter Output
400	- 60	-71.20	-63.85
600	- 70	-78.09	-62.56
1200	- 77	-84.97	-64.66
1800	- 77	-86.23	-63.88

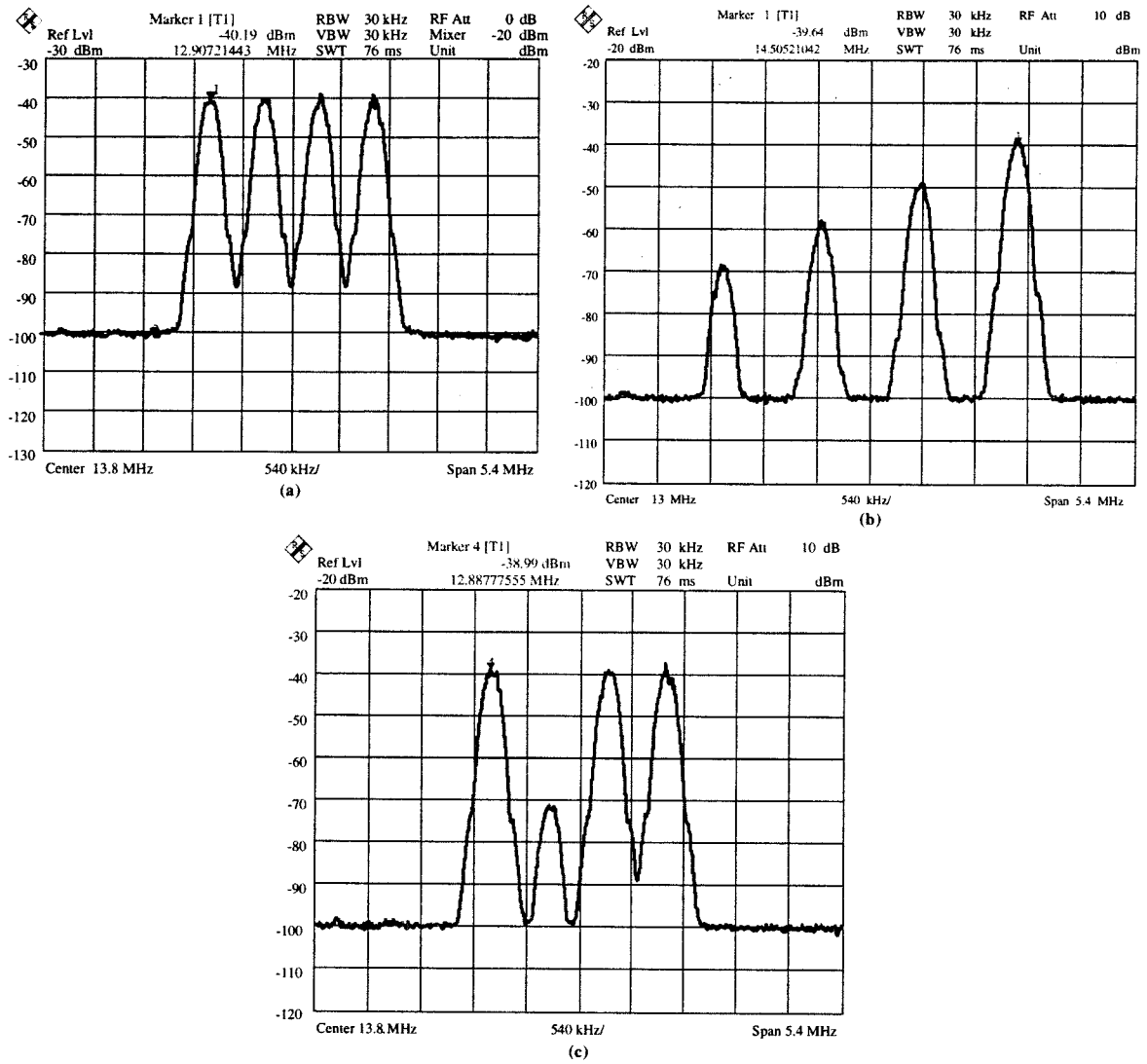

Fig. 13. Measured four carriers. (a) At maximum dynamic power level. (b) With different power levels (relative power-level difference is 10 dB). (c) One is 32 dB below the others.

The single carrier in Fig. 12 fulfills the modulation spectrum requirements for microcell base stations [26]. Fig. 13(a) shows the multicarrier output, where all carriers are at maximum dynamic power level. Fig. 13(b) and (c) shows carriers with different power levels. The problem with a digital ramp generator and output power-level controller is the reduced carrier-to-noise C/N ratio at low dynamic power-control levels because the dynamic power control is realized by scaling in the digital domain. However, according to the specification, the modulation spectrum is measured only at the maximum dynamic power-control level [26] and, hence, the reduced C/N ratio at low power-control levels does not present a problem in meeting the specifications. The effect of the C/N ratio degradation on the inband signal quality is negligible, since even at the lowest dynamic power-control level, the relative noise power is small enough not to affect signal quality.

VIII. Conclusion

The multicarrier GMSK modulator with a 14-bit on-chip D/A converter is presented. The digital modulator fulfills spectrum and phase-error specifications for GSM 900/1800/1900 base stations for pico-, micro-, and macrocells. The switching transients power levels and power spectra measured at the D/A converter output cannot conform to the target requirements due to the dynamic range limitations of the D/A converter. The new digital ramp generator and output power-level controller performs both the burst ramping and the dynamic power control in the digital domain. The maximum dynamic performance is obtained by multiplexing two D/A converters with output sampling switches. The major limiting factor of digital IF multicarrier modulator performance at base-station applications is the D/A converter, because the development of D/A converters does not keep up with the capabilities of digital signal processing with faster technologies. The die area of the chip is 26.8 mm^2 in 0.35-μm CMOS (in BiCMOS) technology. Power consumption is 706 mW at 3.3 V with 52 MHz.

Acknowledgment

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