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# A 14-bit 110 MHz CMOS D/A Converter

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## Abstract

A 14-bit D/A current steering converter is presented. A segmented current source architecture is utilised and well designed and carefully laid out switch drivers and current switches are used. The measured INL and DNL are 1.04 and 0.83 respectively. The D/A converter operates with a power supply of 3.3 V. The power consumption is 52 mW at 100 MHz. The D/A converter was fabricated with a 0.35  $\mu\text{m}$  CMOS technology.

## 1. Introduction

There is a trend toward fully integrated systems in wireless communication, therefore the interfaces between digital and analog parts becomes more and more important and challenging as high-speed and high-accuracy digital-to-analog converters are needed.

For high-speed and high-resolution applications (>50 MHz, >10 bits), the current source switching architecture is preferred since it can drive a low impedance load directly without the need for a voltage buffer. This paper describes a high speed current steering D/A converter with a resolution of 14 bits.

In the following paragraphs the realisation of the D/A converter will be presented in more detail. Among other things the effect of output cascades in the current cells is studied. Finally the measurement results are presented.

## 2. D/A Architecture

The major limiting factor of digital IF modulator performance at base station applications is the D/A converter, because the development of D/A converters does not keep up with the capabilities of digital signal processing with faster technologies [1]. The wordlength was chosen to be 14 bits in order to allow the modulator to have a multi-carrier feature that imposes high dynamic range requirements for the D/A converter. The 14-bit D/A converter is based on a segmented current steering architecture [2]. It consists of a 6b MSB matrix (2b binary and 4b thermometer coded), and an 8b binary coded LSB matrix (Figure 1). The D/A-converter is implemented with a differential design, which results in reduced even-order distortions and provides a common-mode rejection to disturbances.

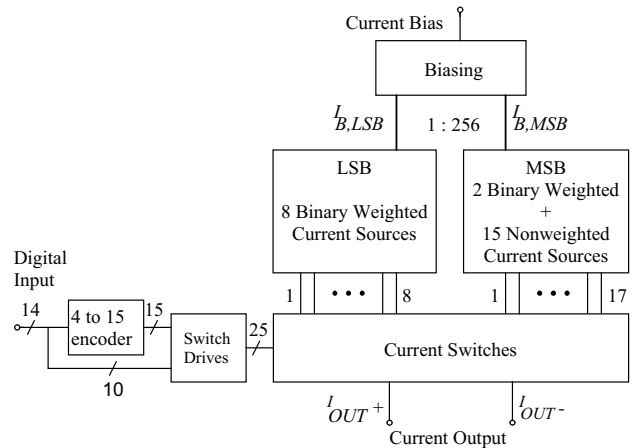


Figure 1. Block diagram of the D/A converter

### 2.1. Linearity

Dynamic linearity is important in this D/A converter since the modulator inputs a strongly varying signal, whilst good static linearity is a prerequisite for obtaining a good dynamic linearity. For a current-steering D/A converter, static linearity is mainly determined by the matching behaviour of the current sources and the finite output impedance of the current source. The static linearity is achieved by sizing the current sources for intrinsic matching [2] and using layout techniques and increasing current cell output impedance by biasing the switch transistors in the saturation region and adding cascode devices.

### 2.2. Switch Drivers

It is well known that the dynamic performance of a current-steering D/A converter is limited by three factors: 1) voltage fluctuation in the output nodes of the current sources due to improper timing of the switching off and on of the switch transistors; 2) feedthrough of the control signals to the output lines; and 3) imperfect synchronisation of the control signals of the switching transistors. To minimise these three effects, a well designed and carefully laid out synchronised switch driver is used [2]. A major function of the switch driver shown in Fig. 2 is to adjust the cross point of the control voltages, and to limit their amplitude at the gates of the current switches, so that these transistors are never simultaneously off and that the

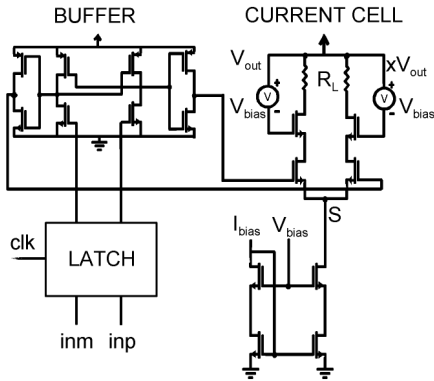


Figure 2. Switch driver and current cell

feedthrough is minimised. The crossing point of the control signals is set by using different rise and fall times for the driver's differential output [2, 3] and by delaying the falling edge of the signal [4].

A buffer is inserted between the latch and the current cell to adjust further the crossing point of the differential outputs. The reduced voltage swing is achieved by lowering the power supply of the buffer. Dummy switch transistors were used to improve the synchronisation of control signals of the switch transistors.

### 2.3. Current cells

By dividing the current source array into separately biased MSB- and LSB-arrays, so that they both contain current sources for half the bits and that the MSB unit current source is 256 times wider than the LSB unit source, the number of unit current sources required falls from 4096 to 63+255 in a 14-bit D/A converter [5]. This improves the settling time of the converter [6] and the output impedance at the higher signal frequencies [5]. On the downside, the current generated by the MSB unit current sources has to be a very accurate 256 times the LSB unit current. This requires a trimmable biasing scheme for the MSB current sources. Therefore a  $4\frac{1}{2}$ -LSB digital calibration system and an analog calibration system were implemented in the biasing scheme. Disturbances connected to the external bias current are filtered out on-chip with a simple one pole low-pass filter.

### 2.4. Cascode transistors

Cascode transistors between the current sources and the switches are used to increase the output impedance of the current cell, which improves the linearity of the D/A-converter shown in Figure 2 [4].

The effect of cascode transistors in the output lines was studied by bypassing the cascode transistors in the layout in such a way that the bypassing metal paths could be cut in postprocessing. The purpose of the cascode transistors is to isolate the drains of the switch transistors from the output lines and thus minimise the feedthrough to the output lines and to increase the output impedance further in the current cell [4]. Unfortunately, these cascodes increase the output settling time and cause different rise and fall

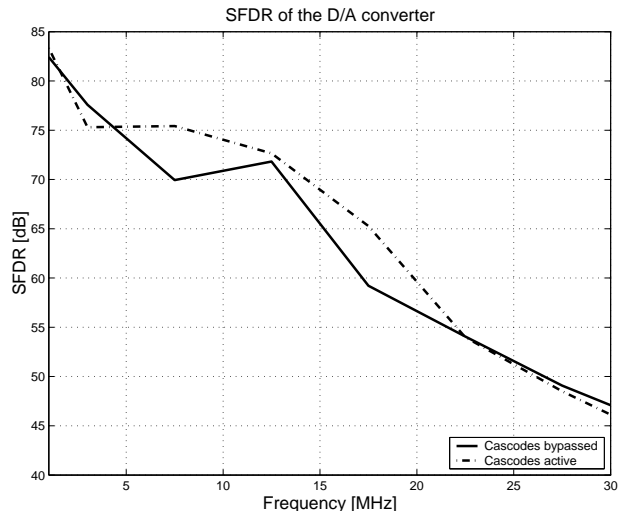


Figure 3. SFDR comparison with cascodes bypassed and active.

times for single-ended outputs, though the latter is cancelled partly in the differential output. The measurements show that between 5 MHz and 20 MHz the cascode transistors slightly improve the SFDR and between 22 MHz and 30 MHz the SFDR is slightly better without the cascode transistors. The results are shown in Figure 3.

## 3. Measurements

To evaluate the multi-standard modulator and the D/A converter, a test board was built and a computer program was developed to control the measurements. Figure 4 illustrates the block diagram of the test system. Measurements were performed with a 50  $\Omega$  doubly terminated cable. The sampling rate of the D/A converter was 76.8 MHz in most of the measurements. Figure 5 shows that typical integral linearity (INL) and differential linearity (DNL) errors are 1.04/0.83 LSB, respectively. The spurious free dynamic range (SFDR) is shown as a function of the output frequency in Figure 6. The SFDR to Nyquist frequency is better than 80 dBc at low synthesized frequencies, decreasing to 62 dBc at high synthesized frequencies in the output frequency band (single tone). Here the biasing current was optimised unlike in Figure 3. The output signal in Figure 7 meets the EDGE spectrum mask requirements [7]. Figure 8 shows the WCDMA output with a crest factor of 11.43 dB, where the adjacent channel leakage powers (ACLR1/2) are 65.84 and 67.67 respectively. The adjacent channel specifications are met (45/50 dB) [8]. The measurement results are summarised in Table 1.

## 4. Conclusion

A 14-bit differential current steering has been realised in a 0.35  $\mu\text{m}$  CMOS technology. The measured INL and DNL are 1.04 and 0.83 respectively. The D/A converter operates with a power supply of 3.3 V. The power consumption is 52 mW at 100 MHz. The chip microphotograph is presented in Figure 9. The die area of the D/A converter is 3.45  $\text{mm}^2$ .

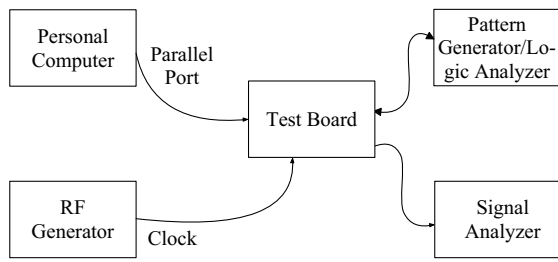


Figure 4. Block diagram of the test system

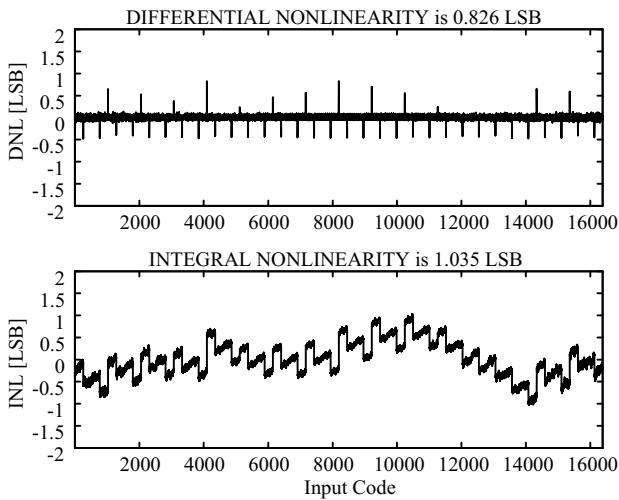


Figure 5. Typical INL and DNL

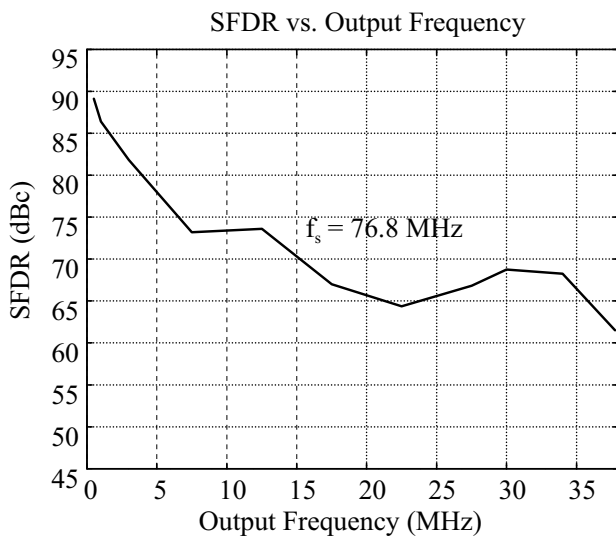


Figure 6. SFDR as function of output frequency at full-scale (0 dBFS)

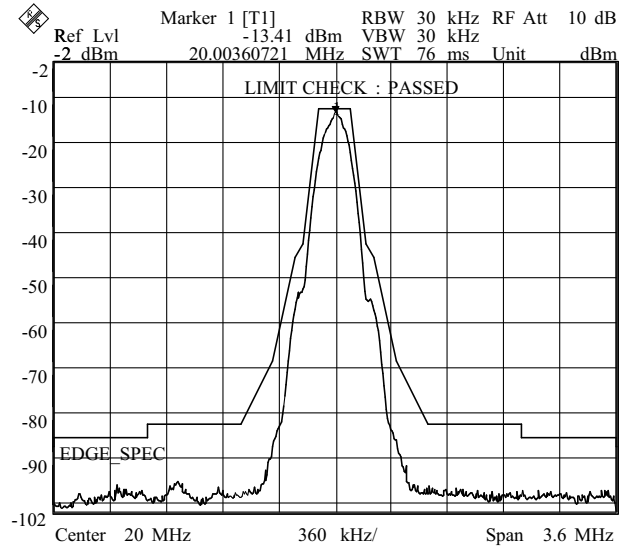


Figure 7. Power spectrum of EDGE signal

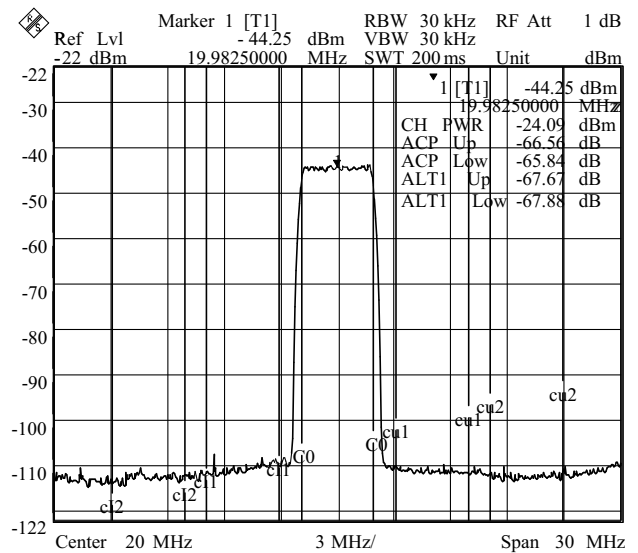


Figure 8. Power spectrum of WCDMA signal

Table 1. Measured D/A converter performance

Resolution	14
INL	1.04
DNL	0.83
Full scale output current	12.8 mA
Sampling rate	Up to 110 MHz
SFDR ( $f_s = 76.8$ MHz, $f_{\text{signal}} = 30$ MHz)	68 dBc
Power dissipation ( $f_s = 100$ MHz, $f_{\text{signal}} = 20$ MHz)	52 mW
Process	0.35 $\mu\text{m}$ CMOS
D/A converter area	3.45 $\text{mm}^2$

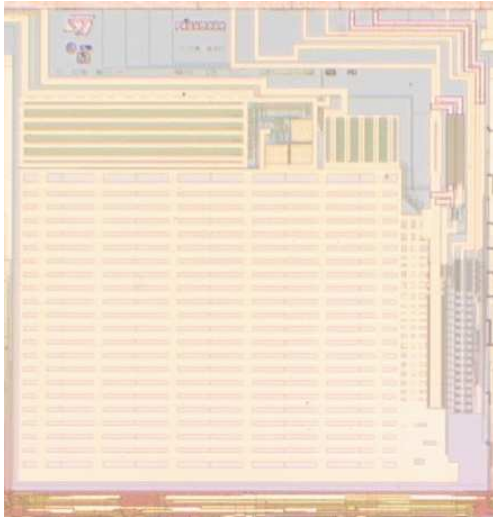


Figure 9. Microphotograph of the D/A converter

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