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A Digital Quadrature Modulator With On-Chip D/A Converter

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***Abstract*—The first analog IF mixer stage of a transmitter can be replaced with this digital quadrature modulator. The modulator interpolates orthogonal input carriers by 16 and performs digital quadrature modulation at carrier frequencies $f_s/4, -f_s/4, f_s/2$ (f_s is the sampling frequency). A 12-b digital-to-analog (D/A) converter is integrated with the digital quadrature modulator. A segmented current source architecture is combined with a proper switching technique to reduce spurious components and to enhance dynamic performance. The digital quadrature modulator is designed to fulfill the spectral, phase, and EVM specifications of GSM, EDGE, and WCDMA base stations. The die area of the chip is 27.09 mm^2 (0.35-μm CMOS technology) and the total power consumption is 1.02 W with 2.8 V at 500-MHz output sampling rate (0.78-W digital modulator, 0.24-W D/A converter).**

***Index Terms*—Digital quadrature modulator, digital–analog conversion, mixed analog–digital integrated circuits, multirate signal processing.**

I. Introduction

A LOGICAL progression from the previous multistandard modulator [1] and multicarrier work [2] is to move the digital-to-analog (D/A) interface even closer to the antenna in the base station transmitter structure. In traditional transmitters, a complex baseband signal is digitally modulated to the first intermediate frequency (IF) and then mixed to the second IF frequency and to the radio frequency (RF) in the analog domain. The first analog IF mixer stage of the transmitter can be replaced with the digital quadrature modulator presented in this paper as shown in Fig. 1. The two complex modulators are in series with the quadrature modulator as shown in Fig. 2. In the digital complex modulators, the baseband in-phase I and quadrature Q channels are modulated onto orthogonal carriers (X, Y) at the IF frequency at the lower sampling rate. The tunable complex modulator, steered by the carrier NCO, enables the fine tuning of the transmitted carrier frequency with subhertz resolution, whereas the digital quadrature modulator is used for the coarse tuning. It is beneficial to implement the fine tuning at lower sampling frequencies and the coarse tuning at the higher frequencies, because of the smaller amount of hardware associated with the coarse tuning implementation. The quadrature modulator interpolates orthogonal input carriers by 16 and performs a digital quadrature modulation at carrier frequencies $f_s/4, -f_s/4,$ and $f_s/2$ (f_s is the sampling frequency). It allows the quadrature modulation to be performed in the digital domain with high precision and perfect I/Q-channel matching. The major limiting factor of digital IF modulator performance at base station applications is the D/A converter, because the development of D/A converters does not keep up with the capabilities of digital signal processing with faster technologies [3].

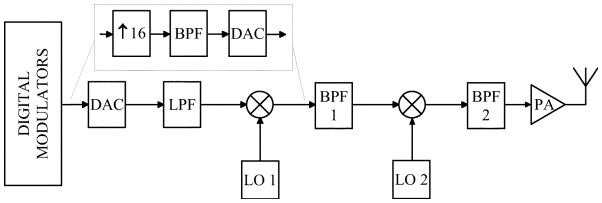

Fig. 1. Digital quadrature modulator replacing the first analog IF mixer stage.

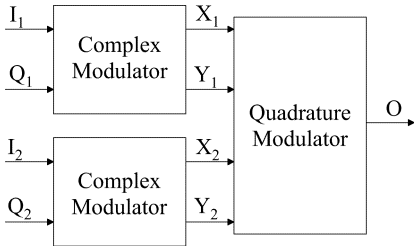

Fig. 2. Two complex modulators in series with the quadrature modulator.

This paper is organized as follows. Section II provides a description of the multiplier-free quadrature modulation, while Section III describes the interpolation filters. The on-chip D/A converter is described in Section IV. The topic of Section V is the need for a significant design effort at the physical level with respect to mixed-signal high-speed monolithic devices. Finally, experimental results obtained from the chip are presented in Section VI; this is followed by a few concluding comments.

II. Multiplier-Free Quadrature Modulation

The outputs of the complex modulators in Fig. 2 are

$$X_i(n) = I_i(n)\cos(\omega_{Ci}n) + Q_i(n)\sin(\omega_{Ci}n)$$
$$Y_i(n) = Q_i(n)\cos(\omega_{Ci}n) - I_i(n)\sin(\omega_{Ci}n) \quad (1)$$

where $I_i(n)$ and $Q_i(n)$ are pulse-shaped and interpolated in-phase and quadrature-phase data symbols, which are modulated onto the orthogonal [in-phase $(X_i(n))$ and quadrature-phase $(Y_i(n))$] carriers at frequency f_{Ci} [1], [2]. The output of the quadrature modulator in Fig. 2 is

$$O(n) = X(n)\cos(2\pi n f_{\text{out}}/f_s) + Y(n)\sin(2\pi n f_{\text{out}}/f_s) \quad (2)$$

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TABLE I
SOLUTIONS FOR MULTIPLIER-FREE QUADRATURE MODULATION

f_{out}/f_s	$\cos(2\pi n f_{out}/f_s)$	$\sin(2\pi n f_{out}/f_s)$	$X(n)\cos(2\pi n f_{out}/f_s) + Y(n)\sin(2\pi n f_{out}/f_s)$
0	$\cdots 1 \cdots$	$\cdots 0 \cdots$	$\cdots X(n) \cdots$
1/2	$\cdots 1, -1 \cdots$	$\cdots 0, 0 \cdots$	$\cdots X(n), -X(n) \cdots$
1/3	$\cdots 1, -0.5, -0.5 \cdots$	$\cdots 0, \frac{\sqrt{3}}{2}, -\frac{\sqrt{3}}{2} \cdots$	$\cdots X(n), -X(n)/2+Y(n)\frac{\sqrt{3}}{2}, -X(n)/2-Y(n)\frac{\sqrt{3}}{2} \cdots$
1/4	$\cdots 1, 0, -1, 0 \cdots$	$\cdots 0, 1, 0, -1 \cdots$	$\cdots X(n), Y(n), -X(n), -Y(n) \cdots$
-1/4	$\cdots 1, 0, -1, 0 \cdots$	$\cdots 0, -1, 0, 1 \cdots$	$\cdots X(n), -Y(n), -X(n), Y(n) \cdots$
1/6	$\cdots 1, 0.5, -0.5, -1, -0.5, 0.5 \cdots$	$\cdots 0, \frac{\sqrt{3}}{2}, \frac{\sqrt{3}}{2}, 0, -\frac{\sqrt{3}}{2}, -\frac{\sqrt{3}}{2} \cdots$	$\cdots X(n), X(n)/2+Y(n)\frac{\sqrt{3}}{2}, -X(n)/2+Y(n)\frac{\sqrt{3}}{2}, -X(n), -X(n)/2-Y(n)\frac{\sqrt{3}}{2}, X(n)/2-Y(n)\frac{\sqrt{3}}{2} \cdots$
1/8	$\cdots 1, \frac{1}{\sqrt{2}}, 0, -\frac{1}{\sqrt{2}}, -1, -\frac{1}{\sqrt{2}}, 0, \frac{1}{\sqrt{2}} \cdots$	$\cdots 0, \frac{1}{\sqrt{2}}, 1, \frac{1}{\sqrt{2}}, 0, -\frac{1}{\sqrt{2}}, -1, -\frac{1}{\sqrt{2}} \cdots$	$\cdots X(n), X(n)/\sqrt{2}+Y(n)/\sqrt{2}, Y(n), -X(n)/\sqrt{2}+Y(n)/\sqrt{2}, -X(n), -X(n)/\sqrt{2}-Y(n)/\sqrt{2}, -Y(n), X(n)/\sqrt{2}-Y(n)/\sqrt{2}, \cdots$

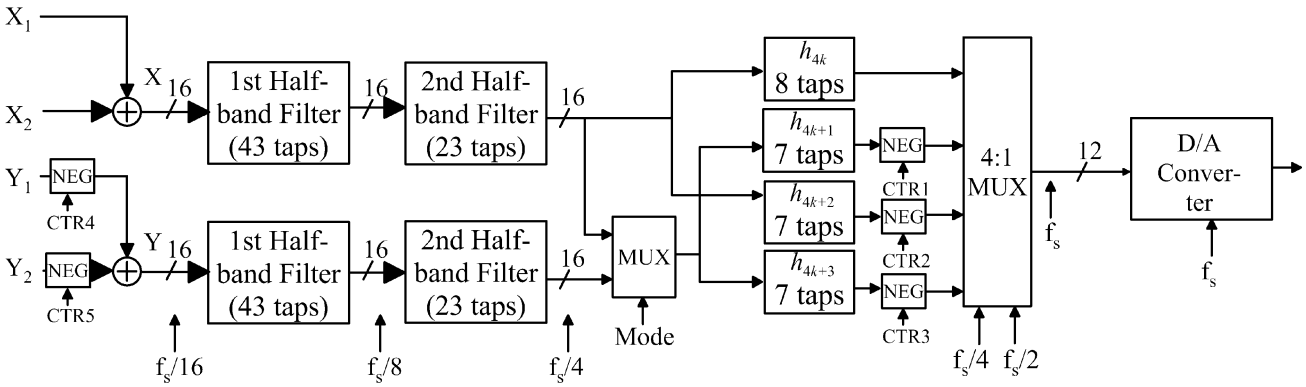

Fig. 3. Detailed block diagram of digital quadrature modulator in Fig. 2.

where f_s and f_{out} are the sampling and output frequency, and $X(n), Y(n)$ are interpolated in-phase and quadrature-phase carriers, respectively. Solutions for the quadrature modulation, when f_{out}/f_s is equal to $0, 1/2, 1/3, 1/4, -1/4, 1/6$, and $1/8$, are listed in Table I. In order to implement a multiplier-free quadrature modulation, we must therefore require that for all values of n, the quadrature modulator output (2) leads either to $+1, -1$, or 0 for sine and cosine terms in Table I. However, it should be noted that the multiplications by $0.5, -0.5, 1/\sqrt{2}, -1/\sqrt{2}, \sqrt{3}/2$, and $-\sqrt{3}/2$ in other cases are also relatively simple to implement with hardware shifts and canonic signed digit (CSD) multipliers. The multiplications could also be included in the filter coefficients of X and Y branches. Furthermore, if we require that either the sine or cosine term is zero in (2) for every n, then for each output value only one of the in-phase or quadrature-phase part needs to be processed, which reduces hardware [4], [5]. It can be seen from Table I that when f_{out}/f_s is equal to $0, 1/2, 1/3, 1/4$, and $-1/4$, our requirements are fulfilled. Using these values, high-speed digital multipliers and adders are not needed in the implementation of the quadrature modulation in (2). Instead, multiplexers (MUXs) and negators (NEGs) can be used.

The well known Coordinate Rotation Digital Computer (CORDIC) rotator could be also used as a quadrature modulator [1], [2], [6]. It can be implemented as a multiplier-free solution having only shift and add operations. However, since an N-bit input requires approximately N stages, the complexity is higher than in the implementation in Fig. 3. Since the CORDIC is inherently sequential, with the input of one stage depending on the result from the previous stage, parallelizing CORDIC-based systems can be difficult. Therefore, the speed requirement (500 MHz) is difficult to meet with the CORDIC algorithm.

III. INTERPOLATION FILTERS

The in-phase and quadrature-phase parts of the carriers from two complex modulators can be summed in the digital quadrature modulator (Fig. 3), which allows the formation of the multicarrier signal. The sampling rate of the input samples is first increased by four with two half-band interpolation filters as shown in Fig. 3. The passband of the first half-band filter restricts the maximum output frequency of the complex modulator in Fig. 2 to be about 2/5 of the input sampling rate of the quadrature modulator. The last filter has an interpolation ratio of four, therefore, the polyphase decomposition has four polyphase filters. The quadrature modulation in (2) for $f_{\text{out}}/f_s = 0, 1/2, 1/4, -1/4$ (see Table I) can be performed by negators in the polyphase filter outputs and 4 : 1 MUX as shown in Fig. 3. In the low-pass mode [$f_{\text{out}}/f_s = 0$ in (2)], the output

consists only of in-phase carriers (see Table I). Therefore, only the X samples are driven to the polyphase filters. This is selected by the mode signal illustrated in Fig. 3. Furthermore, the negators are disabled in the low-pass mode. In the band-pass mode [$f_{\rm out}/f_s = 1/4$ or $f_{\rm out}/f_s = -1/4$ in (2)], the output consists of the interleaved X and Y samples (see Table I). Furthermore, every second X and Y sample is negated. Therefore, the X samples are driven to the first and third polyphase filter and the Y samples to the second and fourth polyphase filter. The third and fourth polyphase filter outputs are negated. The quadrature modulation by $f_{\rm out}/f_s = 1/4$ or $f_{\rm out}/f_s = -1/4$ can be performed by selecting whether to negate the Y branches or not (control signals CTR4 and CTR5 in Fig. 3). In the high-pass mode [$f_{\rm out}/f_s = 1/2$ in (2)], the output consists only of in-phase carriers and every second sample is negated (see Table I). Therefore, the X samples are driven to the polyphase filters, and the second and fourth of the polyphase filter outputs are negated.

The digital quadrature modulator interpolates input carriers by 16. Therefore, the transition band for the analog reconstruction filter is increased and the images are suppressed more in the low-pass mode, thus reducing the complexity of the analog reconstruction filter. Furthermore, the $\sin(x)/x$ rolloff over the effective passband is significantly reduced. In the low-pass and high-pass modes, the information in the quadrature-phase carrier is lost, because the output consists only of in-phase carriers in those modes (Table I). The output frequency of the complex modulator in Fig. 2 should be higher than dc in those modes, because then the quadrature-phase data $Q_i(n)$ is modulated to the in-phase carrier in (1). Furthermore, the frequency should be considerably higher than dc in the low-pass and high-pass modes, so that the images generated by the analog upconversion could be filtered by the band-pass filter (BPF 2 in Fig. 1) (low-pass mode), and the images generated by the D/A conversion could be filtered by the analog reconstruction filter (BPF 1 in Fig. 1) (high-pass mode). In the band-pass mode, there are no such restrictions.

As mentioned, the quadrature modulation in (2) is performed by the negators and 4 : 1 MUX shown in Fig. 3. This may be considered to represent a frequency upshift of the interpolation filters' passband to the desired frequency. The digital modulator magnitude responses in the low-pass, band-pass, and high-pass modes are shown in Fig. 4. The combination of the filters provides more than 74-dB image rejection (pass-band ripple of 0.004 dB). The transition band in the low-pass mode (Fig. 4) is from 0.023–0.04 f_s. The images related to the last interpolation stage are shown in Fig. 5. The image selection is achieved by changing the filter passband. In the band-pass mode, the first or second image in Fig. 5 can be chosen by the negation of Y branches (control signals CTR4 and CTR5 in Fig. 3). This selection can be made independently from each orthogonal carrier, thus almost doubling the output bandwidth in the band-pass mode as shown in Fig. 5. If the odd image is used, then the output spectrum can be inverted (mirrored about carrier frequency) in the complex modulator [1]. This is achieved by changing the sign of the complex modulator carrier frequency (the direction of the vector rotation) in (1).

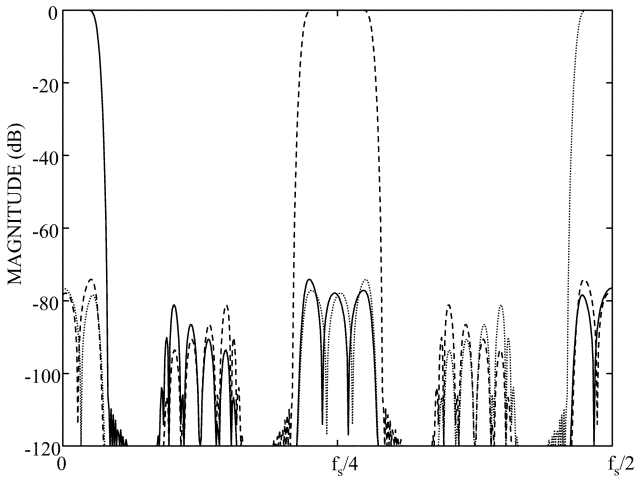

Fig. 4. Digital quadrature modulator magnitude response in the low-pass (-), band-pass (–) and high-pass modes (··).

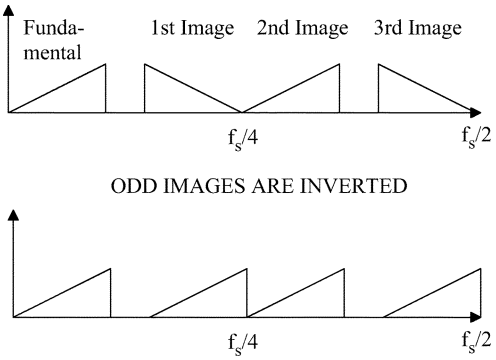

Fig. 5. Images in frequency domain.

The internal wordlengths of the modulator are shown in Fig. 3. The wordlengths were chosen such that the 12-bit D/A converter quantization noise dominates the digital output noise.

IV. D/A Converter

From a systems perspective, integration of the D/A converter into the digital system is desirable to avoid high-speed multibit data crossing over the interchip boundary. The 12-bit on-chip D/A converter is based on a segmented current-steering architecture. It consists of a 6-b MSB matrix (2-b binary and 4-b thermometer coded) and a 6-b binary-coded LSB matrix as shown in Fig. 6. Dynamic linearity is important in this modulator because of the strongly varying signal, although good static linearity is a prerequisite for obtaining a good dynamic linearity. For a current-steering D/A converter, the static linearity is mainly determined by the matching behavior of the current sources and the finite output impedance of the current source. The static linearity is achieved by sizing the current sources for intrinsic matching, using layout techniques and increasing current cell output impedance by biasing the switch transistors in the saturation region and adding cascode devices.

The integral nonlinearity (INL) of a D/A converter is in this paper defined to be the difference between the analog output value and the straight line drawn between the output values corresponding to the smallest and the largest input code, divided by

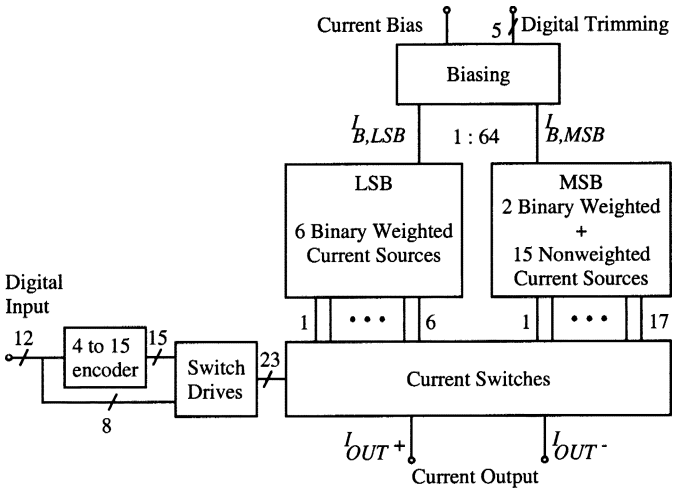

Fig. 6. Block diagram of the 12-b D/A converter.

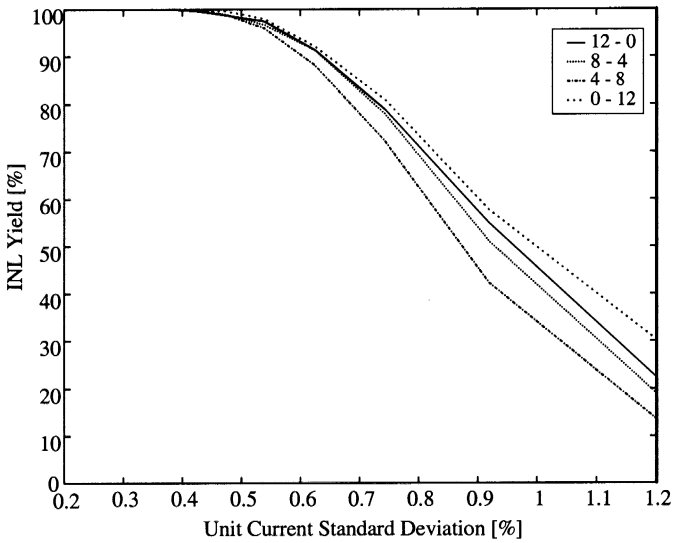

Fig. 7. Yield estimation as function of the unit current source standard deviation (with zero mean).

the average LSB step. The INL yield is then given by the ratio of the number of functional D/A converters ($|\mathrm{INL}| < \pm 1/2\,\mathrm{LSB}$) to the total number of tryouts. A direct relationship exists between the INL yield and the transistor matching of the used technology that can be expressed by the relative unit current source standard deviation $\sigma(I)/I$ [7]. Assuming that each unit current source has a value that follows a normal distribution, the required accuracy is given by [7]

$$\frac{\sigma(I)}{I} = \frac{1}{2C\sqrt{2^N - 1}} \tag{3}$$

where C depends only on the INL yield requirement and N is the number of bits. The relationship between the INL yield requirement and the C for a fully segmented and binary weighted D/A converter, based on Monte Carlo simulations, has been presented [8]. For partially segmented architectures, corresponding values have not been presented. Monte Carlo simulations are, therefore, used to estimate the INL yield as a function of the unit current source standard deviation as shown in Fig. 7. In Fig. 7, the INL performance, which is dependent on the segmentation level, is shown for four segmentation levels (0-12, 4-8, 8-4, 12-0), where the first number tells the number of the segmented bits. Interestingly, neither the fully segmented (12-0) nor binary weighted (0-12) converter gives the worst yield as shown in Fig. 7. At the segmentation level of (4-8), the D/A converter suffers more severely from INL than differential nonlinearity (DNL) according to the simulations, therefore, the INL yield defines the requirements for standard deviation. In this case, for an INL yield of 99.99%, a unit current source standard deviation of 0.26% is required (Fig. 7).

It is well known that the dynamic performance of a current-steering D/A converter is limited by three factors: 1) voltage fluctuation in the output nodes of the current sources due to improper timing of the switching off and on of the switch transistors; 2) feedthrough of the control signals to the output lines; and 3) imperfect synchronization of the control signals of the switching transistors. To minimize these three effects, a well-designed and carefully laid out synchronized switch driver is used [9]. A major function of the switch driver shown in Fig. 8 is to adjust the cross point of the control voltages, and to limit their amplitude at the gates of the current switches, in such a way that these transistors are never simultaneously in the off state and that the feedthrough is minimized. The crossing point of the control signals is set by using different rise and fall times for the driver's differential output [9], [10]. A buffer is inserted between the latch and the current cell to further adjust the crossing point of the differential outputs. The reduced voltage swing is achieved by lowering the power supply of the buffer (Vbuf in Fig. 8). Dummy switch transistors were used to improve the synchronization of the control signals of the switch transistors. The sizing of the dummy transistors was optimized by simulations. The cascode transistor between the current sources and the switches is used to increase the output impedance of the current cell, which improves the linearity of the D/A converter shown in Fig. 8 [11]. To minimize the feedthrough to the output lines and to increase the output impedance further in the current cell, the drains of the switching transistors are isolated from the output lines by adding cascode transistors [11]. Unfortunately, these cascodes increase the output settling time and cause different rise and fall times for single-ended outputs, although the latter is cancelled partly in the differential output. By dividing the current source array into separately biased MSB and LSB arrays, in such way that they both contain current sources for half the bits and that the MSB unit current source is 64 times wider than the LSB unit source, the number of unit current sources required falls from 1024 to $63+63$ in a 12-b D/A converter [12]. This layout reduces the parasitic capacitances at the drain nodes of the current source transistors by reducing the amount of wiring needed to connect the transistors, as well as by reducing the parasitic capacitances caused by the transistors themselves [12]. This improves the settling time of the converter [13] and the output impedance at the higher signal frequencies [12]. The scheme also reduces the area required by the current source matrices by allowing routing on top of the MSB transistors, as well as by reducing the amount of silicon area wasted in the process dependent spaces between the transistors [12]. The drawback is that the current generated by the MSB unit current sources has to

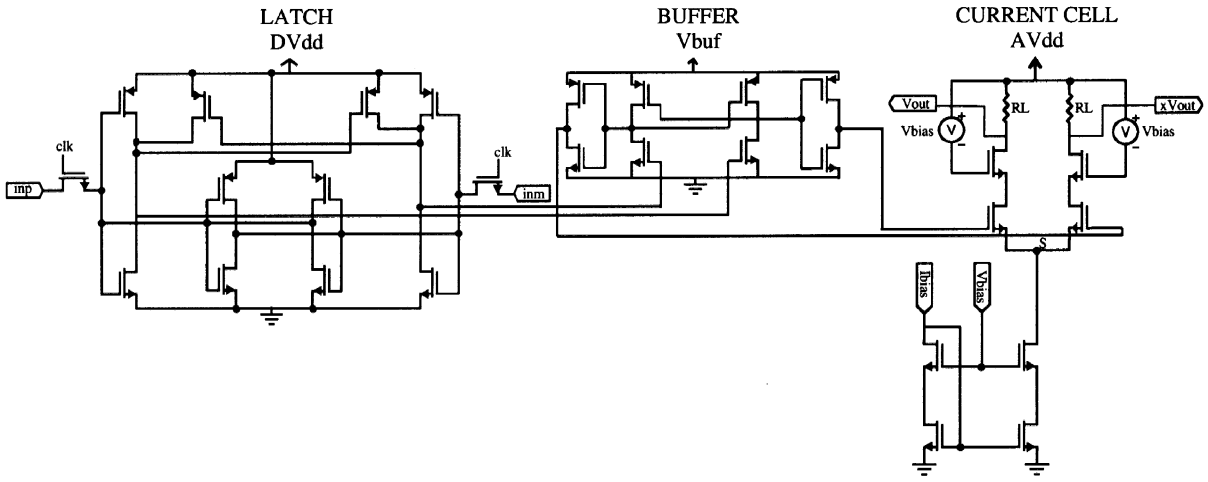

Fig. 8. Switch driver and current cell.

be very accurately 64 times the LSB unit current. This requires a trimmable biasing scheme for the MSB current sources.

V. Implementation and Layout

The digital part of the quadrature modulator, excluding the 4 : 1 MUX illustrated in Fig. 3, was synthesized from the VHDL description using a standard 0.35-μm CMOS cell library. Multirate systems are efficiently implemented using a polyphase structure in which sampling rate conversion and filtering operations are combined. The problem is that for a series of polyphase filters in Fig. 3, during some of the sampling instants there is much more computation than during others. Thus, the switching noise is periodic, and this tends to affect the timing on the D/A converter current switches, introducing a large phase modulation (PM) component. The use of the divided clocks in Fig. 3 can cause more jitter at every other D/A converter sampling instant, which raises unwanted sideband in the band-pass mode. The PM component is reduced by shielding the D/A converter clock. Furthermore, the power supplies of the digital logic and the analog part are routed separately and the digital and analog parts are placed to isolated wells to minimize the noise coupling to the analog output through the substrate. The last filter stage shown in Fig. 3, was implemented using a pipelined carry–save architecture due to the high-speed requirements. The taps of the folded transposed direct form finite impulse response (FIR) filters were realized with CSD coefficients. The static timing check and pre-layout timing simulations were performed for the netlist, and the chip layout was completed using place and route tools. Finally, based on the parasitic information extracted from the layout, the post-layout delays were back annotated to ensure satisfactory chip timing. Since the output of the 4 : 1 MUX shown in Fig. 3 operates at f_s, the multiplexer has been manually designed and laid out at the transistor level. In order to reduce the ground bounce in the digital part and to minimize the coupling of the switching noise from the digital logic to the D/A converter output, on-chip decoupling capacitors (total capacitance of 2 nF) are used. To enhance the D/A converter dynamic performance, the layout of the switch drivers and current outputs were designed as symmetrical as possible. A clock delay line was used to ensure optimal settling of switch driver control signals at the sampling instants.

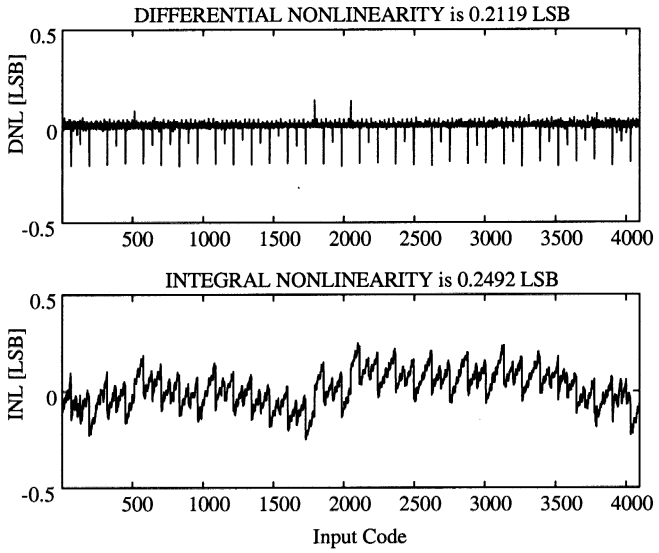

Fig. 9. Typical DNL and INL.

VI. Measurement Results

The orthogonal carriers to the digital quadrature modulator are generated by the multistandard modulator [1] in measurements. The on-chip D/A converter was used in measurements. Measurements are performed with a 50-Ω doubly terminated cable. Fig. 9 shows that typical INL and DNL errors are 0.25/0.21 LSB, respectively. Fig. 10 shows the spurious free dynamic range (SFDR) as a function of relative output frequency. The digital quadrature modulator was bypassed in the SFDR measurements (Fig. 10), because the output frequency response of the digital quadrature modulator has only low-pass, band-pass, and high-pass modes (see Fig. 4). The data was driven directly to the D/A converter. The maximum operation frequency of the input pads was 250 MHz, which is the highest sampling frequency in Fig. 10. The D/A converter performance is summarized in Table II.

TABLE II
MEASURED D/A CONVERTER PERFORMANCE

Resolution	12 bit
INL	0.25 LSB
DNL	0.21 LSB
Full-scale output current	17.2 mA
Sampling rate	Up to 500 MHz
Two tone SFDR (f_s = 150 MHz, f_{out1} = 39.75 MHz, f_{out2} = 45.75 MHz)	58.7 dBc
Power consumption (f_s = 500 MHz)	240 mW
Process	0.35μm CMOS
D/A converter core area	3.73 mm^2

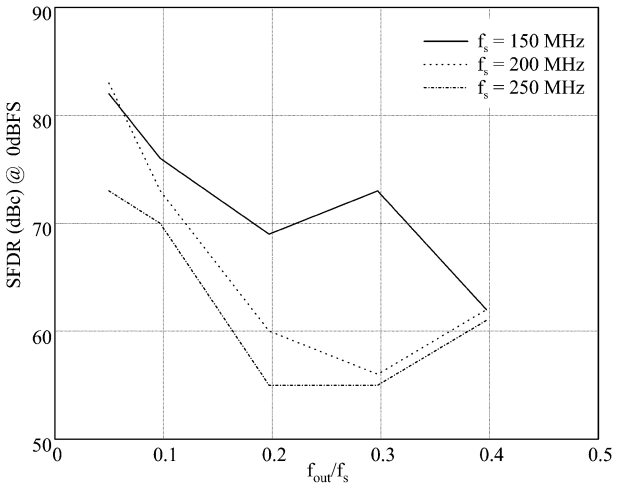

Fig. 10. SFDR as function of relative output frequency at full-scale (0 dBFS).

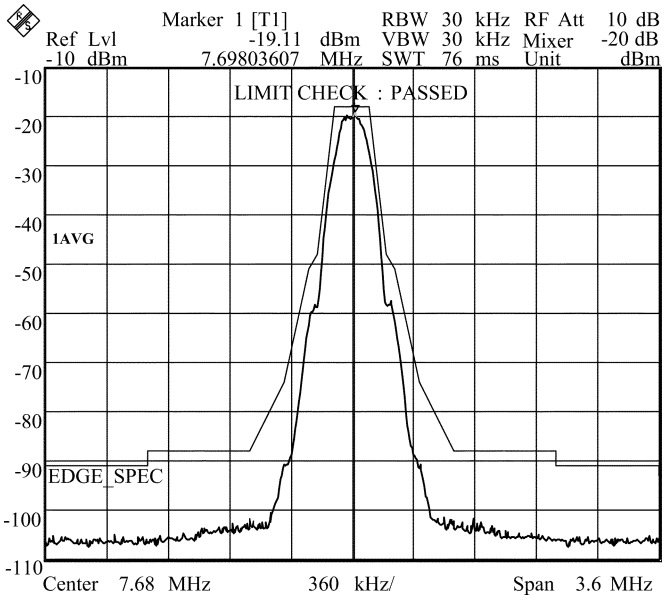

Fig. 11. Power spectrum of the EDGE signal in the low-pass mode.

The digital quadrature modulator is designed to fulfill the spectral, phase, and EVM specifications of GSM, EDGE, and WCDMA base stations. The EDGE output signal in the low-pass mode fulfills the EDGE spectrum mask requirements set out in Fig. 11 [14]. Fig. 12 shows the WCDMA output with

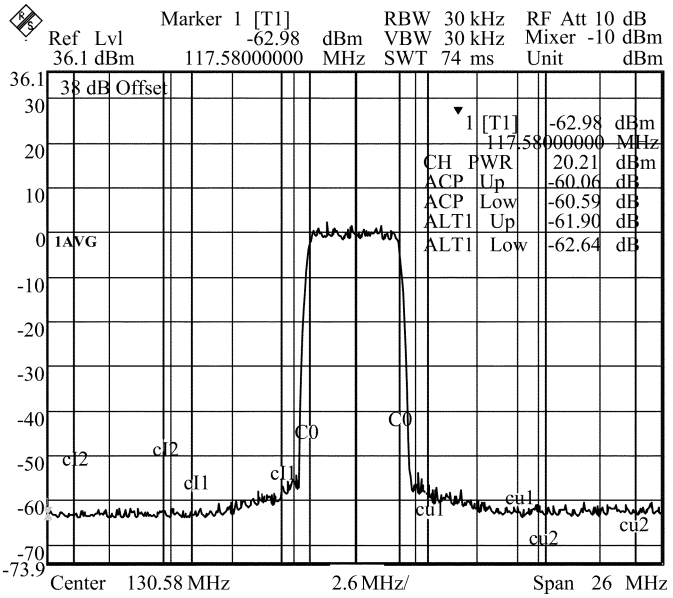

Fig. 12. Power spectrum of the WCDMA signal in the band-pass mode.

a crest factor of 8.48 dB in band-pass mode, where the adjacent channel leakage powers (ACLR1/2) are 60.06 and 61.90 dB, respectively, which fulfill the specifications (45/50 dB) [15]. The ACLR1/2 are 77.07 and 82.12 dB at the D/A converter input, so most of the errors are generated less by quantization errors in the digital domain and more by the D/A converter analog nonidealities. The D/A converter sampling frequency was 491.52 MHz in the Figs. 11 and 12, and the input carrier sampling frequency was 30.72 MHz ($f_s/16$ in Fig. 3). The measured phase error in GSM signal is 0.31° rms with a maximum peak deviation of 0.91°. The phase error specifications are 5° with a peak of 20° [14]. The phase error is low, because the quadrature modulation is performed digitally with high precision.

VII. CONCLUSION

The first analog IF mixer stage of a transmitter can be replaced with this digital quadrature modulator. The modulator interpolates orthogonal input carriers by 16 and performs $f_s/4, -f_s/4, f_s/2$ digital quadrature modulation. A 12-b D/A converter is integrated with the digital quadrature modulator. A segmented current source architecture is combined with a

Fig. 13. Chip microphotograph.

proper switching technique to reduce spurious components and enhance dynamic performance. The die area of the chip is 27.09 mm^2 (0.35-μm CMOS technology). Total power consumption is 1.02 W at 2.8 V at 500-MHz output sampling rate (0.78-W digital modulator, 0.24-W D/A converter). The IC is in a 160-pin CQFP package. Fig. 13 displays the chip microphotograph.

REFERENCES

[1] J. Vankka, J. Ketola, J. Sommarek, O. Väänänen, M. Kosunen, and K. Halonen, "A GSM/EDGE/WCDMA modulator with on-chip D/A converter for base stations," *IEEE Trans. Circuits Syst. II*, vol. 49, pp. 645–655, Oct. 2002.

[2] M. Kosunen, J. Vankka, M. Waltari, and K. Halonen, "A multicarrier QAM modulator for WCDMA basestation with on-chip D/A converter," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 2001, pp. 301–304.

[3] J. Vankka and K. Halonen, *Direct Digital Synthesizers: Theory, Design and Applications*. Norwood, MA: Kluwer, 2001.

[4] B. C. Wong and H. Samueli, "A 200-MHz all-digital QAM modulator and demodulator in 1.2-μm CMOS for digital radio applications," *IEEE J. Solid-State Circuits*, vol. 26, pp. 1970–1979, Dec. 1991.

[5] S. Darlington, "On digital single-sideband modulators," *IEEE Trans. Circuit Theory*, vol. CT-17, pp. 409–414, Aug. 1970.

[6] J. E. Volder, "The CORDIC trigonometric computing technique," *IRE Trans. Electron. Comput.*, vol. EC-8, pp. 330–334, Sept. 1959.

[7] A. Van den Bosch, M. Steyaert, and W. Sansen, "An accurate statistical yield model for CMOS current-steering D/A converters," *Analog Integrat. Circuits Signal Process.*, vol. 29, pp. 173–180, Dec. 2001.

[8] Y. Cong and R. L. Geiger, "Formulation of INL and DNL yield estimation in current-steering D/A converters," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2002, pp. III.149–III.152.

[9] A. Van den Bosch, M. A. F. Borremans, M. S. J. Steyaert, and W. Sansen, "A 10-bit 1-Gsample/s Nyquist current-steering CMOS D/A converter," *IEEE J. Solid-State Circuits*, vol. 36, pp. 315–324, Mar. 2001.

[10] T. Y. Wu, C. T. Jih, J. C. Chen, and C. Y. Wu, "A low-glitch 10-bit 75-MHz CMOS video D/A converter," *IEEE J. Solid-State Circuits*, vol. 30, pp. 68–72, Jan. 1995.

[11] H. Takakura, M. Yokoyama, and A. Yamaguchi, "A 10-bit 80-MHz glitchless CMOS D/A converter," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1991, pp. 26.5.1–26.5.4.

[12] J. Bastos, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 12-bit intrinsic accuracy high-speed CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1959–1969, Dec. 1998.

[13] S. Y. Chin and C. Y. Wu, "A 10-bit 125-MHz CMOS digital-to-analog converter (DAC) with threshold-voltage compensated current sources," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1374–1380, Nov. 1994.

[14] "Radio Transmission and Reception," GSM Recommendation 05.05, Dec. 1999.

[15] "Radio Transmission and Reception," 3rd Generation Partnership Project, Technical Specification Group Radio Access Networks, UTRA (BS) FDD, 3G TS 25.104, V3.3.0, June 2000.

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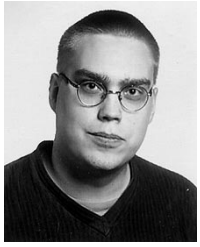

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