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Digital Modulator with Bandpass Delta-Sigma Modulator

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Abstract

A digital quadrature modulator with a bandpass $\Delta\Sigma$-modulator is presented that interpolates orthogonal input carriers by 16 and performs a digital quadrature modulation at carrier frequencies $f_s/4$, $-f_s/4$, (f_s is the sampling frequency). After quadrature modulation, the signal is converted into an analogue IF signal using a bandpass $\Delta\Sigma$ modulator and a 1-bit D/A converter. The die area of the chip is 5.2mm^2(0.13μm CMOS technology). The total power consumption is 139mW at 1.5V with a clock frequency of 700MHz (D/A converter full-scale output current 11.5mA).

Keywords: current steering differential pair, digital quadrature modulator, bandpass $\Delta\Sigma$-modulator, 1-bit D/A-converter, multirate system

1. Introduction

In traditional transmitters, a complex baseband signal is usually modulated to the first intermediate frequency (IF) in the digital domain and then mixed to the second IF and to the radio frequency (RF) using analogue mixers. We present a digital quadrature modulator that modulates the signal from the first IF to the second IF in the digital domain, thus only one analogue mixer is needed as illustrated in Fig. 1. The digital quadrature modulator is fed by two digital complex modulators, shown in Fig. 2, which modulate the baseband in-phase (I) and quadrature (Q) channels into orthogonal carriers (X, Y) at the first IF frequency. One example of such a complex modulator suitable for this purpose is presented in [1]. These complex modulators can be operated at a much lower sampling frequency than the quadrature modulator. The complex modulators take care of the fine tuning of the transmitted carrier frequency with a sub-Hz resolution, whereas the digital quadrature modulator is used for the coarse tuning. It is beneficial to implement the fine tuning at lower sampling frequencies and the coarse tuning at the higher frequencies, because of the smaller amount of hardware associated with the coarse tuning implementation. The quadrature modulator interpolates orthogonal input carriers by 16 and performs a digital quadrature modulation moving the carriers around frequencies $f_s/4$ and $-f_s/4$, where f_s is the output sampling frequency. The key advantages in performing the quadrature modulation in the digital domain are the high precision achieved and the perfect I/Q-channel matching.

The major limiting factor of digital IF modulator performance in base station applications is the D/A converter, because the development of D/A converters does not keep up with the capabilities of digital signal processing with faster technologies [2]. In this design, the multi-bit D/A converter in [2] is replaced by the bandpass delta-sigma ($\Delta\Sigma$) modulator and 1-bit D/A converter. In addition, the sampling frequency f_s is increased to 700MHz. As the 1-bit delta sigma ($\Delta\Sigma$) D/A converter has only two levels, any misplacement of the levels results only in gain error or offset. Neither of those are of great importance in many applications. The 1-bit $\Delta\Sigma$-D/A converter is an all digital circuit, which has numerous advantages over analogue signal processing, such as flexibility, noise immunity, reliability and potential improvements in

performance and power consumption because of the scaling of the technology. In addition, the design, synthesis, layout and testing of digital systems can be highly automated. The DDS with 1-bit $\Delta\Sigma$-D/A converter is attractive in digital transmitters, where it allows the output transistors to be operated in a power-efficient switching mode, and thus may result in an efficient power amplifier [3, 4, 5, 6].

2. Digital Quadrature Modulator

Figure 3 shows the block diagram of the designed digital quadrature modulator. In order to produce a multi-carrier signal, the in-phase and quadrature-phase parts of the carriers from two complex modulators are summed in the quadrature modulator. After summing the carriers, the sampling rate is quadrupled using two half-band interpolation filters shown in Fig. 3. The passband of the first half-band filter restricts the maximum carrier frequency of the feeding complex modulators in Fig. 2 to be about two-fifths of the input sampling rate of the quadrature modulator. The last filter has an interpolation ratio of 4 and thus it is composed of four polyphase filters. After the quadrature modulation, the signal is converted into an analogue IF signal using a bandpass $\Delta\Sigma$ modulator and a 1-bit D/A converter.

2.1. Multiplier-free Quadrature Modulation

The conventional quadrature modulator requires two multipliers and an adder [7]. When performing a quadrature modulation to the frequency $f_s/4$, the output consists of interleaved X and Y samples, such that every other X and Y sample is negated ($\cdots X(n), Y(n), -X(n), -Y(n) \cdots$). This is achieved by arranging the outputs of the polyphase filters of the last interpolation filter appropriately using a 4:1 multiplexer and by negating the third and the fourth polyphase filter outputs as shown in Fig. 3 [8, 9]. These negations can be included in the coefficients of the third and fourth polyphase filters. The modulation to the frequency - $f_s/4$ instead of $f_s/4$ can be performed by negating the entire Y-branch ($\cdots X(n), -Y(n), -X(n), Y(n) \cdots$). The selection can be done independently for each of the orthogonal input carriers using the control signals CTR1 and CTR2 shown in Fig. 3. This functionality enables almost a doubled bandwidth.

The quadrature modulation may be considered to represent a frequency up-shift of the passband of the interpolation filters to - $f_s/4$ or $f_s/4$. The combination of the filters provides more than 74dB image rejection (passband ripple of 0.004dB).

2.2. Bandpass $\Delta\Sigma$ modulator

A block diagram of a digital fourth order bandpass $\Delta\Sigma$ modulator used in this design is shown in Fig. 4. Scaling factors have been added to the signal path to prevent overflows. The noise transfer function of the $\Delta\Sigma$ modulator produces a notch in the quantisation noise at the frequency of interest, i.e. $f_s/4$. The sampling frequency of 700MHz is demanding for the successive adders in Fig. 4. Moreover, due to the feedback loops, it is not possible to pipeline the structure in a conventional manner. The inherent delay elements (D) of the $\Delta\Sigma$ modulator have been utilised to ensure the right timing of the feedback loops when pipelining the design [10]. The $\Delta\Sigma$ modulator pipelined using this technique is illustrated in Fig. 5. The critical path of the structure in Fig. 5 consists of only one inverter and two full adders (FAs), instead of an inverter and 13 full adders needed in a conventional structure.

3. 1-bit D/A converter

Since the output of the 1 bit D/A converter is an analogue signal, it is susceptible to clock jitter, waveform fall/rise asymmetry and noise coupling. In the fully differential system used here, the D/A converter output rise and fall are inherently symmetric, so a simple non-return-to-zero output suffices [11]. The 1-bit D/A converter is a simple current steered differential pair with a current source as shown in Fig. 6. The latch and driver shown in Fig. 6 adjust the crossing

point of the control voltages and limit their amplitude at the gates of the current switches, so that that these transistors are never simultaneously off. This minimises the glitch energy at the output. The crossing point is set by the cross-coupled inverters, which generate differential output with different rise and fall times. A driver is inserted between the latch and the current switch to adjust further the crossing point of the differential outputs and to make the transitions smoother. The reduced voltage swing is achieved by increasing the negative power supply (V_{bias}) of the driver output so that the feedthrough to the output is minimised. Disturbances connected to the external bias current (I_{bias}) are filtered out on-chip with a simple one-pole low-pass filter. The 1-bit D/A converter in Fig. 6 does not need cascode current sources to enhance linearity as multi-bit D/A converters do. So it is suitable for low supply voltage operation.

4. Implementation

The digital part of the quadrature modulator was synthesised from a VHDL description using a standard 0.13μm CMOS cell library. Multirate systems are efficiently implemented using a polyphase structure in which sampling rate conversion and filtering operations are combined. The last filter stage shown in Fig. 3 was implemented using pipelined carry-save architecture due to the high speed requirements. The taps of the folded transposed direct form FIR filters were realised with canonic signed digit (CSD) coefficients. The static timing check and pre-layout timing simulations were performed for the netlist and the chip layout was completed using place and route tools. Finally, based on the parasitic information extracted from the layout, the post-layout delays were back-annotated to ensure satisfactory chip timing. In order to reduce the ground bounce in the digital part and to minimise the coupling of the switching noise from the digital logic to the D/A converter output, on-chip decoupling capacitors (total capacitance of 260pF) are used.

5. Measurement results

The digital part of the quadrature modulator was synthesised from a VHDL description using a standard 0.13μm CMOS cell library. Figure 7 shows the GSM signal at the 1-bit digital output. Figure 8 shows the GSM signal at the 1-bit D/A converter output, where the sampling and output frequencies are 700MHz and 175MHz, respectively. In Fig. 8 the GSM signal measured at the 1-bit D/A converter output fulfils the GSM spectrum mask requirements [12]. The spectral degradation at the analogue output (Fig. 8), is due to the clock jitter and non-ideal differential output. Figure 9 shows the WCDMA signal at the 1-bit D/A converter output, where the adjacent channel leakage power ratios ($\mathrm{ACLR}_{1,2}$) are 50.26dB and 40.27dB. Due to the ACLR specifications of 45/50dB [13], a bandpass filter is required to remove the remaining quantisation noise from the second adjacent channel.

6. Conclusions

The first analogue IF mixer stage of a transmitter can be replaced with this digital quadrature modulator. The modulator interpolates orthogonal input carriers by 16 and performs digital quadrature modulation at carrier frequencies $f_s/4$, $-f_s/4$, (f_s is the sampling frequency). After the quadrature modulation the signal is converted into an analogue IF signal using a bandpass $\Delta\Sigma$ modulator and a 1-bit D/A converter. The die area of the chip is 5.2mm^2 (0.13μm CMOS technology). The typical power consumption of the chip is 139mW with a 1.5V supply voltage, when 700MHz clock frequency and 11.5mA D/A converter full-scale output current are used. The IC is in a 144-pin BGA package.

7. References

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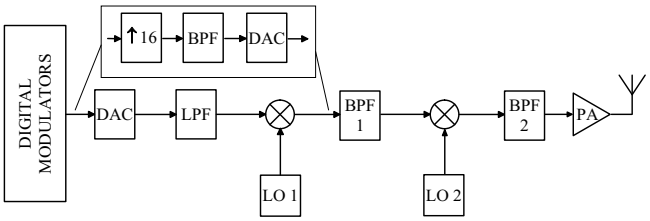

Fig. 1. The digital quadrature modulator replacing the first analogue IF mixer stage.

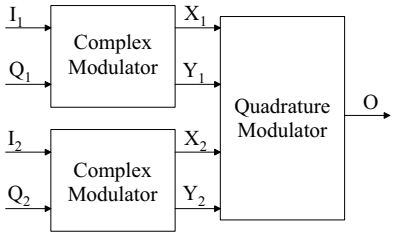

Fig. 2. Two complex modulators in series with the quadrature modulator.

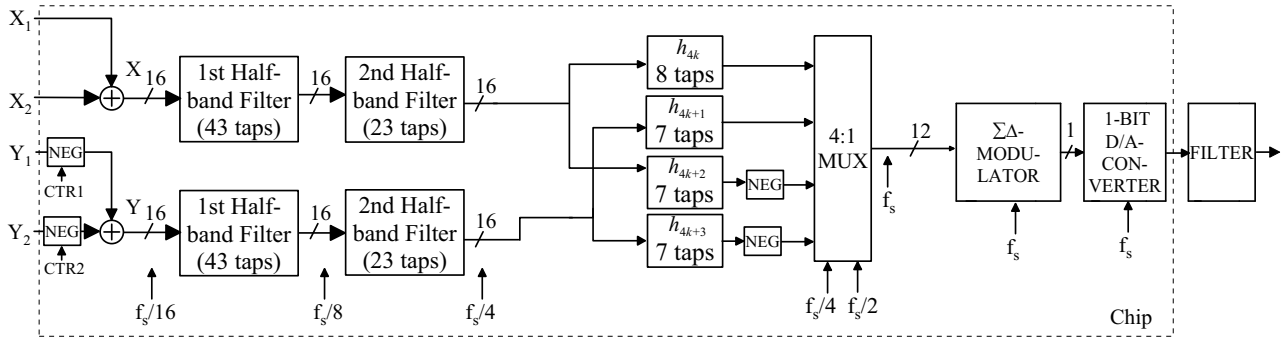

Fig. 3. Digital quadrature modulator.

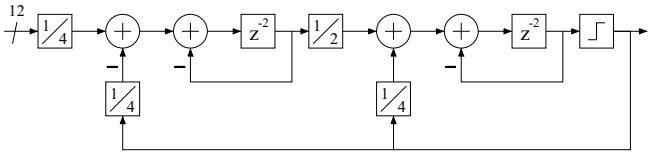

Fig. 4. 4th order bandpass $\Delta\Sigma$-modulator.

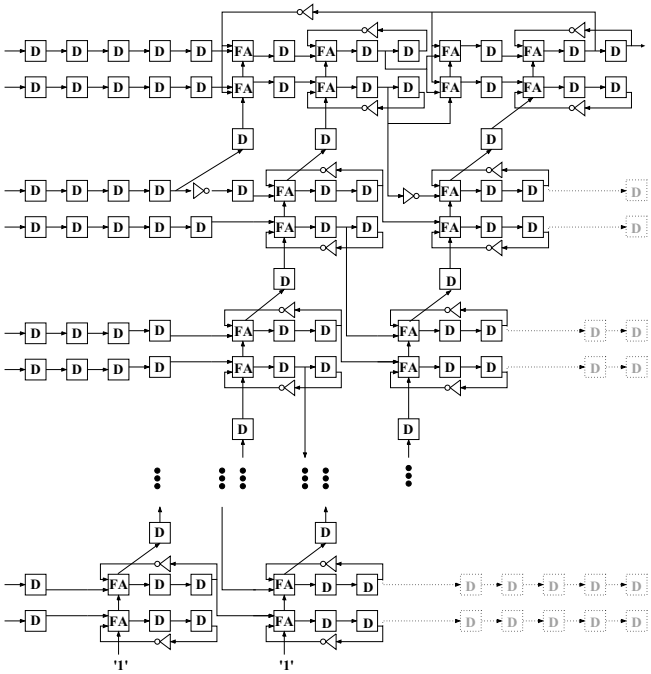

Fig. 5. Pipelined structure of 12-bit 4th order bandpass modulator.

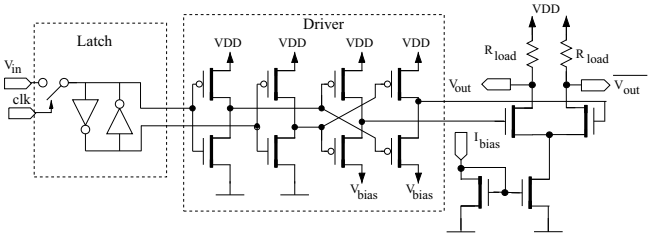

Fig. 6. Schematic of the 1-bit D/A converter.

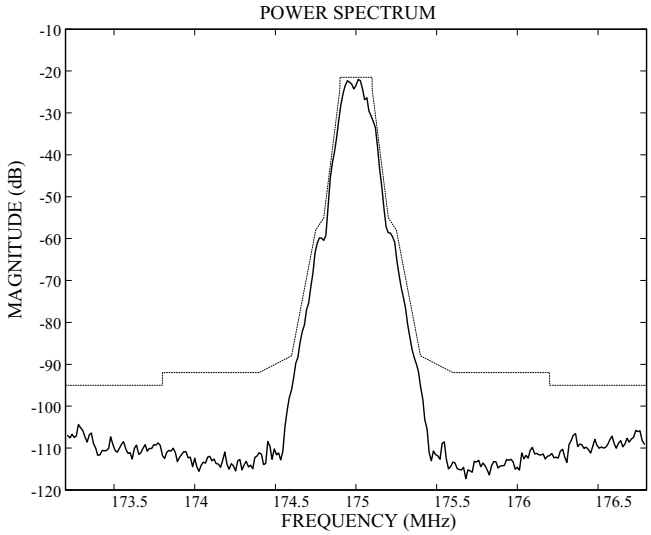

Fig. 7. Power spectrum of GSM signal at 1-bit digital output.

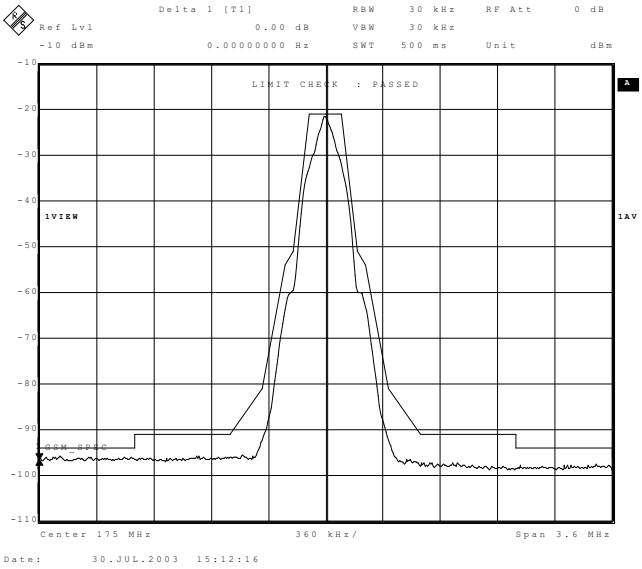

Fig. 8. Spectrum of GSM signal at 1-bit D/A converter output.

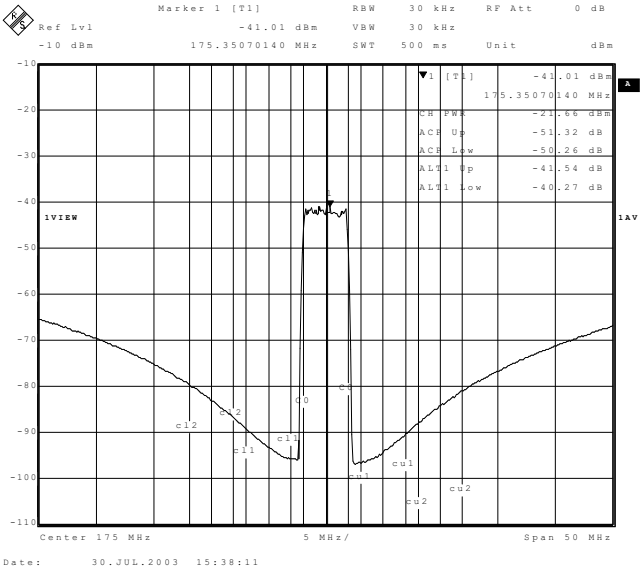

Fig. 9. Spectrum of WCDMA signal at 1-bit D/A converter output.