J. Lindeberg, J. Vankka, J. Sommarek and K. Halonen, A 1.5-V Direct Digital Synthesizer with Tunable Delta-Sigma Modulator in 0.13-µm CMOS, IEEE Journal of Solid-State Circuits, Vol. 40, No. 9, pp. 1978-1982, September 2005.

© 2005 IEEE

Reprinted with permission.

This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of Helsinki University of Technology's products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee.org.

By choosing to view this document, you agree to all provisions of the copyright laws protecting it.

A 1.5-V Direct Digital Synthesizer With Tunable Delta-Sigma Modulator in 0.13-μm CMOS

Jonne Lindeberg, Jouko Vankka, Johan Sommarek, and Kari Halonen

***Abstract*—In direct digital synthesizer (DDS) applications, the drawback of the conventional delta sigma ($\Delta\Sigma$) modulator structure is that its signal band is fixed. In the new architecture presented in this paper, the signal band of the $\Delta\Sigma$ modulator is tuned according to the DDS output frequency. We use a hardware-efficient phase-to-sine amplitude converter in the DDS that approximates the first quadrant of the sine function with 16 equal-length piecewise second-degree polynomial segments. The DDS is capable of frequency, phase, and quadrature amplitude modulation. The die area of the chip is 2.02 mm^2 (0.13 μm CMOS technology). The total power consumption is 138 mW at 1.5 V with an output frequency of 63.33 MHz at a clock frequency of 200 MHz (D/A converter full-scale output current: 11.5 mA).**

***Index Terms*—Delta sigma ($\Delta\Sigma$) modulator, direct digital synthesizer (DDS), digital quadrature modulator, digital-to-analog (D/A) converter.**

I. Introduction

TABLE I shows spurious free dynamic ranges (SFDRs) to Nyquist frequency in recently published direct digital synthesizers (DDSs) and D/A converters [1]–[6]. It is easy to achieve 100-dBc SFDR in the digital domain [6]. In the wide-output bandwidth DDSs, most spurs are generated less by quantization errors in the digital domain (see Table I, row 3) and more by analog nonidealities in the D/A converter (see Table I, row 4), because the development of D/A converter is not keeping pace with the capabilities of the digital signal processing with faster technologies [7].

A multibit D/A converter is susceptible to glitches and spurious noise (as the output frequency increases), which is difficult to remove by filtering. D/A converters with excellent amplitude resolution and frequency response tend to consume excess power and are expensive. As a 1-bit delta sigma ($\Delta\Sigma$) D/A converter has only two levels, any misplacement of the levels only results in gain error or offset. Neither of those is of great importance in many applications. The 1-bit $\Delta\Sigma$ D/A converter is an all-digital circuit, which has numerous advantages over analog signal processing, such as flexibility, noise immunity, reliability, and potential improvements in performance and power consumption because of the scaling of the technology. In addition, the design, synthesis, layout, and testing of digital systems can be highly automated. The DDS with a 1-bit $\Delta\Sigma$ D/A converter is attractive in digital transmitters, where it allows the output transistors to be operated in a power-efficient switching mode [8]–[11].

Manuscript received December 3, 2004; revised February 20, 2005.

The authors are with the Electronic Circuit Design Laboratory, Helsinki University of Technology, FIN-02150 Espoo, Finland (e-mail: jlindebe@ecdl.hut.fi).

Digital Object Identifier 10.1109/JSSC.2005.848140

The paper is organized as follows. The blocks of DDSs with tunable $\Delta\Sigma$ modulators are introduced in Section II. Experimental results are presented in Section III, followed by a few concluding comments.

II. Direct Digital Synthesizer With Tunable $\Delta\Sigma$ Modulator

The DDS with a tunable $\Delta\Sigma$ modulator is shown in a simplified form in Fig. 1. It has the following basic blocks: a phase accumulator, phase adder, phase-to-amplitude converter (sine output), multiplier, $\Delta\Sigma$ modulator, and 1-bit D/A converter. The DDS is capable of frequency, phase, and quadrature amplitude modulation.

A. Direct Digital Synthesizer

The phase value is generated using the modulo 2^j overflowing property of a j-bit phase accumulator ($j = 32$) in Fig. 1. The rate of the overflows is the output frequency [12], [13]

$$f_{\text{out}} = \frac{\Delta P f_s}{2^j}, \quad f_{\text{out}} \leq \frac{f_s}{2} \tag{1}$$

where ΔP is the phase increment word and f_s is the sampling frequency. The constraint in (1) comes from the sampling theorem. The phase increment word in (1) is an integer, and therefore the frequency resolution is found by setting $\Delta P = 1$

$$\Delta f = \frac{f_s}{2^j}. \tag{2}$$

The numerical period of the DDS output sequence (in clock cycles) is

$$Pe = \frac{2^j}{\text{GCD}(\Delta P, 2^j)} \tag{3}$$

where GCD $(\Delta P, 2^j)$ represents the greatest common divisor of ΔP and 2^j. By setting the least significant bit of the phase increment word to one, the numerical period is maximal. This has the effect of randomizing the errors introduced by the quantized phase-to-amplitude converter samples, because in a long output period the error appears as "white noise" [7]. The disadvantage is that it introduces an offset into the output frequency of the DDS. The offset will be small, if the ratio of the sampling frequency to the power of two of the phase accumulator length is low in (2). Another method is to use a dither signal to randomize the quantization error to prevent idle tones [8].

B. Quadrature Modulator

The frequency modulation could be superimposed on the hopping carrier by simply adding and subtracting a frequency

0018-9200/$20.00 © 2005 IEEE

TABLE I
SINGLE-TONE SFDR

Measured at	[1]	[2]	[3]	[4]	[5]	[6]	This work
Sampling Frequency	150 MHz	200 MHz	150 MHz	165 MHz	400 MHz	200 MHz	200 MHz
Digital Data at D/A Converter Input †	90.3 dBc	84.3 dBc	72 dBc	-	-	100 dBc	84 dBc
Analog Signal at D/A Converter Output	51.48 dBc @ 11.1 MHz Output	58.50 dBc @ 12 MHz Output	52 dBc @ 75 MHz Output	57 dBc @ 50 MHz Output	73 dBc @ 200 MHz Output	-	83 dBc @ 100 MHz Output ††

† In the digital domain, SFDR is achieved over tuning range (0 to Nyquist frequency)

†† In the analog domain, SFDR is achieved over in-band (2.5MHz)

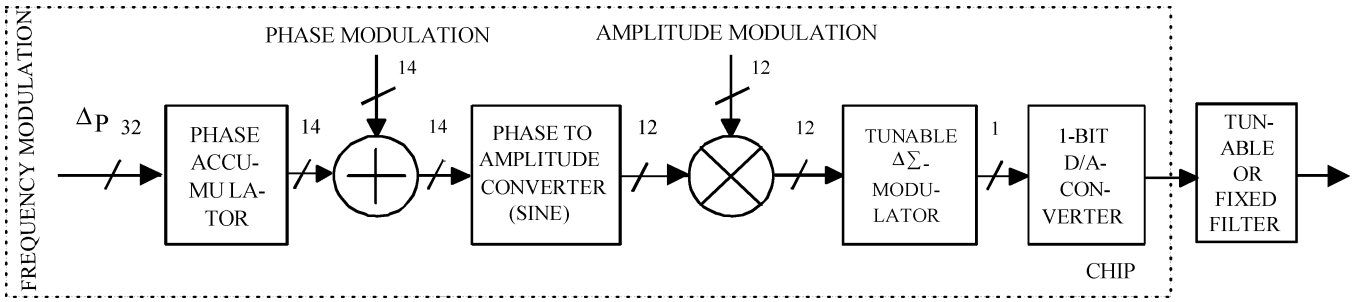

Fig. 1. DDS with tunable $\Delta\Sigma$ modulator.

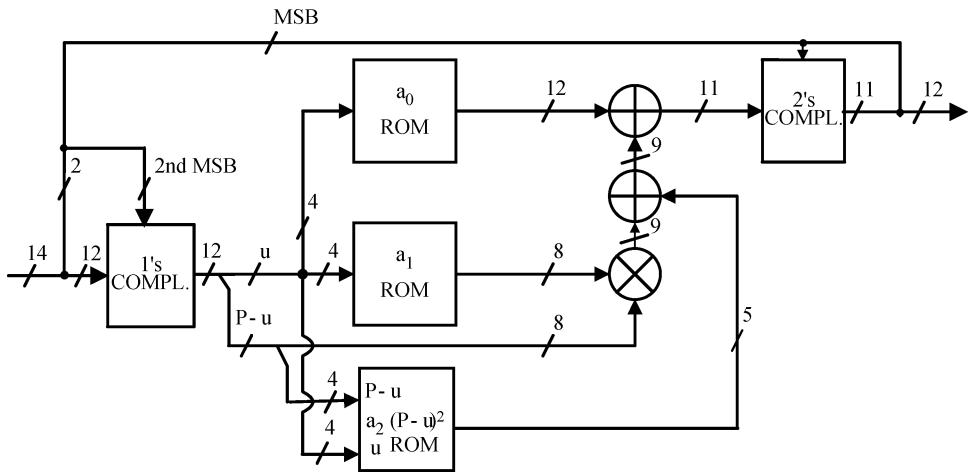

Fig. 2. Phase-to-amplitude converter for sine function in Fig. 1.

offset to/from ΔP. The quadrature amplitude modulation (QAM) could be performed

$$\begin{aligned} I_{\text{out}} &= I(n)\cos(\omega_{\text{out}}n) + Q(n)\sin(\omega_{\text{out}}n) \\ &= A(n)\cos\left(\omega_{\text{out}}n - P(n)\right) \end{aligned}$$

where

$$A(n) = \sqrt{I(n)^2 + Q(n)^2}$$

and

$$P(n) = \arctan\left(\frac{Q(n)}{I(n)}\right) \tag{4}$$

where $\arctan$ is the four-quadrant arctangent of the in-phase $(I(n))$ and quadrature phase data $(Q(n))$. The in-phase output is only needed in Fig. 1, which requires one adder for phase modulation $(P(n))$ before the phase-to-amplitude converter (sine) and a multiplier for amplitude modulation $(A(n))$ after the phase-to-amplitude converter according to (4).

C. Phase-to-Amplitude Converter

Due to the symmetry of the sine wave, only a quarter of the full samples are calculated. The full-wave output can be recovered by inverting the phase and amplitude appropriately, as shown in Fig. 2. The two most significant phase bits are used to decode the quadrant, while the remaining 12 bits are used to address a one-quadrant sine look-up table. The most significant bit determines the required sign of the result, while the second most significant bit determines whether the amplitude is increasing or

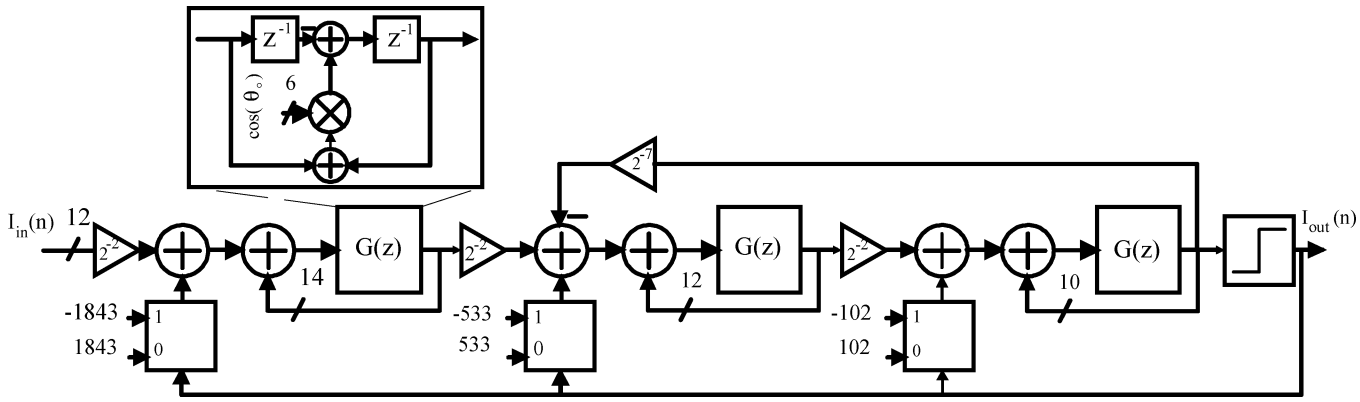

Fig. 3. Tunable sixth-order modulator.

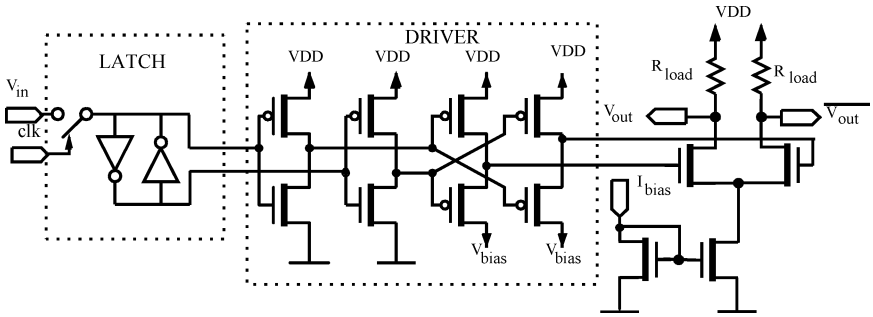

Fig. 4. Schematic of the 1-bit D/A converter.

decreasing. The quarter-wave sine function is approximated by the second-degree polynomial

$$\sin\left(\frac{\pi P}{2}+\frac{2\pi}{2^{15}}\right)=a_0(u)+a_1(u)(P-u)+a_2(u)(P-u)^2 \tag{5}$$

where $a_0(u)$, $a_1(u)$, and $a_2(u)$ are polynomial coefficients. A 1/2-LSB phase offset $(2\pi/2^{15})$ was introduced into the phase in order to reduce hardware [7]. The phase address of the quarter of the sine wave "P" is divided into the upper phase address "u" and the lower phase address "$P-u$." While higher order polynomials can be employed, their contribution to the accuracy is very small and, therefore, of little weight in this application. The coefficients are chosen using least-squares polynomial fitting. These coefficients vary according to the upper phase address "u." This method is the piecewise parabolic interpolation. The four most significant bits of the input phase are selected as the upper phase address "u," which is transferred simultaneously to two read-only memories (ROMs) as address signals as shown in Fig. 2. The output of the "a_0" ROM is the first term of the polynomial in (5) and is transferred to a first adder, where it will be summed with the remaining terms involved. The least significant bits "$P-u$" are multiplied by the output of the "a_1" ROM to produce the second term of the polynomial. The third term is computed in the ROM by multiplying the coefficient "a_2" and the square of the lower phase address "$P-u$." This is done by selecting the upper bits of "$P-u$" and "u" values as a portion of the address for the ROM. This is possible since the last term only roughly contributes four LSBs to the output. The discrete Fourier transform (DFT) of the sine wave approximated by the second-degree polynomial gives an SFDR of 87.09 dBc.

D. Tunable $\Delta\Sigma$ Modulator

With a basic $\Delta\Sigma$ modulator, only a small fraction of the bandwidth can be occupied by the required signal. The whole Nyquist bandwidth can be made available if a tunable $\Delta\Sigma$ modulator is employed. This is achieved by using the discrete-time low-pass-to-bandpass transform

$$z^{-1}\rightarrow -z^{-1}\frac{z^{-1}-\cos(\theta_o)}{1-\cos(\theta_o)z^{-1}} \tag{6}$$

which preserves both the realizability and maximum out-of-band gain constraint [8]. The notch frequency of the all-pass transfer function is

$$f_o=\frac{f_s\theta_0}{2\pi} \tag{7}$$

which is set the same as the DDS output frequency from (1).

A third-order noise transfer function (NTF) was designed for a maximum out-of-band gain of 1.52 (3.62 dB) with zeros optimized for minimum in-band noise at an over-sampling ratio of 64. The number of bits required in each stage and the interstage scaling coefficients were optimized using simulations. The complete modulator, including word lengths and coefficients, is depicted in Fig. 3. The order of the NTF is doubled by the substitution (6), since each delay is replaced by a second-order subfilter. Errors in approximating the coefficients for $\cos(\theta_o)$ simply result in a frequency shift of the filter's tuned notch, because the NTF zeros are shifted around the unit circle of the z plane. The block diagram of the all-pass transfer function $G(z)$ from (6) is shown in Fig. 3. Tuning is accomplished by changing the $\cos(\theta_o)$ multiplier of the all-pass network.

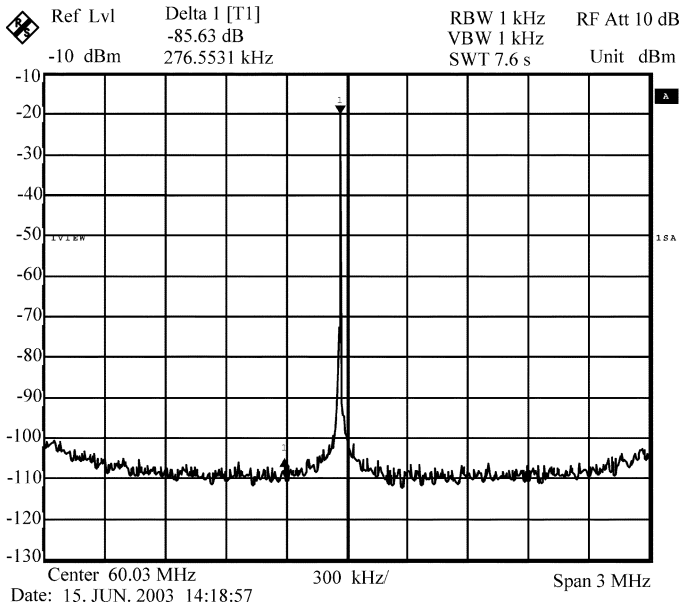

Fig. 5. Spectrum of 60-MHz sine wave with full-scale amplitude at 1-bit $\Delta\Sigma$ D/A converter output, where the sampling frequency is 200 MHz.

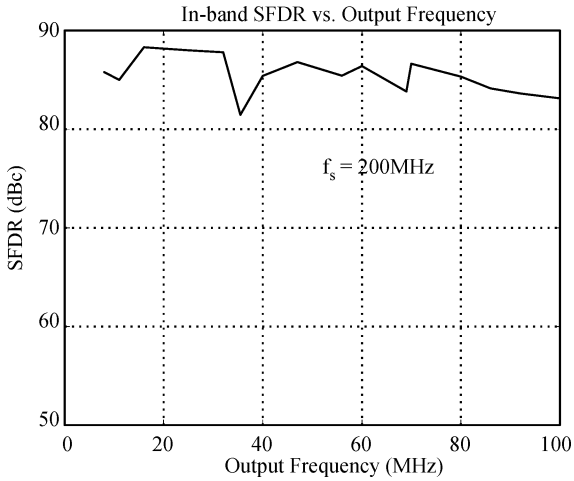

Fig. 6. In-band SFDR as function of output frequency at full scale (0 dBFS).

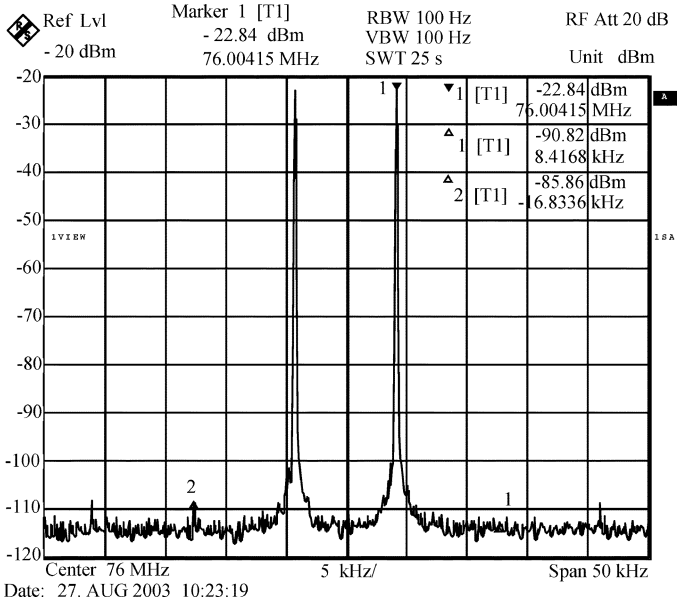

Fig. 7. Measured IMD.

E. 1-B D/A Converter

Since the output of the 1-bit D/A converter is an analog signal, it is susceptible to clock jitter, waveform fall/rise asymmetry and noise coupling [14]. In the fully differential system used here, the D/A-converter output rise and fall are inherently symmetric (the D/A-converter output is not data-dependent), so that a simple nonreturn-to-zero (NRZ) output suffices [15]. Furthermore, to reduce clock jitter sensitivity, the NRZ instead of return-to-zero (RZ) pulse shaping is utilized. The 1-bit D/A converter is a simple current steering differential pair with a current source as shown in Fig. 4. A major function of the latch and driver shown in Fig. 4 is to adjust the crossing point of the control voltages and limit the amplitude at the gates of the current switches in such a way that these transistors are never simultaneously in the off state. This minimizes glitch energy at the output. The crossing point of the control signals is set by the cross-coupled inverters, which generate differential output with different rise and fall times. A driver is inserted between the latch and the current switch to further adjust the crossing point of the differential outputs and to make the transitions smoother. The reduced voltage swing is achieved by increasing the negative power supply (V_{bias}) of the driver output so that the feedthrough to the output is minimized. Disturbances connected to the external bias current (I_{bias}) are filtered out on-chip with a simple one-pole low-pass filter. The 1-bit D/A converter in Fig. 4 does not need cascode current sources to enhance the linearity as the multibit D/A converters do. Thus, it is suitable for low supply voltage operation.

III. Measurement Results

Fig. 5 shows the 1-bit $\Delta\Sigma$ modulator output, where the signal frequency is 60 MHz. The in-band noise floor is approximately -85 dBFS. The in-band noise floor is approximately -85 dBFS. The major limiting factor of the in-band SFDR in Fig. 5 is the spectrum analyzer performance (noise floor). The sampling frequency of the DDS with a tunable $\Delta\Sigma$ modulator was 200 MHz in Figs. 5–9. The SFDR is shown as a function of the output frequency in Fig. 6. The in-band (2.5 MHz) single-tone SFDR is better than 83 dBc from dc to Nyquist frequency. Fig. 7 shows two-tone intermodulation distortion (IMD) at 76 MHz (sampling frequency 200 MHz) to be better than -85 dBc. It can be noticed from Fig. 7 that the odd-order distortion of the system does not limit the SFDR performance. Fig. 8 shows the QAM modulated output where the adjacent channel leakage power ratio is 61.63. The QAM signal has a symbol rate of 390.6 kHz (input symbols are filtered by root raised cosine filter $(\alpha = 0.22)$) in Fig. 8. In Fig. 9, the EDGE signal at the 1-bit D/A converter output fulfills the EDGE spectrum mask requirements [16].

The die area of the chip is 2.02 mm^2 (0.13 μm CMOS technology). Total power consumption is 138 mW at 1.5 V with an output frequency of 63.33 MHz at a clock frequency of 200 MHz (D/A converter full-scale output current 11.5 mA). The IC is in a 64-pin TQFP package.

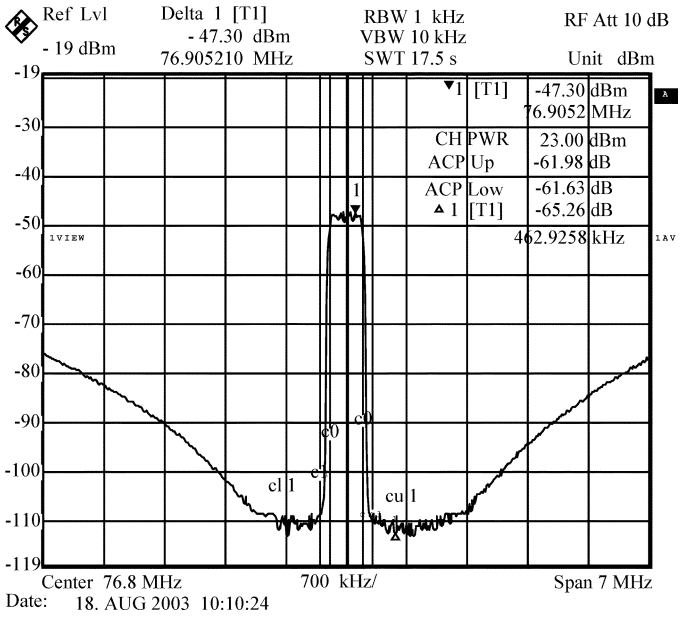

Fig. 8. Spectrum of QAM-modulated carrier at 1-bit $\Delta\Sigma$ D/A converter output, where the sampling frequency is 200 MHz and the carrier frequency is 76.8 MHz.

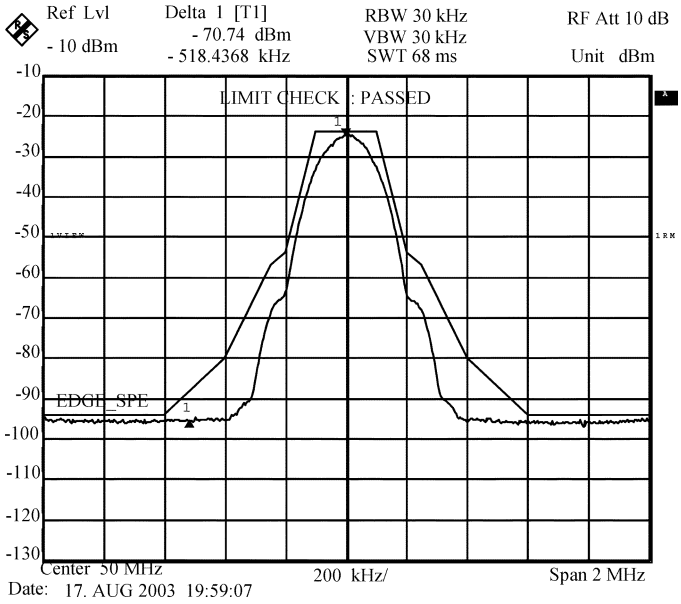

Fig. 9. Spectrum of EDGE modulated carrier at 1-bit $\Delta\Sigma$ D/A converter output, where the sampling frequency is 200 MHz and the carrier frequency is 50 MHz.

IV. Conclusion

The DDS with the tunable 1-bit $\Delta\Sigma$ D/A converter was designed and implemented. Since the 1-bit $\Delta\Sigma$ D/A converter has only one bit, the glitch problems and resulting spurious noise from the use of the multibit D/A converter are avoided. The in-band of the DDS with the tunable $\Delta\Sigma$ D/A converter could be placed anywhere in the Nyquist interval, so it gives a high degree of flexibility in sampling frequency planning.

References

[1] H. T. Nicholas and H. Samueli, "A 150-MHz direct digital frequency synthesiser in 1.25-m CMOS with −90-dBc spurious performance," *IEEE J. Solid-State Circuits*, vol. 26, no. 12, pp. 1959–1969, Dec. 1991.

[2] L. K. Tan and H. Samueli, "A 200 MHz quadrature digital synthesizer/mixer in 0.8 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 193–200, Mar. 1995.

[3] J. Vankka, M. Waltari, M. Kosunen, and K. Halonen, "Direct digital syntesizer with on-chip D/A-converter," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 218–227, Feb. 1998.

[4] "AD9744 14-bit, 165 MSPS TxDAC D/A converter, Data sheet," Analog Devices, May 2002.

[5] W. Schofield, D. Mercer, and L. St. Onge, "A 16 bit 400 MS/s DAC with −80 dBc IMD to 300 MHz and −160 dBm/Hz noise power spectral density," in *ISSCC Dig. Tech. Papers*, San Francisco, CA, Feb. 2003, pp. 126–127.

[6] I. Janiszewski, B. Hoppe, and H. Meuth, "Numerically controlled oscillators with hybrid function generators," *IEEE Trans. Ultrason., Ferroelect. Frequency Control*, vol. 49, no. 7, pp. 995–1004, Jul. 2002.

[7] J. Vankka and K. Halonen, *Direct Digital Synthesizers: Theory, Design and Applications*. Boston, MA: Kluwer, 2001.

[8] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters, Theory, Design, and Simulation*. New York: IEEE Press, 1997.

[9] A. Jayaraman, P. F. Chen, G. Hanington, L. Larson, and P. Asbeck, "Linear high-efficiency microwave power amplifiers using bandpass delta-sigma modulators," *IEEE Microw. Guided Wave Lett.*, vol. 8, no. 3, pp. 121–123, Mar. 1998.

[10] J. Keyzer, J. Hinrichs, A. Metzger, M. Iwamoto, I. Galton, and P. Asbeck, "Digital generation of RF signals for wireless communications with band-pass delta-sigma modulation," in *IEEE Microwave Symp. Dig.*, vol. 3, 2001, pp. 2127–2130.

[11] M. Iwamoto, A. Jayaraman, G. Hanington, P. F. Chen, A. Bellora, W. Thornton, L. E. Larson, and P. M. Asbeck, "Bandpass delta-sigma class-S amplifier," *Electron. Lett.*, vol. 36, no. 12, pp. 1010–1012, Jun. 2000.

[12] J. A. Webb, "Digital signal generator synthesizer," U.S. Patent 3,654,450, Apr. 4, 1972.

[13] J. Tierney, C. Rader, and B. Gold, "A digital frequency synthesizer," *IEEE Trans. Audio Electroacoust.*, vol. AU-19, no. , pp. 48–57, Mar. 1971.

[14] A. J. Magrath and M. B. Sandler, "Digital power amplification using sigma-delta modulation and bit flipping," *J. Audio Eng. Soc.*, vol. 45, no. 6, pp. 476–487, Jun. 1997.

[15] J. F. Jensen, G. Raghavan, A. E. Cosand, and R. H. Walden, "A 3.2-GHz second-order delta-sigma modulator implemented in InP HBT technology," *IEEE J. Solid-State Circuits*, vol. 30, no. 10, pp. 1119–1127, Oct. 1995.

[16] *Radio Transmission and Reception, GSM Recommendation 05.05*, Dec. 1999.