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COMPARISON OF DIFFERENT CLASS-D POWER AMPLIFIER TOPOLOGIES FOR 1-BIT RF BAND-PASS DELTA-SIGMA D/A CONVERTERS

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ABSTRACT

The suitabilities of different class-D power amplifier architectures for 1-bit bandpass ΔΣ D/A converters operating with RF signals are compared. The objective is to find out which architecture provides the best efficiency. The architectures considered are two-transistor voltage-mode class-D amplifier, H-bridge voltage-mode class-D amplifier, Transformer-coupled voltage-mode class-D amplifier, Transformer-coupled current-mode class-D amplifier and two-transistor current-mode class-D amplifier. These architectures are compared by APLAC simulation for discrete GaAs MESFET realisations.

1. INTRODUCTION

Today's smaller, faster and more effective portable electronics demand high power with only little losses. A good RF amplifier has high power gain, good efficiency, low noise and no distortion. Traditional class-A and class-B power amplifiers are linear but can only achieve efficiencies of 50% and 78.5% in ideal cases. Switched-mode amplifiers use push-pull technique and they can ideally achieve 100% efficiencies. A Class-D power amplifier is a switched mode amplifier with 100% efficiency in ideal case. These type of amplifiers are widely used in small electronics, which need to have small size and which need to function for a long time with same batteries. Applications using class-D amplifiers include for example hearing aids, wireless speakers, notebook computers etc. The motivating factor for the use of a class-D amplifier is its good efficiency. Another advantage is that the ΔΣ-modulated 1-bit sequence does not need a multibit D/A converter [1]. In this paper different types of class-D circuit topologies are simulated with APLAC in order to find out which one will be the best suited to amplify a ΔΣ-signal at 175MHz.

2. CLASS-D AMPLIFIER CIRCUITS

Class-D amplifiers can be divided into two categories: current-mode (CMCD) and voltage-mode (VMCD) amplifiers. A voltage-mode amplifier has a constant supply voltage whereas a current-mode amplifier has a constant current floating into the circuit. This paper compares five different class-D amplifier topologies. Two of them are current-mode and the rest are voltage mode amplifiers. In this section the switches are assumed to be ideal. Ideal class-D amplifiers achieve 100% drain efficiency [2].

2.1 Two-transistor voltage-mode class-D amplifier

Figure 1 shows a simple voltage-mode class-D amplifier. It consists of two n-type transistors and a third order LC band-pass filter. Transistor gates are driven with input signals, which are 180° out of phase.

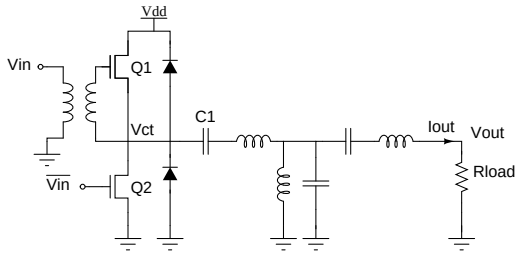

Figure 1. A schematic of a voltage mode class-D amplifier

When V_{in} is high, Q1 is on and Q2 is off. The potential V_{ct} between the two transistors is V_{dd}. Adversely Q2 is on and Q1 is off when V_{in} is low and V_{ct} is zero. Thus the signal at V_{ct} is a square wave varying between zero and V_{dd}. Fourier-series of a square-wave signal V_{ct} is shown in (1).

$$V_{ct} = \frac{1}{2}V_{dd} + \frac{2V_{dd}}{\pi}(\sin(2\pi f_s t) + \frac{1}{3}\sin(6\pi f_s t) + ...) \quad (1)$$

V_{ct} is then filtered with a bandpass filter, whose centre frequency is set to signal frequency f_s. Voltage V_{out} at the output is an amplified replica of the input signal with maximum value $V_{out,max}$ [2].

$$V_{out,max} = \frac{2V_{dd}}{\pi} \quad (2)$$

A half-wave rectified sine current is pulled to the circuit whenever Q1 is on. It charges the filter capacitor C1. When Q1 turns off, the same current flows back through Q2 to ground and capacitor discharges. This forms a sinusoidal current I_{out} at frequency f_s through the load.

$$I_{out} = \frac{2V_{dd}}{\pi R_{load}}\sin(2\pi f_s t) \quad (3)$$

Average value I_{dc} of a half-wave rectified current pulled through Q1 is given by (4).

$$I_{dc} = \frac{I_{out,max}}{\pi} = \frac{2V_{dd}}{\pi^2 R_{load}} \quad (4)$$

Input power is determined by (5). Output power P_{out} can be calculated by multiplying the maximum value of output voltage from (2) by the maximum value of output current from (3) and dividing the product by two (effective value of a sine wave). The result shows that output power equals input power and efficiency really equals 100% in the ideal case.

$$P_{in} = P_{out} = I_{dc}V_{dd} = \frac{2V_{dd}^2}{\pi^2 R_{load}} \quad (5)$$

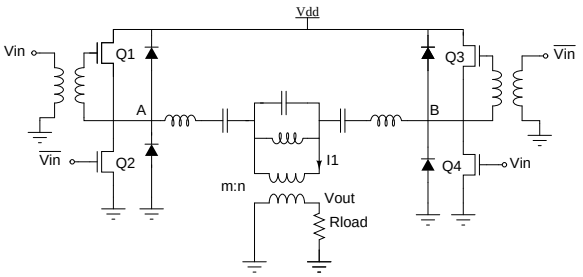

Figure 2. An H-bridge voltage-mode Class-D amplifier

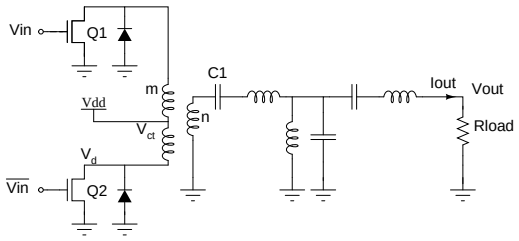

Figure 3. A transformer-coupled voltage-mode class-D amplifier

2.2 H-Bridge voltage-mode class-D amplifier

A differential version of the previous VMCD PA is shown in Fig. 2, it is called an H-bridge class-D amplifier [3]. Both sides of this circuit function the same way as the circuit in Fig. 1.

2.3 Transformer-coupled VMCD amplifier

A transformer-coupled voltage-switching class-D amplifier is shown in Fig. 3 [2]. Voltage V_{ct} at the centre-tap is constantly V_{dd} and current I_{ct} is a full-wave rectified sine. As Q1 and Q2 turn on and off alternately, a square wave with amplitude $(-n/m)V_{dd}$ is induced to the secondary winding of the centre tapped transformer. Because one of two transistors is always on and ideally grounded, voltage V_d over the other transistor must be a square wave with voltage levels 0 and $2V_{dd}$. The fundamental component of the voltage signal in the secondary winding passes through the filter, thus voltage V_{out} at output is

$$V_{out} = \frac{4}{\pi}\frac{n}{m}V_{dd}\sin(2\pi f_s t). \tag{6}$$

This causes current $I_{out}(= V_{out}/R_{load})$ to flow through the secondary winding. Output power P_{out} is then

$$P_{out} = \frac{I_{out,max}V_{out,max}}{2} = \frac{8}{\pi^2 R_{load}}(\frac{n}{m})^2 V_{dd}^2. \tag{7}$$

Current $(n/m)I_{out}$ is transformed to the primary winding causing half-wave rectified sinusoidal current with a peak value same as $I_{out,max}$ to flow through each transistor. Also the full-wave rectified sine current I_{ct} that flows from V_{dd} has peak value $I_{out,max}$. DC value I_{dc}, i.e. the average value of I_{ct} is twice the value from (4).

2.4 Transformer-coupled CMCD amplifier

In a transformer-coupled current-mode switching configuration, which is shown in Fig. 4 [2], a constant current I_{dc} is pulled through the choke into transformer centre-tap causing square wave drain currents that vary between 0 and I_{dc}. A

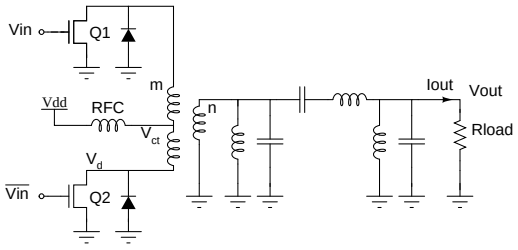

Figure 4. A transformer-coupled current-mode class-D amplifier

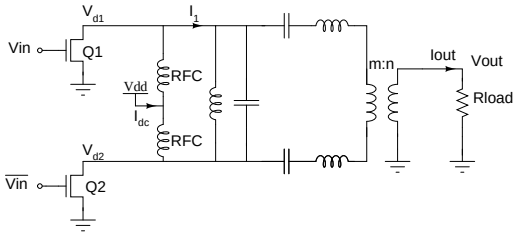

Figure 5. A circuit-model of a current-mode class-D amplifier

square wave current with levels $-I_{dc}$ and I_{dc} appears at the secondary winding. Only the fundamental component I_{out} flows through the filter.

$$I_{out} = \frac{4}{\pi}\frac{m}{n}I_{dc}\sin(2\pi f_s t) \tag{8}$$

Output voltage V_{out} is transformed to both primary windings causing half-wave rectified sinusoidal drain voltages V_d with a peak value of $2(m/n)V_{out,max}$. Voltage V_{ct} is full-wave rectified sine, whose average value is V_{dd} and peak value half of the drain voltage V_d. On the other hand peak voltage of a full-wave rectified sine signal with DC component V_{dd} is $\pi V_{dd}/2$. Combining these conditions the value of I_{dc} can be determined as follows.

$$\frac{1}{2}\pi V_{dd} = (\frac{m}{n})^2\frac{4}{\pi}I_{dc}R_{load} \Rightarrow I_{dc} = \frac{\pi^2}{8}(\frac{n}{m})^2\frac{V_{dd}}{R_{load}} \tag{9}$$

Input power and in ideal case also the output power of this transformer coupled current-mode class-D amplifier is

$$P_{in} = P_{out} = \frac{\pi^2}{8}(\frac{n}{m})^2\frac{V_{dd}^2}{R_{load}}. \tag{10}$$

2.5 Two transistor current-mode class-D amplifier

A current-mode class-D amplifier with two transistors, is shown in Fig. 5. It works almost the same way as the one above. Constant current I_{dc} flows to the circuit through two current chokes. When Q1 is off and Q2 on, half of the current I_{dc} goes through the filter circuit to Q2. The other half flows directly to Q2 through second choke. Current I_1 flowing to the filter circuit is a square wave with amplitude $I_{dc}/2$.

$$I_1 = \frac{4I_{dc}}{2\pi}\left(\sin(2\pi f_s t) + \frac{1}{3}\sin(6\pi f_s t) + ...\right) \tag{11}$$

Only the first harmonic flows through the primary winding of the balun. Other frequency components pass through the parallel LC circuit. I_1 is transformed to the secondary winding, where it flows through the load causing output voltage V_{out}.

$$V_{out} = \frac{I_{out}}{R_{load}} = \frac{2I_{dc}R_{load}}{\pi}\frac{m}{n}\sin(2\pi f_s t) \tag{12}$$

Voltage V_d over the primary winding is a sinusoidal wave with peak value $(m/n)V_{out,max}$. Because one of the transistors is always on, one side of R_{load} is always at potential zero. Voltage over one transistor is half-wave rectified sine whose DC-component is V_{dd} and maximum value $V_{d,max}$. When we know from (4) that the peak value of V_d is $V_d\pi$, the value of I_{dc} can be deduced from (12).

$$I_{dc} = (\frac{n}{m})^2 \frac{\pi^2 V_{dd}}{2R_{load}}. \quad (13)$$

Input power P_{in} of a current mode class-D amplifier shown in Fig. 5 is given in (14). Because I_{dc} multiplied by V_{dd} equals the output power, efficiency of the amplifier is 100%.

$$P_{in} = P_{out} = V_{dd} I_{dc} = (\frac{n}{m})^2 \frac{\pi^2 V_{dd}}{2R_{load}} \quad (14)$$

2.6 Losses in class-D amplifier circuits

Power is lost in switched-mode circuit with four main mechanisms: conduction loss, turn-on switching loss, turn-off switching loss and gate drive loss [4]. Conductor loss consists of resistive impedances in the circuit. It is only dependent of frequency through skin effect. At frequencies higher than tens of MHz skin effect cannot be ignored [4]. For a copper wire at frequency 175 MHz, the skin depth is 4,9 μm.

Turn-on loss occurs when switch turns on. During the transistor turn-on and turn-off there is always a period of time when neither the drain voltage V_d nor the drain current I_d are zero. During this crossover period power equal to $V_d * I_d$ is lost at any given moment. The value of power lost is proportional to the length of this period.

Bigger loss mechanism during the switching is the charging and discharging of the output capacitance [4]. If FET transistors are used, output capacitance is the drain capacitance C_d. Drain capacitance is charged to rail voltage V_{dd} every time the transistor turn off and then discharged when transistor turns on. Each cycle energy E_d is lost [4] causing power loss P_d at switching-frequency f_{sw} in a transistor.

$$P_d = E_d f_{sw} = \frac{1}{2} C_d V_{dd}^2 f_{sw} \quad (15)$$

Capacitive power is lost in every transistor placed between the supply voltage and ground. For a two transistor VMCD the power lost is that of (15), but for the rest of the VMCD topologies the loss will be double.

Inductance L_d in the drain causes power losses when the switch turns off. At the moment of turn-off current I_d flows through the transistor and inductive energy E_L is stored to the parasitic inductances. This energy is then released when the current suddenly stops. E_L is lost every cycle, but only when switch turns off. Power P_L is lost at switching frequency f_{sw} in every transistor connected to ground [4].

$$P_L = E_L f_{sw} = \frac{1}{2} L_d I_d^2 f_{sw} \quad (16)$$

Losses appear also at the capacitive gate during the switching. Gate charges and recharges as the switch turns on and off. At small frequencies loss is very small, but as the frequency grows gate drive loss cannot be ignored anymore. Gate can be modeled as a series RC circuit consisting of a gate resistance R_g and gate capacitance C_g [4]. Gate drive loss is dependent on the drive signal and is thus different with sine wave than it is with square wave. If the gate is driven with a square wave, current to the gate is a pulse whenever gate voltage V_{gs} is changed. As the voltage at the gate rises to maximum, charge Q is stored in the gate capacitance. Q is then lost when the gate voltage drops again. Energy E_g is lost every time the gate turns on and off. Total power P_{gs} lost in the gate at square wave switching frequency f_{sw} is then

$$P_{gs} = E_g f_{sw} = \frac{1}{2} V_{gs} Q. \quad (17)$$

When a sinusoidal gate drive is used current I_g to the gate is sinusoidal. Power $P_{g,\sin}$ lost at the gate drive at frequency f_{sw} is then

$$P_{g,\sin} = \frac{1}{2} I_g^2 R = \frac{1}{2} (2\pi f_{sw} Q)^2 R. \quad (18)$$

In previous formula R is the sum of gate resistance and drive circuit resistance [4]. At this point it is good to mention, that current mode class-D amplifier must be driven with square wave drive, but voltage mode class-D amplifier can be driven either with sinusoidal or square wave drive [5]. Turn-on and turn-off switching loss is clearly dominant loss mechanisms in modern Class-D amplifiers working at MHz and GHz range. Capacitive loss becomes the dominant loss mechanism when switching frequencies rise to hundreds of MHz and the significance of inductive loss gets smaller [2]. In order to reduce the capacitive loss, the voltage across the switch should be zero when it turns on or off. This is called zero-voltage-switching (ZVS). ZVS can be achieved with the CMCD amplifiers presented above, if switching frequency is the same as the signal frequency. Another way to reduce turn-on and turn-off loss by minimising the series inductive loss is zero-current-switching (ZCS), where current is always zero when the switch turns on or off. ZCS is, however, less important than ZVS at high frequencies [4].

3. SIMULATIONS

Simulations were carried out in time domain with APLAC-circuit simulator's transient analysis using ideal components and APLAC's MESFET model. Baluns were simulated as ideal transformers. An ideal third-degree Butterworth LC bandpass filter was used as a filter stage of simulated class-D amplifiers. A 175 MHz bandpass $\Delta\Sigma$-modulated bit-sequence, with a clock frequency of 700 MHz, was used as a drive signal for class-D amplifiers. The 1000 bit sequence had voltage levels -0.1 V and -3 V. The transistors used in the simulations were GaAs MESFETs.

3.1 Simulations with a $\Delta\Sigma$-modulated drive signal

Figures 6 and 7 show the simulated currents and voltages of an H-bridge VMCD amplifier (Fig. 2). Voltage at node A follows nicely the input signal. Current on the other hand has high peaks every time the gate voltage changes. These peaks get higher when the drain capacitance grows. When one transistor is on for duration of several bit lengths, output current will continue to flow as before. This forces a negative current through the transistor Q1 as shown in Fig. 6, because the current cannot pass through Q2. Therefore a diode must be placed between drain and source to pass the negative current and to protect the transistor from braking up. The H-bridge VMCD had efficiencies of 20.3%, 16.0% and

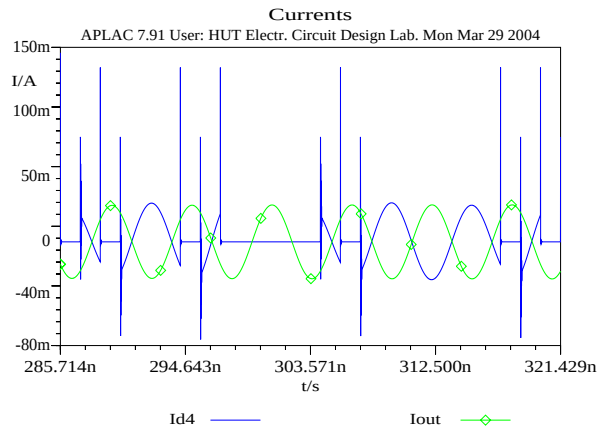

Figure 6. Currents in a H-bridge VMCD amplifier.

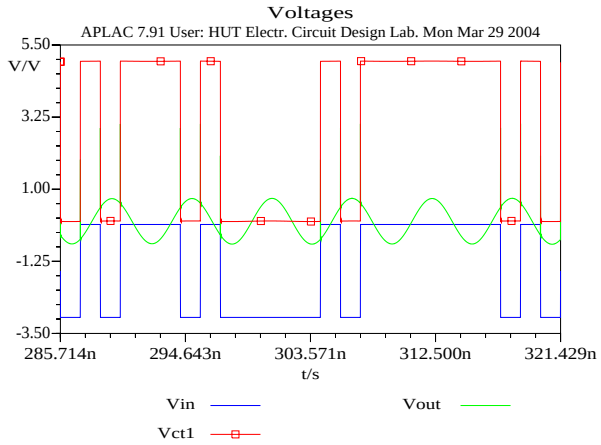

Figure 7. Voltages in a H-bridge VMCD amplifier.

14.9% with drain capacitances C_d of 0pF, 0.31pF and 0.61pF respectively.

A two transistor voltage-mode amplifier (VMCD) from Fig. 1 had same kind of voltage and current waveforms. Its efficiencies were 17.5%, 15.3% and 14.5% with C_d:s of 0pF, 0.31pF and 0.61pF respectively. This is also much greater loss than that determined by (15). Currents in a transformer-coupled voltage-mode circuit didn't show the same form as the previous ones. Efficiency of TC-VMCD was only 0.6%.

Simulations of CMCD amplifiers were carried out by trying different drain capacitance and choke inductance values to find the pair of values that gives the best efficiency. The best results were achieved when the series inductances and drain capacitance formed a LC resonance at signal frequency 175 MHz. For the two transistor CMCD the optimum was a drain capacitance C_d of 15.5pF and choke inductance L_{choke} of 50 nH. With this configuration an efficiency of 11.5 % was achieved. Because of the resonance at signal frequency, a high 175 MHz current is pulled through the LC-circuit. However, I_{dc} cannot be greater than the transistor saturation current I_{dss}, because the rest of the frequencies must still flow through the transistor. This way I_{dc} stays near I_{dss}. The drain voltage tries to be a half-wave rectified sine signal with peak value $V_{out,max}$. However, every time the gate voltage changes there is a voltage peak caused by the filter inductance placed between the two drains.

Table 1. Simulated efficiencies with square wave and ΔΣ-modulated signals.

Circuit Topology	η_{sq}	$\eta_{\Delta\Sigma}$	C_d
VMCD (Fig. 1)	99	15.3	0.31pF
H-Bridge (Fig. 2)	89	16.0	0.31pF
TC-VMCD (Fig. 3)	83	0.6	0.31pF
TC-CMCD (Fig. 4)	94	11.9	8.3pF
CMCD (Fig. 5)	93	11.5	15.5pF

The best efficiency for transformer-coupled CMCD was 11.9%. This was achieved when the value L_{choke} was 50 nH and the value of C_d was 8.3pF. With these values choke inductance, transformer inductance and drain capacitance formed a resonance frequency at signal frequency. Also for this circuit the DC current stayed near I_{dss}. Table 1 shows simulated drain efficiencies when circuits are driven with a square wave (η_{sq}) and with a ΔΣ-modulated signal ($\eta_{\Delta\Sigma}$). Supply voltage V_{dd} in all these simulations was 5 Volts.

Efficiencies drop dramatically when circuits are driven with ΔΣ-modulated signal, because the signal frequency component is only a small portion of the overall signal. Only the power at signal frequency is passed to the load, and the switching activity due to the outside band power will cause switching losses. Moreover, in a class-D circuit, which is driven with a ΔΣ-modulated signal currents and voltages have different frequencies; voltage changes at switching frequency and the current at signal frequency or vice versa. This can be seen clearly in figures 6 and 7. Thus, it is impossible to have zero voltage over a transistor every time the current is zero and ZVS or ZCS cannot be achieved. Turn on and turn off losses cannot be avoided. According to these simulations voltage-mode power amplifiers give better efficiency with a ΔΣ-modulated signal.

4. CONCLUSIONS

5 different class-D power amplifier circuits were compared and simulated to find out which one would be the best choice to amplify a 175 MHz ΔΣ-modulated signal with 700 MHz clock frequency. Two of the circuits were current-mode amplifiers and the rest were voltage-mode amplifiers. Circuits were simulated with ideal filters and APLAC MESFET models. Simulations show that an H-bridge VMCD amplifier has the best efficiency (20.3%) of all these alternatives.

REFERENCES

[1] D. Dapkus, "Class-D power amplifiers: an overview", in *ICCE 2000*. June 2000, pp. 400-401

[2] H. L. Krauss, C. W. Bostian and F. H. Raab, *Solid State Radio Engineering*, New York: Wiley 1980

[3] W.-H. Lau, H.S.-H. Chung, C.M. Wu and F.N.K. Poon, "Realization of digital audio amplifier using zero-voltage-switched PWM power converter", *IEEE Trans. on Circuits and Systems-I: Fundamental theory and applications*, Vol. 47, No. 3, pp. 303 - 311, March 2000

[4] S. El-Hamamsy, "Design of High-Efficiency RF Class-D Power Amplifier", *IEEE Trans. on Power Electronics*, Vol. 9, No. 3, May 1994

[5] H. Kobayashi, J. M. Hinrichs and P. M. Asbeck, "Current-Mode Class-D Power Amplifiers for High-Efficiency RF Applications", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 49, NO. 12, December 2001