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Comparison of Different Class-D Power Amplifier Topologies for 1-bit Band-Pass Delta-Sigma D/A Converters

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Abstract

The suitabilities of two different class-D power amplifier architectures for 1-bit bandpass $\Delta\Sigma$ D/A converters operating with RF signals are compared. The objective is to find out which architecture provides the best efficiency. The architectures considered are H-bridge voltage-mode class-D amplifier and transformer-coupled voltage-mode class-D amplifier. These architectures are compared by APLAC simulation using a $\Delta\Sigma$ modulated signal and by measuring discrete component GaAs MESFET realisations.

1. Introduction

Today's smaller, faster and more effective portable electronics demand high power with only little losses. A good RF amplifier has high power gain, good efficiency, low noise and no distortion. Traditional class-A and class-B power amplifiers are linear but can only achieve efficiencies of 50% and 78.5% in ideal cases. Switched-mode amplifiers use push-pull technique and they can ideally achieve 100% efficiencies. A Class-D power amplifier is a switched mode amplifier with 100% efficiency in ideal case. These type of amplifiers are widely used in small electronics, which need to have small size and which need to function for a long time with same batteries. Applications using class-D amplifiers include for example hearing aids, wireless speakers, notebook computers etc. The motivating factor for the use of a class-D amplifier is its good efficiency. Another advantage is that the $\Delta\Sigma$-modulated 1-bit sequence does not need a multi-bit D/A converter [1]. In this paper different types of class-D circuit topologies are simulated with APLAC in order to find out which one will be the best suited to amplify a $\Delta\Sigma$-signal at 175 MHz.

2. Class-D amplifier circuits

Class-D amplifiers can be divided into two categories: current-mode (CMCD) and voltage-mode (VMCD) amplifiers. A voltage-mode amplifier has a constant supply voltage whereas a current-mode amplifier has a constant current floating into the circuit. This paper compares two different voltage mode class-D amplifier topologies. In this section the switches are assumed to be ideal. Ideal class-D amplifiers achieve 100% drain efficiency [2].

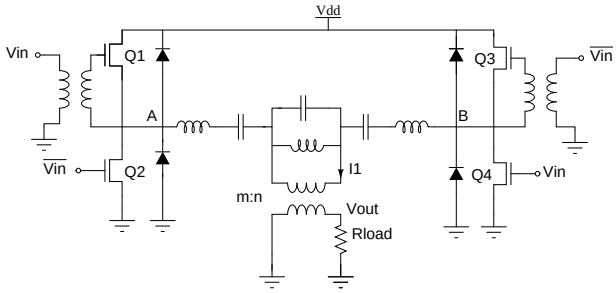

Figure 1. An H-bridge voltage-mode Class-D amplifier

2.1. H-Bridge voltage-mode class-D amplifier

Figure 1 shows a differential voltage-mode class-D amplifier, it is called an H-bridge class-D amplifier [3]. It consists of four n-type transistors and an LC bandpass filter. Transistor gates are driven with input signals, which are 180° out of phase. Both sides of this circuit function exactly the same way, which doubles the output power compared to a non-differential circuit. Because the output voltage appears in the middle of the circuit, a balun with transformation ratio n:m is needed to separate the load R_{load} from the circuit. Two input transformers are needed to keep the V_{gs} high enough.

When Q1 and Q4 are on, Q2 and Q3 are off. Adversely when Q1 and Q4 are off, Q2 and Q3 are on. Characteristics of this circuit can also be deduced from the Fourier-series of a square wave signal. In this case the square wave appearing between points A and B has twice the amplitude of the amplifier using only two transistors. Hence the voltage levels are V_{dd} and $-V_{dd}$. Fourier transform of this square-wave signal is

$$V_{AB} = \frac{4V_{dd}}{\pi}(\sin(2\pi f_s t) + \frac{1}{3}\sin(6\pi f_s t) + ...) \quad (1)$$

After filtering, only the fundamental component of V_{AB} appears at the balun's primary winding. The output voltage across the secondary winding is

$$V_{out} = \frac{4V_{dd}}{\pi}\frac{n}{m}\sin(2\pi f_s t). \quad (2)$$

V_{out} causes output current I_{out} to flow through the load R_{load}.

$$I_{out} = \frac{4V_{dd}}{\pi R_{load}}\frac{n}{m}\sin(2\pi f_s t) \quad (3)$$

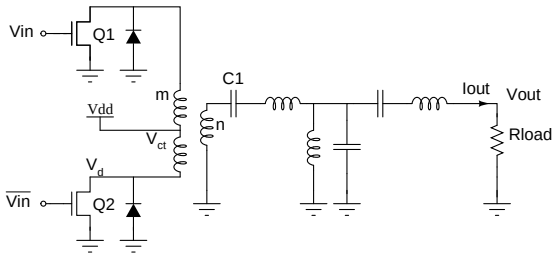

Figure 2. A transformer-coupled voltage-mode class-D amplifier

Because in an ideal transformer currents in primary and secondary windings must have ratio $n : m$, the current I_1 through the primary winding must be the following sine wave.

$$I_1 = \frac{n}{m} I_{out} = \frac{4V_{dd}}{R_{load}\pi}(\frac{n}{m})^2 \sin(2\pi f_s t) \quad (4)$$

A half-wave rectified sine current is pulled to the circuit alternately through Q1 and Q3. The sum of these currents is the current I_1. Average value I_{dc} of a half-wave rectified current pulled through Q1 is given by (5).

$$I_{dc} = \frac{I_{out,max}}{\pi} = \frac{2V_{dd}}{\pi^2 R_{load}} \quad (5)$$

Power P_{in} fed to the circuit can be determined by multiplying the average current I_{dc} pulled to the circuit by the supply voltage. I_{dc} flowing through two transistors is twice the value given in (5). This power appears also at the output.

$$P_{in} = P_{out} = I_{dc}V_{dd} = \frac{I_{1,max}V_{dd}}{\pi} = \frac{4V_{dd}}{R_{load}\pi^2}(\frac{n}{m})^2 \quad (6)$$

2.2. Transformer-coupled VMCD amplifier

A transformer-coupled voltage-switching class-D amplifier is shown in Figure 2 [2]. Voltage V_{ct} at the centre-tap is constantly V_{dd} and current I_{ct} is a full-wave rectified sine. As Q1 and Q2 turn on and off alternately, a square wave with amplitude $(-n/m)V_{dd}$ is induced to the secondary winding of the centre tapped transformer. Because one of two transistors is always on and ideally grounded, voltage V_d over the other transistor must be a square wave with voltage levels 0 and $2V_{dd}$. The fundamental component of the voltage signal in the secondary winding passes through the filter, thus voltage V_{out} at output is

$$V_{out} = \frac{4}{\pi}\frac{n}{m}V_{dd}\sin(2\pi f_s t). \quad (7)$$

This causes current $I_{out}(= V_{out}/R_{load})$ to flow through the secondary winding. Output power P_{out} is then

$$P_{out} = \frac{I_{out,max}V_{out,max}}{2} = \frac{8}{\pi^2 R_{load}}(\frac{n}{m})^2 V_{dd}^2. \quad (8)$$

Current $(n/m)I_{out}$ is transformed to the primary winding causing half-wave rectified sinusoidal current with a peak value same as $I_{out,max}$ to flow through each transistor. Also the full-wave rectified sine current I_{ct} that flows from V_{dd} has peak value $I_{out,max}$. DC value I_{dc}, i.e. the average value of I_{ct} is twice the value from (5).

2.3. Losses in class-D amplifier circuits

Power is lost in switched-mode circuit with four main mechanisms: conduction loss, turn-on switching loss, turn-off switching loss and gate drive loss [4]. Conductor loss consists of resistive impedances in the circuit. It is only dependent of frequency through skin effect. At frequencies higher than tens of MHz skin effect cannot be ignored [4]. For a copper wire at frequency 175 MHz, the skin depth is 4,9 μm.

Turn-on loss occurs when switch turns on. During the transistor turn-on and turn-off there is always a period of time when neither the drain voltage V_d nor the drain current I_d are zero. During this crossover period power equal to $V_d * I_d$ is lost at any given moment. The value of power lost is proportional to the length of this period.

Bigger loss mechanism during the switching is the charging and discharging of the output capacitance [4]. If FET transistors are used, output capacitance is the drain capacitance C_d. Drain capacitance is charged to rail voltage V_{dd} every time the transistor turn off and then discharged when transistor turns on. Each cycle energy E_d is lost [4] causing power loss P_d at switching-frequency f_{sw} in a transistor.

$$P_d = E_d f_{sw} = \frac{1}{2}C_d V_{dd}^2 f_{sw} \quad (9)$$

Capacitive power is lost in every transistor placed between the supply voltage and ground. For a two transistor VMCD the power lost is that of (9), but for the rest of the VMCD topologies the loss will be double.

Inductance L_d in the drain causes power losses when the switch turns off. At the moment of turn-off current I_d flows through the transistor and inductive energy E_L is stored to the parasitic inductances. This energy is then released when the current suddenly stops. E_L is lost every cycle, but only when switch turns off. Power P_L is lost at switching frequency f_{sw} in every transistor connected to ground [4].

$$P_L = E_L f_{sw} = \frac{1}{2}L_d I_d^2 f_{sw} \quad (10)$$

Losses appear also at the capacitive gate during the switching. Gate charges and recharges as the switch turns on and off. At small frequencies loss is very small, but as the frequency grows gate drive loss cannot be ignored anymore. Gate can be modeled as a series RC circuit consisting of a gate resistance R_g and gate capacitance C_g [4]. Gate drive loss is dependent on the drive signal and is thus different with sine wave than it is with square wave. If the gate is driven with a square wave, current to the gate is a pulse whenever gate voltage V_{gs} is changed. As the voltage at the gate rises to maximum, charge Q is stored in the gate capacitance. Q is then lost when the gate voltage drops again. Energy E_g is lost every time the gate turns on and off. Total power P_{gs} lost in the gate at square wave switching frequency f_{sw} is then

$$P_{gs} = E_g f_{sw} = \frac{1}{2}V_{gs}Q. \quad (11)$$

When a sinusoidal gate drive is used current I_g to the gate

is sinusoidal. Power $P_{g,\sin}$ lost at the gate drive at frequency f_{sw} is then

$$P_{g,\sin} = \frac{1}{2} I_g^2 R = \frac{1}{2} (2\pi f_{sw} Q)^2 R. \qquad (12)$$

In previous formula R is the sum of gate resistance and drive circuit resistance [4]. At this point it is good to mention, that current mode class-D amplifier must be driven with square wave drive, but voltage mode class-D amplifier can be driven either with sinusoidal or square wave drive [5]. Turn-on and turn-off switching loss is clearly dominant loss mechanisms in modern Class-D amplifiers working at MHz and GHz range. Capacitive loss becomes the dominant loss mechanism when switching frequencies rise to hundreds of MHz and the significance of inductive loss gets smaller [2]. In order to reduce the capacitive loss, the voltage across the switch should be zero when it turns on or off. This is called zero-voltage-switching (ZVS). ZVS can be achieved with the CMCD amplifiers presented above, if switching frequency is the same as the signal frequency. Another way to reduce turn-on and turn-off loss by minimising the series inductive loss is zero-current-switching (ZCS), where current is always zero when the switch turns on or off. ZCS is, however, less important than ZVS at high frequencies [4].

3. Simulations

Simulations were carried out in time domain with APLAC-circuit simulator's transient analysis using ideal components and APLAC's MESFET model. Baluns were simulated as ideal transformers. An ideal third-degree Butterworth LC bandpass filter was used as a filter stage of simulated class-D amplifiers. A 175 MHz bandpass $\Delta\Sigma$-modulated bit-sequence, with a clock frequency of 700 MHz, was used as a drive signal for class-D amplifiers. The 1000 bit sequence had voltage levels -0.1 V and -3 V. For comparison the circuits were also simulated using a 175 MHz square wave. The transistors used in the simulations were GaAs MESFETs.

3.1. Simulations with a $\Delta\Sigma$-modulated drive signal

Figures 3 and 4 show the simulated currents and voltages of an H-bridge VMCD amplifier (Figure 1). Voltage at node A follows nicely the input signal. Current on the other hand has high peaks every time the gate voltage changes. These peaks get higher when the drain capacitance grows. When one transistor is on for duration of several bit lengths, output current will continue to flow as before. This forces a negative current through the transistor Q1 as shown in Figure 3, because the current cannot pass through Q2. Therefore a diode must be placed between drain and source to pass the negative current and to protect the transistor from breaking up. The H-bridge VMCD had efficiencies of 20.3%, 16.0% and 14.9% with drain capacitances C_d of 0 pF, 0.31 pF and 0.61 pF respectively. This is much greater loss than that predicted by (9). Currents in the transformer-coupled voltage-mode circuit didn't show the same form as in the H-bridge simulations. The efficiency of the TC-VMCD was only 0.6%.

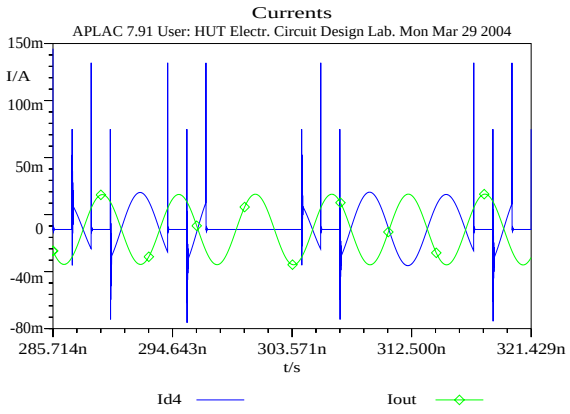

Figure 3. Currents in a H-bridge VMCD amplifier.

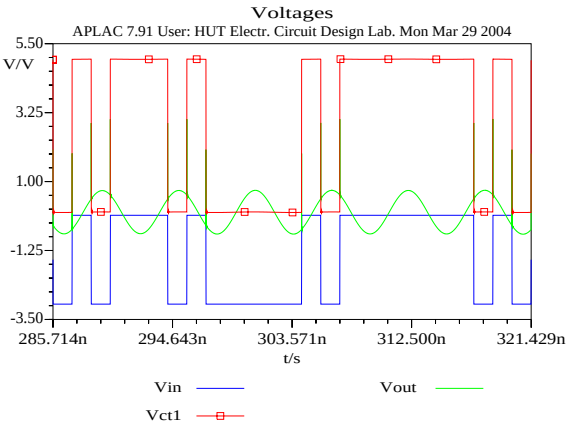

Figure 4. Voltages in a H-bridge VMCD amplifier.

When simulated with a 175 MHz square wave there are no substantial glitches in the current and voltage waveforms. The efficiencies were 83% and 89% for transformer coupled VMCD and H-bridge VMCD respectively.

Efficiencies drop dramatically when circuits are driven with $\Delta\Sigma$-modulated signal, because the signal frequency component is only a small portion of the overall signal. Only the power at signal frequency is passed to the load, and the switching activity due to the outside band power will cause switching losses. Moreover, in a class-D circuit, which is driven with a $\Delta\Sigma$-modulated signal currents and voltages have different frequencies; voltage changes at switching frequency and the current at signal frequency or vice versa. This can be seen clearly in figures 3 and 4. Thus, it is impossible to have zero voltage over a transistor every time the current is zero and ZVS or ZCS cannot be achieved. Turn on and turn off losses cannot be avoided.

4. Measurement results

A printed circuit board was fabricated to test the H-bridge power amplifier architecture in practice. FLK027WG [6] GaAs MESFETs were used as switches. The diodes used were 1N4001 low voltage drop diodes. The schematic of the measured circuit is shown in Figure 5.

The H-bridge architecture PA requires diodes between the gates and sources to adjust the switch control signal

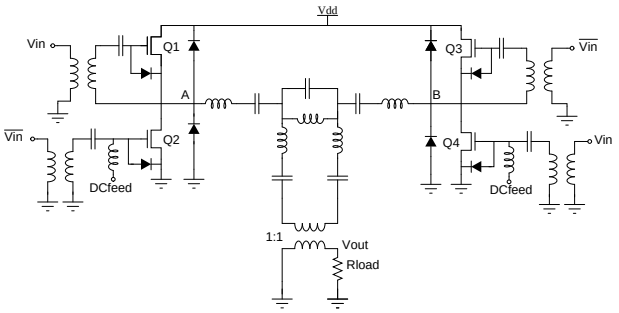

Figure 5. Schematic of the measured H-Bridge VMCD.

suitable for the switches when depletion type GaAsFETs are used. DC-block capacitors are needed between the terminals of the transformers and the gates of the transistors in order to adjust the DC-level of the control signals of the switches. Obviously the gate-source diodes should have as low a voltage drop and threshold voltage as possible so that the transistors are conducting simultaneously as short a time as possible, in order to maximise the efficiency. The bandpass filter was tuned to a centre frequency of 17 MHz with an insertion loss 4 dB and 3 dB bandwidth of 3 MHz. Phicomp surface mount multilayer ceramic nickel barrier NP0 capacitors and Coilcraft ceramic core 0805HQ-27NXJBC RF inductors (Q > 20) were used.

Figure 6 shows the measured spectrum of a sine signal fed in as 1-bit $\Delta\Sigma$-sine signal from a pattern generator. The output power is 16 dBm or 40 mW and the power dissipation is 495 mW (60 mA from a supply of 8.28 V) yielding a drain efficiency of 8%. The low efficiency is mostly caused by all the transistors being on for a relatively long time simultaneously when the switches change states and bad output impedance matching and losses in the output filter due to parasitics. The primary reason is caused by the bad quality of the switch control signals, which in turn is mostly caused by the limited bandwidth of the transformers. The clock frequency in the measurements was 167 MHz and the noise around the sine signal in the spectrum is possibly caused by phase-noise (or jitter) in the pattern generator, this could be tested by feeding the pattern generator signal directly into the spectrum analyser.

A transformer coupled voltage-mode class-D power amplifier was measured as well, a schematic of the measured circuit is shown in Figure 2. The transistors were the same as above and the filter was a single ended version of the filter used above with a 3 dB insertion loss, 17 MHz centre frequency and a 3 dB bandwidth of 3 MHz. The output power is 7 dBm or 5 mW and the power dissipation is 1.16 W (137 mA from a supply of 8.5 V) yielding a drain efficiency of 0.4%.

The measurements corroborated the results from the simulations and showed that the H-bridge topology is better suited for amplifying bandpass $\Delta\Sigma$ signal.

5. Conclusions

Two different class-D power amplifier circuits were compared and simulated to find out which one would be the best choice to amplify a 175 MHz $\Delta\Sigma$-modulated signal

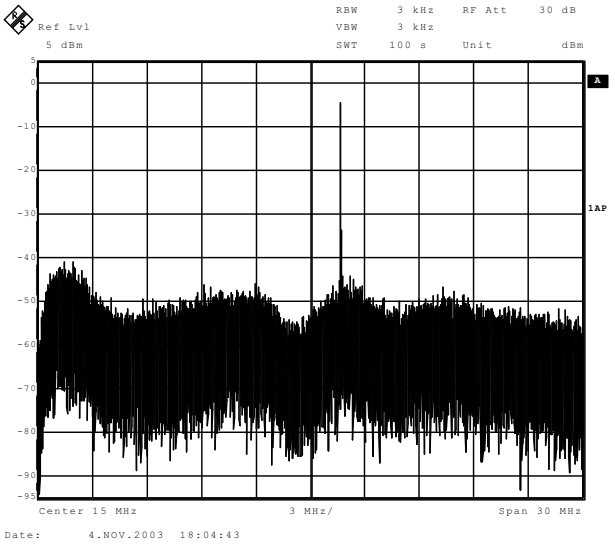

Figure 6. Spectrum of sine signal at the output of a H-bridge based power class-D power amplifier using a 20 dB attenuator

with 700 MHz clock frequency. Circuits were simulated with ideal filters and APLAC MESFET models. Simulations show that an H-bridge VMCD amplifier has better efficiency (20.3%) of these alternatives. The result is confirmed by the measurement results.

6. References

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