Appendix A - Errata

Errata 1 – Correction to Figure 12 in [P.III].

Figure 12 is now depicted as:

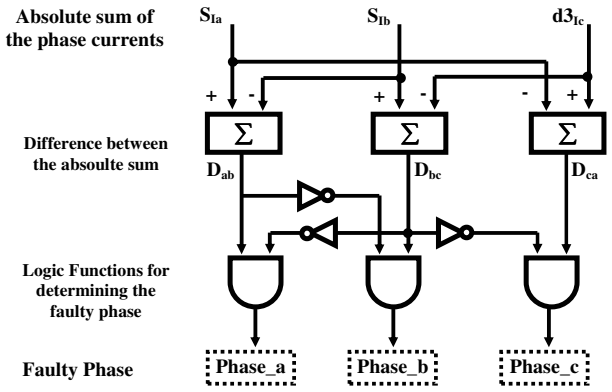

Fig. 12 The equivalent Logic circuit for determining the faulty phase.

It should be shown as:

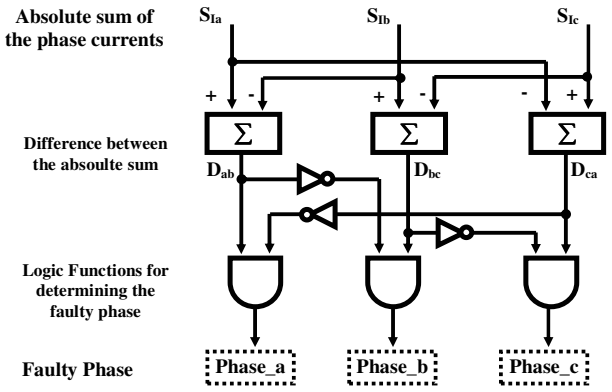

Fig. 12 The equivalent Logic circuit for determining the faulty phase.

Errata 2 – Correction to equation (6) in [P.V] and equation (8) in [P.VI].

The equation (6) in [P.V] now reads:

$$P_{a(Feeder\ j)}(k) = \sum_{n=k-2N+1}^{k} \left| d3_{Va}(n) \times d3_{Ia(Feeder\ j)}(n) \right| \tag{6}$$

It should be written as:

$$P_{a(Feeder\ j)}(k) = \sum_{n=k-2N+1}^{k} d3_{Va}(n) \times d3_{Ia(Feeder\ j)}(n) \tag{6}$$

The equation (8) in [P.VI] now reads:

$$P_{d3}(k) = \sum_{n=k-2N+1}^{k} \left| d3\_u_r(n) \times d3\_i_r(n) \right| \tag{8}$$

It should be written as:

$$P_{d3}(k) = \sum_{n=k-2N+1}^{k} d3\_u_r(n) \times d3\_i_r(n) \tag{8}$$