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Influence of Inverter Output Filter on the Selection of PWM Technique

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***Abstract*— This paper deals with the suitability of various pulse-width modulation techniques for a variable-speed AC drive equipped with a sinusoidal differential-mode and common-mode filter at the inverter output. Simulations and experiments are used for the investigation. If the average common-mode voltage is changed abruptly, the filter resonance may be excited, and the common-mode voltage at the motor terminals may rise to values higher than those obtained without the filter. This phenomenon may cause difficulties when the modulation is started, and it also creates a fundamental problem when a two-phase modulation method is used. The resonance problem can be avoided by selecting a modulation technique that does not cause sudden changes in the average common-mode voltage. A starting algorithm is proposed, enabling a trouble-free start of the drive equipped with a sinusoidal common-mode filter.**

I. Introduction

The output voltage of a pulse-width modulated (PWM) inverter may cause problems in AC motor drives. Harmonics at the switching frequency and its multiples give rise to additional losses and acoustic noise in the motor, and pulse reflections expose the motor insulations to additional voltage stresses. These problems can be reduced by adding a sinusoidal LC filter—having the cut-off frequency well below the switching frequency—to the output of the inverter. Furthermore, to avoid capacitive leakage currents and bearing currents, the filter can be designed to reduce the common-mode voltage.

Various sinusoidal filters reducing both differential-mode (DM) and common-mode (CM) voltages have been proposed. The star point of the LC filter capacitors has been connected to the negative dc bus in order to provide a route for a CM current [1]. A separate CM inductor has been added in front of an LRC filter, the star point of the filter capacitors being connected to the negative dc bus through a series connected capacitor and resistor [2]. Separate DM and CM filters (with dc link connections to both negative and positive dc buses) have also been used [3]. A combination of a differential-mode LC filter and a common-mode transformer with one winding connected to the dc-link midpoint has been proposed [4]. The influence of pulse-width modulation techniques on the operation of output filters were not discussed in these papers.

The classical sinusoidal pulse-width modulation (SPWM) [5] is the basis of state-of-the-art PWM techniques. An important improvement was the addition of a zero-sequence component to the voltage references. The modulation method developed in [6] has been later implemented more effectively and called symmetrical suboscillation method [7] or space vector PWM (SVPWM) [8]. Important inventions in the modulation were two-phase modulation methods, also known as discontinuous PWM (DPWM) [9]–[12]. The advantage of DPWM methods is the reduced switching losses. Pulse-width modulation techniques that reduce the CM voltage have also been proposed [13]–[15]. These methods are usually based on the replacement of the zero vectors by active vectors, which causes an increased current ripple.

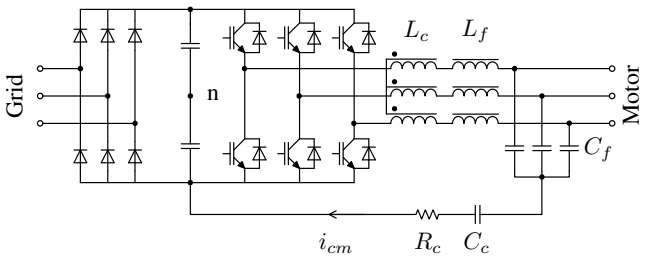


Fig. 1. Circuit diagram of frequency converter and output filter.

The CM voltage at the inverter output depends on the modulation method. An abrupt change in the average CM voltage may excite the resonance of the CM filter. In this paper, the effects of modulation techniques are compared using simulations and experiments. A filter similar to that proposed in [2] is used. Furthermore, the starting problem originating from the saturated common-mode inductor [3] is studied, and a starting algorithm is proposed.

II. Filter Topology

Fig. 1 shows the circuit diagram of the inverter output filter. An LC filter, consisting of a three-phase inductor L_f and three capacitors C_f, attenuates high frequencies of the differential-mode voltage. The star point of the LC filter capacitors is connected to the negative dc bus through a series connected capacitor C_c and resistor R_c. An additional CM inductor L_c increases the CM inductance without affecting the DM circuit. This topology provides a route for the CM current and reduces the CM voltage at the motor terminals. In this paper, all common-mode voltages are measured against the midpoint of the dc-link capacitors, marked with n in Fig. 1.

III. PWM Methods

The investigated PWM methods represent different types of modulation techniques. The widely used SVPWM represents

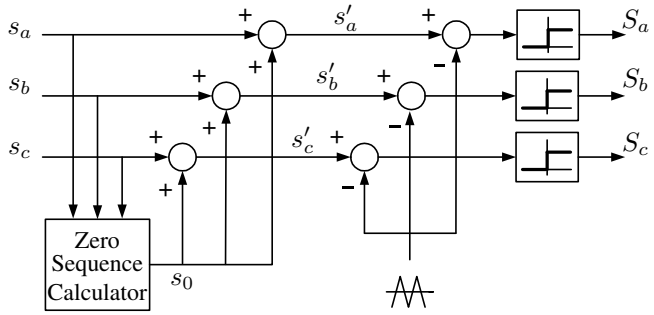


Fig. 2. Triangle-intersection technique with zero-sequence injection.

continuous PWM techniques with zero-sequence injection. The DPWM technique proposed in [9] represents two-phase modulation techniques. The third modulation method is a CM voltage reduction PWM proposed in [14]. These three methods are briefly explained in the following.

Fig. 2 illustrates a triangle-intersection technique with zero-sequence signal injection. The inputs are the scaled voltage reference signals

$$s_x = \frac{u_x^*}{u_{dc}/2}, \quad x = a, b, c \tag{1}$$

where u_x^* is the reference phase voltage and u_{dc} is the dc-link voltage. A modified reference signal s'_x is obtained by adding a zero-sequence signal s_0 to s_x. The amplitude of the triangle carrier signal is unity. The outputs of the modulator are the switching functions for each phase.

The maximum linear modulation index is an important performance criterion for the modulator. The modulation index is defined as [16]

$$M = \frac{u_1}{2u_{dc}/\pi} \tag{2}$$

where u_1 is the fundamental component of the phase-to-neutral inverter output voltage. In the SPWM method, no zero-sequence injection is used and the maximum linear modulation index is 0.785.

A. Symmetrical Suboscillation (SVPWM)

The only difference between symmetrical suboscillation and the SPWM is the zero-sequence signal. The zero-sequence signal can be calculated based on the minimum and maximum of the scaled voltage reference signals [7]:

$$s_0 = \frac{-\min(s_a, s_b, s_c) - \max(s_a, s_b, s_c)}{2} \tag{3}$$

An example of the modified reference signal and zero-sequence signal for the SVPWM method is depicted in Fig. 3(a), where θ is the angle of the voltage vector. The zero-sequence injection improves the maximum linear modulation index to 0.907.

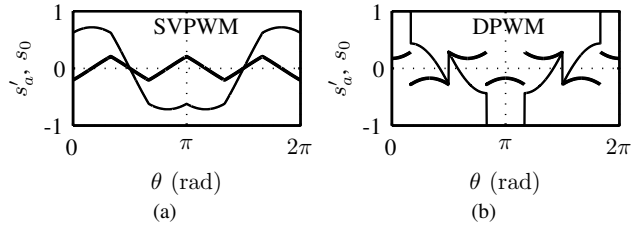


Fig. 3. Examples of modified reference signal s'_a (thin line) and zero-sequence signal s_0 (thick line) for (a) SVPWM and (b) DPWM ($M = 0.65$).

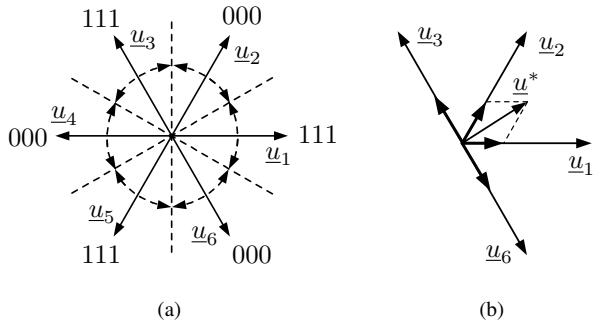


Fig. 4. (a) Zero vectors used in DPWM method. (b) Example switching period of NSVM3: zero vectors are replaced with active vectors $\underline{u}_3$ and $\underline{u}_6$

B. Two-Phase Modulation (DPWM)

In the two-phase (discontinuous) modulation method, the switching of one phase is stopped during a switching period. Consequently, only one of the zero vectors is used during the switching period and the switching losses decrease by about one third. The DPWM method developed in [9] can be implemented in the following way [12]. The zero-sequence signal is defined by the voltage reference signal having the largest instantaneous magnitude. If, for example, $|s_a| \geq |s_b|, |s_c|$, the zero-sequence signal is

$$s_0 = \text{sign}(s_a) - s_a \tag{4}$$

Fig. 3(b) shows an example of the modified reference signal and zero-sequence signal for the DPWM method. The zero-sequence signal is a discontinuous function of the angle θ. Fig. 4(a) shows the zero vectors (denoted by 111 and 000 for all phases connected to the positive or negative dc bus, respectively) used in each sector. The maximum linear modulation index of the DPWM is equal to that of the SVPWM.

C. CM Voltage Reduction PWM (NSVM3)

The NSVM3 method [14] is a common-mode voltage reduction PWM technique. The switching times for the active vectors are calculated as in the SVPWM method, but the zero vectors are replaced by two opposite active vectors as illustrated in Fig. 4(b). The switching pattern for this example switching period is $\underline{u}_6 \rightarrow \underline{u}_1 \rightarrow \underline{u}_2 \rightarrow \underline{u}_3 \rightarrow \underline{u}_3 \rightarrow \underline{u}_2 \rightarrow \underline{u}_1 \rightarrow \underline{u}_6$, and the on-durations of the vectors $\underline{u}_3$ and $\underline{u}_6$ are equal. The maximum linear modulation index is equal to that of the SVPWM method.

TABLE I

MOTOR AND FILTER DATA

Motor Ratings		*Filter Parameters*	
Power	2.2 kW	Inductance L_f	5.1 mH
Voltage	400 V	Capacitance C_f	6.8 μF
Current	5.0 A	Series resistance R_{Lf}	0.1 Ω
Frequency	50 Hz	CM inductance L_c	20 mH
Speed	1430 r/min	CM capacitance C_c	2.2 μF
Torque	14.6 Nm	CM resistance R_c	10 Ω

IV. SIMULATION RESULTS

The effects of different modulation techniques on the operation of a 2.2-kW induction motor drive equipped with a sinusoidal filter were simulated using the MATLAB/Simulink software. The data of the motor and filter are given in Table I. In the following examples, the drive was controlled with a constant volts-per-hertz control method. The switching frequency was 5 kHz.

The differential-mode LC filter was designed according to the design rules described in [17], [18]. The resonance frequency was 855 Hz. The resonance frequency of the common-mode LC filter was 767 Hz. To avoid excessive losses, the resistance R_c was selected small. The quality factor of the CM filter was 9.5, being slightly higher than that in [2].

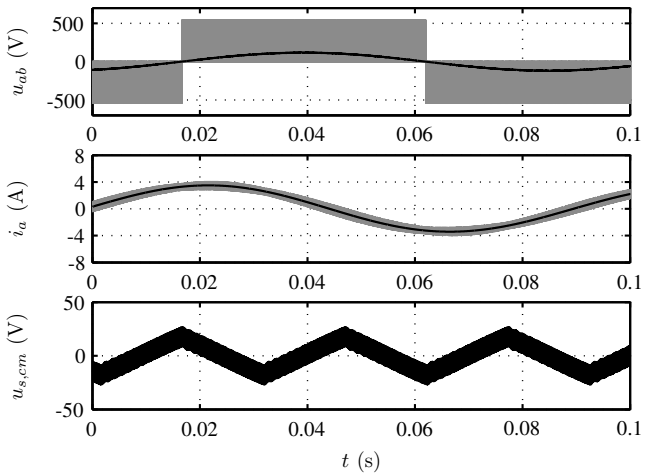
Fig. 5 shows the simulation results obtained using the SVPWM method. The modulation index $M = 0.2$ is selected because it is close to the worst operating condition ($M = 0$) but the fundamental frequency is non-zero. It can be seen that the stator voltage and current are very close to sinusoidal. The injected zero-sequence signal is visible in the CM voltage as a triangular waveform having three times the fundamental frequency. The maximum CM voltage is 26 V, and the maximum CM current of the filter is 0.6 A.

The simulation results obtained using the DPWM method are shown in Fig. 6. The difference between the SVPWM and DPWM methods is clear. In the DPWM method, the abrupt change in the average CM voltage at each sector boundary excites the resonance of the common-mode LC filter. The CM voltage at the motor terminals is higher than it would be without the filter. In addition, the maximum CM current of the filter is high, about 4 A, and would cause saturation of the CM inductor. The saturation was not included in the simulation.

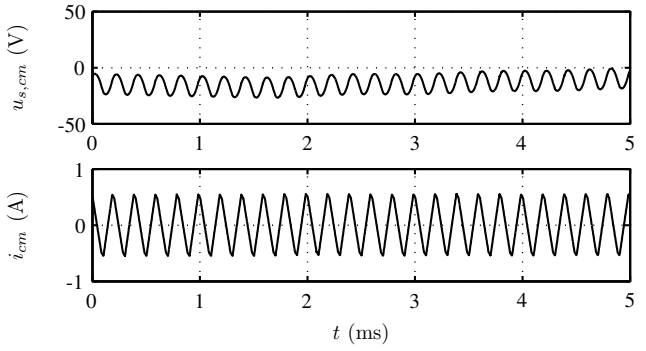
Fig. 7 shows the simulation results obtained using the NSVM3 method. The switching-frequency component of the CM voltage is reduced as expected. The low-frequency content of the CM voltage is equal to that of the SVPWM, and the maximum CM current of the filter is smaller than that of the SVPWM. The switching-frequency ripple in the inverter output phase current is large. The resonance of the differential-mode LC filter is excited, which can be seen both in the phase-to-phase stator voltage and in the stator current.

V. EXPERIMENTAL RESULTS

The experimental setup consists of a frequency converter controlled by a dSPACE DS1103 PPC/DSP board, a 2.2-kW four-pole induction motor, and a sinusoidal filter. The data of



(a) Fundamental-frequency-based time scale



(b) Switching-frequency-based time scale

Fig. 5. Simulation results showing steady-state operation using SVPWM method with $M = 0.2$. (a) The first subplot shows the inverter output voltage (phase-to-phase) and the stator voltage (phase-to-phase). The second subplot shows the inverter output current and the stator current. The third subplot shows the CM voltage at the motor terminals. (b) CM voltage at the motor terminals and CM current through the filter.

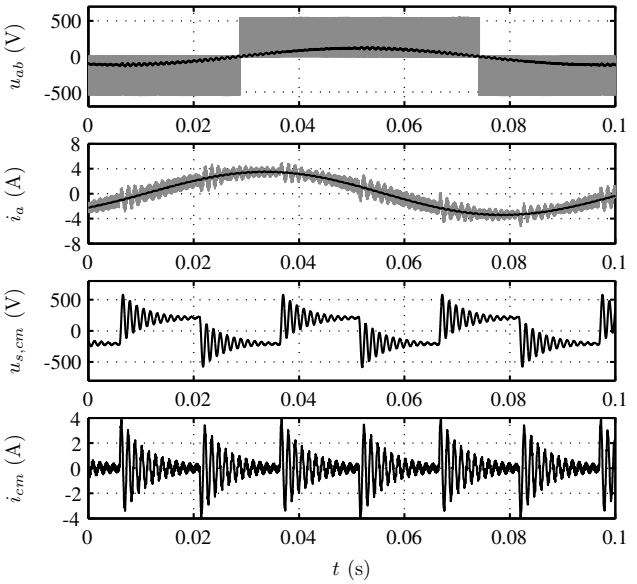
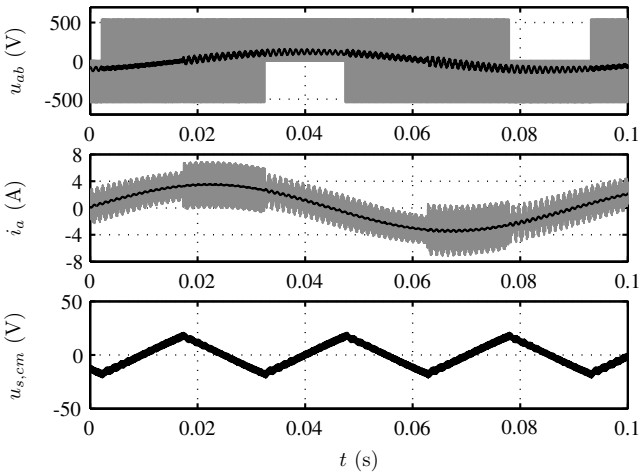
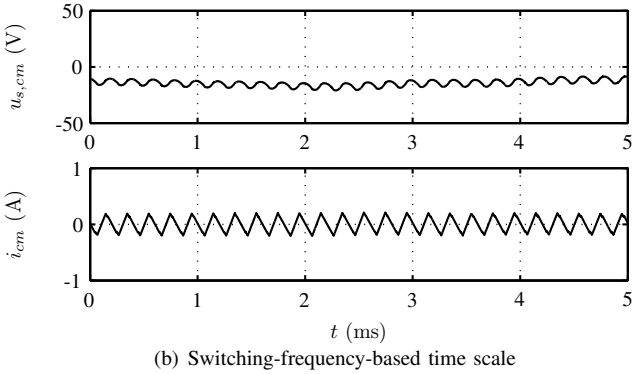


Fig. 6. Simulation results showing steady-state operation using DPWM method with $M = 0.2$. The explanations of the curves can be found in Fig. 5.



(a) Fundamental-frequency-based time scale



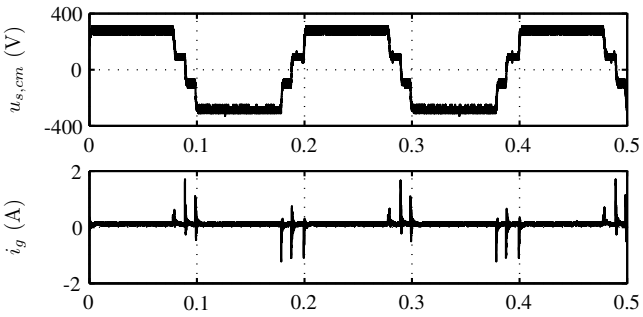
(b) Switching-frequency-based time scale

Fig. 7. Simulation results showing steady-state operation using NSVM3 method with $M = 0.2$. The explanations of the curves are as in Fig. 5.

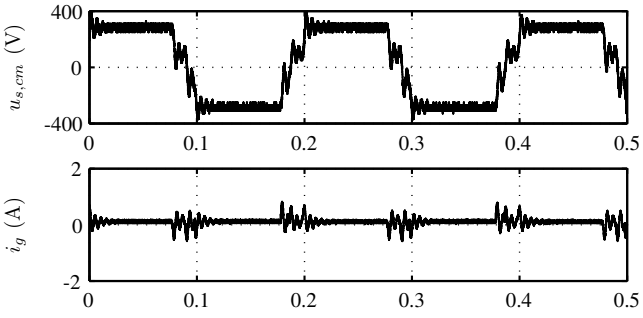
the experimental setup are given in Table I. The common-mode inductor is constructed of a toroidal core with all three windings wound in the same direction. The material of the toroidal core is high-permeability nanocrystalline tape. Due to the magnetic saturation, the inductance decreases if the CM current exceeds approximately 1 A.

A digital oscilloscope was used for the measurements. The common-mode voltage at the motor terminals was measured by means of three star-connected resistors (100 kΩ each).

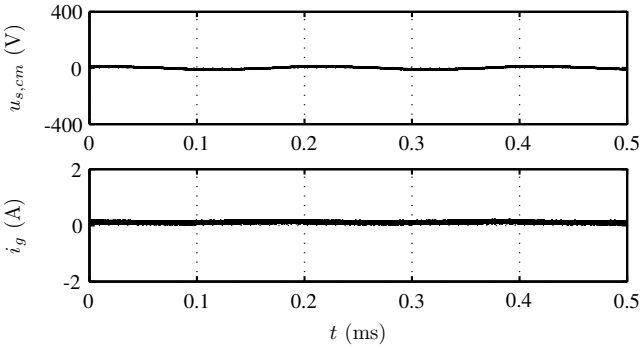
Before the comparison of the modulation methods, the influence of the output filter on the CM voltage and CM leakage current of the motor is illustrated using the SVPWM method. Fig. 8(a) shows steady-state operation without any filter. The CM leakage current of the motor, measured from the grounding conductor, reaches nearly 2 A at switching instants. Fig. 8(b) shows the CM voltage of the motor and the motor leakage current as a differential-mode LC filter was used. The LC filter changes the CM circuit: the resonance frequency of the CM circuit is decreased, and the damping is lowered. The CM voltage is higher than without the filter. Fig. 8(c) shows the CM quantities as the filter shown in Fig. 1 was used. The CM voltage at the motor terminals is significantly decreased, and the CM leakage current of the motor is very low.



(a) No filter



(b) Differential-mode LC filter



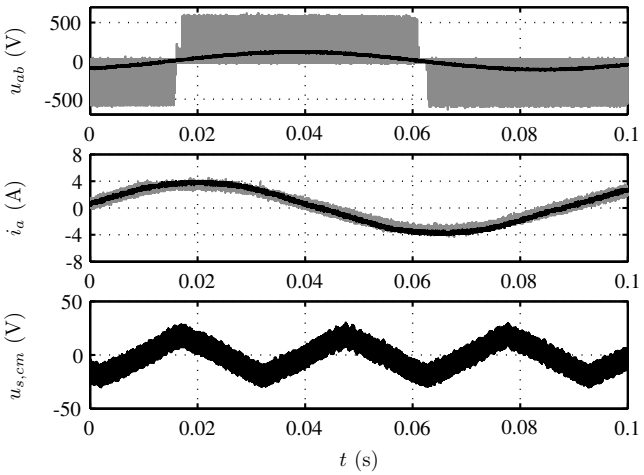
(c) Differential- and common-mode LC filter

Fig. 8. Experimental results showing steady-state operation obtained (a) without filter, (b) with differential-mode LC filter, and (c) with differential- and common-mode LC filter. The first subplot shows the CM voltage at motor terminals. The second subplot shows the CM leakage current of the motor.

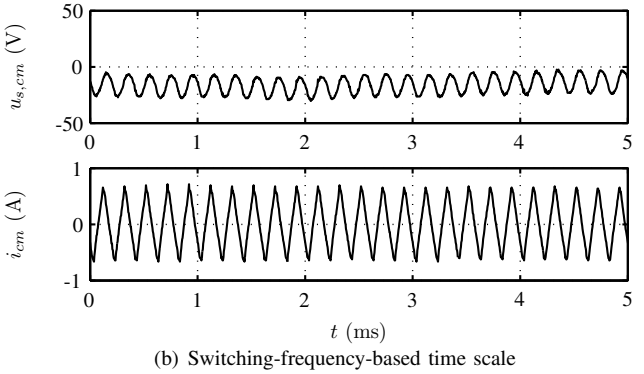
Fig. 9 shows the experimental results for the SVPWM method with $M = 0.2$. The triangular shape in the CM voltage can be seen as in the corresponding simulation in Fig. 5. The maximum CM current of the filter is 0.7 A, and it does not saturate the CM inductor.

The two-phase modulation method (DPWM) caused an overcurrent trip as was expected based on the simulations. The CM filter resonance was excited by the abrupt change of the average CM voltage, and caused the saturation of the CM inductor. The highest CM current peak was nearly 25 A, which triggered the overcurrent protection. Consequently, the DPWM method is unfit for use with the sinusoidal CM filter.

The NSVM3 method was not implemented because the



(a) Fundamental-frequency-based time scale



(b) Switching-frequency-based time scale

Fig. 9. Experimental results showing steady-state operation using SVPWM method with $M = 0.2$. The explanations of the curves are as in Fig. 5.

modulator interface of the experimental setup did not support the switching patterns needed by the NSVM3 method.

Fig. 10 shows the experimental results for the SVPWM method as the modulation index is varied from 0 to 0.95. The highest CM current is obtained at zero modulation index. When the modulation index is increased, the switching-frequency components of the CM voltage and CM current decrease. The low-frequency component of the CM voltage increases with the zero-sequence signal. At the end of the sequence, the inverter operates in the overmodulation range.

VI. Starting Problem and Its Solution

A. Starting Problem

The common-mode filtering presents a problem: the drive may trip on overcurrent when the modulation is started. The problem has been reported in [3] for a slightly different filter topology.

Fig. 11(a) shows a modulation start of the drive equipped with the output filter shown in Fig. 1. The SVPWM is started, the modulation index being $M = 0$, and the initial value of the CM current of the filter is zero. The initial voltage over the CM capacitor is half of the dc-link voltage because the dc link is floating and all power switches are open before the

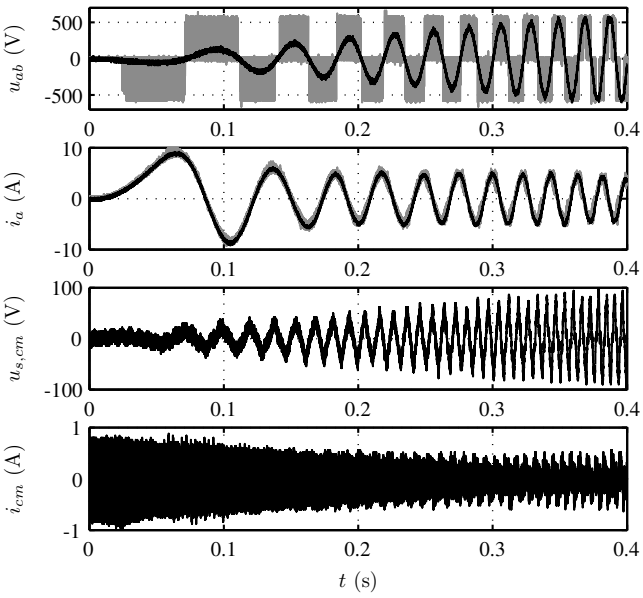


Fig. 10. Experimental results showing acceleration using SVPWM. The modulation index is varied from 0 to 0.95. The overmodulation starts at $t = 0.36$ s. The explanations of the curves can be found in Fig. 5.

modulation start. During the first zero vector 000, the CM current of the filter saturates the CM inductor, and the CM capacitor is discharged. After the change of the zero vector to 111, the voltage across the CM inductor is approximately the full dc-link voltage. The CM current again saturates the CM inductor, and the CM capacitor is charged to the full dc-link voltage. The oscillation continues, in the worst case, for several seconds. The first CM current peak is -13 A, and the second one is 30 A.

A hardware solution for the starting problem was proposed in [3]: a dynamic damping circuit consisting of an additional winding around the CM inductor core, a full-bridge rectifier, a filtering capacitor, and a resistive load. The damping circuit solves the problem, but it may affect the filter performance. Furthermore, the additional hardware makes the damping circuit less attractive.

B. Proposed Starting Algorithm

A simple starting algorithm is proposed to solve the starting problem without any hardware modifications. The idea of the algorithm is to modify the on-durations of the zero vectors at the start. During the switching period T_s, the on-durations of the zero vectors 111 and 000 are denoted by T_{0+} and T_{0-}, respectively. The relative on-time of the 111 zero vector is defined as

$$d_z = \frac{T_{0+}}{T_{0-} + T_{0+}}. \tag{5}$$

The severe oscillation can be avoided by preventing the back and forth heavy charging of the CM capacitor. This improvement is achieved by starting with a short on-duration of the zero vector 111, and then slowly lengthening it, i.e. d_z

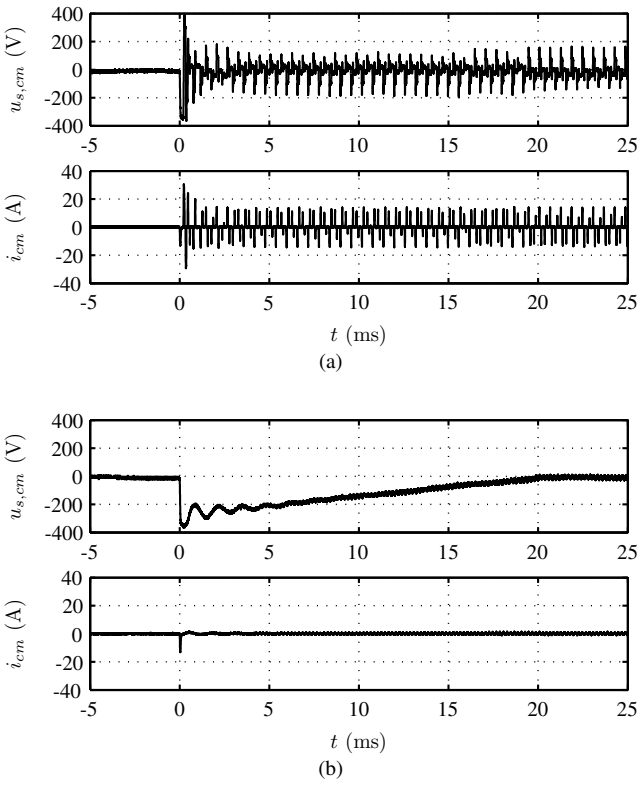


Fig. 11. Experimental results showing CM voltage and CM current at the start (a) without and (b) with starting algorithm.

is ramped from 0 to 0.5 at the start. The value $d_z = 0.5$ corresponds to the SVPWM method. The zero-sequence signal can be calculated from d_z and from the scaled voltage reference signals as

$$s_0 = 2d_z - 1 - d_z \max(s_a, s_b, s_c) + (d_z - 1)\min(s_a, s_b, s_c) \quad (6)$$

If the voltage reference is zero, (6) reduces to $s_0 = 2d_z - 1$.

Fig. 11(b) shows the modulation start when the proposed starting algorithm is used. Only the first CM current peak (-13 A) remains. A significant improvement is thus obtained at the start.

VII. Conclusion

When the inverter output voltage is filtered by a sinusoidal LC filter with CM attenuation characteristics, the PWM method should be selected carefully. According to the simulation and experimental results, the SVPWM is the most suitable method. The two-phase modulation (DPWM) is not suitable because it excites the CM filter resonance and causes an overcurrent trip. According to simulations, the CM voltage reducing NSVM3 method is not a good choice for a drive equipped with a sinusoidal output filter. Although the NSVM3 reduces the CM voltage and the CM current, it causes a high differential-mode current ripple. The starting problem originating from the saturated CM inductor can be solved by modifying the on-durations of the zero vectors at the modulation start.

Acknowledgment

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