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# Development of multi-step processing in silicon-on-insulator for optical waveguide applications

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## Abstract

Multi-step processing for a silicon-on-insulator (SOI) platform was developed. It allows the incorporation of additional grooves and steps into the basic optical waveguide structures, so that light can be adiabatically coupled between waveguides with different cross-sections. The processes were based on simple fabrication methods easily scalable for mass production. Two options for the fabrication sequence were tested, both having one silicon etch step with an oxide mask and another etch step with a resist mask. The applicability of the developed processes was tested with different waveguide structures. An additional groove etched beside a bent 10  $\mu\text{m}$  thick rib waveguide suppressed the bend losses to below 1 dB/90° with a 5 mm bending radius. A waveguide mirror exhibited optical losses below 1 dB/90°. The excess losses of a vertical taper between 10 and 4  $\mu\text{m}$  thick rib waveguides were 0.7 dB. A converter between a rib and a strip waveguide showed negligible losses, below 0.07 dB.

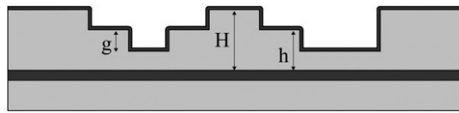
**Keywords:** integrated optics, optical device fabrication, optical losses, optical waveguides, silicon-on-insulator technology

## 1. Introduction

Based on the recent advances achieved in silicon-based photonics [1–5], it is now seen that silicon might well become the dominant material for photonics, as it has been for electronics since the early seventies. The ability to integrate both electronic and photonic circuits on a single silicon chip provides unique advantages and possibilities that cannot be reached with any other technology, at least for a competitive price. In silicon microphotonics, silicon can be used not only as a substrate, but also as a waveguide core material. Silicon-on-insulator (SOI) offers the most convenient platform for realizing silicon waveguides. SOI substrates allow monolithic and hybrid integration of different electronic and photonic functions. The very high index contrast in SOI waveguides allows the extreme miniaturization of optical devices by means of e.g. photonic nanowires or photonic crystal waveguides. This creates the potential for a significant increase in the

density and integration of optical devices, which is a necessity for the increased performance and lower cost required for future microphotonic circuits.

The operation of the microphotonic components usually requires a single-mode (SM) behaviour. Other basic requirements are a small footprint enabling low cost, and a low-loss connection to the optical fibres, which couple the light into and out of the chip. Unfortunately, these requirements often conflict. For example, thick Si rib waveguides offer SM operation and a low-loss connection to standard optical fibres. However, they usually require very long bending radii, which results in large components. Thus, it is important to develop techniques for bend size reduction in thick Si waveguides. Significantly smaller bending radii are achieved with thinner waveguides, but then the coupling to standard SM fibres becomes inefficient. Here, a convenient solution is an on-chip coupler between a thick and a thin waveguide [6, 7]. More generally, it would be useful to combine different



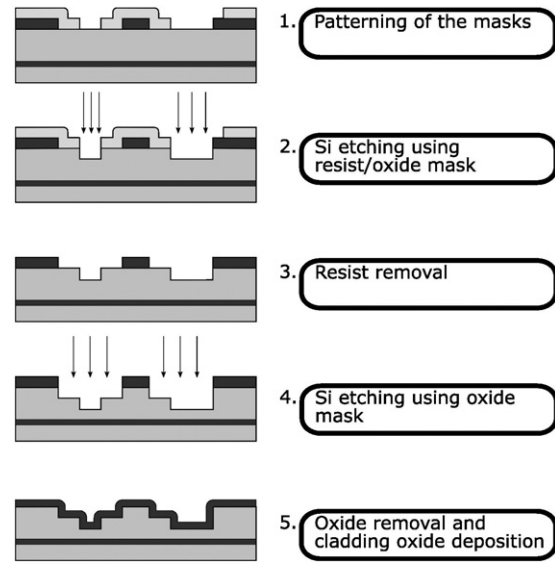
**Figure 1.** Multi-step structure in silicon. The SOI layer is patterned with two separate etching steps and covered with a cladding oxide layer.

waveguide cross-sections, each optimized for a given purpose, within a single silicon waveguide device. This can be achieved by using more than one etch step (and mask) in the fabrication process. The resulting multi-step structures can provide adiabatic conversions between different waveguide cross-sections.

In this study, multi-step processing in SOI was demonstrated using standard microelectronic fabrication methods. The target of the processes was the multi-step structure shown in figure 1. By changing the depths of the etch steps ( $H-h$  and  $g$ ), various waveguide types and optical structures could be monolithically integrated on a single chip. The concept has been proposed before [8], but here the experimental work related to the fabrication and optical characterization of the multi-step structures is presented. Unlike in the processes proposed by others, no costly or complicated process steps such as epitaxial growth [6], grey-scale lithography [7] or e-beam lithography [9] were used. The processes reported here were based on two mask layers and two silicon dry etch steps. A contact mask aligner was used for lithographic exposures, ensuring fast and economical lithography. The applicability of the developed multi-step processing was tested with different waveguide structures. Additional grooves enabling a bend size reduction as proposed in [10] were realized in  $10\ \mu\text{m}$  thick rib waveguides. A waveguide mirror [11, 12] coupled to  $10\ \mu\text{m}$  thick rib waveguides was fabricated. Finally, two types of low-loss converters between different waveguides were fabricated and characterized. The first was a vertical taper [13–15] coupling rib waveguides with  $10$  and  $4\ \mu\text{m}$  thicknesses. The other was a rib–strip converter coupling waveguides of different types, as proposed in e.g. [8, 16].

## 2. Fabrication and characterization

The base for the fabrication was a  $10\ \text{cm}$  diameter BESOI (bond and etch-back SOI) wafer. The SOI layer and the buried oxide (BOX) were  $9.5 \pm 0.5\ \mu\text{m}$  and  $1.00 \pm 0.01\ \mu\text{m}$  thick, respectively. On top of the SOI layer a  $1\ \mu\text{m}$  oxide layer was deposited with a TEOS (tetra-ethyl-ortho-silicate) process in a low-pressure chemical vapour deposition (LPCVD) furnace. For the multi-step processing presented here, two photolithography masks were required. The first mask defined the upper step of the structure ( $H-h$ ) and it was used to realize the basic waveguide structure. The default waveguide structure used for e.g. the input and output coupling was a  $10\ \mu\text{m}$  thick rib waveguide. The dimensions of the waveguides were chosen so that the SM condition was maintained [17]. The etch depth  $H-h$  and waveguide width varied slightly in different samples, but for the default rib waveguides dimensions with ratio  $h/H \sim 0.5$  and waveguide



**Figure 2.** Double-masking multi-step process.

width of  $\sim 9\ \mu\text{m}$  were used. The second mask defined the lower etch step, marked with the letter  $g$  in figure 1. It was used in realizing additional grooves for waveguide bends, mirrors, and optical mode-converters. The openings of the second mask were effective only when they overlapped with the openings of the first mask. This enabled the passive alignment of the two masks, which alleviated the effect of the limited alignment accuracy ( $\pm 1\ \mu\text{m}$ ) of the contact mask aligner. This feature of the multi-step process was especially useful in the realization of waveguide mirrors, where a deep vertical facet composed of two separate etch steps was realized. Two different process sequences, which could be used to fabricate the structure in figure 1, are described below.

### 2.1. Double-masking process

The first option was to use the *double-masking process* shown in figure 2. The essence of this process was to first pattern both mask layers and then etch the structures into silicon. The advantage of this approach was that the difficult lithography after a deep silicon etching was avoided. The upper etch step was defined first by patterning a  $1\ \mu\text{m}$  TEOS oxide layer with standard photolithography and dry oxide etching in a parallel plate plasma etcher. The patterned oxide was not used as an etch mask for silicon at this point, but a new photoresist layer was applied. This resist layer defined the lower step ( $g$ ) and was used in the first Si etching step. Silicon etching was done using an inductively coupled plasma (ICP) type reactive ion etcher made by Surface Technology Systems (STS). The etching recipe was specially designed for low-loss optical waveguide applications [18]. After the etching, the resist was removed and the second etching step used the oxide layer as the etch mask, defining the dimension  $H-h$ . After the oxide mask removal, a cladding oxide layer was deposited. TEOS oxide was chosen for the cladding oxide, since among the available oxidation processes it generated the lowest stress to the waveguide structures [4].

The *double-masking process* is capable of achieving accurate mask patterning for both etch steps, since the lithography is always done on the unpatterned silicon surface. The only challenging part of this process is the second Si etching (step 4 in figure 2). After the first etch, there is topography in the structure, and etching this topography deeper in silicon results in localized surface roughness. The roughness is generated at the upper corners of the lower etch step in the form of a spiky structure along the corners. It can be reduced by a subsequent thermal oxidation or Si wet etching, but it is difficult to remove the residuals completely. However, the excess Si roughness might be avoided by slightly compromising the smooth waveguide side walls and verticality of the etch. This should be studied more, since the *double-masking process* is preferred when accurate lithography and deep etching is required.

## 2.2. Sequential process

The other process option was the *sequential process*, in which the basic waveguide structure and the additional grooves were fabricated sequentially, as shown in figure 3. The upper Si etch step was defined first by patterning the oxide layer with photolithography and dry oxide etching. After the Si etch, the resist was removed, while the patterned oxide was left on the unetched areas. The second lithography was then done, defining the lower etch (g). The spinning process over topography required special attention. Here, lithography with sufficient quality was achieved by changing the resist dispensing parameters and optimizing the exposure time. The exposure was done in the multi-exposure mode so that the lamp was on three times for a period of 20 s. For comparison, the standard exposure time for the contact aligner (Karl Süss MA6) used here was 30 s for the 2.1  $\mu\text{m}$  thick resist (SPRT515). The total exposure time of 60 s and development time of 120 s (in AZ726 developer) proved sufficient parameters for the lithography. After the second Si etch, the resist mask and the oxide mask were removed. Finally, TEOS oxide cladding was deposited.

The use of the *sequential process* results in very smooth Si surfaces and corners, but the resolution of the lithography on the uneven surface limited the dimensions achievable with the process. The maximum etch depth before the second lithography depends greatly on the mask patterns and the lithography process used. With the lithography process used here the maximum depth of the first etch was approximately 6  $\mu\text{m}$ . However, by using resists designed for high aspect ratio, structures with small features and deep etches can also be realized with the process. The *sequential process* is advisable when shallow etches are used, or when sharp corners must be achieved in the multi-step structure.

## 2.3. Optical characterization

The optical properties of the fabricated structures were determined using the insertion loss measurements. The setup enabled separate transmission measurements for both TE and TM polarization. In the measurement the laser light was polarized and butt-coupled into a waveguide with a polarization-maintaining fibre. One axis of the fibre was aligned parallel to the chip surface, i.e. horizontally. This

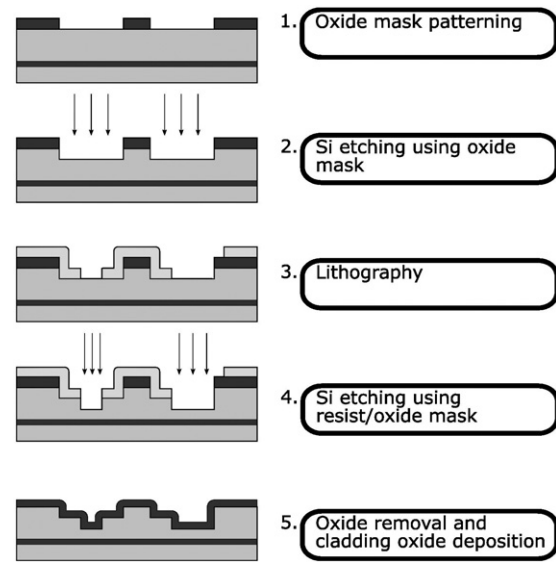


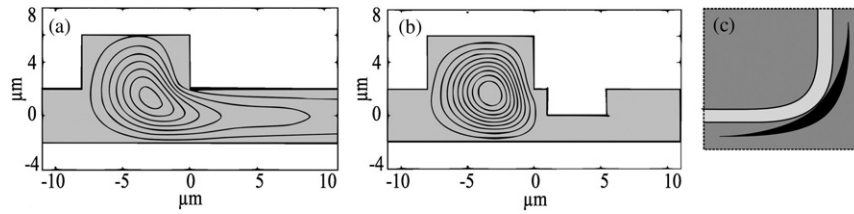
Figure 3. Sequential multi-step process.

ensured that the polarization modes of the input fibre were coupled directly to the polarization modes of the waveguide with minimum cross-talk (below  $-25$  dB). The transmitted light was coupled into a single-mode fibre and guided to a detector. The multi-step test structures had equally long reference waveguides on the mask set. They had a cross-section identical to the input and output waveguides of the corresponding multi-step structure. Thus, the coupling losses, as well as the losses of the input and output waveguides could be subtracted from the total (fibre-to-fibre) insertion loss. The accuracy of the resulting on-chip insertion loss determination was estimated as  $\pm 0.5$  dB. The measurement accuracy was further improved by joining identical successive components and measuring the on-chip insertion loss through several elements. Thus, the inaccuracy of the on-chip insertion loss measurement was divided between the successive elements. The measurements were carried out at 1550 nm wavelength.

## 3. Applications of the multi-step processing

### 3.1. Waveguide bends

The combination of SM operation and a large field profile requires very long bending radii. This was confirmed in the simulations carried out with the commercial TempSelene software (version 4.3.04) for SOI rib waveguides with various thicknesses. The minimum bending radius for a given bending loss depends significantly on the waveguide dimensions. For example, if the acceptable loss is set to a relatively high value of 1 dB/90°, a bending radius above 20 mm has to be used for 10  $\mu\text{m}$  thick waveguides. This is clearly too large for useful components. A bend size reduction can be achieved by reducing the waveguide dimensions, but at the same time the advantages of large mode-field are lost. Another solution is the continuous fine-tuning of waveguide width and bending radius along the bend. However, the improvements with this approach are rather limited. The multi-step processing principle can provide an elegant and a radical solution for reducing the



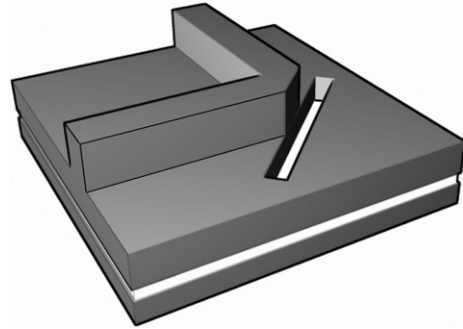
**Figure 4.** Cross-sections and calculated intensity distributions of SOI waveguides with a bending radius of 10 mm (a) without and (b) with an additional groove. (c) Top view showing the positioning of the groove in a bent waveguide.

size of a waveguide bend. By etching an additional groove to the outer edge of a bent rib waveguide (figure 4), one can increase its horizontal effective index contrast. Here, the groove bend test structures were fabricated with the *double-masking process*. The upper Si step was  $5.1 \mu\text{m}$  deep for the bent  $10 \mu\text{m}$  thick rib waveguide. The additional grooves were designed to approach the bent waveguide from a distance, so that coupling losses between the straight and bent waveguide sections were minimized. The width of the groove was of the same order as the rib of the bent waveguide. Each bend test structure was composed of four successive  $45^\circ$  bends.

Two bending radii were used for the test bent waveguides with a groove, 5 and 10 mm. For the 5 mm bending radius, the bend loss was determined as  $0.9 \pm 0.1 \text{ dB}/90^\circ$  and  $0.7 \pm 0.1 \text{ dB}/90^\circ$  for the TE and TM polarizations, respectively. Thus, the groove enabled a significant decrease of the bending radius from over 20 to 5 mm with  $10 \mu\text{m}$  thick SOI waveguides, if the  $1 \text{ dB}/90^\circ$  bending loss limit is used. For comparison, a similar waveguide with 5 mm bending radius without the groove resulted in a bending loss over  $10 \text{ dB}/90^\circ$  for both polarizations. Similar results were achieved for the 10 mm bending radius. This suggests that the bending losses measured here were not dominated by the loss factor proportional to the bending radius, but another loss mechanism emerged. Since the *double-masking process* was used, the spiky Si residuals along the corner of the additional groove probably caused excess scattering losses along the bend. It is expected that by fabricating the grooves with the *sequential process*, the bending losses can be further decreased. It is worth noticing that the additional groove measured here was through-etched until the BOX layer, unlike the partially etched groove in figure 4. Generally, this enhances the multimode behaviour in a bend, reduces the bending losses through a higher index contrast, and increases the scattering losses at the etched surface.

### 3.2. Waveguide mirrors

Another application of the proposed multi-step process is a through-etched mirror facet monolithically integrated with a partially etched,  $10 \mu\text{m}$  thick SM rib waveguide. The main advantage of the rib-type waveguide mirror is that it occupies a very small footprint when added to a SM rib waveguide circuit. The waveguide mirror fabricated in this study is schematically illustrated in figure 5. The angle between the input and output waveguides was  $90^\circ$ . The multi-step processing described here enabled a passive alignment of the lower etch step to the mirror facet. Thus, the alignment of the mirror to the input and output waveguides was not affected by the limited



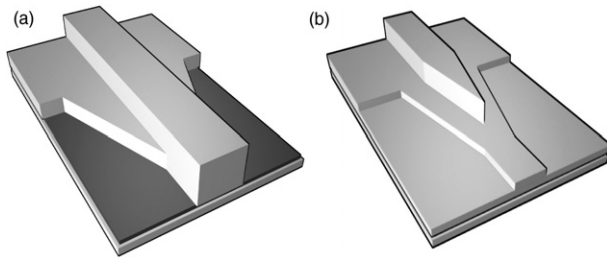
**Figure 5.** SOI waveguide mirror monolithically integrated with rib waveguides.

alignment resolution. Since the mirror facet is not formed during a single etch step, but two successive steps are used, it is crucial to avoid a discontinuity at the junction of the etch steps. This kind of discontinuity is typical for the *sequential process* due to the limited resolution of the second lithography. Thus, the fabrication of the waveguide mirror was done with the *double-masking process*. With this process, a uniform and smooth mirror facet was achieved. The upper Si etch step was  $4.9 \mu\text{m}$  deep, while the lower etch step was done through the remaining SOI layer. Each mirror test structure involved eight  $90^\circ$  mirrors.

The best loss results for the  $90^\circ$  rib waveguide mirrors were measured as  $0.59 \pm 0.06 \text{ dB}/90^\circ$  and  $0.74 \pm 0.06 \text{ dB}/90^\circ$  for the TE and TM polarization, respectively. As the footprint of the mirror is significantly smaller than that of the bend, the use of the mirrors for thick waveguides is very attractive. It should be noted, however, that the optical losses of the mirror are very sensitive to the verticality and roughness of the mirror facet. Here, the *double-masking process* and the specially designed ICP Si etch process enabled the low optical losses of the waveguide mirror.

### 3.3. Waveguide converters

Thick Si rib waveguides have many advantages, such as simultaneous SM operation and good fibre coupling efficiency, which are impossible for strip-type waveguides. However, Si strip waveguides can also offer some advantages, such as simple design and simulation due to the vertical symmetry, low inter-waveguide cross-talk, extremely small bending radii, and a lack of waveguide dispersion. Therefore, a low-loss converter between strip and rib waveguides is very useful in the design and minimization of the microphotonic chips. Another

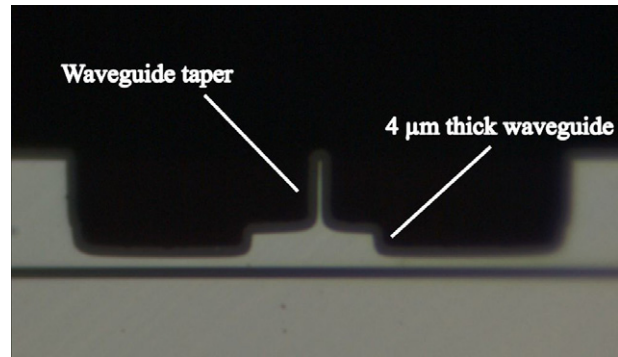


**Figure 6.** Schematic illustration of (a) a rib-strip converter and (b) a vertical taper.

useful element for microphotonics is a vertical taper, which adiabatically changes the thickness of an SM rib waveguide. Rib-strip converters and vertical tapers are schematically illustrated in figure 6. In the rib-strip converter (figure 6(a)) the additional grooves realized beside the rib waveguide are spread, until a strip waveguide is formed. In the vertical taper (figure 6(b)), the thick rib waveguide is narrowed down until it vanishes. By then, the light is coupled from the thicker waveguide into the thinner rib waveguide. It should be noted that the converters and vertical tapers can be modified by tuning the depths of the two etch steps (without modifying mask layouts). In figure 6 the etch depths relative to the SOI layer thickness are approximately 50% + 50% for the converter and 60% + 20% for the vertical taper. However, by using e.g. 50% + 25% etch steps for the converter, the conversion would appear between two rib waveguides with clearly different slab thicknesses and  $h/H$  ratios. Thus, the converter can be considered as a structure for changing the horizontal confinement of a waveguide. Similarly, using e.g. 60% + 40% etch steps for the vertical taper would provide a transformation between a thick rib waveguide and a thinner strip waveguide (instead of a thinner rib waveguide). Thus, the vertical taper essentially changes the waveguide thickness.

The vertical taper was fabricated with the *sequential process*, which ensured a low top surface roughness of the thinner waveguide. The upper etch was about 6  $\mu\text{m}$  deep, defining the 10  $\mu\text{m}$  thick rib waveguide. The thickness of the thinner waveguide was also defined by this etch step to 4  $\mu\text{m}$ . The depth of the lower etch step was 2  $\mu\text{m}$ . The taper section is illustrated in figure 7. In the figure, the 10  $\mu\text{m}$  waveguide is narrowed well below 1  $\mu\text{m}$ . The test mask had six successive vertical taper elements adjoint, so that the light was coupled from the 10  $\mu\text{m}$  thick waveguide into the 4  $\mu\text{m}$  waveguide and vice versa three times. Thus, the measurement accuracy for a single vertical taper was better than  $\pm 0.1$  dB. Based on the results, the excess losses for a single vertical taper were  $0.7 \pm 0.1$  dB, including the impact of the polarization dependent loss.

The *double-masking process* was used for the strip-rib converter. The upper etch step was 5  $\mu\text{m}$ . This formed the basic rib structure for the input waveguides. The lower etch step reached through the remaining  $\sim 5$   $\mu\text{m}$  of the SOI layer. The losses induced by the rib-strip converter were determined by measuring the transmission of 22 successive elements, which gave a measurement accuracy of  $\pm 0.02$  dB. The resulting excess losses for a single rib-strip converter were  $0.05 \pm 0.02$  dB for TE and  $-0.01 \pm 0.02$  dB for TM.



**Figure 7.** Microscope image of a cross-section of a vertical taper. Both 4  $\mu\text{m}$  and tapered 10  $\mu\text{m}$  rib waveguides are visible.

(This figure is in colour only in the electronic version)

The apparently negative loss for TM is due to the finite measurement accuracy. In conclusion, the excess loss and the polarization dependent loss are both below 0.07 dB for a single rib-strip converter.

#### 4. Conclusions

Multi-step processing to be used in microphotonic applications was studied. Two options for the fabrication sequence were tested, both having one silicon etch step with an oxide mask and another with a resist mask. The *double-masking process* utilized two lithography steps before the two silicon etching steps. In the *sequential process*, each lithography step was followed by an etching step. The choice between the two options depends on the special requirements of the targeted structure. The multi-step processing was tested with different optical waveguide structures. An additional groove etched in a bent 10  $\mu\text{m}$  thick rib waveguide enabled a significant bend loss reduction with a bending radius of 5 mm. Optical losses below 1 dB/90° were measured for a waveguide mirror. A vertical taper for coupling rib waveguides of different thicknesses had excess losses of  $0.7 \pm 0.1$  dB. A converter coupling a rib waveguide to a strip waveguide showed a negligible loss below 0.07 dB. In the future, the multi-step fabrication will be extended to structures with more masks and etch steps to further increase the versatility of the technique.

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