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CMOS RADIO FREQUENCY CIRCUITS FOR SHORT-RANGE DIRECT-CONVERSION RECEIVERS

Doctoral Dissertation

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Helsinki University of Technology
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Abstract

The research described in this thesis is focused on the design and implementation of radio frequency (RF) circuits for direct-conversion receivers. The main interest is in RF front-end circuits, which contain low-noise amplifiers, downconversion mixers, and quadrature local oscillator signal generation circuits. Three RF front-end circuits were fabricated in a short-channel CMOS process and experimental results are presented.

A low-noise amplifier (LNA) is typically the first amplifying block in the receiver. A large number of LNAs have been reported in the literature. In this thesis, wideband LNA structures are of particular interest. The most common and relevant LNA topologies are analyzed in detail in the frequency domain and theoretical limitations are found. New LNA structures are presented and a comparison to the ones found in the literature is made. In this work, LNAs are implemented with downconversion mixers as RF front-ends. The designed mixers are based on the commonly used Gilbert cell. Different mixer implementation alternatives are presented and the design of the interface between the LNA and the downconversion mixer is discussed.

In this work, the quadrature local oscillator signal is generated either by using frequency dividers or polyphase filters (PPF). Different possibilities for implementing frequency dividers are briefly described. Polyphase filters were already introduced by the 1970s and integrated circuit (IC) realizations to generate quadrature signals have been published since the mid-1990s. Although several publications where the performance of the PPFs has been studied either by theoretical calculations or simulations can be found in the literature, none of them covers all the relevant design parameters. In this thesis, the theory behind the PPFs is developed such that all the relevant design parameters needed in the practical circuit design have been calculated and presented with closed-form equations whenever possible. Although the main focus was on two- and three-stage PPFs, which are the most common ones encountered in practical ICs, the presented calculation methods can be extended to analyze the performance of multistage PPFs as well.

The main application targets of the circuits presented in this thesis are the short-range wireless sensor system and ultrawideband (UWB). Sensors are capable of monitoring temperature, pressure, humidity, or acceleration, for example. The amount of transferred data is typically small and therefore a modest bit rate, less than 1 Mbps, is adequate. The sensor system applied in this thesis operates at 2.4-GHz ISM band (Industrial, Scientific, and Medical). Since the sensors must be able to operate independently for several years, extremely low power consumption is required. In sensor radios, the receiver current consumption is dominated by the blocks and elements operating at the RF. Therefore, the target was to develop circuits that can offer satisfactory performance with a current consumption level that is small compared to other receivers targeted for common cellular systems.

On the other hand, there is a growing need for applications that can offer an extremely high data rate. UWB is one example of such a system. At the moment, it can offer data rates of up to 480 Mbps. There is a frequency spectrum allocated for UWB systems between 3.1 and 10.6 GHz. The UWB band is further divided into several narrower band groups (BG), each occupying a bandwidth of approximately 1.6 GHz. In this work, a direct-conversion RF front-end is designed for a dual-band UWB receiver, which operates in band groups BG1 and BG3, i.e. at 3.1 – 4.8 GHz and 6.3 – 7.9 GHz frequency areas, respectively. Clearly, an extremely

wide bandwidth combined with a high operational frequency poses challenges for circuit design. The operational bandwidths and the interfaces between the circuit blocks need to be optimized to cover the wanted frequency areas. In addition, the wideband functionality should be achieved without using a number of on-chip inductors in order to minimize the die area, and yet the power consumption should be kept as small as possible.

The characteristics of the two main target applications are quite different from each other with regard to power consumption, bandwidth, and operational frequency requirements. A common factor for both is their short, i.e. less than 10 meters, range. Although the circuits presented in this thesis are targeted on the two main applications mentioned above, they can be utilized in other kind of wireless communication systems as well. The performance of three experimental circuits was verified with measurements and the results are presented in this work. Two of them have been a part of a whole receiver including baseband amplifiers and filters and analog-to-digital converters. Experimental circuits were fabricated in a 0.13-μm CMOS process. In addition, this thesis includes design examples where new circuit ideas and implementation possibilities are introduced by using 0.13-μm and 65-nm CMOS processes. Furthermore, part of the theory presented in this thesis is validated with design examples in which actual IC component models are used.

Tiivistelmä

Tässä väitöskirjassa esitetty tutkimus keskittyy suoramuunnosvastaanottimen radiotaajuudella (radio frequency, RF) toimivien piirien suunnitteluun ja toteuttamiseen. Työ keskittyy vähäkohinaiseen vahvistimeen (low-noise amplifier, LNA), alassekoittajaan ja kvadratuurisen paikallisoskillaattorisignaalin tuottavaan piiriin. Työssä toteutettiin kolme RF-etupäätä erittäin kapean viivanleveyden CMOS-prosessilla, ja niiden kokeelliset tulokset esitetään.

Vähäkohinainen vahvistin on yleensä ensimmäinen vahvistava lohko vastaanottimessa. Useita erilaisia vähäkohinaisia vahvistimia on esitetty kirjallisuudessa. Tämän työn kohteena ovat eritoten laajakaistaiset LNA-rakenteet. Tässä työssä analysoidaan taajuustasossa yleisimmät ja oleellisimmat LNA-topologiat. Lisäksi uusia LNA-rakenteita on esitetty tässä työssä ja niitä on verrattu muihin kirjallisuudessa esitettyihin piireihin. Tässä työssä LNA:t on toteutettu yhdessä alassekoittimen kanssa muodostaen RF-etupään. Työssä suunnitellut alassekoittimet perustuvat yleisesti käytettyyn Gilbertin soluun. Erilaisia sekoittajan suunnitteluvaihtoehtoja ja LNA:n ja alassekoittimen välisen rajapinnan toteutustapoja on esitetty.

Tässä työssä kvadratuurinen paikallisoskillaattorisignaali on muodostettu joko käyttämällä taajuusjakajia tai monivaihesuodattimia. Erilaisia taajuusjakajia ja niiden toteutustapoja käsitellään yleisellä tasolla. Monivaihesuodatinta, joka on alunperin kehitetty jo 1970-luvulla, on käytetty integroiduissa piireissä kvadratuurisignaalin tuottamiseen 1990-luvun puolivälistä lähtien. Kirjallisuudesta löytyy lukuisia artikkeleita, joissa monivaihesuodattimen toimintaa on käsitelty teoreettisesti laskien ja simuloinnein. Kuitenkaan kaikkia sen suunnitteluparametreja ei tähän mennessä ole käsitelty. Tässä työssä monivaihesuodattimen teoriaa on kehitetty edelleen siten, että käytännön piirisuunnittelussa tarvittavat oleelliset parametrit on analysoitu ja suunnitteluyhtälöt on esitetty suljetussa muodossa aina kuin mahdollista. Vaikka työssä on keskitytty yleisimpiin eli kaksi- ja kolmiasteisiin monivaihesuodattimiin, on työssä esitetty menetelmät, joilla laskentaa voidaan jatkaa aina useampiasteisiin suodattimiin asti.

Työssä esiteltyjen piirien pääkohteina ovat lyhyen kantaman sensoriradio ja erittäin laajakaistainen järjestelmä (ultrawideband, UWB). Sensoreilla voidaan tarkkailla esimerkiksi ympäristön lämpötilaa, kosteutta, painetta tai kiihtyvyyttä. Siirrettävän tiedon määrä on tyypillisesti vähäistä, jolloin pieni tiedonsiirtonopeus, alle 1 megabitti sekunnissa, on välttävä. Tämän työn kohteena oleva sensoriradiojärjestelmä toimii kapealla kaistalla 2,4 gigahertsin ISM-taajuusalueella (Industrial, Scientific, and Medical). Koska sensorien tavoitteena on toimia itsenäisesti ilman pariston vaihtoa useita vuosia, täytyy niiden kuluttaman virran olla erittäin vähäistä. Sensoriradiossa vastaanottimen tehonkulutuksen kannalta määräävässä asemassa ovat radiotaajuudella toimivat piirit. Tavoitteena oli tutkia ja kehittää piirirakenteita, joilla päästään tyydyttävään suorituskykyyn tehonkulutuksella, joka on vähäinen verrattuna muiden tavallisten langattomien tiedonsiirtojärjestelmien radiovastaanottimiin.

Toisaalta viime aikoina on kasvanut tarvetta myös järjestelmille, jotka kykenevät tarjoamaan erittäin korkean tiedonsiirtonopeuden. UWB on esimerkki tällaisesta järjestelmästä. Tällä hetkellä se tarjoaa tiedonsiirtonopeuksia aina 480 megabittiin sekunnissa. UWB:lle on varattu taajuusalueita 3,1 ja 10,6 gigahertsin taajuuksien välillä. Kyseinen kaista on edelleen jaettu pienempiin taajuusryhmiin (band group, BG), joiden kaistanleveys on noin 1,6 gigahertsiä. Tässä työssä on toteutettu RF-etupää radiovastaanottimeen, joka pystyy toimimaan BG1:llä ja BG3:lla eli taajuusalueilla 3,1 – 4,7 GHz ja 6,3 – 7,9 GHz. Erittäin suuri kaistanleveys

yhdistettynä korkeaan toimintataajuuteen tekee radiotaajuuspiirien suunnittelusta haasteellista. Piirirakenteiden toimintakaistat ja piirien väliset rajapinnat tulee optimoida riittävän laajoiksi käyttämättä kuitenkaan liian montaa piille integroitua kelaa piirin pinta-alan minimoimiseksi, ja lisäksi piirit tulisi toteuttaa mahdollisimman alhaisella tehonkulutuksella.

Työssä esiteltyjen piirien kaksi pääkohdetta ovat hyvin erityyppisiä, mitä tulee tehonkulutus-, kaistanleveys- ja toimintataajuusvaatimuksiin. Yhteistä molemmille on lyhyt, alle 10 metrin kantama. Vaikka tässä työssä esitellyt piirit onkin kohdennettu kahteen pääsovelluskohteeseen, voidaan esitettyjä piirejä käyttää myös muiden tiedonsiirtojärjestelmien piirien suunnitteluun. Tässä työssä esitetään mittaustuloksineen yhteensä kolme kokeellista piiriä yllämainittuihin järjestelmiin. Kaksi ensimmäistä kokeellista piiriä muodostaa kokonaisen radiovastaanottimen yhdessä analogisten kantataajuusosien ja analogia-digitaali-muuntimien kanssa. Esitetyt kokeelliset piirit on toteutettu käyttäen 0,13 μm:n viivanleveyden CMOS-tekniikkaa. Näiden lisäksi työ pitää sisällään piirisuunnitteluesimerkkejä, joissa esitetään ideoita ja mahdollisuuksia käyttäen 0,13 μm:n ja 65 nm:n viivanleveyden omaavia CMOS-tekniikoita. Lisäksi piirisuunnitteluesimerkein havainnollistetaan työssä esitetyn teorian paikkansapitävyyttä käyttämällä oikeita komponenttimalleja.

Preface

Experience is that marvelous thing that enables you to recognize a mistake when you make it again.

Franklin P. Jones

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Jouni Kaukovuori

Vantaa, February 2008

Contents

Symbols

A	amplitude
A	gain
A_{bal}	amplitude balance
A_i	insertion gain
$A_{i,max}$	maximum insertion gain
A_v	voltage gain
BW_{-3dB}	–3-dB bandwidth
BW_{dev}	bandwidth deviation factor
BW_{Iout}	output signal current bandwidth
BW_{rel}	relative bandwidth
$BW_{rel,eff}$	efficient relative bandwidth
$BW_{rel,Iout}$	relative output signal current bandwidth
$BW_{rel,S11}$	relative input matching bandwidth
BW_{S11}	input matching bandwidth
c	noise correlation coefficient
C	system capacity
C_C	coupling capacitance
C_{fb}	feedback capacitance
C_{gd}	gate-drain capacitance
C_{gs}	gate-source capacitance
C_{in}	input capacitance
CLK_{IN}	input clock signal
C_{par}	parasitic capacitance
C_{pn}	parasitic capacitance, n = 1, 2, 3, …
C_S	shunt capacitor
C_T	total capacitance
C_V	virtual ground capacitor
$e_{n,out}$	output noise voltage
f	frequency
F	noise factor
$f_{S11=-10dB}$	frequency where S_{11} equals –10 dB
$f_{S11=-10dB,HI}$	upper corner frequency where S_{11} equals –10 dB
$f_{S11=-10dB,LO}$	lower corner frequency where S_{11} equals –10 dB

F_{DSB}	double-sideband noise factor
f_{in}	input frequency
$f_{Iout,HI}$	maximum output current signal frequency
$f_{Iout,LO}$	minimum output current signal frequency
f_{max}	maximum oscillation frequency
f_{out}	output frequency
$f_{S11,HI}$	maximum input matching frequency
$f_{S11,LO}$	minimum input matching frequency
F_{SSB}	single-sideband noise factor
f_T	unity (current) gain frequency
F_{TOT}	total noise factor
G	power gain
G_{conv}	conversion gain
g_{d0}	output conductance at zero drain-source voltage
g_{ds}	channel conductance
g_g	induced gate noise factor
g_m	transconductance
$g_{m,eff}$	effective transconductance
$g_{m,n}$	transconductance of an NMOS transistor
$g_{m,p}$	transconductance of a PMOS transistor
g_{mb}	substrate transconductance
H	transfer function
I_{bias}	bias current (source)
I_{boost}	boost current (source)
I_D	drain current
$\overline{i_d^2}$	drain current noise
I_E	additional current source
$\overline{i_g^2}$	gate-induced current noise
I_{LNA}	low-noise amplifier current
I_{LO}	LO buffer current
I_{out}	output signal current
$I_{out,max}$	maximum output signal current
I_{REF}	reference bias current
IRR_{gain}	image-reject ratio defined with magnitude balance only
$IRR_{min,n}$	minimum image-reject ratio of an n-stage polyphase filter

IRR_{phase}	image-reject ratio defined with phase balance only
I_{SWI}	switch transistor current
k	magnetic coupling factor
k_B	Boltzmann's constant, $1.380658 \cdot 10^{-23}$ J/K
k_B	capacitor ratio
k_L	load impedance coefficient
$k_{L,opt,n\text{-}stg}$	optimum load impedance coefficient of an n-stage polyphase filter
k_n	coefficient for NMOS transistor
k_n	relative pole frequency factor, n = 1, 2, 3, …
k_{nC}	capacitor ratio, n = 1, 2, 3, …
k_{nR}	resistor ratio, n = 1, 2, 3, …
k_{par}	parasitic capacitance coefficient
k_S	source impedance coefficient
k_Z	ratio of polyphase filter output and input impedances
L	channel length
L	inductor
L	loss
L_{Cpar}	additional loss due to parasitic capacitance
L_d	drain inductance
L_g	gate inductance
L_{in}	input inductance
LO_{EXT}	external LO signal
LO_{VCO}	LO signal from a VCO
L_P	primary inductor
L_S	source inductance
L_S	secondary inductor
$L_{tot,n\text{-}stg}$	total loss of an n-stage polyphase filter
m	shunt-peak load design parameter
M	mutual inductance
M_{LOAD}	load transistor
M_n	MOS transistor, n = 1, 2, 3, …
M_{Nn}	NMOS transistor, n = 1, 2, 3, …
M_{Pn}	PMOS transistor, n = 1, 2, 3, …
M_{SWI}	switch transistor
n	number of fingers

n	turns ratio
N_{DSB}	input-referred double-sideband noise power
NF_{DSB}	double sideband noise figure
NF_{MIN}	minimum noise figure
NF_{SSB}	single sideband noise figure
N_S	source noise power
N_{SSB}	input-referred single-sideband noise power
p	resonator design parameter
P	power
P_{fund}	power of a fundamental signal
P_{IMDn}	power of an input-referred n^{th}-order intermodulation component
P_{in}	input power
P_{out}	output power
q	electron charge, $1.6021773 \cdot 10^{-19}$ C
Q	quality factor
Q_{in}	input network quality factor
Q_L	inductor quality factor
Q_r	resonator quality factor
R	resistor
r_{ds}	drain-source resistance
R_{eq}	equivalent (input) resistance
R_{fb}	feedback resistance
RF_{in}	input RF signal
r_g	gate resistance
R_{in}	real part of an input impedance
R_L	load resistance
R_{Lin}	series resistance of an input inductor
R_{Ls}	inductor series resistance
R_{max}	maximum resistance value
R_{min}	minimum resistance value
r_o	output resistance
R_p	shunt resistance
R_S	source resistance
R_{sh}	silicide sheet resistance
R_{typ}	typical resistor value

s	Laplace variable
S	sensitivity level
S_{11}	input matching
$S_{11,BW}$	input matching bandwidth
SNR_{in}	signal-to-noise ratio at the input
SNR_{min}	minimum signal-to-noise ratio
SNR_{out}	signal-to-noise ratio at the output
T	absolute temperature
T	signal period
T	transformer
$V_{D,sat}$	drain-source saturation voltage
$V_{dc,out}$	output common mode voltage
V_{DD}	supply voltage
V_{DS}	drain-source voltage
$\overline{v_g^2}$	gate voltage noise
V_{GS}	gate-source voltage
V_{in}	input voltage
V_{LO}	local oscillator amplitude
V_{out}	output voltage
V_{pp}	peak-to-peak voltage
V_{REF}	reference voltage
V_{RF}	RF signal amplitude
V_S	source voltage
V_T	threshold voltage
W	channel width
Z	impedance
Z_0	source (reference) impedance
Z_{fb}	feedback impedance
Z_g	gate impedance
Z_{gd}	gate-drain impedance
Z_{gs}	gate-source impedance
Z_{in}	input impedance
$Z_{in,PPF}$	polyphase filter input impedance
$Z_{in,\omega n}$	input impedance at the frequency ω_n, n = 1, 2, 3, …
Z_L	load impedance

$Z_{L,Cpar}$	load impedance with parasitic capacitance
Z_{LC}	LC resonator characteristic impedance
Z_{out}	output impedance
$Z_{out,\omega n}$	output impedance at a frequency ω_n, n = 1, 2, 3, …
$Z_{out,PPF}$	polyphase filter output impedance
Z_{rel}	relative impedance
Z_S	source impedance
α	noise parameter
α_n	n^{th}-order nonlinearity coefficient, n = 0, 1, 2, …
β	feedback factor
ϕ	control signal
δ	gate induced noise factor
χ	ratio of a transistor substrate transconductance g_{mb} and transconductance g_m
Γ	reflection coefficient
γ	drain current noise factor
ω	angular frequency
ω_0	center (angular) frequency
ω_c	corner frequency
$\omega_{c,max}$	maximum corner frequency
$\omega_{c,min}$	minimum corner frequency
$\omega_{c,n\text{-}stg}$	geometric center frequency of an n-stage polyphase filter
$\omega_{c,RCdev}$	center frequency, device values deviating from typical values
$\omega_{c,RCtyp}$	center frequency, typical device values
ω_{Fmin}	minimum noise factor frequency
$\omega_{Iout,max}$	maximum output signal current frequency
$\omega_{IRR,min}$	minimum image-reject ratio frequency
ω_{max}	maximum frequency
ω_{min}	minimum frequency
ω_n	pole (angular) frequency, n = 1, 2, 3, …
ω_r	resonance (angular) frequency
$\omega_{S11=-10dB}$	angular frequency where S_{11} equals –10 dB
$\omega_{S11=-10dB,HI}$	upper angular frequency where S_{11} equals –10 dB
$\omega_{S11=-10dB,LO}$	lower angular frequency where S_{11} equals –10 dB
ω_T	unity gain (angular) frequency
$\Delta\omega_{-3dB}$	–3-dB bandwidth

$\Delta\theta$	phase deviation
ΔL	loss difference
ΔP_n	ratio between fundamental signal and the n^{th}-order intermodulation product
ΔR	resistance value deviation
ΔR_{max}	relative maximum resistor value deviation
ΔR_{min}	relative minimum resistor value deviation
ΔT	turn on time
ΔV	differential (voltage) signal

Abbreviations

ac	alternative current
ADC	analog-to-digital converter
AGC	automatic gain control
BB	baseband
BG	band group
BT	Bluetooth
BT LEE	low-end extension for Bluetooth
BW	(noise) bandwidth
BWER	bandwidth extension ratio
CD	common-drain
CDMA	code division multiple access
CG	common-gate
CLK	clock
CMOS	complementary metal oxide semiconductor
CMRR	common-mode rejection ratio
CS	common source
CSMA	carrier sense multiple access
DAC	digital-to-analog converter
dc	direct current
DCR	direct-conversion receiver
DCS	Digital Cellular System
DSB	double-sideband
ESD	electrostatic discharge
FCC	Federal Communications Commission
FDD	frequency division duplex
FDMA	frequency division multiple access
FET	field effect transistor
GFSK	gaussian frequency shift keying
g_mC	transconductance-capacitor
GPS	Global Positioning System
GSM	Global System for Mobile Telecommunications
I	in-phase
IC	integrated circuit

ICP	input compression point
IDCS	inductively degenerated common-source
IEEE	Institute of Electrical and Electronics Engineers, Inc
IF	intermediate frequency
IIP2	input referred second-order intercept point
IIP3	input referred third-order intercept point
IMD2	second-order intermodulation distortion
IMD3	third-order intermodulation distortion
IP2	second-order intercept point
IP3	third-order intercept point
IRR	image-reject ratio
ISM	Industrial, Scientific, and Medical
LC	inductor-capacitor
LNA	low-noise amplifier
LO	local oscillator
MBOA	Multiband OFDM Alliance
MB-OFDM	multiband OFDM
MOS(FET)	metal oxide semiconductor (field-effect transistor)
NF	noise figure
NMOS	N-channel metal oxide semiconductor transistor
OFDM	orthogonal frequency division multiplexing
P_{1dB}	input compression point
PA	power amplifier
PCB	printed circuit board
PCS	Personal Communication Services
PDC	Personal Digital Cellular, (Pacific Digital Cellular)
PLL	phase-locked loop
PMOS	P-channel metal oxide semiconductor transistor
PPF	polyphase filter
PSD	power spectral density
PVT	process, voltage, and temperature
Q	quadrature phase
RC	resistor-capacitor
RF	radio frequency
RLC	resistor-inductor-capacitor

RSSI	received signal strength indicator
RX	receiver
SAW	surface acoustic wave
SCL	source-coupled logic
SNR	signal-to-noise ratio
SPF	single-stage polyphase filter
SSB	single-sideband
TX	transmitter
UMTS	Universal Mobile Telecommunications System
U-NII	Unlicensed National Information Infrastructure
UWB	ultrawideband
VCO	voltage controlled oscillator
VGA	variable gain amplifier
WCDMA	Wideband Code Division Multiple Access
Wi-Fi	Wireless Fidelity
WiMAX	Worldwide Interoperability for Microwave Access
WLAN	wireless local area network
WPAN	wireless personal area network

1 Introduction

During the last decade, we have seen the emergence of numerous new radio technologies and applications. The development has been rapid and the field of new innovations is wide. Lately, the development of wireless systems has diverged, with the trend now being to offer quite different data rates. High data rates and wide bandwidths are provided to enable consumers to transfer larger volumes of data in smaller amounts of time. Ultrawideband (UWB), which is capable of providing data rates up to 480 Mbps, is one example of such a system. On the other hand, there exist a class of applications that do not require such high speed or bandwidth, but would still gain benefit from a wireless connection. Wireless sensors are an example of applications where a modest, i.e. less than 1 Mbps, capacity is adequate. Sensors operate with extremely low power providing autonomous operation for several years with minimal maintenance cost and effort.

The CMOS technology evolution is mainly driven by the microprocessor industry. As line width continues to shrink, the transistors occupy less silicon area and switch faster, which is crucial for digital computing. Radio frequency (RF) designs have also gained benefit from technology scaling. The typical figures of merit, cut-off frequency f_T and maximum oscillation frequency f_{MAX}, are approximately inversely proportional to the channel length, and both have exceeded the 100 GHz limit [1]. The speed of active devices is therefore more than adequate for the common wireless systems such as GSM, WCDMA, Bluetooth, and WLAN (IEEE 802.11a/b/g), which operate at frequencies below 6 GHz. In addition, their speed is sufficient for UWB, for which maximum operational frequencies are around 10 GHz.

Clearly, the design of digital and analog circuits in modern deep-submicron process faces several new challenges. For example, gate current leakage, lowering self gain g_m/g_{ds}, device matching etc. are the primary challenge in scaled CMOS technologies [2]. Except for the switching time, the analog performance of the transistors is getting worse, along with ever-shrinking gate length. Thus, analog/RF ICs profit less from new technology generations than pure digital electronics. The decreasing supply voltages are making the design of analog and RF circuits more challenging, while the continuous power supply voltage reduction does not lead to lower power consumption [2]. RF circuits are usually dominated by passive components, the size of which does not scale proportionately. As a result, the RF chip area does not shrink as much as digital circuits do. Despite of all the challenges, there is a need to realize complete transceivers and baseband processors on a single CMOS chip to minimize the silicon area and costs. Lately, innovative receivers, where the digital signal processing functions are brought closer to the LNA, have been published [3], [4]. Still, most of the RF front-ends, including at least an LNA and mixer, are designed in the analog domain.

1.1 Research contribution and publications

This thesis concentrates on the design and implementation of RF circuits for low-power short-range applications such as sensor systems and UWB. The main interest is in LNAs, downconversion mixers, and quadrature local oscillator (LO) signal generation circuits for direct-conversion receivers. The author provides solutions related to low-power and wideband applications. The thesis includes theory involved in analyzing the performance of the existing

circuits and proposes new ones. It should be noted that the circuits presented here are not limited to these two main applications, but can be utilized in other kinds of wireless communication systems as well.

A large number of receivers for sensor applications and UWB have been reported in the literature. It is not the purpose of this thesis to review these comprehensively. Nor is the focus of this thesis on developing models for different IC components or on deriving requirements for different blocks based on system specifications and receiver partitioning.

This thesis is mainly based on the previously published work of the author in [P1] – [P7]. The short summary and contribution of each publication is given below. In addition, the author has authored or co-authored other publications related to the topics in [P8] – [P12], which are not included in this thesis.

Paper P1 is a journal article presenting a receiver design for a 2.4-GHz sensor system. It includes a front-end consisting of an LNA, which is merged with the downconversion mixers, LO buffers, and one baseband channel. The receiver was designed, implemented, and measured by a research team, which consisted of four members, including the author. The other members were Prof. J. Ryynänen, J. Järvinen, and D.Sc. J. Jussila. The author is responsible for the design and implementation of the RF front-end with Prof. J. Ryynänen. J. Järvinen and D.Sc. J. Jussila are responsible for designing the analog baseband parts. The idea of the presented current boosting method was originally proposed by Prof. J. Ryynänen. The other authors, D.Sc. K. Kivekäs and M. Honkanen, are mainly responsible for writing the details covering the sensor system. Prof. K. Halonen gave valuable comments on the manuscript.

Paper P2 is a conference article that deals the circuit design for the sensor system presented in [P1]. Compared to the first demonstrator [P1], the LNA and mixer are separated, the 90-degree phase shift generation circuit is included, the second baseband channel is added, and the receiver also includes improved limiters for A/D conversion, the received signal strength indicator (RSSI), and on-chip bias current generator. However, the active area from the first receiver is not increased. The contribution is same as for paper [P1].

Paper P3 is a conference paper that demonstrates the RF front-end design in a 65-nm CMOS. The front-end includes the low-noise amplifier, folded quadrature mixers, frequency divider for quadrature LO signal generation, and LO buffers. The author designed all the circuits and had the main responsibility for writing the manuscript under the supervision of Prof. J. Ryynänen.

Papers P4 and P5 are conference articles that analyze the performance of the inductively degenerated common-source and common-gate LNAs, respectively. The presented design examples are targeted for the UWB system. The theory presented in these papers was carried out by the author under the supervision of Prof. J. Ryynänen.

Paper P6 is a conference article, which covers the RF front-end design for the dual-mode UWB WiMedia receiver. The front-end consists of multi-stage LNAs, the downconversion mixers, the passive polyphase filters, and LO buffers. The author is responsible for the design, implementation, and measurements of the RF front-end, in addition to the writing of the manuscript under the supervision of Prof. J. Ryynänen. Prof. K. Halonen gave valuable comments for the manuscript.

Paper P7 is a journal article accepted for publication. It presents the analysis and design of passive polyphase filters in detail. The author is responsible for all the presented analysis and

has a major responsibility for the manuscript. K. Stadius is responsible for writing the introduction. He was also involved in the brainstorming of the needed analysis and, together with the other authors, suggested several improvements to the manuscript.

[P1] J. A. M. Järvinen, J. Kaukovuori, J. Ryynänen, J. Jussila, K. Kivekäs, M. Honkanen, and K. Halonen, "2.4-GHz receiver for sensor applications", *IEEE Journal of Solid-State Circuits*, vol. 40, no. 7, July 2005, pp. 1426-1433.

[P2] J. Kaukovuori, J. A. M. Järvinen, J. Ryynänen, J. Jussila, K. Kivekäs, and K. A. I. Halonen, "Direct-conversion receiver for ubiquitous communications," *Radio and Wireless Symposium (RWS'06)*, San Diego, CA, 17-19 Jan. 2006, pp. 103-106.

[P3] J. Kaukovuori, J. Ryynänen, and K. A. I. Halonen, "A direct-conversion RF front-end in a 65-nm CMOS," *Norchip Conference*, Linköping, Sweden, 20-21 Nov. 2006, pp. 235-238.

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Other publications related to the topic.

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[P10] M. Kaltiokallio, J. Kaukovuori, and J. Ryynänen, "Analysis of feedbacks in LNA matching," *European Conference on Circuit Theory and Design (ECCTD'07)*, Sevilla, Spain, 26-30 Aug. 2007, pp. 68-71.

[P11] M. Hotti, J. Kaukovuori, J. Ryynänen, J. Jussila, K. Kivekäs, and K. Halonen, "A direct conversion RF front-end for 2-GHz WCDMA and 5.8-GHz WLAN applications," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC'03)*, Philadelphia, PA, 8-10 June 2003, pp. 45-48.

[P12] J. Kaukovuori, M. Hotti, J. Ryynänen, J. Jussila, and K. Halonen, "A linearized 2-GHz SiGe low noise amplifier for direct conversion receiver," *IEEE International Symposium on Circuits and Systems (ISCAS'03)*, Bangkok, Thailand, 25-28 May 2003, pp. II-200-203.

1.2 Organization of the Thesis

This thesis is organized into six chapters. After the introduction, Chapter 2 contains the background information related to the topic of the thesis. Receiver architectures and fundamental definitions related to the receiver design are discussed. A brief introduction to sensor networks and UWB systems is given.

Chapter 3 concentrates on low-noise amplifier design. First, narrowband LNAs based on inductively degenerated common-source and common-gate topologies are discussed. Then, several LNA topologies for wideband applications are presented and analyzed. The main emphasis is on the input matching and insertion gain bandwidth analysis and optimization. Subsequently, the issues related to the bonding pad and LNA load design are covered.

Chapter 4 is focused on the downconversion mixer design. A short overview of passive mixers is provided, but most of the chapter is devoted to active Gilbert cell mixer design. The issues related to the mixer input stage, switch quad, and load design and interfaces with other blocks are discussed.

In Chapter 5, techniques to generate a quadrature signal are discussed. The main emphasis is on the analysis and design of passive polyphase filters. The design of static and dynamic frequency dividers is also presented.

The circuit implementations and design examples are included in Chapter 6. First, direct-conversion receivers targeted to low-power sensor systems are presented. Then, a design example of a 2-GHz RF front-end simulated with a 65-nm CMOS is given. The wideband LNA design examples and a processed front-end IC targeted for UWB are presented. Finally, the thesis is summarized.

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2 Overview of RF IC design for wireless radio systems

The purpose of this chapter is to provide an overview to the design of wireless short-range radio systems. Fundamental issues related to receiver design are discussed at a general level to give background information for the reader and to justify the chosen solutions presented later in the thesis. The purpose is not to provide in-depth discussion on all relevant aspects, but references to the literature are comprehensively given.

First, the common receiver architectures are briefly discussed. Next, the fundamental receiver parameters needed in RF circuit design are defined. Since this thesis also includes some circuit analysis, the MOS transistor small-signal model used in calculations is described. Wireless sensor systems and UWB, which are the two main target applications for the design examples presented in Chapter 6, are then briefly discussed.

2.1 Receiver architectures

The main purpose of the RF receiver is to provide certain tasks for the received signal such as amplifying, filtering, demodulation, and analog-to-digital conversion with adequate signal-to-noise ratio (SNR) before digital signal processing. The received RF signal can be strong or extremely weak, while there can be a strong blocking signal(s) with a certain offset from the wanted frequency, which needs to be rejected. These translate into requirements in terms of dynamic range, sensitivity, blocking, and intermodulation performance [1]. The choice of the receiver architecture affects the power dissipation, requirements, and achievable performance. The integration level with the number of external components determines the cost, which is also a crucial criterion in selecting the proper receiver architecture. In addition, external filters typically require a rather low impedance level to drive them. Therefore, when the target is to design the receiver with low power consumption, the number of such filters should be minimized.

In the following, the most common radio receiver topologies, i.e. superheterodyne, direct-conversion, low-IF, and wideband IF, are briefly introduced. Since software defined radios [2], sub-sampling receivers [3], and super-regenerative receivers [4] – [6] differ remarkably from the typical receiver topologies regarding the implementation of RF parts, they are left out of this thesis.

2.1.1 Direct-conversion architecture

The direct-conversion topology is also called as *zero-IF* or *homodyne* architecture [7]. It was published in 1924 by F. M. Colebrook [8] and the first practical implementations were introduced in 1947 [9]. However, it was not until the beginning of 1990s that the DCR was suitable for IC integration due to difficulties of handling the problems associated with second-order nonlinearity and dc offsets. The first IC DCRs were applied on paging receivers [10].

The block diagram of a typical direct-conversion receiver is shown in Fig 2.1. Because the selectivity of the front-end usually is not adequate, the RF signal after the antenna is pre-filtered to attenuate the signals out of the reception band. The signal is amplified in the low-noise amplifier (LNA) before being downconverted to zero intermediate frequency (IF). In CDMA

and WCDMA systems, an external interstage filter after the LNA can be used to attenuate the TX signal leakage and to relax the linearity requirements of the succeeding mixer [11], [12]. For phase- and frequency-modulated signals, the downconversion must be performed in quadrature to prevent signal sidebands from aliasing on one another [13]. Because the LO is centered in the desired channel, useful signal and noise occupy both the upper and lower sidebands. The low-pass filter with a bandwidth of a half of the symbol rate removes adjacent channels at baseband. Because the filtering is performed at low frequencies, the filters can be realized on-chip without external high-Q components.

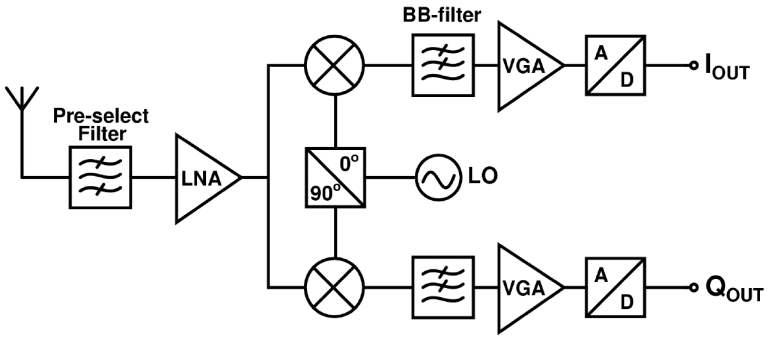

Fig 2.1. Direct-conversion receiver.

From a power consumption point of view, the direct-conversion architecture is a tempting solution. The number of internal nodes operating at RF frequency is small and there is no need for buffering the high-frequency signals off-chip. Because the RF signal is converted directly to zero intermediate frequency (IF), the image consists of the channel itself. Therefore, DCR architecture eliminates the image-reject problem existing in other radio architectures [13]. However, insufficient amplitude and phase balance between in-phase (I) and quadrature phase (Q) signals can increase the bit error rate. Compared to other architectures, the requirement for the image-rejection ratio is less stringent [11], [14].

DCR has its own drawbacks, for example, a high sensitivity to flicker noise and dc offsets [13], [15]. Wideband communications systems, e.g. WCDMA, WLAN, and UWB, reduce the influence of the flicker noise and, depending on the system specifications, the dc offset problem can be relaxed by highpass filtering without deteriorating the SNR [11]. On the other hand, in narrowband systems such as GSM, PCS, and Bluetooth, most of the signal power is located close to dc frequency and therefore highpass filtering is not possible [14], [16]. Self-mixing, LO leakage, and even-order distortion, which can deteriorate the received signal, are covered in detail in, for example, [13], [15], [17], and [18].

2.1.2 Superheterodyne receiver

The superheterodyne architecture was introduced by E. Armstrong in 1918 [19]. The block diagram of a superheterodyne receiver is shown in Fig 2.2. The pre-section filter suppresses the signals out of the reception band. The LNA output is matched to the image-reject filter, which attenuates the unwanted signals and noise at the image-frequencies. The channel-select filter after the first downconversion is usually at the fixed frequency. Therefore, the first intermediate frequency is typically set by the VCO, which frequency is adjustable to cover the whole

reception band. The first IF must be higher than half of the reception bandwidth (i.e. the bandwidth of the pre-selection filter) to keep the image signal out of the downconverted band. After the channel-select filter, the signal is amplified and divided into I and Q branches in the demodulator. The selectivity can be improved by increasing the number of IF steps, but this comes at the expense of an additional filter stage.

The main drawback of a superheterodyne is the number of external filters, which are difficult to integrate on-chip with current IC technologies. That leads to a low integration level and both the cost and power consumption are increased due to increased number of off-chip components and due to buffering high-frequency signals off-chip. However, superior sensitivity and selectivity can be achieved with superheterodyne architecture [20]. The superheterodyne architecture is the most current-consuming receiver and requires expensive external components. It is therefore not applicable to multi-mode receivers or low-power systems.

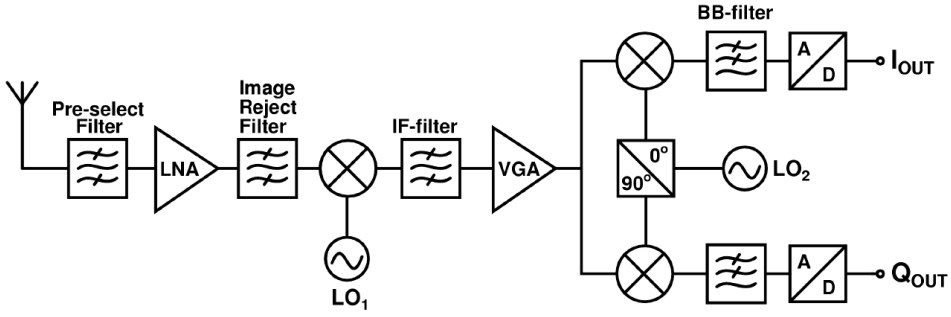

Fig 2.2. Superheterodyne receiver.

2.1.3 Low-IF architecture

Basically, the block diagram of the low-IF receiver is same as for the DCR (see Fig 2.1). The low-IF receiver downconverts the input signal directly to a low IF frequency, which is above dc, but lower than half of the reception bandwidth. Single-stage downconversion is performed in quadrature, and a low-IF receiver does not need an external intermediate filter. Thus, a high integration level is achieved. Compared to the DCR, the low-IF receiver does not suffer from the dc offset problem. Because there is not a signal at dc, the dc offsets can be filtered out without removing the signal. In addition, the flicker noise is less problematic.

The drawback of the low-IF receiver is that the mirror (image) signal, which has an offset from the LO frequency equal to the desired channel but which is on the opposite side of the LO, is different from the wanted signal. Thus, the low-IF architecture requires a good matching for image rejection [21]. The choice of the IF frequency offers design tradeoffs. A very low IF relaxes the image-rejection requirement but complicates the requirements for the frequency synthesizer [16]. In addition, if the IF frequency is too low, the signal can be corrupted by $1/f$ noise and the fractional bandwidth, where the image must be rejected, becomes larger [22]. High IF frequency, however, increases the complexity and the current consumption of the IF stages. The low-IF receiver is feasible for narrowband systems having a moderate IRR requirement, e.g. GSM [23], GPS [24], DCS-1800 [25], and Bluetooth [16]. Low-IF topology is proposed for 2.4-GHz WLAN as well [22].

2.1.4 Wideband-IF

In a wideband-IF receiver architecture, such as that shown in Fig 2.3, the signal is downconverted in two phases to zero frequency [20], [26], [27]. First, the whole reception band is downconverted with quadrature mixers such that a large bandwidth signal at IF is maintained. A simple low-pass filter is used at IF to remove any upconverted frequency components, allowing all channels to pass to the second stage of mixers [20]. At the second downconversion to zero-IF, the wanted channel is selected by adjusting the frequency of the second LO. The channel filtering is finally performed at baseband as in DCR. Although downconversion is performed in multiphase, as in the typical superheterodyne receiver, discrete filters are avoided. The image rejection is achieved with the second downmixing step, which is similar to the Weaver technique [28], [29].

Compared to DCR, wideband-IF has several advantages. First, there are no local oscillators, which operate at the same frequency as the receiver RF signal, thus minimizing problems related to time-varying dc offsets. In addition, if the channel selection is performed by tuning only the frequency of the second LO, reduction in phase noise in the first LO can be achieved [20]. In addition, the flicker noise requirement for the first mixer is relaxed. However, care has to be taken in the accuracy of the first downconversion not to deteriorate the image-reject capability and the sensitivity of the receiver [30]. In addition, the multistage realization increases the power consumption.

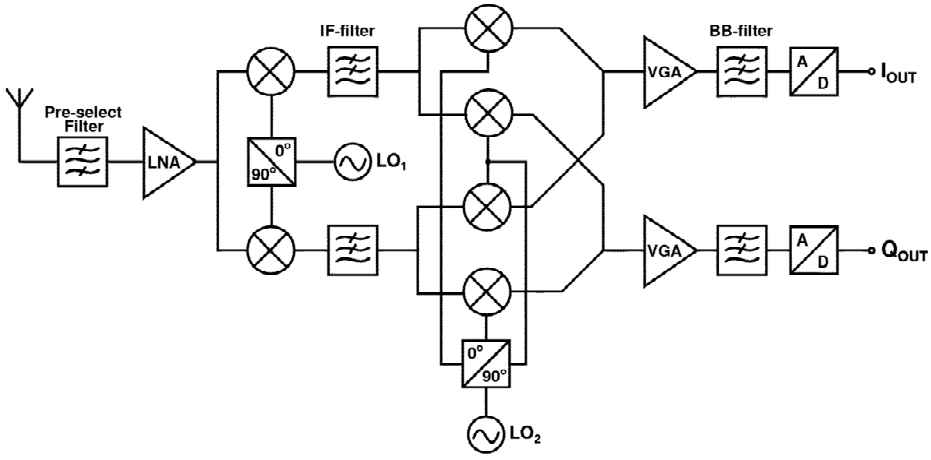

Fig 2.3. Wideband-IF receiver.

2.1.5 RF front-end in different receiver topologies

As stated earlier, the choice of the most suitable receiver topology is constrained in several ways. The most popular receiver topology candidates for CMOS integration nowadays are low-IF and direct-conversion. The demonstrator receivers presented in Chapter 6 are all targeted for direct-conversion receiver. From a RF front-end point of view, however, there is no significant difference, which the targeted receiver topology is. The LNA is required in all receiver topologies, and most of the receiver topologies include mixer(s) as well. Therefore, the LNA

and mixer design methods presented in this thesis are suitable for most of the receiver topologies. It should be noted that the mixer directly follows the LNA in the experimental RF front-ends presented in Chapter 6. Therefore, LNA output matching is not required. If the LNA load is an external filter or if there is a need to measure the performance of the LNA separately, then the LNA output needs to be matched to a certain impedance.

2.2 Definitions and general receiver design parameters

This section is devoted to giving definitions of the most typical design parameters, which are encountered in analog RF circuit analysis, simulations, and measurements and which are used in later parts of this thesis. More details related to the characteristics of wireless communication systems can be found in, for example, [1], [30], [31], and [32].

2.2.1 Input matching and stability

The input of the LNA must be matched to a specific impedance level so as not to deteriorate the performance of the preceding filter or balun. The input matching is defined with the reflection coefficient Γ, which is defined as

$$\Gamma = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{2.1}$$

and $20\log|\Gamma|$ is defined as the return loss. In (2.1) Z_{in} is the LNA input impedance and Z_0 is the reference (source) impedance. Usually, Z_0 is defined by the pre-select filter or balun and return loss better than –10 dB is targeted [33], [34]. The stability of the LNA is checked by ensuring that the real part of the input impedance remains positive at all frequencies [7].

For two-ports, scattering parameters (s-parameters) are typically defined and measured. For example, the s-parameter S_{11} measures the quality of the matching of port 1 when the port 2 is terminated. Commonly, the parameter S_{11} is used to measure the input matching even though the port 2 is not well-defined. As was mentioned, this is the case for example in direct-conversion receivers, where the LNA can be directly followed by a mixer. Therefore, in this thesis, S_{11} is always used to represent the quality of the input matching.

2.2.2 Voltage gain and insertion gain

For the superheterodyne receiver, where both the input and output ports are matched, the power gain is a suitable figure-of-merit for the gain. Different power gain definitions are given for example in [7] and [35]. However, for the direct-conversion and low-IF receivers, the LNA is typically the only block requiring input matching and output matching is not required. In such cases, the most common figure-of-merit for the gain is the voltage gain, which is defined as a ratio of output and input voltages:

$$A_v = \frac{V_{out}}{V_{in}}. \tag{2.2}$$

The output voltage at load impedance Z_L is $V_{out} = I_{out}Z_L$, where I_{out} is the output signal current of the input stage. Therefore, the voltage gain can be expressed as

$$A_v = \frac{V_{out}}{V_{in}} = \frac{I_{out} Z_L}{V_{in}} = g_{m,eff} Z_L \,, \tag{2.3}$$

where $g_{m,eff}$ is the effective transconductance of the input stage, as shown in Fig 2.4. In general, at least for LNAs, $g_{m,eff}$ is different from the transconductance g_m of the input transistor due to the effect of the input matching circuit, as is discussed later. In addition, for downconversion mixers, the effective gain is different due to conversion loss. In narrowband applications, where the reception bandwidth is typically less than 100 MHz, it is sufficient to give the LNA gain at the center frequency only. Therefore, as is shown in (2.3), the LNA gain is set by appropriately designing the effective transconductance $g_{m,eff}$ and the load impedance Z_L.

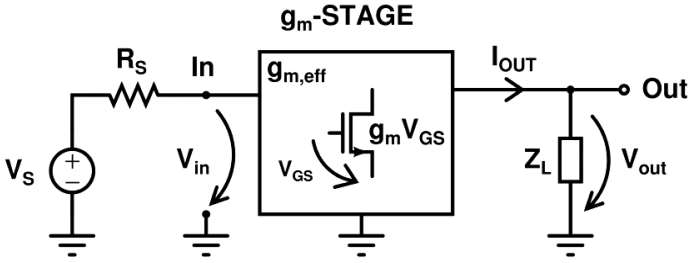

Fig 2.4. General transconductance stage including source and load impedances. In the case of LNA, g_m-element includes the input matching circuit as well.

In a perfectly matched case, the input voltage V_{in} is half of the source voltage V_S. However, LNAs have a perfect input match only in a specific frequency area. Therefore, for wideband LNAs having several 100 MHz or over 1 GHz bandwidth, a more suitable merit is the insertion gain A_i[1] defined as the ratio of the output signal voltage to half of the voltage of the source driving the LNA input [36], i.e.

$$A_i = \frac{V_{out}}{\frac{V_S}{2}} = 2\frac{V_{out}}{V_S} = 2\frac{I_{out} Z_L}{V_S} \,. \tag{2.4}$$

The insertion gain measures only the variation of the output voltage and is fundamentally limited by either the variation in Z_L or output signal current I_{out} as given in (2.4). Therefore, both the Z_L and I_{out} should have adequate bandwidths to achieve the required insertion gain over the wanted frequency area. When insertion gain is referred to later in this thesis, the definition given in (2.4) is used.

2.2.3 Linearity

Linearity is an important measure of a single block or the whole receiver. The receiver must be able to receive a weak signal in the presence of strong interfering ones. There are several measures of linearity. The most commonly used receiver linearity tests are input 1-dB compression point (ICP or P_{1dB}) and the third-order intercept point (IP3). In addition, the second-order intercept point (IP2) is a figure-of-merit for certain receiver architectures, such as

[1] In this thesis, A_i always represents the insertion gain, not the current gain.

DCRs. Linearity tests are typically performed with single-tone or two-tone sinusoidal signals. Linearity tests can be specified for modulated signals as well, but the use of such signals in simulations is tedious. Therefore, the relation between modulated test signal(s) and corresponding sinusoidal test signal(s) can be derived, but to do so is not within the scope of this thesis.

2.2.3.1 Compression and desensitization

For a memoryless nonlinear system, the input-output relationship can be approximated with a polynomial

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t), \tag{2.5}$$

where α_n are constant in a time-invariant system [7]. When $A\cos(\omega t)$ is used as an input signal for a nonlinear system depicted with (2.5), the output signal is

$$y(t) = \alpha_0 + \frac{1}{2}\alpha_2 A^2 + \left(\alpha_1 + \frac{3}{4}\alpha_3 A^3\right)\cos(\omega t) + \frac{1}{2}\alpha_2 A^2 \cos(2\omega t) + \frac{\alpha_3}{4} A^3 \cos(3\omega t). \tag{2.6}$$

The signal at the fundamental frequency decreases when α_1 and α_3 have opposite signs. The input compression point measures the level of the input signal, which causes the 1-dB drop from the small-signal gain. This is graphically presented in Fig 2.5. Moreover, the largest voltage swing in the front-end is typically achieved at the mixer output node (assuming a voltage mode operation). The gain compresses due to the limited the supply voltage and the signal amplitude does not increase along with the input signal level. When this is the case, the signal clipping at the mixer output can dominate the front-end compression point.

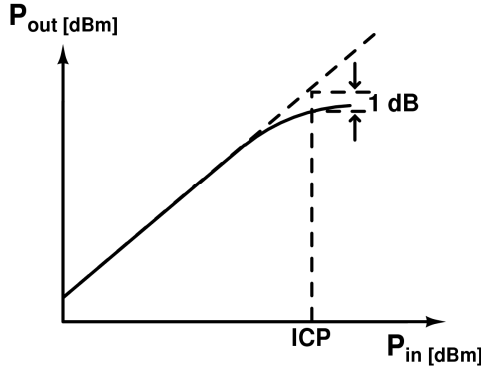

Fig 2.5. Definition of the input 1-dB compression point.

The receiver inability to process a weak desired signal is called desensitization [37]. In practice, there are two main mechanisms causing desensitization. Blocking occurs when the gain of the wanted weak signal compresses in the presence of large interferers. Blocking is caused by third-order nonlinearity. When a two-tone input signal $A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)$ is fed into a nonlinear system depicted by (2.5) such that A_1 is the amplitude of a weak wanted signal and A_2 is the amplitude of a strong interferer, the gain at the wanted signal is

$$y_{\omega 1}(t) = \left(\alpha_1 + \frac{3}{4}\alpha_3 A_1^2 + \frac{3}{2}\alpha_3 A_2^2\right) A_1 \cos(\omega_1 t) \approx \left(\alpha_1 + \frac{3}{2}\alpha_3 A_2^2\right) A_1 \cos(\omega_1 t). \tag{2.7}$$

Therefore, the signal at the fundamental frequency decreases when the amplitude of the large unwanted signal increases. The second desensitization mechanism is caused by second-order nonlinearity, which causes the low-frequency noise components to be upconverted to the desired frequency [37].

2.2.3.2 Intermodulation

When two sinusoidal test signals with different frequencies are applied to a nonlinear system, the output signal consists of harmonics of the input signal and intermodulation components. When a two-tone input signal $A_1\cos(\omega_1 t)+A_2\cos(\omega_2 t)$ is fed into a nonlinear system of (2.5), the third-order intermodulation terms of interest are [38]

$$y_{IMD3}(t)=\frac{3}{4}\alpha_3 A_1^2 A_2\cos(2\omega_1 t-\omega_2 t)+\frac{3}{4}\alpha_3 A_1 A_2^2\cos(2\omega_2 t-\omega_1 t). \tag{2.8}$$

If the amplitudes of the test signals are equal, the amplitude of the intermodulation term depends on the third power of the input signal. In other words, the power of the third-order intermodulation component at the output increases by 3 dB when the level of the input test signals is increased by 1 dB. This is shown in Fig 2.6. The third-order intermodulation intercept point is defined as the point where the extrapolated curves of the wanted signal and third-order intermodulation distortion terms intercept in a log-log-scale.

Similarly, the second-order intermodulation terms of interest are

$$y_{IMD2}(t)=\alpha_2 A_1 A_2\cos(\omega_1 t-\omega_2 t)+\alpha_2 A_1 A_2\cos(\omega_2 t-\omega_1 t). \tag{2.9}$$

The power of the second-order intermodulation component at the output increases by 2 dB when the level of the input test signals is increased by 1 dB. As is shown in Fig 2.6, the second-order intermodulation intercept point is defined as the point where the extrapolated curves of the wanted signal and the second intermodulation distortion terms intercept in a log-log-scale.

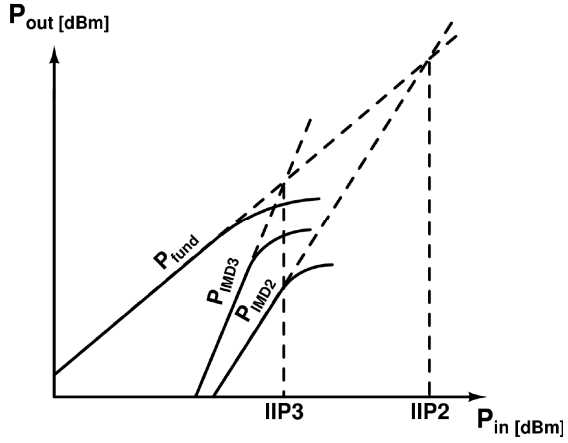

Fig 2.6. Definition of the IIP2 and IIP3.

The IIP3 and IIP2 can be calculated as

$$IIP3=\frac{3}{2}P_{out}-\frac{1}{2}P_{IMD3}-G=P_{in}+\frac{\Delta P_3}{2} \tag{2.10}$$

and

$$IIP2 = 2P_{out} - P_{IMD2} - G = P_{in} + \Delta P_2 , \tag{2.11}$$

where P_{out} is the output power, P_{in} is the input power of one tone, P_{IMD3} and P_{IMD2} are the powers of the intermodulation products at the output, G is the power gain, and ΔP_3 and ΔP_2 are the differences between the fundamental signal and the intermodulation products. The voltage gain can be used instead of the power gain in (2.10) and (2.11) [31]. For cascaded stages, the input intercept point can be calculated with an equation similar to Friis' noise formula:

$$\frac{1}{IIP3_{tot}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \ldots + \frac{\prod_{i=1}^{n-1} G_i}{IIP3_n} . \tag{2.12}$$

In (2.12), $IIP3_n$ and G_n are the input intercept point and power gain of the n^{th} stage. The power gain in (2.12) can be replaced with the square of the voltage gain. More general equations taking into account the selectivity of each stage is presented in [39].

In some cases, the IIP3 requirement needs to be defined by a method other than the conventional intermodulation test. For example, in the WCDMA system, the transmitter signal can leak to the LNA input as a result of finite out-of-band characteristics of the pre-filter. If there is a blocker located between the transmit and reception bands, it is possible that the interfering signal overlaps the wanted signal. Therefore, IIP3 defined for signals with different power is given as

$$IIP3 = \frac{1}{2} P_{\omega 1} + P_{\omega 2} - \frac{1}{2} P_{IMD3} , \tag{2.13}$$

where $P_{\omega 1}$ and $P_{\omega 2}$ are the input powers of the two interferers and P_{IMD3} is the power of the input-referred third-order intermodulation component [40]. It should be noted that (2.13) is valid only when $\omega_2 > \omega_1$, i.e. when the two interfering signals are at lower frequency than the intermodulation component. Otherwise, the factors of $P_{\omega 1}$ and $P_{\omega 2}$ should be interchanged.

2.2.4 Sensitivity and noise

The sensitivity determines the minimum detectable signal level. The signal quality is typically determined by bit or frame error rate. The sensitivity level is determined as

$$S = -174 dBm + 10\log(BW) + SNR_{\min} + NF , \tag{2.14}$$

where –174 dBm is the available noise power from the source at a temperature of 290 K, BW is the channel bandwidth, SNR_{min} is the minimum signal-to-noise ratio, and NF is the receiver noise figure. The SNR_{min} depends on the required bit error rate and the used modulation method. General level information related to requirements of SNR_{min} in different communication systems can be found from [31], for example.

2.2.4.1 Noise figure

The noise performance of a single block is characterized by a noise factor (F) or a noise figure ($NF = 10\log F$). The noise factor determines how much the given circuit or system degrades the signal-to-noise ratio and is defined as

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{\text{total output noise}}{\text{total output noise due to the source}}, \tag{2.15}$$

where SNR_{in} and SNR_{out} are the signal-to-noise ratios at the input and output, respectively. For a single block, the noise factor can be derived as

$$F = \frac{V_S^2 / \left(4k_B T \cdot BW \cdot R_S\right)}{V_{out}^2 / e_{n,out}^2} = \frac{e_{n,out}^2}{4k_B T \cdot BW \cdot R_S \left(\frac{V_{out}}{V_S}\right)^2}, \tag{2.16}$$

where V_S is the source voltage, V_{out} and $e_{n,out}$ are the output signal and output noise voltages, k_B is Boltzmann's constant, BW is the bandwidth, and R_S is the source resistance. The Friis' equation for the noise factor of cascaded blocks is given as [41]

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_n - 1}{\prod_{i=1}^{n-1} G_i}, \tag{2.17}$$

where $F_1 \ldots F_n$ are the noise factors of the successive blocks of the receiver and $G_1 \ldots G_n$ are their available power gains. Equation (2.17) is not suitable for most of the IC receivers, since power-matched interfaces are required. Therefore, the noise contribution can be rewritten in the form of

$$F_{tot} = F_1 + \frac{F_2 - 1}{A_{0,1}^2 A_{v1}^2} + \frac{F_3 - 1}{A_{0,1}^2 A_{1,2}^2 A_{v2}^2} + \ldots + \frac{F_n - 1}{\prod_{i=1}^{n-1} A_{i-1,i}^2 A_{vi}^2}, \tag{2.18}$$

where A_{vn} in the voltage gain of the n^{th} stage to high-impedance load and $A_{n\text{-}2,n\text{-}1}$ is the voltage division ratio between stages n-2 and n-1 [31]:

$$A_{n-2,n-1} = \frac{Z_{in,n-1}}{Z_{in,n-1} + Z_{out,n-2}}. \tag{2.19}$$

In (2.19), $Z_{in,n\text{-}1}$ and $Z_{out,n\text{-}2}$ are the input and output impedances of the cascaded stages. In practical IC realizations $Z_{in,n\text{-}1} >> Z_{out,n\text{-}2}$ and therefore (2.19) is close to unity. As a result, the total noise factor of a typical receiver can be given with voltage gains.

As is shown in (2.16), the noise figure cannot be determined without the source impedance level. Except the LNA, the inputs of the block used in DCR are not matched and therefore a better measure for noise performance is the input referred noise voltage [40]. In addition, the possible noise from the image band of the mixers should be taken into account [39]. Anyway, if Friis' formula is being used, the noise factors of blocks after the LNA can be defined as input-referred noise voltage scaled to the noise in a hypothetical 50-Ω resistor [42]. Whichever cascaded noise factor formula is used, the overall noise contribution of the whole receiver front-end can be quickly estimated. The noise contribution of the mixers and baseband is reduced when the (voltage) gain of the LNA is increased. Therefore, the gain of the first blocks trade-off between the cascaded linearity and noise performance of the whole system.

2.2.4.2 Noise factor definitions for mixers

Because the mixer translates the signal and noise from both the main and image frequencies, two noise factors are defined for mixers, single-sideband (SSB) noise figure and double-sideband (DSB) noise figure. Which noise figure measure should be used depends mainly on the receiver architecture. The SSB noise figure is applicable to the architectures where the RF signal is downconverted to IF frequency, which is higher than half of the system (image-reject filter) bandwidth [7]. Therefore, the SSB noise figure is applicable for superheterodyne receivers, low-IF receivers, and for the first downconversion stage of the wideband-IF receiver. The DSB noise figure is applicable to the direct-conversion receiver. In [43] it is shown that mixers in the heterodyne architecture have twice as many noise contributors as that in the direct-conversion architecture. Thus, the difference between SSB and DSB noise factors can be approximated with

$$\underbrace{\left(1+\frac{N_{SSB}}{N_S}\right)}_{F_{SSB}}=\left(1+\frac{2N_{DSB}}{N_S}\right)<2\underbrace{\left(1+\frac{N_{DSB}}{N_S}\right)}_{F_{DSB}}\Rightarrow F_{SSB}<2F_{DSB}\,, \tag{2.20}$$

where N_{SSB} and N_{DSB} are the input-referred single-sideband and double-sideband noise power of the mixer, F_{SSB} and F_{DSB} are the single-sideband and double-sideband noise factors, respectively, and N_S is the noise from the source. If N_{DSB} is much larger than N_S, the SSB noise figure is approximately 3 dB higher than the DSB noise figure [43].

2.3 MOS transistor small-signal model and noise sources

Since some circuit analysis is presented later in this thesis, the MOS transistor small-signal model used in calculations is briefly described. A simple small-signal model of MOS transistor is depicted in Fig 2.7. The discussion of different MOS transistor models is not within the scope of this thesis. That issue is covered in the literature, for example in [44] and [45]. Since the circuits analyzed in this work typically include several transistors, a simple enough model is needed to achieve useful and understandable equations for RF IC design. Therefore, in this thesis, the MOS transistors are replaced with a simple unilateral small-signal model having only gate-source capacitance C_{gs} and transconductance g_m, i.e. C_{gd} capacitor, gate resistance r_g, and output (drain-source) resistance r_o are omitted for the sake of simplicity. Several equations derived in this thesis were validated with simulations with actual transistor models provided by the foundry. Despite the simplicity of the used MOS model, the discrepancy between the theory and simulations was found to be rather small when operating at the frequencies of the designed circuits presented in thesis.

The major noise sources are also included into the MOS model shown Fig 2.7. Although the in-depth noise analysis of the LNAs and mixers is mostly omitted from this thesis, an understanding of the basics of the MOS noise sources is crucial in RF IC design. They are therefore briefly described in the following.

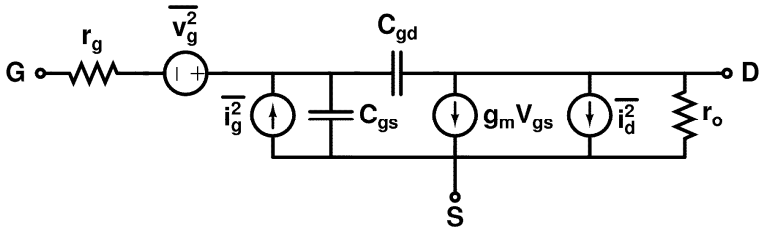

Fig 2.7. Simple MOS transistor model including the major noise sources.

At RF frequencies, the noise is dominated by the drain and gate current sources, which are due to the thermal fluctuations of channel charge in MOSFET [46]. At low frequencies, the 1/*f* noise (flicker noise) is the dominant noise source. In downconversion mixers, the 1/*f* noise increases the low-frequency noise and in and the VCO it increases phase noise due to upconversion. In LNAs, the flicker noise can be neglected, because the operational frequencies are well above the noise corner frequency. In addition, in modern short-channel MOSFETs, the gate resistance increases the gate current noise remarkably. The spectral noise current densities of the three noise sources depicted in Fig 2.7 are

$$\overline{i_d^2} = 4k_B T g_{d0} \gamma \Delta f \ , \tag{2.21}$$

$$\overline{i_g^2} = 4k_B T \delta g_g \Delta f \ , \tag{2.22}$$

$$\overline{v_g^2} = 4k_B T r_g \Delta f \ . \tag{2.23}$$

g_{d0} is the MOSFET output conductance at zero drain-source bias and γ and δ are coefficients describing the magnitude of the noise power. The theoretical long-channel value for γ and δ in saturation are 2/3 and 4/3, respectively [47]. For short-channel transistors, γ increases partly due to thermal noise of parasitic resistances and partly due to short channel effects such as velocity saturation and channel length modulation [46]. For short channel transistors, δ enhances due to the effect of the gate resistance. The analytical derivation for γ and δ for short channel devices is complex if not impossible to obtain [48].

Occasionally, the g_{d0} is replaced by g_m in saturation. The relation between g_{d0} and g_m is given by

$$\alpha = \frac{g_m}{g_{d0}} \ , \tag{2.24}$$

which is unity for long-channel devices, but can be much less than one for short-channel devices [49]. The g_g in (2.22) is given as

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \ . \tag{2.25}$$

Due to the same physical origin, drain and induced gate current noise sources are partially correlated. For long-channel devices, the correlation factor *c* is

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}} \approx -j0.395 \ , \tag{2.26}$$

when the noise source polarities are as indicated in Fig 2.7. For short-channel transistors some discrepancy from theoretical value has been observed [46].

The gate resistance is a significant contributor to the measured gate current noise in short-channel devices [46], [50]. The gate resistance for a single gate finger connected at both ends is

$$r_g = \frac{1}{12}\frac{R_{sh}}{n^2}\frac{W}{L}, \tag{2.27}$$

where R_{sh} is the silicide sheet resistance and n is the number of fingers. In addition, the resistance of a metal1-to-polysilicon via and the silicide-to-polysilicon contact gives rise to the gate resistance [46]. The gate resistance noise is heavily dependent upon the transistor layout. The noise can be decreased by optimizing the layout by using transistors with multiple fingers (known as interdigitating or folding) and by connecting the gate from both ends. If the gate was contacted only at the one end, the factor of the term in (2.27) would be $^1/_3$ instead of $^1/_{12}$. Too much folding, however, increases the wiring parasitic capacitances, which lowers the cut-off frequency of the transistor.

2.4 Overview of short-range radio systems

There exist several wireless personal area network (WPAN) standards, such as Bluetooth (BT) [51], ZigBee [52], and Ultrawideband (UWB) [53]. These have quite different requirements in terms of operational frequencies and bandwidths, which affect the overall system performance and design challenges. According to Shannon's theorem, the system capacity C is a logarithmic function of signal-to-noise ratio (SNR) but a linear function of bandwidth (BW), i.e.

$$C = BW \log_2\left(1 + SNR\right), \tag{2.28}$$

when a channel is perturbed by white Gaussian noise [54]. Therefore, increasing the system bandwidth has significant improvement on system capacity. UWB takes the advantage of wide operational bandwidth to achieve the high capacity. On the other hand, with modest BW, a reasonable capacity can be still achieved if the signal-to-noise ratio is relaxed. This is common for sensor networks, which can achieve several-year autonomous operation by trading the system requirements with low power consumption. A short introduction to sensor applications and UWB system, which are the targeted systems for the experimental circuits of this thesis, is provided next.

2.4.1 Wireless sensor systems

Sensors are encountered in every day life. Sensors typically monitor temperature, pressure, humidity, acceleration etc. These small devices could also benefit from wireless connection to a personal computer or a mobile terminal, for example. The envisioned use cases for wireless sensors are wide. They can provide monitoring and control capability for a number of applications such as transportation, manufacturing, biomedical, environmental monitoring, and safety and security systems [55]. For such devices, an occasional wireless interconnection with the maximum data rate of only a few tens or a few hundreds of kilobits per second is needed. In addition, the maximum connection range of a few meters only is usually required.

2.4.1.1 General requirements

The extremely low power consumption and material costs are the key requirements for sensor radio modules. To achieve over-1-year stand-alone operation, extremely small active and stand-by currents are required. Therefore, the sensors are at the sleep mode for most of the time, with the duty cycle in the order of 0.1 to 1 percent [56]. In addition, the wake-up time should be minimized [P1]. One-dollar bill material costs on a timescale of a few years require a small device with a minimum number of external components. A high integration level can be achieved by using, for example, the direct-conversion receiver or low-IF architecture. The demand for low cost requires the use of CMOS technology without additional process options, like high-quality resistors or capacitors. Currently, the speed of the transistors in modern deep submicron CMOS processes is not the limiting factor. However, the challenges for receiver (RX) design emerge from the poor "analog" performance of the transistor. For example, the available gain from a single transistor is only moderate. In addition, in a CMOS DCR, the flicker noise increases the NF significantly and must be considered already in the downconversion mixers. A higher NF than, for example, in cellular systems, can be tolerated because the sensors are typically short-range devices [57]. Because the bit rate is low and operating range short, the sensitivity of the receiver can be relaxed compared to typical cellular radios [57]. Due to the unique nature of sensor networks, new circuit and system solutions have been presented recently [56] – [60].

Quite a few of the current short-range radio systems fulfill requirements set by sensor networks in a satisfactory manner. Standard Bluetooth consumes too much power and suffers from relatively long device discovery and connection setup times [P1].[2] The IEEE 802.15.4 (ZigBee) is a standard, which overcomes some of the limitations that Bluetooth encounters. However, it does not support dynamic topologies very well, while this is an essential requirement for mobile sensor solutions and has only slight improvements in power consumption compared to standard Bluetooth [P1]. The demonstrator receivers presented in [P1] and [P2] are targeted for a system that uses Bluetooth as a basis, but has slight changes made in the BT radio parameters, as is briefly described next.

2.4.1.2 Overview of low-end extension for Bluetooth (BT LEE)

In typical radios, the current consumption increases along with the operational frequency. For that reason, operating at the sub-1-GHz frequency ISM band would be beneficial to reach the minimal power consumption [42], [56], [61]. However, the current mobile terminals usually have Bluetooth as the short-range wireless connection. Thus, to avoid the need for yet another radio, Bluetooth with slight changes in the radio parameters was utilized to overcome the shortcomings that it has from the sensor networks viewpoint [P1]. Some of the BT radio parameters, such as data rate, receiver sensitivity, and transmitted power, are relaxed to enable very low-power implementation. Table 2.1 shows the basic radio parameters for BT LEE. The details can be found in [62].

[2] It should be noted that an ultra low power Bluetooth specification has been recently created. [Online] Available: http://www.bluetooth.com/Bluetooth/Learn/Technology/lowpower

Table 2.1. Basic BT LEE radio parameters.

Physical bit rate	333 kbps
Frequency band	2.4 GHz (ISM band)
Modulation	2GFSK (h = 2.4, BT = 0.5)
Duplex	TDD
Co-existence of multiple devices Connection setup channel Data delivery	 CSMA FDMA
Jamming avoidance	FDMA

2.4.2 Ultrawideband

Recently, integrated ultrawideband RF circuits have received considerable attention [63] – [69]. According to the Federal Communications Commission (FCC), the unlicensed frequency spectrum allocated for UWB systems is 3.1 – 10.6 GHz. According to WiMedia UWB standard[3], the UWB band is further divided into several narrower sub-bands each occupying a bandwidth of 528 MHz [53]. As is shown in Fig 2.8, the sub-bands are grouped such that the 12 first sub-bands form four band groups (BGs), each consisting of three sub-bands, and the last two sub-bands form a fifth BG. During the time this thesis was written, in the first ECMA-368 standard version, the bandgroup-1 (BG1) formed by the first three sub-bands was mandatory for UWB communications and the remaining BGs were optional to expand the system capability. At the moment, in the second ECMA-368 standard version, there are no mandatory BGs [53]. It should be noted that there is also a competing approach for the OFDM-based UWB communications that is based on the impulse radio technique [64]. The circuit techniques presented in this thesis, however, are towards the OFDM based solution.

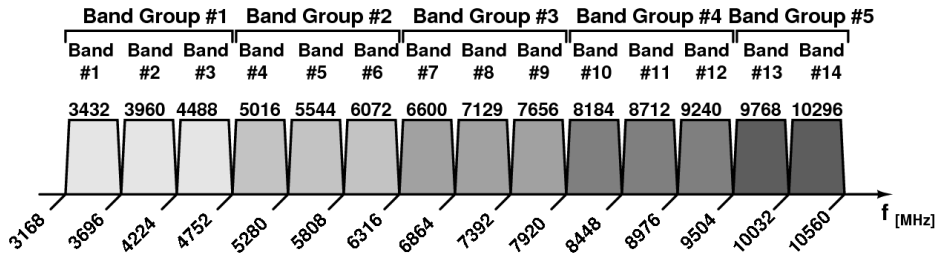

Fig 2.8. WiMedia UWB band group allocation.

2.4.2.1 Target applications

The primary driving factor for UWB systems is to provide high-data-rate communication for short ranges. The target range is 10 meters for 110 Mbps. The range can be reduced for higher bit rates [63]. As envisioned in use cases, UWB is targeted to become a general solution for cable replacement between consumer electronic equipment or as a wireless link between peripheral device to laptop or mobile phone. In addition to high-throughput applications, UWB

[3] Formerly known as Multiband OFDM Alliance (MBOA) standard.

is also being considered for low-data-rate sensor networks [64]. The impulse-based UWB is accepted as an alternative physical layer for IEEE 802.15.4a standard [65].

2.4.2.2 Multisystem challenges

Due to the wide operational band of UWB, interference with other existing radio systems is unavoidable. Therefore, the challenges set by other RF systems are briefly discussed. The FCC requires that the power spectral density (PSD) of UWB devices measured in 1-MHz bandwidth must not exceed the −41.25 dBm level, which is low enough not to cause interference to other wireless systems sharing the same bandwidth. This presents a serious challenge to UWB, since the other systems operating at the same band typically have much higher transmit powers. An example of a hostile environment is a mobile handset, where several other radios can be simultaneously on. The transmit powers of cellular radios can be up to +30 dBm, which is several orders of magnitude higher than UWB transmitters are permitted [63]. Fig 2.9 shows the frequency allocation for the most common cellular systems operating within 800 MHz to 8 GHz. As shown in (2.13), despite pre-filtering, non-overlapping systems like GSM900 and 2.4-GHz WLAN or Bluetooth can corrupt UWB signal reception as a result of intermodulation at BG1 frequencies. Furthermore, a WiMAX interferer (not shown in Fig 2.9 due to regulatory requirements for the RF spectrum usage in different countries) is an in-band blocker in BG1, having a larger power level than the wanted signal [69]. Therefore, UWB receivers are susceptible to strong interferers caused by other active radios.

To expand the UWB system capability, the additional BGs are considered in addition to the mandatory BG1. The frequency spectrum allocated for the whole UWB system overlaps with IEEE 802.11a bands, which are located at 5.15 – 5.875 GHz area. As a result, the strong interference caused by Wi-Fi radios in the vicinity or within the same terminal can desensitize the UWB receiver. Therefore, the coexistence of Wi-Fi radios prevents the effective use of BG2, which limits the number of sub-bands that a MB-OFDM UWB radio can cover in practice [68]. Although high operational frequency sets its own challenges, BG3 is a more viable solution for a mobile handset due to less congested frequency usage. The utilization of BG3 is not trivial, since path loss and complexity of the hardware increase along with higher operational frequencies. The circuit design and experimental results of a dual-band RF front-end designed for WiMedia UWB receiver operating in BG1 and BG3 are presented in Section 6.6.

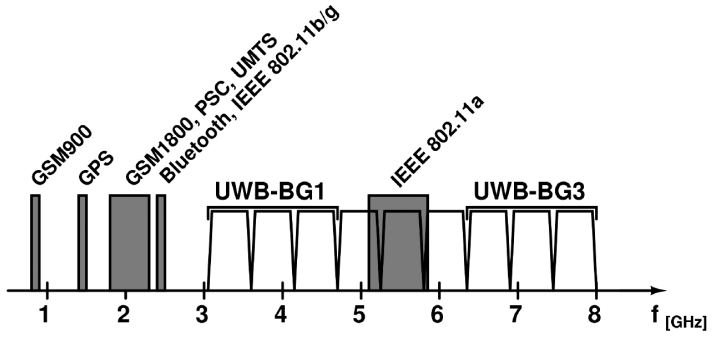

Fig 2.9. Frequency spectrum allocation for the most common wireless systems between 800 MHz and 8 GHz.

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3 Low-noise amplifier design

The subject of this chapter is the design of low-noise amplifiers (LNAs) for wireless applications. First, narrowband LNAs based on inductively degenerated common-source (IDCS) and common-gate (CG) topologies are discussed. Then, in Section 3.3, several LNA topologies for wideband applications are presented and analyzed. The main emphasis is on input matching and insertion gain bandwidth analysis and optimization. Compared with the literature, the major part of the analysis and equations presented in that section is new. The effect of the input pad is briefly discussed in Section 3.4 and a method to neutralize its effect is proposed. Finally, LNA load structures for narrowband and wideband applications are presented in Section 3.5.

A wide variety of different LNA topologies is presented in the literature [1]. The purpose is not to present and compare all of them in this thesis. The focus is on the most relevant and the most-used LNA topologies utilized in wireless applications. For example, distributed LNAs are omitted due to their high current consumption and large layout requirement.

3.1 General LNA design aspects

The LNA is usually the first amplifying stage in a receiver. According to Friis' equation, the LNA sets the minimum noise figure of the receiver. In addition, it should provide enough gain to overcome the noise of subsequent stages, which may otherwise degrade the receiver sensitivity. Simultaneously, the gain of the LNA should not overload the following stages and compromise the dynamic range. The bandwidth of the LNA should be large enough to cover the whole reception band with some design margin but narrow enough to perform some pre-filtering to suppress unwanted interferers. Typically, the linearity performance of the whole front-end or receiver is dominated by the stages that follow the LNA. However, the linearity of the LNA should be adequate to tolerate large blockers and not to produce unwanted intermodulation tones in the reception band. Sufficient input matching performance is required because the properties of the filter preceding the LNA will degrade if the input of the LNA is not properly matched to a certain impedance. As a result, to design a proper LNA, there are several figures-of-merit to be fulfilled. Moreover, some of the requirements are difficult to achieve simultaneously.

The choice between single-ended and balanced structures can already be made in the LNA input. Balanced topology gives immunity against the substrate and supply noise and interferers, but it consumes more current to achieve similar noise figures and gains compared to its single-ended counterpart. LNA typically includes one or two on-chip inductors, which dominate the overall layout area. Since differential coils are available in most of the design kits, the layout area difference between single-ended and balanced LNAs is small. Of course, keeping the number of on-chip inductors low or even zero, as is presented in, for example, [2] and [3], is essential to achieve a small layout area and to keep floor-planning as simple as possible.

Because the LNA is usually based on structures where there are only one or two stacked transistors, the minimum supply voltage of approximately 1 – 1.5 volts is easily achieved with current process technologies. Therefore, the ever-lowering supply voltage typically is not the

main problem of the LNA, but rather the problem concerns other blocks like the downconversion mixer, where more devices are stacked.

In addition to the basic design targets, the LNA can offer several other possibilities such as variable gain or the LNA can include adjustability to make it capable of operating in multisystem applications. The implemented LNAs in this work have generally been a part of a single-system RF front-end. Therefore, the issues related to the design of a multi-mode LNA are not included in this thesis. The design of variable gain methods and issues related to multi-mode LNAs have been covered in [4], for example. In addition, LNAs exploiting thermal noise cancelling have been introduced in the literature [5] – [7]. Noise cancelling LNAs, however, deserve more attention than this thesis can offer.

3.2 Narrowband LNAs

Typically, sufficient performance for narrowband wireless applications is achieved either with inductively degenerated common-source or common-gate LNA topologies, both of which are discussed in this section.

3.2.1 Inductively degenerated common-source LNA

The inductively degenerated common-source (IDCS) amplifier shown in Fig. 3.1a [8] is one of the most commonly used CMOS LNA topologies. The detailed analysis of this topology has been given in several publications [9] – [14]. It has the best noise figure and it provides both current and voltage gain, thereby reducing the noise contribution of the following stages [10]. The equivalent circuit is presented in Fig. 3.1b. The transistor M_1 is replaced with a simple small signal model having only gate-source capacitance C_{gs} and transconductance g_m. An extra C_d capacitance can be added parallel with C_{gs} of the input device, as shown in Fig. 3.1a, to optimize the noise performance [14]. However, when a simple transistor model is assumed, C_d does not affect the calculations, i.e. the C_{gs} in the following figures and formulas can be replaced by the sum of C_{gs} and C_d.

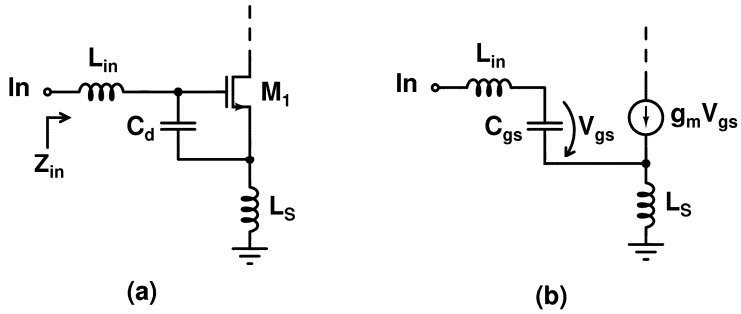

Fig. 3.1. a) Inductively degenerated common-source LNA, b) its simple small-signal equivalent circuit.

3.2.2 Input matching

For the simple input stage presented in Fig. 3.1b, the input matching can be expressed as

$$Z_{in} = s\left(L_{in} + L_S\right) + \frac{1}{sC_{gs}} + \frac{g_m L_S}{C_{gs}}. \tag{3.1}$$

When the Z_{in} is matched to the real-value source impedance R_s, the input matching conditions become:

$$R_{in} = \frac{g_m}{C_{gs}} L_S \approx \omega_T L_S, \tag{3.2}$$

$$\omega_0^2 = \frac{1}{\left(L_{in} + L_S\right) C_{gs}}. \tag{3.3}$$

In previous equations, components L_{in}, L_S, and C_{gs} can be identified from Fig. 3.1 and g_m and ω_T are the transconductance and the unity-gain frequency[4] of input device M_1, respectively. In addition to the ideal components presented in Fig. 3.1, the LNA input is typically involved with parasitic components and the nonidealities in active and passive devices, which complicate the design and analysis. For example, the effect of the pad and ESD protection are discussed in Section 3.4. In addition, the series resistances R_{Lin} and R_{Ls} of inductors L_{in} and L_S, together with input transistors gate resistance r_g, have an effect on the input matching conditions:

$$R_{in} = \frac{g_m L_S}{C_{gs}} + r_g + R_{Lin} + R_{Ls}, \tag{3.4}$$

$$\omega_0^2 = \frac{1 + g_m R_{Ls}}{\left(L_{in} + L_S\right) C_{gs}}. \tag{3.5}$$

The Q-value of an inductor having value of L and series resistance R_L is calculated as

$$Q_L = \frac{\omega L}{R_L}, \tag{3.6}$$

where ω is the frequency of interest. Equation (3.6) is valid if only the series resistance R_L is taken into account in the inductor model. Clearly, models of wire-bond inductance and monolithic inductors include several lumped components, but the detailed description of those is beyond the scope of this thesis. The modeling and characterization of inductors is discussed in the literature in, for example, [15] – [20].

The advantage of inductive source degeneration is that impedance matching is achieved without the use of a physical resistor, which would increase LNA's noise. The input LC matching network can be considered lossless, which does not introduce noise of its own. However, the series resistances of inductors L_{in} and L_S have a slight effect on the NF of the LNA. Typically, L_{in} is realized as wire-bond inductance and, since L_S has low inductance value, it is implemented as an on-chip spiral inductor. Typically, the former has higher Q-values than the latter. To minimize the effect of the series resistance of the source inductor, LNAs utilizing bondwires as degeneration inductance(s) are published as well, in [21] and [22], for example.

[4] For the sake of brevity, in this thesis the angular frequency ω is used synonymously with frequency f.

3.2.2.1 Gain and effective transconductance

As was discussed earlier in Section 2.2.2, the voltage gain is a suitable figure-of-merit for narrowband LNAs. The voltage gain is defined as a product of effective transconductance $g_{m,eff}$ and a load impedance Z_L. The $g_{m,eff}$ of a basic IDCS stage shown in Fig. 3.2 can be evaluated as

$$g_{m,eff} = \frac{I_{out}}{V_{in}} = \frac{g_m V_{gs}}{V_{in}} = \frac{g_m}{sC_{gs}} \frac{I_{in}}{V_{in}} = \frac{g_m}{sC_{gs}} \frac{1}{Z_{in}}, \tag{3.7}$$

where components g_m and C_{gs} have their typical meanings and Z_{in} is calculated according to (3.1). At a resonance frequency, the $g_{m,eff}$ is

$$g_{m,eff} = \frac{1}{\omega_0 L_S} = \frac{g_m}{\omega_0 C_{gs} R_S} \approx \frac{\omega_T}{\omega_0 R_S}. \tag{3.8}$$

Therefore, in a matched case, the $g_{m,eff}$ is independent of the transconductance g_m of M_1 but a relation to g_m exists via the input matching criterion (3.2). Equation (3.7) can be formed to

$$g_{m,eff} = \frac{I_{out}}{V_{in}} = g_m \frac{V_{gs}}{V_{in}} = g_m Q_{in}, \tag{3.9}$$

where the Q_{in} measures the voltage gain between the input of the matching network and the gate-source voltage of the input transistor [23]. This gain is important, because it affects both the voltage gain and the noise of the input transistor and of the overall amplifier. By increasing the Q_{in}, lower g_m is required for the input transistor. Both can be achieved by reducing the size of the input transistor. However, the input matching becomes sensitive to the component value variations if a large Q-value (>3) is utilized [23]. In addition, with small C_{gs}, the input matching circuit becomes sensitive to the parasitic capacitances at the input matching circuit. Therefore, the use of IDCS stage can be impractical with low power levels [24].

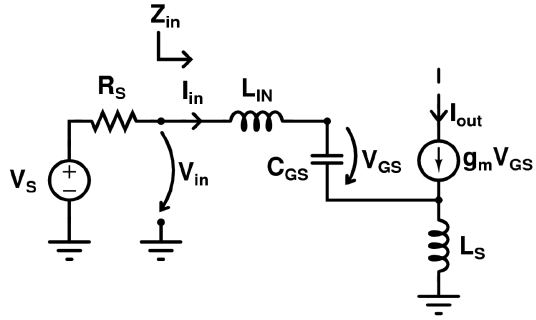

Fig. 3.2. Equivalent circuit to evaluate the effective transconductance and Q-value of an IDCS stage.

3.2.2.2 Noise optimization of IDCS LNA

The noise optimization of an IDCS LNA is widely studied in the literature, in [11] – [14] and [25] – [29], for example. The detailed noise analysis and comparison of noise formulas derived in different publications is beyond the scope of this thesis. A short overview of the topic is given in this section for the sake of clarity and completeness.

The input transistor noise performance optimization usually involves the optimization of the Q-value of the input matching circuit and aspect ratio and drain current of the input transistor [11]. A high Q-value for the input matching network is beneficial to reducing the drain current noise, but it increases the induced gate current noise. The noise factor is expressed as

$$F = 1 + \frac{R_{Lin}}{R_S} + \frac{R_g}{R_S} + \frac{\gamma}{\alpha}\frac{1}{Q_{in}}\left(1 - 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}\right)\left(\frac{\omega_0}{\omega_T}\right) + \frac{\delta\alpha}{5}Q_{in}\left(\frac{\omega_0}{\omega_T}\right), \qquad (3.10)$$

where R_{Lin}, R_g, and R_S are the series resistance on input inductor, the gate resistance, and the source impedance, respectively [11] – [13]. δ, γ, and α are the typical transistor noise factors, Q_{in} is the Q-value of the input matching circuit, and ω_0 and ω_T are the operational and cut-off frequencies, respectively. In addition, c is the correlation coefficient between drain and gate noises. Equation (3.10) is valid when the polarity of the gate current noise source is as indicated in Fig 2.7. It is observed from (3.10) that there are parts that are independent of the Q_{in} or increase or decrease along with Q_{in}. Therefore, an optimum NF exists for a particular Q_{in} [11]. In addition, in general, the NF improves along with higher f_T. However, as was mentioned earlier, the noise factors γ and δ tend to increase along with shorter transistor channels. Fortunately, some parts in (3.10) are given as ratios of noise factors γ and δ, which can be considered nearly constant. This is a reasonable assumption, since both noise sources have the same physical origin [30]. Therefore, the increment of noise factors γ and δ due to short-channel effect is not as severe for the IDCS stage as it is for a common-gate stage, for example. The noise due to gate resistance R_g can be minimized through interdigitation [11], [30]. The noise of the R_{Lin} is small but non-negligible and in certain cases it can become a major noise contributor [31].

The noise figure of an IDCS stage given by (3.10) is plotted in Fig. 3.3 as a function of Q_{in}. The noise due to R_g and R_{Lin} are ignored. The noise parameters δ and γ, shown with a solid line, have classical values of 4/3 and 2/3, respectively. For a comparison, a case where both values are doubled is presented with a dashed line. In addition, the noise is plotted such that the ratio ω_0 / ω_T has the values of 0.05, 0.1, and 0.2. According to (3.10), the noise increases along with the increasing ω_0 / ω_T ratio. Doubling the noise parameters increases the minimum NF by approximately 1 dB, but the optimal Q_{in} value remains nearly unchanged.

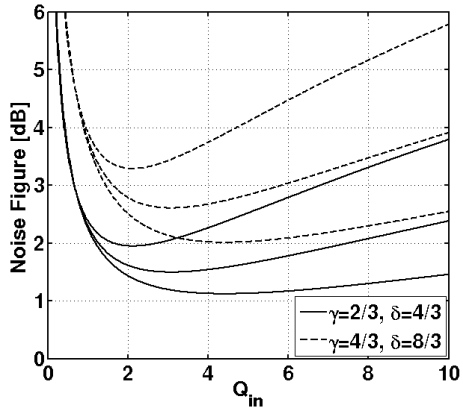

Fig. 3.3. Noise figure of an IDCS LNA. The factor ω_0 / ω_T has the values of 0.05, 0.1, and 0.2. The NF increases along with the larger ω_0 / ω_T ratio.

A noise optimization analysis similar to [11] is given in [14], where an additional capacitor C_d is added in parallel with the intrinsic gate-source capacitance C_{gs} of the input transistor as is shown in Fig. 3.1a. As a result, there is freedom to optimize both the Q_{in} and size of the input device [14]. Thus, the latter technique allows for a better noise minimization when compared to the previously mentioned. The noise factor at a resonance is given by

$$F = 1 + \frac{\frac{\delta}{5}\left(Q_{in}^2 + \frac{1}{4}\right)P^2 + \frac{\gamma}{4}}{R_S Q_{in}^2 g_m}, \tag{3.11}$$

where P is defined as

$$P = \frac{C_{gs}}{C_{gs} + C_d} \tag{3.12}$$

and Q_{in} is the quality factor of the input circuit. The optimum values for width of the M_1 and Q-value of the input matching circuit are also derived in [14]. In [29] it was stated that (3.12) does not take into account the overall impact of all the overlap capacitances. Therefore, P is more accurately given as

$$P \cong \frac{C_{gs}}{C_{gs} + C_{gs,ov} \cdot \left(2 + \frac{g_{m1}}{g_{m2}}\right) + C_d}, \tag{3.13}$$

where $C_{gs,ov}$ is the overlap capacitance between gate and source and g_{m2} is the transconductance of the cascode device [29]. Even when the value of C_d is set to zero, the intrinsic value of P becomes less than unity and the use of additional capacitance C_d becomes unnecessary. For example, the value of P was found as low as 0.3 in a 0.18-μm CMOS process [29].

While equations (3.10) and (3.11) provide good starting points to design the noise optimized LNA input stage, both formulas neglect the noise of the cascode stage and the noise and loss due to series resistance of the source inductor. In addition, the bonding pad and ESD protection needed at the LNA input increase the NF. Both the bonding pad and ESD protection cause a parasitic capacitance to substrate and the LNA noise increases due to two mechanisms. First, the noise and other interferers from the substrate can couple through the bondpad to the LNA input [32]. Secondly, the parasitic components at the LNA input affects the input matching circuit, causing degradation in input impedance and altering noise contribution compared to the traditional LNA noise analysis [31]. As a result, the noise minimization of the LNA is challenging. It should also be noted that the optimum NF is typically found by sweeping the width of the input device in a circuit simulator.

3.2.2.3 Linearity

In addition to the input matching, inductive degeneration induces negative feedback at input transistor's source node. In general, negative feedback reduces the distortion [33]. The IIP3 of an inductively-degenerated LNA is presented in [34], for example. Since the degeneration inductance has low impedance at low frequency, the transconductance stages using inductive degeneration are more linear than those using resistive degeneration with the same bias current [34]. In addition, the linearity of the IDCS stage is affected by the input matching network,

which amplifies the input voltage by its Q-value and decreases the linearity. The distortion analysis based on Volterra's series presented in [34] and [35], however, is tedious for hand calculations. The IIP3 of the IDCS stage can be roughly estimated with

$$IIP3_{LNA} = \frac{IIP3_{FET}}{\left(\frac{V_{gs}}{V_{in}}\right)^2} = \frac{IIP3_{FET}}{Q_{in}^2}, \tag{3.14}$$

where $IIP3_{FET}$ is the intrinsic IIP3 of the input transistor [36]. Typically, the IIP3 improves with higher overdrive voltage. In addition, the common-source stage shows peaking, "sweet spot", when the bias point of the transistor changes from the weak inversion to the strong inversion region. Over a narrow bias range in the moderate inversion region, the drain current follows a nearly square-law behavior with minimized third-order distortion [37]. A simulation example is shown in Fig. 3.4, where a CS stage is simulated with and without inductive source degeneration. The simulation is performed with a 0.13-µm CMOS. The drain-source voltage is set to 0.4 V. A peak in IIP3 is observed with $V_{gs} \approx 0.46$ V.

Since the sweet spot typically occurs over a narrow region of bias voltage, the linearization of an LNA or any other amplifier is challenging when setting the bias point accurately to the sweet spot. Furthermore, the sweet spot is significantly affected by process variation. The location of the sweet spot changes in terms of V_{gs} voltage between process corners primarily due to variations in V_{th}, but the variation is much smaller in terms of the bias currents [37]. The sweet spot phenomenon, however, should not be completely neglected, since the peak shifts to higher drain currents as line widths scale down [38]. Therefore, the bias currents, where the sweet spot occurs, are in the region of interest in RF design [37]. As is shown in Fig. 3.4, in IDCS stages the sweet spot phenomenon is weak due to degeneration [37], [39].

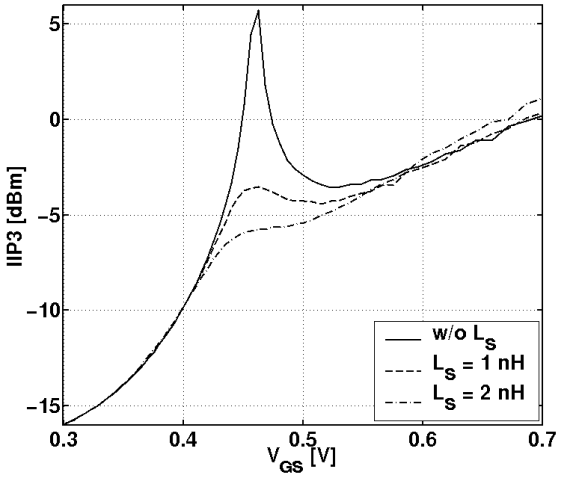

Fig. 3.4. IIP3 of a CS stage. The IIP3 is shown without source inductor and with 1-nH and 2-nH source inductors.

3.2.2.4 Cascode stage

Usually, the CS amplifiers utilize a cascode stage shown in Fig. 3.5a if its usage is not restricted by low supply voltage. There are several benefits from the cascode transistor. Usually, the input impedance of the cascode transistor is smaller than the load impedance. Therefore, the Miller effect of the input stage is reduced, which improves the LNA stability. Due to the larger reverse isolation, the input stage and the load can be separately designed and optimized.

Usually, the noise contribution of a cascode stage to the overall noise of the LNA is small but non-negligible, since at high frequencies the impedance looking into the drain of M_1 is low [10]. The noise contribution of the cascode transistor is decreased by minimizing the parasitic capacitance between input and cascode transistors [40]. The substrate with high resistivity helps to keep this capacitance low [41]. In addition, the parasitic capacitance can be minimized, for example, by utilizing a dual-gate MOS device [42], [43]. This typically improves the noise performance by less than 0.3 dB. The noise contribution of the cascode device can be reduced by resonating the parasitic capacitance out with the additional inductance shown in Fig. 3.5b [44]. However, the large layout area required by on-chip inductors typically limits the use of this method. In addition, due to the finite Q-value, of the on-chip inductor adds the noise of its own. Furthermore, the resonator utilized between the input and cascode stages shown in Fig. 3.5b can be used to filter the image signal [44] or unwanted interferers [45], [P6].

The cascode stage can be used for gain control as shown in Fig. 3.5c. With additional switches, part of the current signal is steered from the LNA load. The accuracy of the gain control depends on matching of transistor sizes and is well controlled over process variations and temperature corners [46]. More details on designing variable gain in low-noise amplifiers can be found in [4], for example.

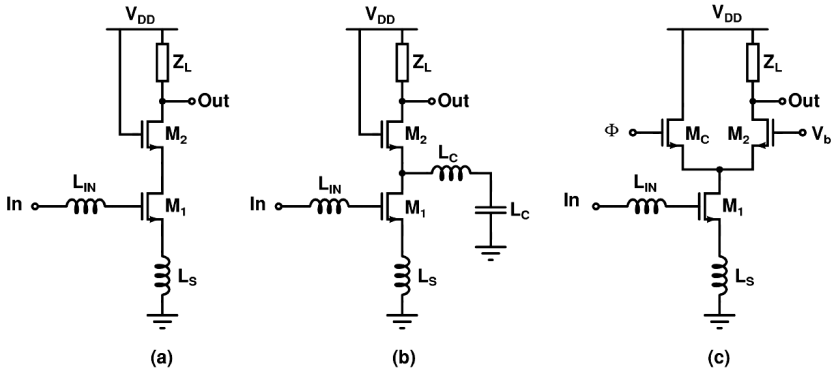

Fig. 3.5. a) IDCS LNA with a cascode stage, b) noise improvement or unwanted signal filtering with internal node resonator, c) variable gain LNA.

If the target is to design an LNA with extremely low supply voltages, the cascode amplifier can be realized with a folded structure as is shown in Fig. 3.6a and Fig. 3.6b. The former uses a PMOS current source to create a wideband high-impedance node to force the current signal to the folded cascode stage. In the latter case, a narrowband LC resonator tuned at carrier frequency f_0 is used instead of a current source. However, at resonance the impedance of the tank can be comparable to the impedance $1/g_{m2}$ seen at the source of M_2. Due to the current

division, a portion of the signal will be lost to the tank [47]. Thus, the gain of the LC-folded cascode topology is lower by a factor of

$$\varsigma \cong \frac{g_{m2}}{g_{m2} + \dfrac{\omega_0 C}{Q_L}} \tag{3.15}$$

than that of the wideband cascode topology [47]. In the previous equation, Q_L is the quality factor of the inductor. The loss is minimized having a large-value inductor with maximal Q-value and small capacitor. The supply voltage reduction is achieved at the expense of an increased number of inductors. In addition, the current consumption is increased, because the two transistors do not share the common dc current path compared to the typical cascode amplifier. The cascode transistor M_2, however, can be biased with smaller dc current than the input device M_1. The bias current of M_2 cannot be reduced too much, because the signal loss of the LC tank can be minimized by increasing the transconductance g_{m2}.

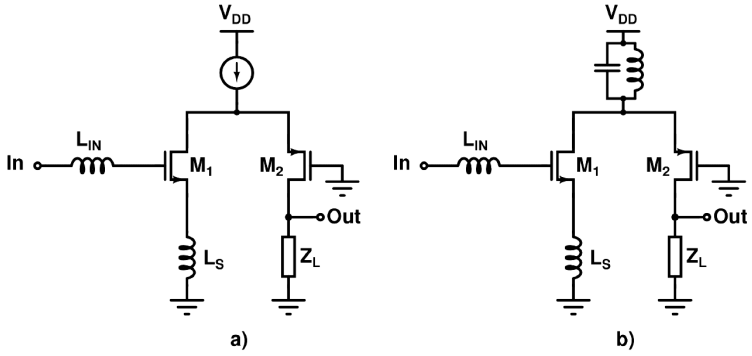

Fig. 3.6. Folded LNA with a) PMOS current source, b) LC resonator.

3.2.3 Common-gate topology

Common-gate (CG) LNA is another widely used topology in wireless communications [24], [48] – [56], [P1]. In this section, the basics of the CG LNA are discussed. First, the input matching and voltage gain are presented and noise figure analysis follows. The last part of this section briefly describes g_m-boosted topology, which combines the CS and CG LNA structures. The more detailed analysis of a CG stage as a function of frequency is presented in Section 3.3.7.

3.2.3.1 Input matching and voltage gain

The desired input impedance of a CG input stage is achieved by adjusting the bias current, aspect ratio, and overdrive voltage such that $1/g_m$ is close to the termination impedance Z_0. Typically, single-ended Z_0 is 50 Ω, and therefore a g_m of approximately 20 mS is required. The simulated g_m of a single input transistor as a function of the transistor width and drain current (I_D) is shown in Section 6.1.1, Fig. 6.3. The CG stage does not suffer from the Miller effect, and thus an adequate reverse isolation can be achieved with a single transistor stage. Therefore, the input matching network and load can be designed separately. In [52] and [56], such a CG LNA

alternative, where feedback is used to adjust the input impedance and frequency transfer function simultaneously, is presented.

Large impedance towards the signal ground is needed to steer the signal into the input transistor source. This can be achieved with a current source I_{bias} shown in Fig. 3.7a. That topology is not typically utilized in the LNA since the current source I_{bias} increases the noise. A better noise performance is achieved by using a source inductor L_S as shown in Fig. 3.7b. The L_S forms a parallel LC resonator with the parasitic capacitance C_{par} associated with the source node of the M_1. When the on-wafer measurements are not applicable, the source node typically needs to be connected either to package or PCB by using a bondwire inductance L_{in} as shown in Fig. 3.7c. The L_{in} is resonated at the wanted frequency with a dc blocking capacitor C_{in}, which can be either an on-chip or an external component.

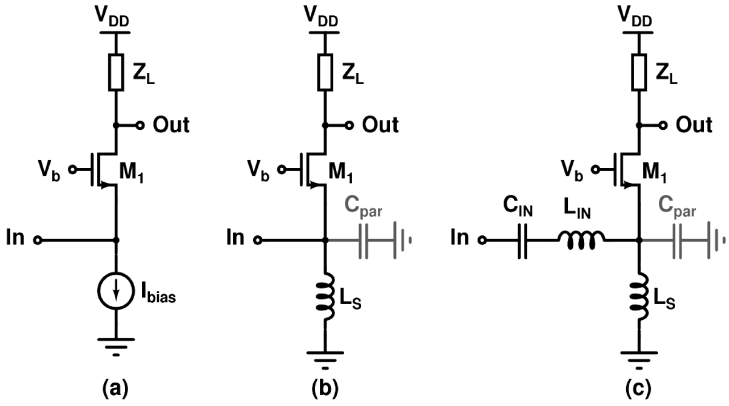

Fig. 3.7. Common-gate LNA input interfaces: a) current source, b) parallel LC resonator, and c) series and parallel LC resonators.

In Fig. 3.7b and Fig. 3.7c, the capacitor C_{par} includes the parasitic capacitances at the source node, i.e. source-body junction capacitance of M_1, substrate capacitance of L_S, and capacitance caused by the bonding pads and on-chip metal wiring. Furthermore, the value of the source inductor L_S can be decreased by adding an additional shunt capacitor C_S in parallel with L_S (the C_S is not shown in Fig. 3.7b or Fig. 3.7c). Therefore, all the capacitance at the source node can be included in a single source capacitor C_T used in the following calculations:

$$C_T = C_{gs} + C_{par} + C_S \,. \tag{3.16}$$

The input impedance Z_{in} of a CG input stage shown in Fig. 3.7b can be calculated as

$$Z_{in} = \frac{sL_S}{1 + sL_S g_m + s^2 L_S C_T} \,. \tag{3.17}$$

The source inductance L_S resonates with the capacitance C_T at the frequency of

$$\omega_0 = \frac{1}{\sqrt{L_S C_T}} \tag{3.18}$$

and at that frequency, (3.17) simplifies to $1/g_m$. The input impedance Z_{in} of a CG input stage shown in Fig. 3.7c is

$$Z_{in} = \frac{1 + s^2 C_{in} L_{in}}{sC_{in}} + \frac{sL_S}{1 + sL_S g_m + s^2 L_S C_T}. \tag{3.19}$$

The detailed analysis of design input and source resonators is presented in Section 3.3.7.

With a perfect impedance matching ($1/g_m = R_S$), the voltage gain of the CG amplifier becomes a division of output load versus the source impedance, i.e. Z_L/R_S. The assumption is valid if the drain-to-source resistor r_{ds} is much larger than the load resistance at the drain. Otherwise, the gain and input impedance formulas should be modified to [49]

$$A_v = \frac{g_m Z_L}{\left(1 + \frac{Z_L}{r_{ds}}\right)} \tag{3.20}$$

and

$$R_{in} = \frac{1}{g_m}\left(1 + \frac{Z_L}{r_{ds}}\right). \tag{3.21}$$

3.2.3.2 Noise of a CG stage

The noise factor of a CG LNA is expressed as [50]

$$F = 1 + \frac{\gamma}{\alpha}\left(\frac{1}{1+\chi}\right)^2 \frac{1}{g_m R_S}, \tag{3.22}$$

where γ is the coefficient of channel thermal noise, g_m is the transistor transconductance, χ is the ratio of the transistor substrate transconductance g_{mb} and g_m, R_S is the source resistance and α is defined as in (2.24). According to (3.22), the noise performance of the common-gate stage is independent of the operation frequency. Because the minimum NF of an IDCS LNA increases along with the frequency, CG LNA can be a better option at very high frequencies [50]. In addition, the noise figure can be maintained with low drain currents by ensuring that proper input matching is achieved by keeping g_m at sufficient level.

When χ is neglected and perfect input matching is assumed, the minimum noise factor typically presented in the literature is achieved:

$$F = 1 + \frac{\gamma}{\alpha} = \frac{5}{3} = 2.2 \text{ dB}. \tag{3.23}$$

For short-channel devices, γ can be much greater than one, and α can be much less than one. Accordingly, the minimum theoretically achievable noise figures tend to be around 3 dB or greater in practice [11]. Therefore, the NF is slightly higher compared to an inductively degenerated common-source LNA, which limits the usage of the common-gate LNA.

With imperfect input matching, the noise factor can be lowered according to [24] [5]

$$F = 1 + \gamma \frac{1 + S_{11}}{1 - S_{11}}, \tag{3.24}$$

[5] It should be noted that (3.24) presents the input matching dependency correctly. There is a misspelling in the original paper [24], where the '+' and '–' signs are interchanged.

where α is neglected. In mass-product applications, however, the optimum input matching performance should be targeted to meet matching specifications also in the presence of process and temperature variations [31].

In addition, (3.22) does not take into account the noise of the load. If resistive load R_L is used, taking into account its noise contribution, the noise factor becomes [7]

$$F = 1 + \frac{1}{g_m R_S}\left(\frac{\gamma}{\alpha} + \frac{\left(1+g_m R_S\right)^2}{g_m R_L}\right) \xrightarrow[g_m = 1/R_S]{} 1 + \frac{\gamma}{\alpha} + \frac{4R_S}{R_L}. \tag{3.25}$$

Thus, the resistive load can make a significant contribution to the overall noise.

The noise equations above assume that the gate induced current noise is neglected. This is a valid assumption since, in a properly interdigitated MOS transistor, the gate resistance is small and the impedance at the gate is low. The noise of the bias current source of the CG-LNA depicted in Fig. 3.7a is thoroughly analyzed in [51]. The low noise current source is designed by minimizing its transconductance and gate (or base) resistance and by using a degeneration resistor [51].

3.2.3.3 G_m-boosted CG stage

The input matching requirement prevents increasing g_m of the input transistor to lower the noise factor. The link between noise factor and input matching can be separated by introducing inverting gain from the source to the gate of the input transistor [57], [58]. As a result, the effective transconductance of the boosted CG stage is

$$g_{m,eff} = \left(1+A\right) g_m, \tag{3.26}$$

where A is the gain between source and gate. The input matching is achieved, when

$$g_m = \frac{1}{R_S}\frac{1}{\left(1+A\right)} \tag{3.27}$$

and the noise factor is reduced to [58]

$$F = 1 + \frac{\gamma}{\alpha}\frac{1}{\left(1+A\right)}. \tag{3.28}$$

According to (3.27) less bias current is required to achieve the required input matching and therefore less drain current noise from the input transistor is obtained.

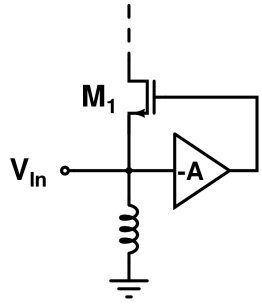

Fig. 3.8. G_m-boosted common-gate input stage.

The inverting gain can be implemented with reactive components so as not to add additional noise. In [57], the capacitor cross-coupling method, which is suitable for differential input configurations, is presented. Due to the capacitor divider between C_{gs} and coupling capacitance C_C, the inverting gain is approximately $A = C_C / \left(C_C + C_{gs} \right)$, which is always less than one [59].

To achieve inverted gain greater than one, the transformer-coupled technique shown in Fig. 3.9b is proposed in [60]. The primary and secondary inductors L_P and L_S form a transformer, which provides an anti-phase operation between gate and source terminals [60]. The method is applicable both for single-ended and fully differential structures. The input admittance is approximately

$$Y_{in} \approx \frac{1}{sL_P} + \left(1 + nk\right) g_m + \left(1 + 2nk + n^2\right) sC_{gs}, \tag{3.29}$$

where $k = M / \sqrt{L_P L_S}$ is the coupling coefficient and $n = \sqrt{L_S / L_P}$ is the turns ratio [60]. The inversion gain factor is $A = kn = k\sqrt{L_S / L_P}$, and therefore the transformer-coupled structure has a freedom to set the desired inversion gain. Since the gate terminal is not ac grounded, the induced gate noise must be taken into account. The noise factor of a transformed-coupled CG-LNA is [60]

$$F = 1 + \frac{\gamma}{\alpha} \frac{1}{1 + nk} + \frac{\delta\alpha}{5} \left(\frac{\omega}{\omega_T} \right)^2 \frac{\left(1 + 2nk + n^2\right)^2}{\left(1 + nk\right)^3}. \tag{3.30}$$

However, the nonidealities related to an on-chip transformer are not included in the noise analysis. For example, losses due to parasitic capacitances and series resistors increase the overall noise figure.

The measured noise figures of g_m-boosted CG-LNAs using capacitor cross-coupling presented in [57] and [61] are 3.0 dB and the one utilizing transformer coupling achieves an NF of 2.5 dB [60]. Therefore, the cross-coupling technique improves the NF only slightly compared to basic CG LNAs, but the transformer-coupled technique seems to benefit from the increased effective transconductance, which results in improved NF.

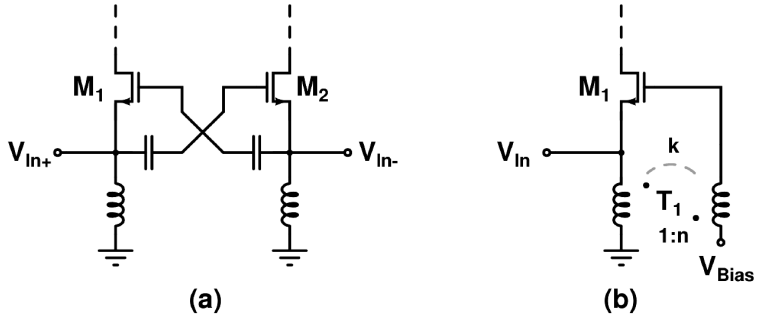

Fig. 3.9. a) Capacitor cross-coupled CG stage [57], b) transformer-coupled CG-stage [60].

3.3 Wideband LNA topologies

In this sub-chapter, LNA topologies for wideband applications are presented. First, the IDCS LNA, which is typically used in narrowband systems, is analyzed in detail to find its suitability and limitations for wideband applications. After that, two alternatives based on IDCS topology are described and an IDCS LNA utilizing Chebyshev input matching is briefly discussed. Then, the resistor-feedback and common-drain-feedback CS LNAs are studied. After that, the CG LNA is analyzed in detail. Finally, LNAs utilizing reactive feedback are briefly described and a summary on wideband LNA design is given.

In this section, the main emphasis is on the analysis of input matching and insertion gain bandwidths. To design a wideband LNA with flat insertion gain response, the effect of the load impedance must be taken into account as well. Different load structures are studied in Section 3.5. For the purpose of comparison, several simulation examples are shown in this section. Some of the simulations are shown with normalized frequencies, i.e. the center frequency is set to 1. When the simulation examples are presented taking into account more realistic component values, the design target is UWB BG1 and then the input matching center frequency is set to 4 GHz.

Appendix A shows a model for a general CS LNA having arbitrary gate, gate-source, gate-drain, source, and load impedances. In the following, some input impedances and insertion gains are calculated by exploiting equations presented there.

3.3.1 IDCS LNA

The performance of the IDCS stage is analyzed in detail as a function of frequency. In the following, the input matching and output signal current bandwidths are analyzed as a function of the input matching circuit Q-value at resonance frequency ω_0. The Q_{in} is a useful parameter, since it also gives a relation to the noise performance and effective transconductance of the IDCS stage, as given in (3.9) and Fig. 3.3. The purpose of the analysis is to find the design rules and limitations, which affect the achievable bandwidth of both S_{11} and I_{out}.

3.3.1.1 Input matching bandwidth

The magnitude of the input matching S_{11} is calculated with (2.1) and (3.1) and by using the basic input matching criteria (3.2) and (3.3):

$$\left|S_{11}\right| = \frac{1}{\sqrt{1+\left(\dfrac{2\omega C_{gs} Z_0}{\omega^2 C_{gs}\left(L_{in}+L_S\right)-1}\right)^2}}. \tag{3.31}$$

In (3.31), Z_0 is the source impedance ($Z_0 = R_{in}$). The frequencies, where the S_{11} equals –10 dB, are:

$$\omega_{S11=-10dB} = \frac{\sqrt{Z_0^2 C_{gs}^2 + 9C_{gs}\left(L_{in}+L_S\right)} \pm Z_0 C_{gs}}{3C_{gs}\left(L_{in}+L_S\right)}. \tag{3.32}$$

Thus, the BW where S_{11} is better than –10 dB is:

$$BW_{S11} = \frac{2}{3}\frac{Z_0}{\left(L_{in} + L_S\right)}. \tag{3.33}$$

The result shows that the S_{11} range can be widened either by minimizing the value of input and source inductances or by increasing the input impedance Z_0. According to (3.2), when the values of inductors are fixed, to maintain the input matching and keeping the C_{gs} unchanged (constant input device size) a larger g_m is needed. Since the aspect ratio of the input transistor cannot be altered, the larger g_m can only be achieved with increased drain current. In addition, pad and ESD protection cause parasitic capacitances at the LNA input node, which tend to lower the input impedance [31]. As a result, having LNA matched to higher Z_0 can become challenging to realize in practice.

Next, the S_{11} performance is analyzed such that Z_0 level is constant and optimum values for the input matching components, C_{gs}, L_{in}, L_S, and g_m, are calculated to achieve maximally wide matching. Perfect matching at ω_0 is assumed. For the following analysis, the Q-value of the input matching circuit at resonance frequency ω_0 is rewritten with (3.8) and (3.9) as

$$Q_{in} = \frac{g_{m,eff}}{g_m} = \frac{1}{\omega_0 L_S g_m} = \frac{1}{\omega_0 C_{gs} R_S}. \tag{3.34}$$

By using the input matching criteria (3.2) and (3.3), Equation (3.32) can be given as a function of Q_{in} by using (3.34):

$$\omega_{S11=-10dB} = \frac{\omega_0}{3}\left(\sqrt{9 + \frac{1}{Q_{in}^2}} \pm \frac{1}{Q_{in}}\right). \tag{3.35}$$

Similarly, the S_{11} bandwidth is expressed as

$$BW_{S11} = \frac{2}{3}\frac{Z_0}{L_S + L_{in}} = \frac{2}{3}\frac{\omega_0}{Q_{in}}. \tag{3.36}$$

Therefore, the input matching bandwidth is inversely proportional to Q_{in}. The S_{11} of an IDCS stage is shown in Fig. 3.10. The simulation is performed such that the center frequency is tuned to 4 GHz and the source inductor is set to 1 nH. The other component values used in simulations are given in Table 3.1. The source impedance is 50 Ω. The Q_{in} has values of 1, 2, and 4. According to (3.34), when perfect matching is targeted, the C_{gs} capacitor decreases along with Q_{in}. Since L_S is kept constant, the g_m is evaluated with (3.2) to maintain the optimum input matching, while the value of the inductor L_{in} is calculated with (3.3) to maintain the center frequency. It should be noted that the S_{11} upper and lower side curves are symmetric with respect to ω_0 in logarithmic scale. Therefore, it is beneficial to set center frequency ω_0 to the geometric average of the corner frequencies of the wanted band. For example, the frequency allocation for UWB BG1 is between 3.168 and 4.752 GHz. Hence, the geometric average frequency is 3.88 GHz and, according to (3.36), the largest Q_{in}, which covers the whole BG1 band, is 1.63.

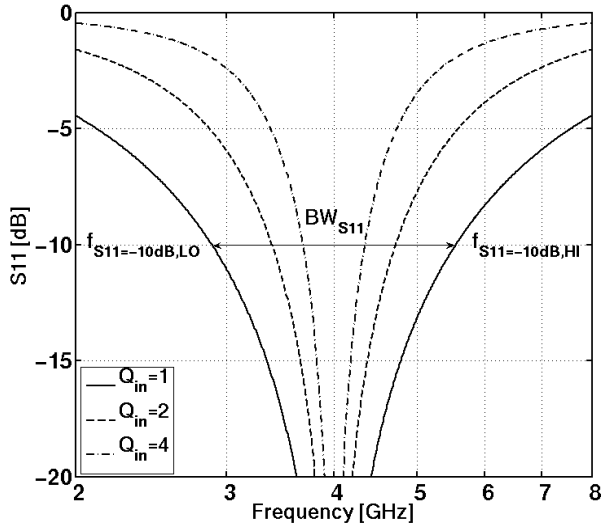

Fig. 3.10. S_{11} of an IDCS stage versus Q_{in}.

Table 3.1. Component values for the simulation shown in Fig. 3.10.

Q_{in}	L_S [nH]	L_{in} [nH]	C_{gs} [fF]	g_{m1} [mS]
1	1.00	0.99	796	39.8
2	1.00	2.98	398	19.9
4	1.00	6.96	199	9.95

3.3.1.2 Output signal current of an IDCS stage

In Section 3.2.2.1, the effective transconductance of the IDSC stage was analyzed at the input matching frequency. In the following, the I_{out} is analyzed in details as a function of frequency. For an IDCS shown in Fig. 3.2, the I_{out} is

$$I_{out} = \frac{g_m V_S}{1 + s\left(g_m L_S + C_{gs} R_S\right) + s^2\left(C_{gs} L_{in} + C_{gs} L_S\right)}. \tag{3.37}$$

By using input matching criteria (3.2) and (3.3), equation (3.37) is expressed as

$$I_{out} = \frac{g_m V_S}{1 + s \cdot 2 g_m L_S + \left(\frac{s}{\omega_0}\right)^2}. \tag{3.38}$$

The magnitude of (3.38) achieves its maximum value at a frequency of

$$\omega_{I_{out},\max} = \omega_0 \sqrt{1 - \frac{2}{Q_{in}^2}}, \tag{3.39}$$

where ω_0 is the input matching resonance frequency given by (3.3) and Q_{in} is defined in (3.34). As a result, the maximum output current frequency is always lower than the optimal input matching resonance frequency. In addition, when $Q_{in} < \sqrt{2}$, (3.39) becomes imaginary. In that case, the maximum I_{out} is achieved at the zero frequency. That case is further analyzed later.

At the frequency given by (3.39) and assuming $Q_{in} > \sqrt{2}$, the maximum output current is

$$I_{out,\max} = \frac{g_{m,eff}}{2} \frac{V_S}{\sqrt{1-\frac{1}{Q_{in}^2}}} . \tag{3.40}$$

The frequencies, where I_{out} is decreased by 3 dB from its maximum value, are

$$\omega_{I_{out},\max-3dB} = \omega_0 \sqrt{1-\frac{2}{Q_{in}^2} \pm \frac{2}{Q_{in}} \sqrt{1-\frac{1}{Q_{in}^2}}} . \tag{3.41}$$

If the lower –3-dB corner frequency is evaluated, the term inside the square root of (3.41) with the '–' sign becomes negative when

$$Q_{in} = \frac{2}{\sqrt{2-\sqrt{2}}} \approx 2.6 . \tag{3.42}$$

If the Q_{in} is smaller than that limit, the scaled I_{out} achieves a –3-dB level already at the zero frequency, as is shown in Fig. 3.11. In that case, the –3-dB bandwidth is solely defined by the upper corner frequency, i.e. by (3.41) with a '+' sign only. The value defined by (3.42) also maximizes the value of (3.41).

When $Q_{in} < \sqrt{2}$, the maximum I_{out} is at zero frequency and then the –3-dB corner frequency is defined by another formula:

$$\omega_{I_{out},\max-3dB,Q_{in}<\sqrt{2}} = \frac{\omega_0}{\sqrt{2}} \sqrt{2-\frac{1}{Q_{in}^2}+\sqrt{8-\frac{4}{Q_{in}^2}+\frac{1}{Q_{in}^4}}} . \tag{3.43}$$

The maximum value of (3.43) is less than the value given by (3.42). Therefore, the I_{out} achieves its maximum –3-dB bandwidth when $Q_{in} \approx 2.6$. Therefore, inserting (3.42) into (3.41), the fundamental upper –3-dB limit for the I_{out} of a perfectly matched IDCS is given as

$$\omega_{I_{out},\max-3dB,\max} = \omega_0 \sqrt{\sqrt{2}} \approx 1.189 \cdot \omega_0 . \tag{3.44}$$

The result generally is independent of the process technology used. The scaled I_{out} is shown as a function of normalized frequency with different Q_{in} values in Fig. 3.11. The frequency, where optimum I_{out} is achieved, becomes closer to ω_0 with larger Q_{in} values, as is given by (3.39), but also the –3-dB bandwidth becomes narrower. Conclusions are drawn in Section 3.3.1.4, where a comparison to BW_{S11} is also made.

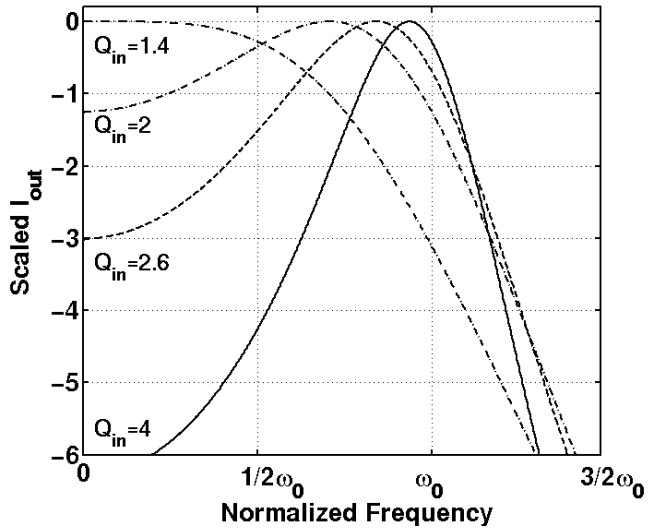

Fig. 3.11. Scaled I_{out} with several Q_{in} values.

3.3.1.3 Noise figure

The noise figure is an important design criterion as well. Since additional components are not added to the IDCS stage, the noise optimization presented in Section 3.2.2.2 still gives the minimum achievable NF. The input matching circuit Q-value must be low to achieve wide enough input matching and output signal current bandwidths. This, however, conflicts with the optimal noise figure presented in Fig. 3.3. The NF starts to increase remarkably when $Q_{in} < 2$. In addition, the minimum NF of the IDCS stage is typically achieved at a slightly lower frequency compared to the optimal input matching frequency. In narrowband applications, the noise increase from the optimal level is significant and nearly optimal NF can be achieved. However, in wideband applications, the noise performance can degrade significantly at high frequencies. This is depicted in a simulation example presented in Section 6.5.1, where an IDCS LNA for UWB BG1 is designed. The NF around 3-GHz frequency is approximately 1.7 dB and it increases to 2.5 dB at 4.7 GHz.

3.3.1.4 Conclusion and remarks

When a proper IDCS stage is designed, both the input matching and output signal current must cover the wanted frequency BW. The minimum and maximum corner frequencies of S_{11} and I_{out} for an optimally matched IDSC stage as a function of Q_{in} are shown in Fig. 3.12. In that figure, $f_{Iout,Max-3dB,HI}$ and $f_{Iout,Max-3dB,LO}$ are the upper and lower corner frequencies, where the output signal current is decreased from the maximum value by 3 dB, respectively, and $f_{S11=-10dB,HI}$ and $f_{S11=-10dB,LO}$ are the upper and lower frequencies where S_{11} equals –10-dB, as is shown in Fig. 3.10. The frequency limits at the y-axis are relative, i.e. corner frequencies are scaled with respect to ω_0. As is shown in Fig. 3.12, relative bandwidths of both the S_{11} and I_{out} decrease along with higher Q_{in}. The upper corner frequencies of S_{11} and I_{out} are nearly identical when Q_{in} is around 2. Then, the lower corner frequency is limited by S_{11} and the relative BW_{S11} is approximately 33 %. With smaller Q_{in} values, the upper corner frequency of I_{out} starts to

decrease rapidly thus limiting the achievable insertion gain BW. Thus, according to (3.36), the input matching can be widened unlimitedly by decreasing Q_{in} but, as shown by Fig. 3.12, the bandwidth of I_{out} cannot.

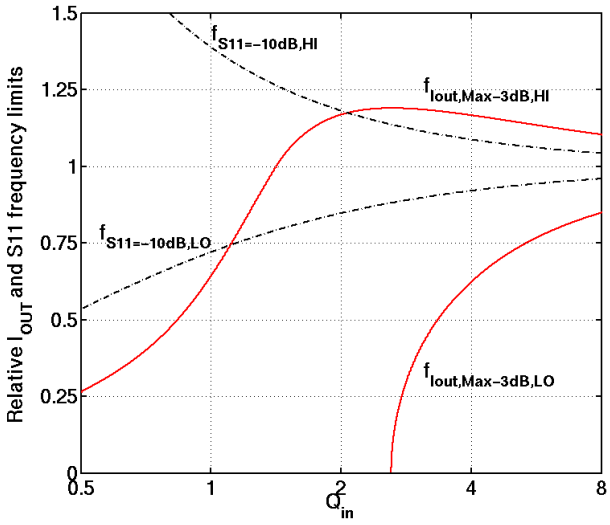

Fig. 3.12. Minimum and maximum corner frequencies of S_{11} and I_{out} as a function of Q_{in}.

Next, the IDCS LNA design possibilities for UWB BG1 are considered. The relative bandwidth BW_{rel} of BG1 is approximately 40 % and the center frequency ω_0 is 3.96 GHz. If the IDCS stage is matched exactly at that frequency, according to (3.44), the maximum upper –3-dB corner frequency of I_{out} is 4.71 GHz, which is not adequate for UWB BG1. To achieve the insertion gain, which covers the whole BG1 with some design margin, the LNA load should be designed to compensate the droop caused by I_{out}. This is challenging to achieve in practice. Since I_{out} corner frequency linearly follows ω_0 as is given by (3.41), it would be beneficial to set the input matching frequency to a frequency higher than 3.96 GHz. That, however, conflicts with the optimum input matching frequency strategy, since, as discussed earlier, to maximize the S_{11} coverage, the ω_0 should be placed at the geometric average of the BG1 corner frequencies (3.88 GHz). To achieve –10 dB input matching covering the whole BG1, $Q_{in} < 1.63$ is needed. That leads to inadequate I_{out} performance since, according to (3.41), the –3-dB corner frequency would be approximately 4.3 GHz. Therefore, the performance of an IDCS LNA is difficult to optimize for applications having wide relative bandwidths. For example, due to higher operational frequency, the BW_{rel} of BG3 is approximately 22 %. It is possible to realize this with the IDCS stage as is presented in Section 6.6.2.1.

The example of S_{11} and insertion gain of an IDCS LNA is presented in Fig. 3.13. The input is tuned at 4-GHz center frequency and the targeted maximum insertion gain is 20 dB to 300-Ω load. The input stage is realized with Q_{in} values of 2, 2.6, and 4. To achieve the targeted insertion gain, first the effective transconductance is evaluated with (2.4) and (3.40). When $g_{m,eff}$ is known, source inductor L_S, C_{gs} capacitance and g_m of the input transistor are evaluated with (3.34). The component values are given in Table 3.2. Clearly, to achieve sufficient input matching performance and gain variation, UWB BG1 is not realizable with IDCS LNA.

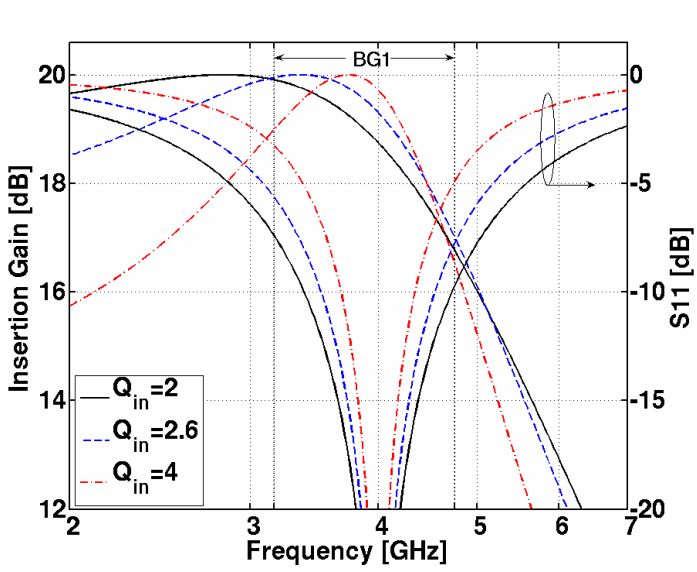

Fig. 3.13. The simulated insertion gain and S_{11} of the IDCS LNA. Both the gain and S_{11} are presented with Q_{in} values of 2, 2.6, and 4. The frequency limits of UWB BG1 are also shown.

Table 3.2. Component values for the simulation shown in Fig. 3.10.

Q_{in}	L_{in} [nH]	L_S [nH]	C_{gs} [fF]	g_{m1} [mS]
2.0	2.60	1.38	398	14.4
2.6	3.88	1.29	306	11.8
4.0	6.73	1.23	199	8.07

As shown in this section, the S_{11} and I_{out} performances of the IDCS stage are tightly related to Q_{in}. To achieve wider relative bandwidths and to maintain sufficient overall performance, additional design parameters are needed to find other ways to separately achieve adequate Q_{in}, S_{11}, and I_{out} performances. Next, two alternatives for basic IDCS LNA are presented. The first uses RC feedback and the other uses an additional common-gate signal path.

3.3.2 IDCS LNA with RC-feedback

An IDCS LNA having RC feedback connected from the input to the output node of the cascode stage is shown in Fig. 3.14a. It has been used in several wideband LNAs, in [7] and [62], for example. In addition, the method to connect the RC feedback to the intermediate node of the shunt-peak load as is shown in Fig. 3.14b is proposed in [P4]. When the feedback is connected to the inductor instead of the output node, the parasitic capacitance at the output node is minimized. The parasitic capacitance at the node between the R_{load} and L_{load} slightly modifies the operation of the shunt-peak load, as is discussed in more detail in Section 3.5.2. According to simulations, there is no significant difference in terms of input matching or noise performance when comparing the structures shown in Fig. 3.14.

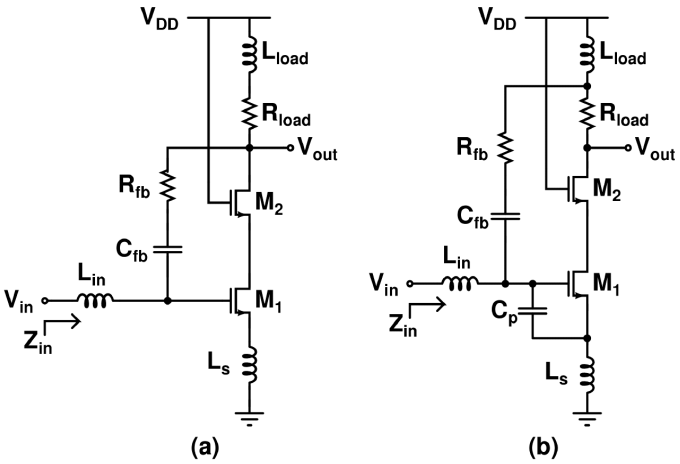

Fig. 3.14. IDCS LNA with RC-feedback topologies a) [62], b) [P4].

To simplify the analysis for LNAs shown in Fig. 3.14, the following modifications are made. According to simulations, C_{fb} has only a small effect and can be removed if it is large compared to intrinsic MOS capacitances. In addition, the cascode stage has an insignificant effect on overall LNA performance and is removed as well. Due to the feedback, the amplifier is not unilateral anymore, and therefore the load has an impact on input matching and gain performance. The simplest case is achieved when the load consists of a plain resistor only. The resulting simple model is shown in Fig. 3.15a, while its small-signal equivalent is depicted in Fig. 3.15b.

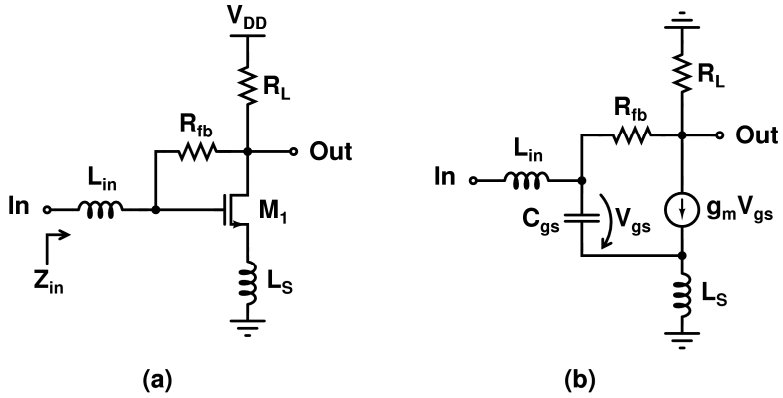

Fig. 3.15. a) Simple IDCS LNA with resistor shunt-feedback, b) its small-signal equivalent.

The input impedance and output signal current can be evaluated with (A.1) and (A.3) found in Appendix A. Despite the simple model shown in Fig. 3.15b, the component values to achieve optimal S_{11} or targeted insertion gain are difficult to present with closed-form formulas. Therefore, the effect of the feedback to the LNA performance is studied with simulations, while the component values are found by means of a manual search. The input matching is targeted at a 4 GHz frequency and the targeted maximum insertion gain is 20-dB to the load impedance of 300 Ω. Two simulation setups with the feedback resistor values of 1 kΩ and 2 kΩ are

investigated. The corresponding simulated Q_{in} values at 4 GHz are 1.3 and 1.7. The other component values are given in Table 3.3. The simulation results are shown in Fig. 3.16. For the purpose of comparison, the performance of a basic IDCS stage without any feedbacks having Q_{in} = 1.7 is also shown with a solid line. The insertion gain and S_{11} with R_{fb} values of 1 kΩ and 2 kΩ are shown with dashed-dotted and dashed lines, respectively. When R_{fb} = 2 kΩ, the S_{11} is better than –10 dB between 3.0 – 5.0 GHz. With the equal Q_{in}, the basic IDCS stage would cover S_{11} only in the frequency area of 3.3 – 4.9 GHz. When the value of R_{fb} is reduced to 1 kΩ, the BW_{S11} extends further.

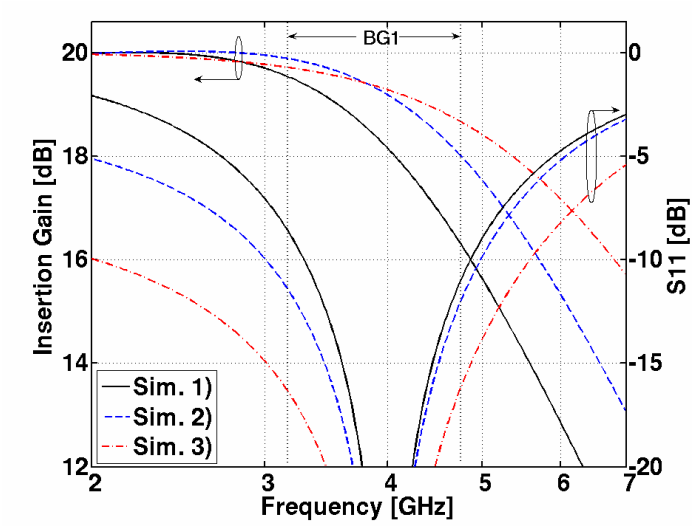

Fig. 3.16. Insertion gain and S_{11} with different RC feedback resistor values.

Table 3.3. Component values for the simulation shown in Fig. 3.16.

Sim. #	Q_{in}	L_{in} [nH]	L_S [nH]	C_{gs} [fF]	g_m [mS]	R_{fb} [kΩ]
1)	1.7	1.91	1.48	468	15.9	-
2)	1.7	2.00	0.77	480	22.0	2.0
3)	1.3	1.40	0.52	500	31.4	1.0

The frequency where the maximum insertion gain of resistor feedback IDCS LNA is achieved is at a frequency lower than optimal input matching frequency ω_0, as was found with the basic IDCS topology (3.39). However, the maximum gain frequency deviation from ω_0 is not as severe as it is with the basic IDCS. In addition, the gain deviation decreases along with lowering R_{fb} values, which is a consequence of negative feedback, i.e. the signal current through R_{fb} cancels part of the signal current provided by the transconductor M_1. Flatter gain response is achieved, but the g_m needs to be increased to maintain the required insertion gain. Hence, utilizing R_{fb} offers a trade-off having wide S_{11} and insertion gain BWs, but it demands higher transconductance from the input transistor, which possibly increases the LNA current consumption. The R_{fb} value cannot be chosen arbitrarily low, since eventually it increases the NF of the whole LNA. A design example of a RC feedback IDCS LNA with actual IC models is presented in Section 6.5.1. In that design example, R_{fb}, with lower than 500 Ω value, becomes

one of the noisiest components in the LNA. In that design example, the RC feedback offers only moderate improvement to the wideband LNA, when S_{11}, insertion gain, and NF performances are considered.

3.3.3 IDCS with additional signal path

An alternative to the RC feedback is having a separate signal path as shown in Fig. 3.17a. When a simple small-signal model is used, the transistor M_2 isolates the output impedance. Therefore Z_L can be set to zero in (A.1) and the input impedance becomes

$$Z_{in} = sL_{in} + \frac{\left(1 + sg_m L_S + s^2 C_{gs} L_S\right) Z_{CG}}{1 + s\left(g_m L_S + C_{gs} Z_{CG}\right) + s^2 C_{gs} L_S}. \tag{3.45}$$

In (3.45), the Z_{GC} is the impedance of the additional CG path:

$$Z_{CG} = \frac{1}{g_{m2} + sC_{gs2}}. \tag{3.46}$$

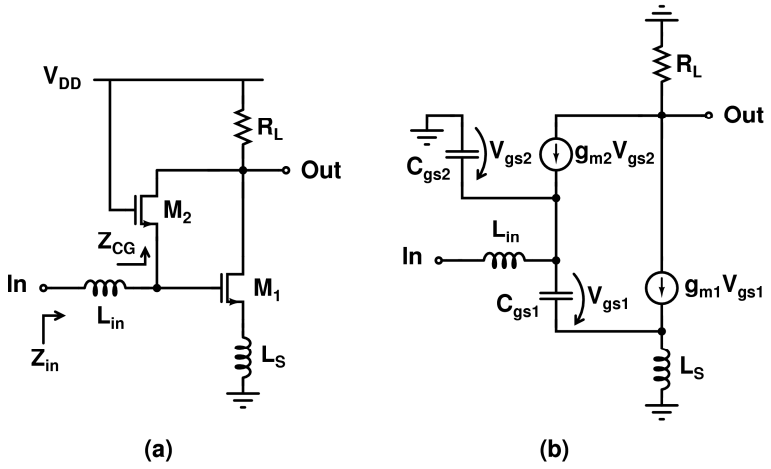

Fig. 3.17. a) LNA with additional signal path, b) its small-signal equivalent.

The Q-value of the input matching circuit can be lowered with the CG signal path. According to simulations, this can be achieved with only a few mS transconductance g_{m2} and therefore the noise from M_2 can be kept small. The effect of the CG dual signal path is analyzed with simulations in three cases: 1) without additional feedback, 2) the g_{m2} of the CG transistor M_2 is set to 3 mS and the source inductor L_S value is set to 0.5 nH, and 3) the $g_{m,2}$ is kept at 3 mS but the L_S set to 1.0 nH. The other components are adjusted to achieve 20-dB insertion gain and optimal S_{11} and the component values are given in Table 3.4. The simulated results are shown in Fig. 3.18. The performance of the basic IDCS stage with $Q_{in} = 2$ is shown with a solid line and simulation cases 2) and 3) are shown with dashed and dashed-dotted lines, respectively. The simulated Q_{in} values at 4 GHz frequency are 2.1 and 1.5 for cases 2) and 3), respectively. According to case 2), although the Q_{in} is increased compared to case 1), the maximum insertion gain frequency is closer to optimal matching frequency and BW_{S11} is slightly wider. With the setup shown with a dashed-dotted line, the Q_{in} is further lowered to 1.5. As a result, the BW_{S11} increases but, due to larger L_S, the maximum insertion gain frequency is lower compared to case

2). Although g_{m2} is kept at 3 mS in cases 2) and 3), the S_{11} and insertion gain performances can be altered with the choice of other components. When comparing case 3) to the IDCS with resistor-feedback case 2), similar S_{11} and insertion performances are achieved and the differences between component values are small. However, compared to the IDCS LNA with the resistive feedback presented in Section 3.3.1.3, the component values can be adjusted more freely with this LNA. In addition, due to the high output impedance of the additional CG path, the reverse isolation is not degraded.

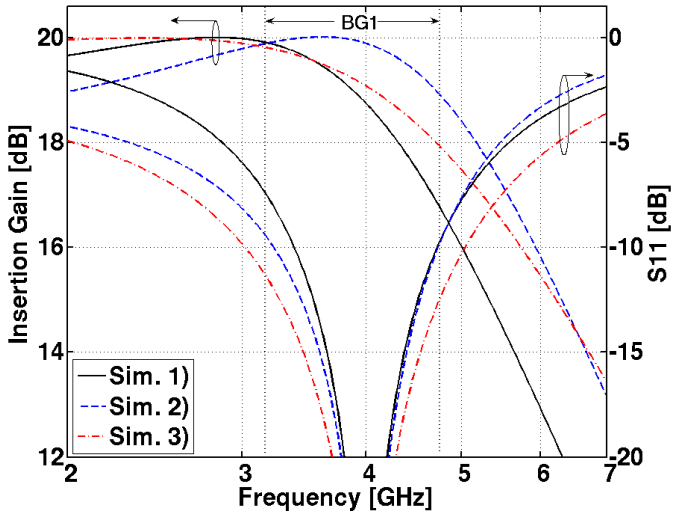

Fig. 3.18. S_{11} with different CG path simulation setups.

Table 3.4. Component values for the simulation shown in Fig. 3.18.

Sim. #	Q_{in}	L_{in} [nH]	L_S [nH]	C_{gs} [fF]	g_{m1} [mS]	g_{m2} [mS]
1)	2.0	2.60	1.38	398	14.4	-
2)	2.1	3.26	0.50	340	18.3	3.00
3)	1.5	2.00	1.00	430	21.4	3.00

3.3.3.1 Comparison of basic IDCS LNA and its alternatives

Two LNA alternatives using a basic IDCS topology as a basis were presented. RC-feedback or an additional CG signal path provides an additional degree of freedom to optimize the S_{11}, gain, and noise performances. A design example, which compares the basic IDCS LNA topology to these two alternatives with actual IC component models, is presented in Section 6.5.1. The input stage Q-value can be decreased by lowering the feedback resistor value or by increasing the g_m of the additional CG path. In that design example, wider S_{11} is achieved at a cost of decreased gain and increased noise. In addition, only one UWB band group can be covered with a single input and the two alternatives can offer only a moderate improvement to the basic topology. If there is a need to cover wider bandwidth with a single LNA, IDCS topology or its alternatives do not offer sufficient performance and other options should be found.

3.3.4 LC ladder matching network

Fig. 3.19 shows one of the first CMOS LNAs designed for the UWB [63]. The core of that LNA is also based on IDCS topology. To have a wide operation BW, a Chebyshev input matching technique and a shunt-peaked load are utilized. The drawback of using wideband input matching is the number of on-chip inductors. Wideband input matching circuit in Fig. 3.19 becomes more troublesome when designing a balanced or differential LNA. Then, all inductors at the input matching cannot be differential, which leads to an even larger number of inductors. To minimize the noise from the input matching circuit and to prevent the current signal leakage into the resonator L_2C_2, inductors having high Q-value are required. As a result, the area of the input matching circuit becomes large. The input impedance, gain, and noise performance of the LNA with Chebyshev input matching are studied in, for example, [63] and [64]. Despite its shortcoming, the Chebyshev input matching technique is an option to be considered, when wide relative gain and S_{11} bandwidths are needed.

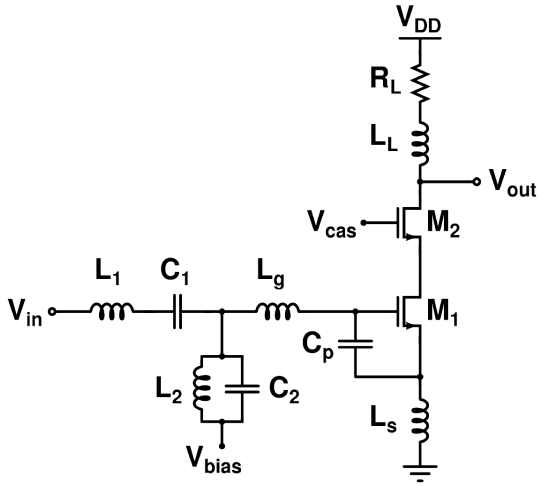

Fig. 3.19. Wideband IDCS-LNA with Chebyshev input matching network [63].

3.3.5 CS with shunt-resistor feedback

In Section 3.3.1 it was found that IDCS LNA cannot provide adequate S_{11} and gain performance for applications having large relative BWs. In addition, neither of its variants presented in Sections 3.3.2 and 3.3.3 could improve the performance significantly, since the source inductor limits the achievable bandwidths and causes the maximum output signal current to be at lower frequency compared to optimal S_{11} frequency. When the source inductor is removed, other input matching techniques are needed. In noise sensitive applications, the resistive input termination is not an option. Therefore, the LNA input matching realization by using feedback is studied. The simplest feedback topology is a resistor (shunt) feedback connected from the gate to the drain of the input transistor, as is shown in Fig. 3.20. For simplicity, the overlap capacitor C_{gd} of M_1 and the parasitic capacitance at the output node are neglected. Although the LNA shown in Fig. 3.20 seems to be a special case of the one shown in Fig. 3.15 having $L_S = 0$, the removal of the source inductor greatly alters the performance of the whole LNA and its input matching circuit. Therefore, it is justified to analyze the LNA of Fig. 3.20 separately.

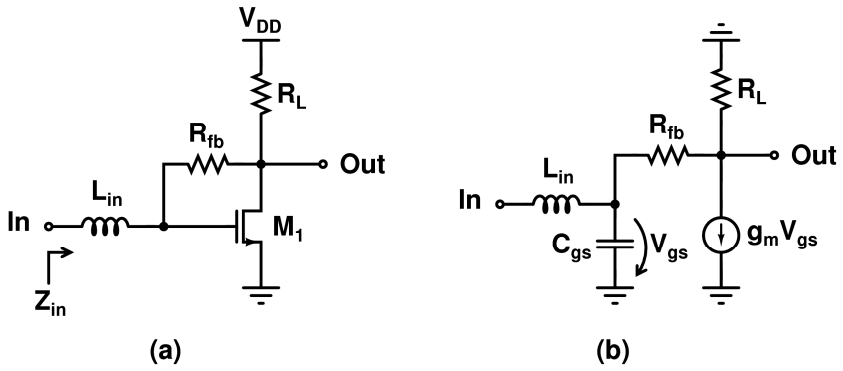

Fig. 3.20. a) Shunt-resistor feedback LNA with resistive load, b) its simple small-signal equivalent circuit.

Typically, the reactive components shown in Fig. 3.20a are neglected when the gain and input matching equations of the shunt-feedback amplifier are presented in the literature. However, the reactive components should be taken into account, since they play a critical role what comes to the performance of the LNA. The capacitor C_{gs} includes the intrinsic capacitance of the input transistor M_1, the parasitic capacitances caused by the pad (not shown in Fig. 3.20) and metal wiring etc. The input inductor L_{in} can be realized with a bondwire, for example. The input impedance of the LNA presented in Fig. 3.20 can be calculated by using a general input impedance equation (A.1):

$$Z_{in} = sL_{in} + \frac{R_{fb} + R_L}{1 + g_m R_L + sC_{gs}\left(R_{fb} + R_L\right)}. \tag{3.47}$$

The rightmost part of (3.47) has an imaginary part, which can be resonated out with L_{in}. As a result, the input matching can have real value without the source inductance. The input matching is met with the following criteria:

$$R_{in} = \frac{L_{in}}{C_{gs}}\left(\frac{1 + g_m R_L}{R_{fb} + R_L}\right), \tag{3.48}$$

$$\omega_0^2 = \frac{1}{L_{in}C_{gs}}\left[1 - \frac{L_{in}}{C_{gs}}\left(\frac{1 + g_m R_L}{R_{fb} + R_L}\right)^2\right] = \frac{1}{L_{in}C_{gs}}\left(1 - \frac{C_{gs}}{L_{in}}R_{in}^2\right). \tag{3.49}$$

The maximum output current signal is achieved at the frequency of (3.49) and is

$$I_{out} = \frac{C_{gs}}{L_{in}}\left(\frac{g_m R_{fb} - 1}{g_m R_L + 1}\right). \tag{3.50}$$

According to the equations above, R_{in}, ω_0 and I_{out} depend on the reactive and resistive component values and on the g_m of the input transistor. Compared to typical IDCS LNAs, there are more components, which affect the relevant design parameters. Since C_{gs}, L_{in}, resistors R_{fb} and R_L, and g_m do not track each other, resistor-feedback LNA is more sensitive to component value deviation from nominal values than basic IDCS topology.

Next, the S_{11} and output signal current bandwidths of the shunt-feedback CS are studied. The corner frequencies, where the output signal current is decreased by 3 dB from the maximum value and S_{11} achieves the –10-dB limit, are

$$\omega_{I_{out},\max-3dB} = \sqrt{\omega_0^2 \pm 2R_{in}\frac{1}{L_{in}\sqrt{L_{in}C_{gs}}}} = \omega_0\sqrt{1 \pm \frac{2}{Q_{in} - \frac{1}{Q_{in}}}}, \tag{3.51}$$

$$\omega_{S_{11}=-10dB} = \sqrt{\omega_0^2 \pm \frac{2}{3}R_{in}\frac{1}{L_{in}\sqrt{L_{in}C_{gs}}}} = \omega_0\sqrt{1 \pm \frac{2}{3}\cdot\frac{1}{Q_{in} - \frac{1}{Q_{in}}}}, \tag{3.52}$$

respectively. In previous equations, Q_{in} is the Q-value of the input network at ω_0

$$Q_{in} = \left|\frac{V_{gs}}{V_{in}}\right|_{\omega=\omega_0} = \sqrt{\frac{C_{gs}}{L_{in}}}\left(\frac{R_{fb}+R_L}{1+g_mR_L}\right) = \sqrt{\frac{L_{in}}{C_{gs}}}\frac{1}{R_{in}}. \tag{3.53}$$

Fig. 3.21 presents a simulation example of the LNA shown in Fig. 3.20. The input inductor L_{in} has the values of 1 nH, 2 nH, and 4 nH and the load resistor is set to 300 Ω. The center frequency is tuned to 4 GHz and the maximum insertion gain level is set to 20 dB. The component values are given in Table 3.5. The maximum insertion gain is achieved at the same frequency with optimum S_{11} frequency. Both the insertion gain and S_{11} have wide bandwidths and the –3-dB insertion gain corner frequency always exceeds the –10-dB corner frequencies of the S_{11}. According to (3.51) and (3.52), both the insertion gain and S_{11} bandwidth increase with smaller L_{in} values. This is also predicted by the Q-value of the input network (3.53). When the value of L_{in} is small enough, the term inside the square root in (3.51) and (3.52) becomes negative when the '–' sign is applied. In that case, the I_{out} and S_{11} corner frequencies are already achieved at the zero frequency, as shown in Fig. 3.21. Then, the I_{out} and S_{11} corner frequencies given by (3.51) and (3.52) are limited by the upper corner frequency, i.e. the '+' sign is only valid.

To maximize both S_{11} and insertion gain bandwidths, the value of L_{in} should be as small as possible. However, when L_{in} is decreased, the value of the feedback resistor should be lowered to maintain the optimum matching. Due to the negative feedback, the resulting overall output signal current decreases along with lower R_{fb} values. Thus, the transconductance of M_1 should be increased to maintain the targeted insertion gain. The noise of a CS LNA with resistor feedback can be approximated with [7]

$$F = 1 + \frac{R_{fb}}{R_S}\left(\frac{1+g_{m1}R_S}{1-g_{m1}R_{fb}}\right)^2 + \frac{1}{R_SR_{load}}\left(\frac{R_{fb}+R_S}{1-g_{m1}R_{fb}}\right)^2 + \frac{\gamma g_{m1}}{\alpha R_S}\left(\frac{R_{fb}+R_S}{1-g_{m1}R_{fb}}\right)^2. \tag{3.54}$$

According to (3.54), the input referred noise from both the load and feedback loop increase along with lowering R_{fb} when other component values are kept constant. Equation (3.54) is suggestive only, since it does not take into account the effect of Q_{in} nor the induced gate current noise.

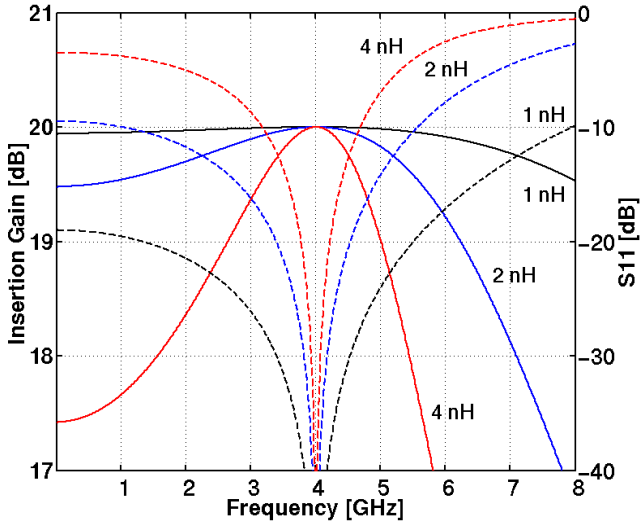

Fig. 3.21. The simulated insertion gain and S_{11} of the resistor feedback CS LNA. The insertion gain is shown with a solid line and S_{11} with a dashed line. Center frequency is tuned to 4 GHz and insertion gain level is set to 20 dB. Both the gain and S_{11} are presented with L_{in} values of 1 nH, 2 nH, and 4 nH.

Table 3.5. Q_{in} and component values for the simulation shown in Fig. 3.21.

Q_{in}	L_{in} [nH]	C_{in} [fF]	R_L [Ω]	R_{fb} [Ω]	g_m [mS]
1.1	1	319	300	622	45.7
1.4	2	398	300	810	33.5
2.2	4	317	300	1375	18.8

It can be concluded that wider S_{11} and insertion gain bandwidths can be obtained with resistor feedback CS LNA compared to basic IDCS. Since a source inductor is absent, it can also be realized with smaller die area. A disadvantage of this is that it results in high current consumption and probably degraded NF performance. An example of wideband LNA utilizing resistive feedback can be found in, for example, [65] and [66].

3.3.6 CS with common-drain feedback

Another active feedback loop is achieved by connecting a source follower (common-drain stage) output node to the input. In a general case shown in Fig. 3.22a, impedances Z_g, Z_L, and Z_{fb} represent the gate, load, and feedback impedances, respectively. The input impedance can be evaluated as

$$Z_{in} = Z_g + \frac{1 + g_{m2}Z_{fb} + sC_{gs2}\left(Z_L + Z_{fb}\right)}{g_{m2}\left(1 + g_{m1}Z_L\right) + sC_{gs1}\left(1 + g_{m2}Z_{fb}\right) + sC_{gs2}\left[\left(1 + g_{m1}Z_L\right) + sC_{gs1}\left(Z_L + Z_{fb}\right)\right]}. \quad (3.55)$$

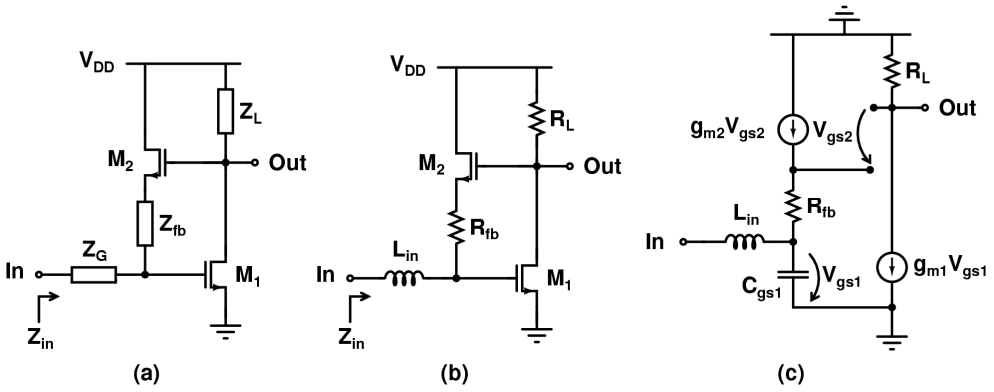

Fig. 3.22. CS amplifier utilizing common-drain feedback, a) general topology, b) Z_G is replaced with bondwire inductance and Z_{GD} and Z_L are replaced with resistors, c) small-signal representation of b).

In a simple case shown in Fig. 3.22b, Z_L and Z_{fb} are realized with resistors R_L and R_{fb}, respectively. The right-hand side without term Z_g has both real and imaginary parts. The real value input impedance can be achieved by resonating the imaginary part with input inductance L_{in}. If C_{gs2} is neglected for the simplicity, the input matching is met with the following criteria:

$$R_{in} = g_{m2}\frac{L_{in}}{C_{gs1}}\left(\frac{1+g_{m1}R_L}{1+g_{m2}R_{fb}}\right), \tag{3.56}$$

$$\omega_0^2 = \frac{1}{C_{gs1}L_{in}}\left[1-g_{m2}^2\frac{L_{in}}{C_{gs1}}\left(\frac{1+g_{m1}R_L}{1+g_{m2}R_{fb}}\right)^2\right] = \frac{1}{C_{gs1}L_{in}}\left(1-\frac{C_{gs1}}{L_{in}}R_{in}^2\right). \tag{3.57}$$

The maximum output signal current is achieved at a frequency given by (3.57). In a perfectly matched case this is

$$I_{out} = \frac{g_{m1}}{g_{m2}}\frac{1+g_{m2}R_{fb}}{1+g_{m1}R_L}\sqrt{\frac{C_{gs1}}{L_{in}}}\,. \tag{3.58}$$

The maximum insertion gain $A_{i,max}$ can be re-expressed with the load resistor R_L and by using (3.56) and (3.57):

$$A_{i,\max} = R_L I_{out} = R_L\frac{g_{m1}}{R_{in}}\sqrt{\frac{L_{in}}{C_{gs1}}} = g_{m1}R_L\sqrt{1+\left(\frac{L_{in}\omega_0}{R_{in}}\right)^2}\,. \tag{3.59}$$

Now, there are six parameters to set three equations. The input matching frequency is tuned at the wanted frequency with L_{in} and C_{in} by (3.57). Then, the maximum gain is set to the required level with g_{m1} and R_L (3.59). Finally, the input matching is set to the desired input impedance with g_{m2} and R_{fb} according to (3.56).

In Fig. 3.23, a simulation example of the LNA shown in Fig. 3.22 is shown. The input matching is tuned at 4 GHz frequency and the input bondwire has the values of 1 nH, 2 nH, and 4 nH, respectively. As in the previous LNA examples, the load resistor value is set to 300 Ω and the other component values are calculated such that the maximum insertion gain of 20 dB is achieved. The result is shown in Fig. 3.23. As was the case with resistor feedback CS LNA, the

maximum bandwidths are obtained by choosing the inductor L_{in} value as small as possible. The choice of g_{m2} or R_{fb} does not affect the gain or input matching bandwidths. Of course, the noise contributions of M_2 and R_{fb} should be taken into account. The noise formulas for a feedback LNA are given in the literature, in [2], [67], and [68], for example. However, the presented noise analyses give suggestive results only, since all the noise sources are not included. Therefore, to achieve a sufficient noise figure, optimum sizing for M_2 and R_{fb} is found with a circuit simulator. Typically, the transistor M_1 makes the major noise contribution, while the effect of M_2 or R_{fb} is small but non-negligible.

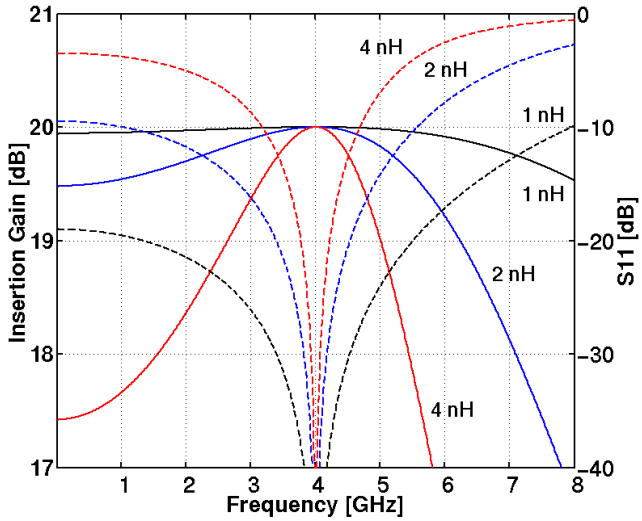

Fig. 3.23. The simulated insertion gain and S_{11} of the common-drain feedback CS LNA. The insertion gain is shown with a solid line and S_{11} with a dashed line. Center frequency is tuned to 4 GHz and insertion gain level is set to 20 dB. Both the gain and S_{11} are presented with L_{in} values of 1 nH, 2 nH, and 4 nH.

Table 3.6. Component values for the simulation shown in Fig. 3.23.

L_{in} [nH]	C_{in} [fF]	R_L [Ω]	R_{fb} [Ω]	g_{m1} [mS]	g_{m2} [mS]
1	319	300	300	29.8	3.10
2	398	300	300	23.5	1.96
4	317	300	300	14.8	0.93

When Fig. 3.21 and Fig. 3.23 are compared, the gain and S_{11} curves are found to be identical. Therefore, in a fully matched case, the bandwidths of resistor feedback and common-drain feedback CS LNAs are set by the reactive input matching components L_{in} and C_{in}, i.e. as is given by (3.51), (3.52), and (3.53). The common-drain (CD) feedback LNA requires smaller transconductance than the resistor feedback LNA to achieve similar gain level. In addition, there is more freedom to choose the appropriate component values for a CD feedback LNA compared to resistor feedback CS LNA. Therefore, CD feedback LNA is better suited for wideband applications. It is utilized, for example, in [2], [67], [68], and [69].

3.3.7 Wideband common-gate LNA

As was shown in Section 3.3.1, the drawback of a typical IDCS LNA is its restricted input matching capabilities, which limit its usage in wideband solutions. To mitigate that problem, the Chebyshev input matching network can be used, but the use of several on-chip inductors degrades the noise performance. The CG input stage, however, offers rather simple input matching realization. The input resistance at the MOSFET source is inversely proportional to the transconductance g_m and the resulting impedance match is wideband [70]. Due to the simple input matching circuit, the NF difference between wideband CG and IDCS LNAs becomes smaller than in narrowband systems. Therefore, CG LNA is a viable option for applications requiring wide operational bands, for example UWB [52], [55].

In Section 3.2.3, the performance of the CG LNA was analyzed at the center frequency only and the operation as a function of frequency was neglected. In this section, the wideband CG LNA design is analyzed in detail taking into account the effect of the input matching network. The CG-LNA is analyzed with the circuit shown in Fig. 3.24. The transistor M_1 is replaced with a simple small-signal model consisting of gate-source capacitor C_{gs} and transconductance g_m. The g_m includes also the substrate transconductance g_{mb}, i.e. the effective transconductance $g_{m,eff}$ of a CG stage is $g_{m,eff} = g_m + g_{mb}$. For simplicity, the $g_{m,eff}$ is marked with a g_m only in all figures and equations. The capacitor C_{par} includes the parasitic capacitances at the source node and all the capacitances at the source node are included in a single capacitance C_T, as is given in (3.16).

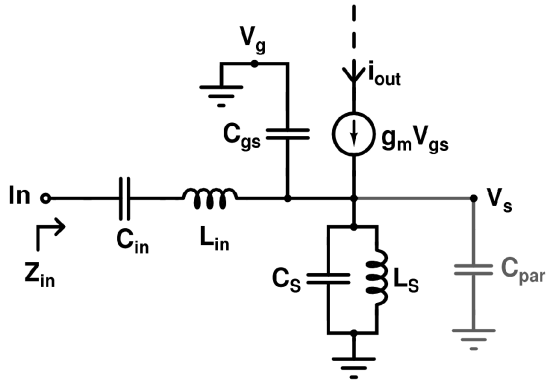

Fig. 3.24. CG stage small-signal model used in analysis.

Next, design parameters related to the source and series input resonators are defined. The Q-value of an ideal lossless parallel resonator formed by L_S and C_T is infinite, but resonators characteristic impedance is expressed as

$$Z_{LC} = \sqrt{\frac{L_S}{C_T}} . \tag{3.60}$$

By combining (3.18) and (3.60), the Z_{LC} can be given as

$$Z_{LC} = \omega_0 L_S = \frac{1}{\omega_0 C_T} . \tag{3.61}$$

Furthermore, when the relative characteristic impedance of the LC source resonator is scaled with respect to the source impedance Z_0, an additional parameter Z_{rel} is introduced as

$$Z_{rel} = \frac{Z_{LC}}{Z_0}. \tag{3.62}$$

In a matched case, i.e. $g_m = 1/Z_0$, when (3.34) and (3.62) are compared, there seems to be a relation $Z_{rel} = 1/Q_{in}$ between Z_{rel} and the Q-value of an IDCS stage. However, this is not a case. Z_{rel} depends on the values of source components L_S and C_T and on input matching frequency ω_0 and typically it has values between 0.5 and 2. However, as defined earlier, the Q_{in} is a ratio between gate-source and input voltages. In Section 3.3.7.1, Q_{in} of a CG stage is shown to be 1 at optimum input matching frequency. In that sense, Q_{in} is not a suitable parameter to analyze CG stage. Thus, in the following analysis, Z_{rel} is used instead.

Next, the input resonator components L_{in} and C_{in} are related to source resonator components L_S and C_T. The input inductance value L_{in} is scaled with respect to L_S with a design parameter p, such that $L_{in} = L_S / p$. To maximize the S_{11} and I_{out} bandwidths, the series resonator should be tuned at the same frequency with the source parallel resonator. Therefore $C_{in} = pC_T$ is needed. As a result, the input impedance of the circuit shown in Fig. 3.24 given in (3.19) is expressed as

$$Z_{in} = \frac{1 + s^2 L_S C_T}{spC_T} + \frac{sL_s}{1 + sL_s g_m + s^2 L_S C_T}. \tag{3.63}$$

Next, the Q-value of the input matching network, the input matching and output signal current BWs, and noise performance of the CG stage are analyzed with design parameters Z_{rel} and p.

3.3.7.1 Input network Q-value

As was discussed earlier, the input matching and output signal current bandwidths are typically related to the Q-value of the input matching network at center input matching frequency ω_0. For an IDCS LNA, for example, the input matching network is a series resonator and Q_{in} is typically larger than two. The fundamental difference of the CG-LNA is that the matching network is a parallel resonator, and therefore its Q-value is lower than that of an IDCS stage [58]. For the CG stage shown in Fig. 3.7b, the gate-source voltage of M_1 is equal to input voltage signal, i.e. Q_{in} is simply one. However, the input series resonator shown in Fig. 3.7c has an effect on the overall Q-value of the CG input. The Q-value of the CG input shown in Fig. 3.24 can be solved as

$$Q_{in,CG} = \frac{V_S}{V_{in}} = p\left(\frac{\omega}{\omega_0}\right)^2 \frac{1}{\sqrt{\left(1-(2+p)\left(\frac{\omega}{\omega_0}\right)^2 + \left(\frac{\omega}{\omega_0}\right)^4\right)^2 + Z_{rel}\frac{\omega}{\omega_0}\left(1-\left(\frac{\omega}{\omega_0}\right)^2\right)^2}}. \tag{3.64}$$

The $Q_{in,CG}$ always equals one at the center frequency ω_0 regardless of p or Z_{rel} values. This is clear, since at ω_0, input and resonator resonators are short-circuit and open circuit, respectively. Although the $Q_{in,CG}$ is one at ω_0, the performance of the CG stage can be affected by the design of input and source resonator, i.e. with p or Z_{rel} variables. By calculating the local optimums of (3.64), it can be shown that, when $Z_{rel} < 2\sqrt{p}$, the input matching network offers voltage gain. The maximum Q-value is obtained at

$$\omega_{Q_{in,CG},\max} = \frac{\omega_0}{2}\sqrt{\left(4 + 2p - Z_{rel}^2\right) \pm \sqrt{\left(2p - Z_{rel}^2\right)\left(8 + 2p - Z_{rel}^2\right)}} \tag{3.65}$$

and at those frequencies the maximum Q-value is

$$Q_{CG_{in},\max} = \frac{2p}{Z_{rel}\sqrt{4p - Z_{rel}^2}}. \tag{3.66}$$

The Q-values of a CG input is plotted in Fig. 3.25 as a function of frequency with several p values such that Z_{rel} = 1. The center frequency is scaled to 1. The peaking causes linearity degradation according to (3.14). This is depicted in the design example shown in Section 6.5.2. The effect of $Q_{in,CG}$ on the noise performance is discussed later in Section 3.3.7.4.

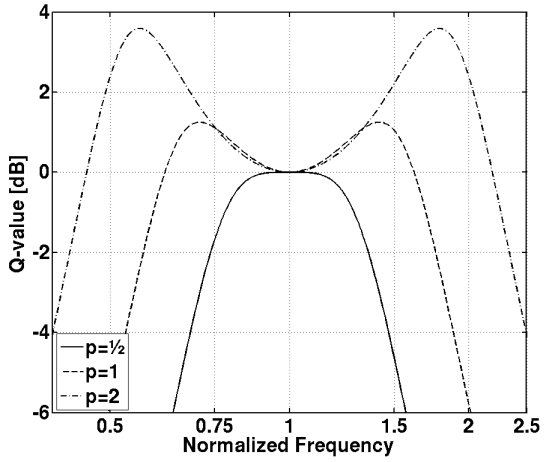

Fig. 3.25. Q-value of the input matching network. The input matching network is simulated with the following design values: Z_{rel} = 1 and p has values of ½, 1, and 2.

3.3.7.2 Input matching bandwidth

First, the effect of the series LC resonator formed by C_{in} and L_{in} is neglected, and only the effect of the source resonator in considered. The input impedance is given by (3.17). Assuming a perfect input matching (g_m=1/Z_0) at ω_0, the corner frequencies where the typical –10 dB S_{11} limit is achieved can be calculated as

$$\omega_{S11=-10dB} = \frac{\omega_0}{3}\sqrt{9 + 2Z_{rel}^2\left(1 \pm \sqrt{1 + \frac{9}{Z_{rel}^2}}\right)}. \tag{3.67}$$

In (3.67), Z_{rel} is given by (3.62). The bandwidth, where S_{11} is better than –10 dB, is achieved by subtracting the two frequencies given by (3.67). The result is scaled with respect to center frequency ω_0 giving the relative input matching bandwidth $BW_{rel,S11}$:

$$BW_{rel,S11} = \frac{BW_{S11}}{\omega_0} = \frac{2}{3}Z_{rel}. \tag{3.68}$$

Because the center frequency ω_0 and source impedance Z_0 are fixed, the relative bandwidth can be widened by increasing the Z_{LC} value. According to (3.61), the maximum value of Z_{LC} is achieved when the value of C_T is minimized, i.e. the additional shunt capacitor C_S is omitted and the value of L_S is increased such that the resonator is tuned at the wanted frequency. In that

case, the center frequency is susceptible to additional parasitic capacitance caused by layout, for example. In addition, it should be noted that the series resistance of the inductor L_S is not taken into account in the simple model shown in Fig. 3.24. Since the impedance level at the source node is low due to $1/g_m$ of the input transistor, the finite Q-value of the L_S has only a slight effect on the input matching bandwidth, as is shown in Section 6.5.2. According to simulations, $Q_{Ls} > 5$ is sufficient not to cause significant error in the BW result achieved by the theory. Such an inductor Q-value is easily achieved with current technology. As is discussed later in Section 3.3.7.4, the choice of the inductor L_S value plays a significant role regarding CG stage noise performance.

An example of BW_{S11} is shown in Fig. 3.26. The S_{11} performance is shown with a solid line for a case where the source parallel resonator is taken into account and $Z_{rel} = 1$.

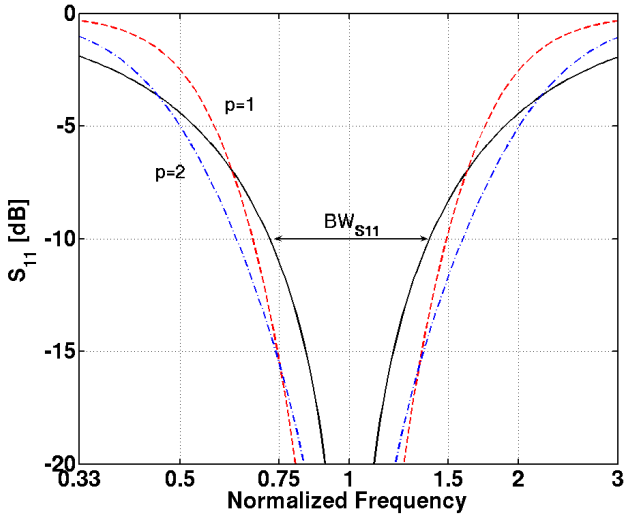

Fig. 3.26. S_{11} bandwidth as a function of normalized frequency. The solid line shows the performance when the source parallel resonator is taken into account ($Z_{rel} = 1$) and dashed and dashed-dotted lines show the performance parameter p values of 1 and 2, respectively.

Next, the effect of input parallel resonator formed by L_{in} and C_{in} is taken into account. The input impedance is given by (3.63). The frequencies where the –10 dB S_{11} limit is achieved are

$$\omega_{S11=-10dB} = \frac{\omega_0}{2\sqrt{3}}\sqrt{F_1 + F_2 \pm \sqrt{2}\sqrt{(F_1 + F_2)F_2 + F_3}}\,, \tag{3.69}$$

where

$$F_1 = -3F_4 + 12\,, \tag{3.70}$$

$$F_2 = \sqrt{9F_4^2 + 16p^2}\,, \tag{3.71}$$

$$F_3 = -4\left(9F_4 + 2p^2\right), \tag{3.72}$$

and

$$F_4 = \left(\frac{p - Z_{rel}^2}{Z_{rel}} \right)^2 . \tag{3.73}$$

The relative input matching bandwidth is shown in Fig. 3.27 as a function of p with several Z_{rel} values.

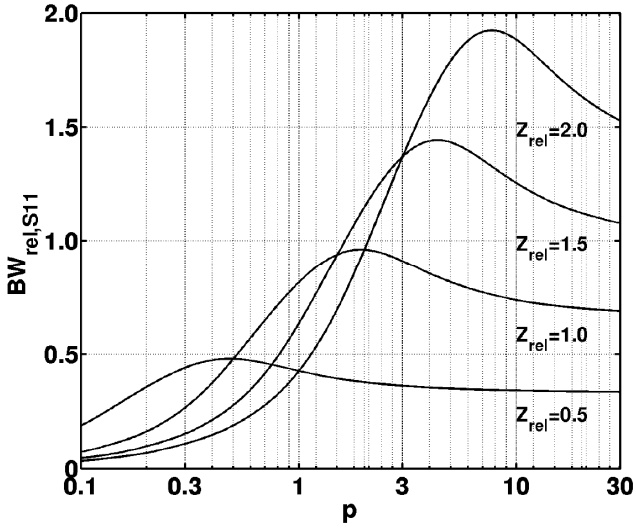

Fig. 3.27. Relative S_{11} bandwidth as a function of resonator design parameter p with several source resonator relative impedance Z_{rel} values.

The maximum $BW_{rel,S11}$ is achieved, when

$$p = 2Z_{rel}^2 , \tag{3.74}$$

and then

$$BW_{rel,S11,\max} = \sqrt{\frac{1}{6}\left(\sqrt{73} - 3\right)} Z_{rel} \approx 0.96 \cdot Z_{rel} . \tag{3.75}$$

Fig. 3.26 shows the S_{11}, when $Z_{rel} = 1$. A case, where both the input and source resonators have equal component values ($p = 1$) is shown with a dashed line. According to (3.74), when $Z_{rel} = 1$, the $BW_{rel,S11}$ achieves its maximum with $p = 2$. This is depicted with a dashed-dotted line in Fig. 3.26.

Fig. 3.28 presents the $BW_{rel,S11}$ as a function of Z_{rel}. The solid line shows the effect of the source parallel resonator only as is given by (3.68). The performance of the whole matching circuit with several series resonator design parameter p values is shown with a dashed line according to (3.69). With certain p and Z_{rel} values, it is possible to achieve wider $BW_{rel,S11}$ with both resonators than with the source resonator only. To extend the $BW_{rel,S11}$, the Z_{rel} of the source resonator should be increased. In addition, the design parameter p should be chosen appropriately not to limit the overall $BW_{rel,S11}$. The Z_{rel} increases proportionally to the source inductor value. Because the optimal value for p depends quadratically on Z_{rel}, the value of input inductor L_{in} is inversely proportional to the value of L_S. The choice of optimal Z_{rel} and p values is not unambiguous when $BW_{rel,S11}$ is known. For example, the minimum and maximum inductor values are typically limited by the technology used.

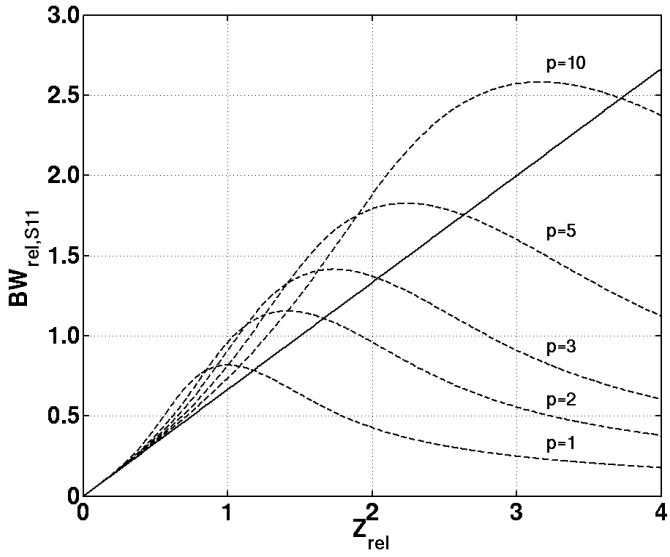

Fig. 3.28. Relative input matching bandwidth as a function of source resonator relative impedance Z_{rel} with several resonator design parameter p values. The solid line shows the effect of the source parallel resonator only.

3.3.7.3 Output signal current of CG stage

The CG stage transforms the voltage signal V_S sensed at the source node to the drain current. At a resonance frequency ω_0, the output current $I_{out} = g_m V_S = g_m V_{in}$, where V_{in} is the voltage signal fed to the LNA input. Both the input and source resonators, however, affect the I_{out} as a function of frequency. The output signal current of the CG stage achieves its maximum value at ω_0. Then such corner frequencies are calculated where the output signal current is decreased by 3 dB compared to the signal current at the resonance frequency. When the effect of the source resonator is considered only, the –3-dB corner frequencies are

$$\omega_{Iout,\max-3dB} = \omega_0 \left(\sqrt{1 + Z_{rel}^2} \pm Z_{rel} \right). \tag{3.76}$$

When the –3-dB corner frequencies are scaled with respect to ω_0 and the BW is calculated by subtracting the two frequencies given by (3.76), the relative –3-dB output signal current BW is:

$$BW_{rel,Iout} = \frac{BW_{Iout}}{\omega_0} = 2Z_{rel}. \tag{3.77}$$

According to (3.77), the output signal current BW improves linearly with source resonator impedance level. An example of a BW_{Iout} of a CG stage having $Z_{rel} = 1$ is shown in Fig. 3.29 with a solid line.

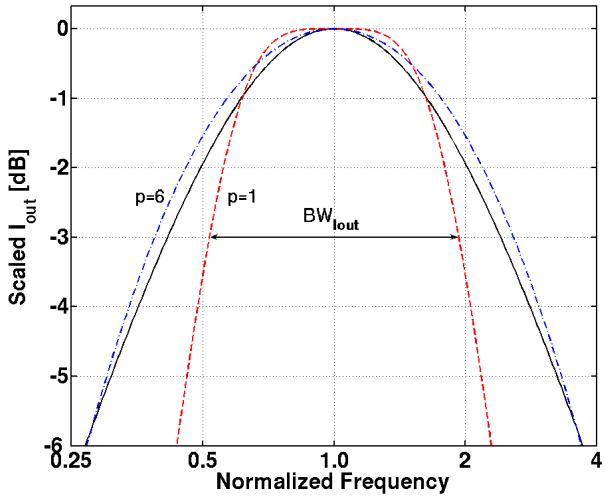

Fig. 3.29. Bandwidth of I_{out} as a function of normalized frequency. The solid line shows the performance when the source parallel resonator is taken into account (Z_{rel} = 1) and dashed and dashed-dotted lines show the performance with parameter p having values of 1 and 6, respectively.

When the effect of the series resonator is taken into account, the relative –3-dB output current BW is

$$BW_{rel,Iout} = \frac{1}{2}\sqrt{F_5 - F_6 \pm \sqrt{2}\sqrt{\left(F_6^2 + 4F_7 - 4\right) - \frac{F_6}{F_5}\left(F_6^2 + 8F_7 + 8\right)}}\,, \tag{3.78}$$

where

$$F_5 = \sqrt{16p^2 + F_4^2}\,, \tag{3.79}$$

$$F_6 = F_4 - 4\,, \tag{3.80}$$

$$F_7 = F_4 + 2p^2 - 3\,, \tag{3.81}$$

and F_4 is given by (3.73). The $BW_{rel,Iout}$ is plotted as a function of p with several Z_{rel} values in Fig. 3.30. The maximum $BW_{rel,Iout}$ is achieved, when

$$p = 6Z_{rel}^2\,, \tag{3.82}$$

which results in

$$BW_{rel,Iout,\max} = \sqrt{\frac{1}{2}\left(\sqrt{1201} - 25\right)}Z_{rel} \approx 2.2 \cdot Z_{rel}\,. \tag{3.83}$$

Compared to the $BW_{rel,S11}$, the $BW_{rel,Iout}$ is wider with equal Z_{rel} and p values. Therefore, it is more challenging to achieve S_{11} better than –10 dB than to gain a flatness of 3 dB. However, when the effect of the load impedance is taken into account, the gain can be limited at high frequencies due to the parasitic capacitance at the output node, as is shown in the design example presented in Section 6.5.2.

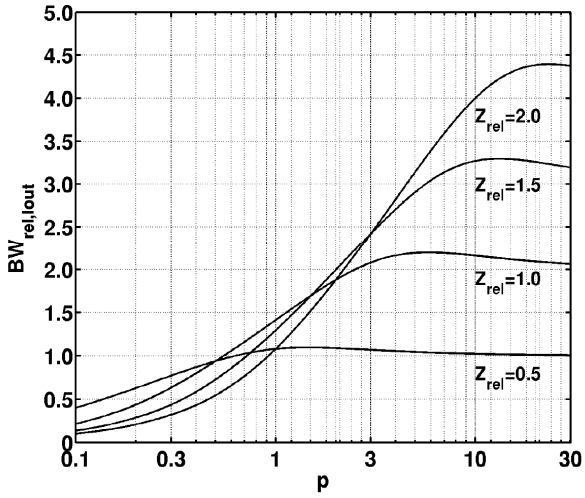

Fig. 3.30. Relative –3-dB output signal current bandwidth as a function of resonator design parameter p with several Z_{rel} values.

The $BW_{rel,Iout}$ is shown as a function of Z_{rel} in Fig. 3.31. The solid line shows the effect of the source parallel resonator only (3.77) and the performance of the whole matching circuit with several series resonator design parameter p values is shown with a dashed line according to (3.78). For example, if both the input and source resonators have equal component values (p = 1), the $BW_{rel,Iout}$ is approximately 1.4 when Z_{rel} is 1. As is presented in Fig. 3.29 and Fig. 3.31, in that case the $BW_{rel,Iout}$ is narrower than with the source resonator case only. According to (3.82), the $BW_{rel,Iout}$ is at its maximum when p = 6 and Z_{rel} is 1. This is depicted with a dashed-dotted line in Fig. 3.29. As can be seen in Fig. 3.29 and Fig. 3.31, when the effect of both resonators is taken into account, BW_{Iout} is only slightly wider compared to the case where only the effect of the source resonator in considered.

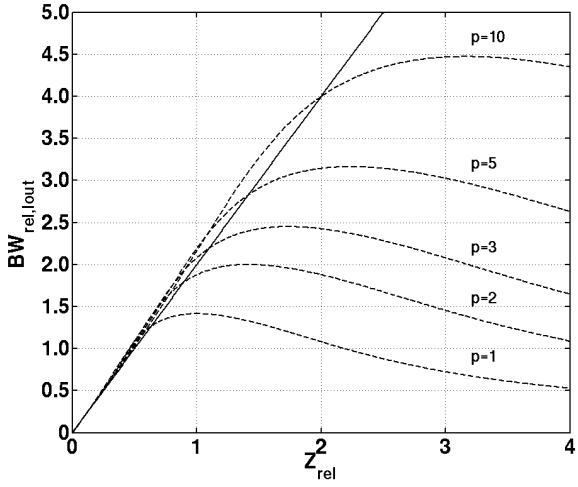

Fig. 3.31. Relative bandwidth of I_{out} as a function of source resonator relative impedance Z_{rel} with several resonator design parameter p values. The solid line shows the effect of the source parallel resonator only.

3.3.7.4 Noise figure

In Section 3.2.3.2, the noise of a CG stage was considered at a center frequency only. In this sub-section, the effect of source and input resonators to CG stage noise behavior in the frequency domain are analyzed. First, the noise caused by input transistor is considered only as shown in Fig. 3.32a. Then, the effect of the finite source inductor series resistance is taken into account as depicted in Fig. 3.32b. Finally, the noise of the CG stage is analyzed in a case when the input series resonator presented in Fig. 3.32c is included but the inductors' series resistances are ignored. The gate induced noise, the substrate transconductance, and the noise due to load are ignored in all cases for the sake of simplicity.

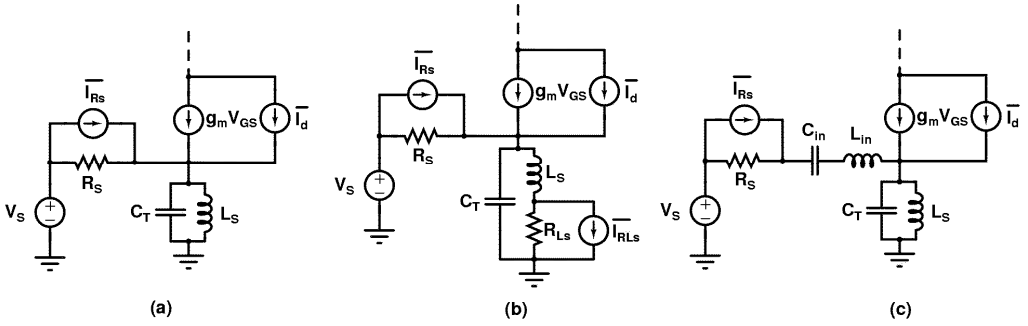

Fig. 3.32. a) Equivalent circuit to analyze the noise of CG transistor only, b) the effect of finite source inductor series resistance is taken into account, c) the effect of the input series resonator is taken into account.

When the effect of source resonator is taken into account (Fig. 3.32a), assuming $\alpha = 1$, the noise factor of a CG LNA is

$$F = 1 + \frac{\gamma}{g_m R_S}\left[1 + \left(\frac{R_S}{L_S\omega}\right)^2\left(1 - \left(\frac{\omega}{\omega_0}\right)^2\right)^2\right]. \tag{3.84}$$

The noise figure of a CG stage is presented in Fig. 3.33 such that $\gamma = 2/3$, $R_S = 50\ \Omega$, and $g_m = 1/R_S$. L_S had values of 1 nH, 2 nH, and 4 nH. The capacitor values of the source resonator are calculated such that the resonance is achieved at $f_0 = 4$ GHz. The minimum noise figure is independent of the source resonator characteristic impedance at the resonance frequency. At other frequencies, however, the source resonator plays a significant role. The frequency bandwidth, where NF is kept at a particular limit, can be increased by maximizing the L_S value, i.e. by having as large a source resonator characteristic impedance as possible.

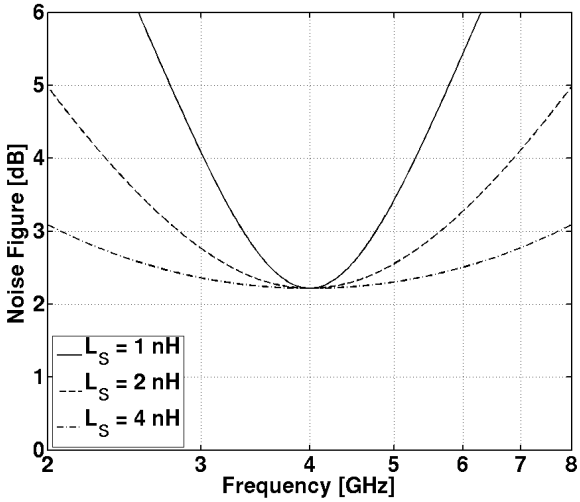

Fig. 3.33. Noise factor as a function of frequency. $\gamma = 2/3$, $f_0 = 4$ GHz, and $L_S = 1$ nH, 2 nH, and 4 nH.

The NF equations above assume that no signal loss is caused at the transistor source node. In practice, when the source is equipped with an LC resonator, the finite series resistance of L_S causes both signal leakage to the resonator and increases the noise of its own (Fig. 3.32b). When the effect of the finite series resistance R_{Ls} of the source inductor is taken into account, assuming $\alpha = 1$, the noise factor of a CG stage can be expressed as

$$F = 1 + \frac{\gamma}{g_m R_S}\left[1 + \frac{R_S^2}{R_{Ls}^2 + L_S^2\omega^2}\left(1 - \left(\frac{\omega}{\omega_0}\right)^2\right)^2 + \frac{R_{Ls}R_S}{R_{Ls}^2 + L_S^2\omega^2}\left(2 + R_{Ls}g_m C_T^2\omega^2\right)\right] + \frac{R_{Ls}R_S}{R_{Ls}^2 + L_S^2\omega^2}. \qquad (3.85)$$

The last term in (3.85) is the noise due to the series resistance R_{Ls} of the source inductor itself. In addition, several terms inside the brackets are also affected by R_{Ls}. Therefore, the R_{Ls} affects the noise performance of a CG stage due to modified noise transfer functions. For example, the finite R_{Ls} affects the frequency where the minimum noise figure is eventually achieved. If $g_m R_{Ls}/\gamma + 2C_T R_{Ls}^2/L_S + 2R_{Ls}/R_S << 1$, the minimum noise factor frequency is approximately

$$\omega_{F_{\min}} \approx \frac{1}{\sqrt{L_S C_T}}\sqrt{1 + R_{Ls}\left(\frac{g_m}{2\gamma} + \frac{1}{R_S}\right)} \qquad (3.86)$$

and at that frequency the minimum noise factor is approximately

$$F_{\min} \approx 1 + \frac{\gamma}{g_m R_S} + \frac{C_T R_{Ls}}{g_m L_S}\left(2\gamma + \gamma\frac{C_T R_{Ls} R_S}{L_S} + g_m R_S\right). \qquad (3.87)$$

In a matched case ($1/g_m = R_S$), (3.87) can be re-expressed as

$$F_{\min} = 1 + \gamma + \frac{1}{Q_L Z_{rel}}\left(1 + 2\gamma + \frac{\gamma}{Q_L Z_{rel}}\right), \qquad (3.88)$$

where Q_L is the Q-value of the source inductor defined in (3.6) and Z_{rel} is the characteristic impedance of the source resonator as given by (3.62). The minimum noise figure of a CG LNA

with γ values 2/3, 1, and 3/2 is shown in Fig. 3.34 as a function of $Q_L Z_{rel}$. It is crucial to have both a high inductor Q-value and large source impedance value to minimize the NF.

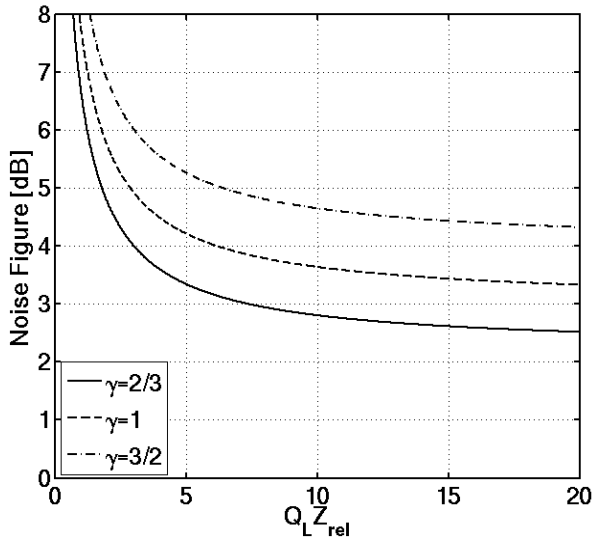

Fig. 3.34. Noise figure of a CG LNA described by source resonator performance. The noise parameter γ has values of 2/3, 1, and 3/2.

The noise factor of a CG stage is plotted in Fig. 3.35 with the same component values as in Fig. 3.33, except the source inductor Q-value is fixed at the moderately low value of 5 at 4 GHz frequency. According to Fig. 3.34, the minimum noise factor improves along with larger source inductor values. Due to finite R_{Ls}, the minimum noise figure frequency also shifts to higher frequency according to (3.86).

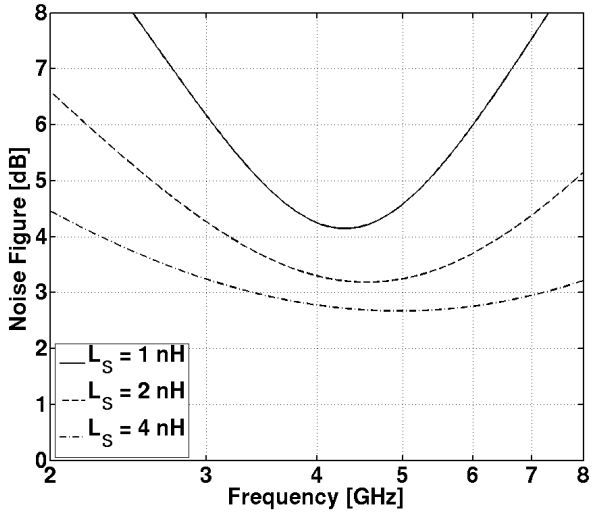

Fig. 3.35. Noise factor as a function of frequency. γ = 2/3, L_S = 1 nH, 2 nH, and 4, nH. The capacitor value is calculated such that f_0 = 4 GHz. The Q-value of the inductor is set to 5 at f_0 = 4 GHz.

The series resonator (Fig. 3.7c) affects the noise figure of the CG-state as well. In a matched case (g_m = $1/R_S$) and assuming α = 1, considering the noise of the input transistor only (the series resistances of inductors are neglected for simplicity), the noise factor for the circuit shown in Fig. 3.24 is expressed as

$$F = 1+\gamma\left[1+\frac{\left(1-\left(\frac{\omega}{\omega_0}\right)^2\right)^2\left(1+\left(\frac{p^2}{Z_{rel}^2}-2-2p\right)\left(\frac{\omega}{\omega_0}\right)^2+\left(\frac{\omega}{\omega_0}\right)^4\right)}{\left(p^2\left(\frac{\omega}{\omega_0}\right)^4\right)}\right]. \tag{3.89}$$

At $\omega = \omega_0$ (3.89) simplifies to $1+\gamma$. The noise figure is plotted as a function of frequency such that Z_{rel} = 1 and p has values of 1, 2, and 4. With certain p and Z_{rel} values, the input matching circuit offers voltage gain and the noise factor of a CG stage is less than the classical limit of $1+\gamma$. There are two frequencies, where the minimum noise factors are achieved:

$$\omega_{F_{\min}} = \frac{\omega_0}{2Z_{rel}}\sqrt{\left(4Z_{rel}^2+2pZ_{rel}^2-p^2\right)\pm\sqrt{\left(2pZ_{rel}^2-p^2\right)\left(8Z_{rel}^2+2pZ_{rel}^2-p^2\right)}}\,. \tag{3.90}$$

At the frequencies of (3.90), the minimum noise factor is

$$F_{\min} = 1+\gamma\frac{p}{Z_{rel}^2}\left(1-\frac{p}{4Z_{rel}^2}\right). \tag{3.91}$$

Equations (3.90) and (3.91) are valid if $p < 2Z_{rel}^2$. Otherwise, the noise factor minimum of $1+\gamma$ is achieved at ω_0. When (3.65) and (3.90) are compared, the noise factor minimum frequencies differ from the input Q-value maximum frequencies. The noise transfer functions for the noise of the source resistance and the drain current noise of the input device are different, which causes the difference in the maximum Q-value and noise factor minimum frequencies.

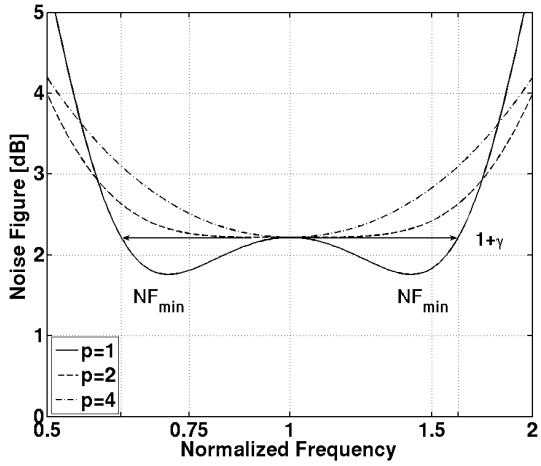

Fig. 3.36. NF of a wideband CG LNA (γ = 2/3). The CG-LNA is simulated with following input matching network design values: Z_{rel} = 1 and p has values of 1, 2, and 4.

The series resistances of the both inductors were omitted from the analysis. If the L_{in} is realized with a wirebond inductance and L_S is an on-chip inductor, the noise contribution of the former

is much smaller compared to the latter. The finite series resistance of the source inductor causes additional noise and loss, as is given by (3.85). In addition, the noise factor optimums are higher than predicted by (3.91). The effect of an input matching circuit on CG LNA noise can be observed in the design example presented in Section 6.5.2.

3.3.7.5 Conclusion and remarks

In this section, the CG LNA was analyzed in the frequency domain. The previous LNA analyses were mainly based on the Q-value of the input matching circuit at the center input matching frequency ω_0. Since Q_{in} of the CG stage is always one at ω_0, two design parameters, Z_{rel} and p, were introduced as suitable design/optimization variables for a CG stage. Relevant merits, such as the input matching network Q-value, the input matching and output signal current BWs, and noise performance of the CG stage, were analyzed in detail using parameters Z_{rel} and p. The analysis showed that it is more challenging to meet the –10-dB S_{11} performance than the 3-dB variation in output signal current. In addition, with certain Z_{rel} and p values the input matching network can have voltage gain, which affects both the linearity (IIP3) and noise figure performance. A design example, which shows the wideband CG LNA design procedure utilizing the presented analysis, is shown in Section 6.5.2. A wideband LNA can be realized with the CG stage, but the disadvantage is the high noise figure. If the high impedance at the source node is realized using an LC resonator, it is crucial to utilize a large-value inductor having a high Q-value to minimize the NF.

3.3.8 Reactive feedback

Recently, LNAs having multiple-GHz bandwidths have been realized with reactive feedback, e.g. [71] – [74]. The use of reactive feedback circumvents the problem associated with the large layout area of a CS LNA having the LC ladder network or noise performance of a CG LNA.

The simplified schematic of the first stage of the LNA presented in [71] is shown in Fig. 3.37a. The gate and drain inductors L_G and L_D having mutual inductance M resonate the output capacitor C_L and capacitances associated transistors M_1 and M_2. The input matching design details can be found in [71]. Although the first stage has wideband S_{11} performance, it has gain peaks at resonance frequencies. Therefore, an additional amplifier stage is required to boost the gain at midband frequencies. This comes with a penalty of reduced linearity.

The simplified schematic of the first stage of the LNA presented in [72] is shown in Fig. 3.37b. The input impedance is approximately [72]

$$Z_{in} \approx \frac{1}{(1+\beta)\beta g_m}, \tag{3.92}$$

where g_m is the transistor M_1 transconductance and β is the feedback factor, which is the inverse of the transformer's effective turns ratio (k/n, where k is the magnetic coupling factor and n is the physical turns ratio) [72]. In [72], the input transformer T_1 has approximately n of 4.5:1 and k of 0.85. The second stage is also utilized in [72] to widen the overall amplifier passband and to mitigate the Miller effect for the input stage. Current-reuse is used to minimize the current consumption.

In Fig. 3.37c, the idea of replacing source and load inductors with a single feedback transformer is presented [73]. As an advantage, smaller inductor values are required and the feedback transformer boosts the gain at the source by a factor of $1+k\sqrt{L_D / L_S}$ and an almost flat frequency response is achieved [74].

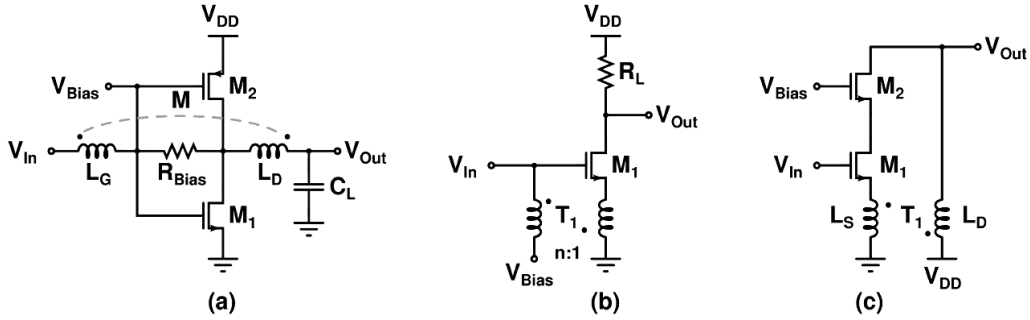

Fig. 3.37. Simplified schematics of LNAs utilizing reactive feedback, a) [71], b) [72], c) [73].

3.3.9 Comparison of wideband LNA topologies

In this sub-section, several different wideband LNA topologies are presented. In single-system narrowband applications, sufficient input matching BW is typically achieved with IDCS LNA. However, when the target is a system having large relative bandwidth, the use of an IDCS input stage can be limited. A slight improvement can be achieved with RC-feedback or additional CG signal path. The input matching BW improves along with lower feedback resistor value or increased g_m of the additional CG path. As a disadvantage, the overall gain and noise performance degrades, and therefore the two alternatives can offer only a moderate improvement to the basic topology. A design example, which compares the basic IDCS LNA topology to these two alternatives with actual IC component models, is presented in Section 6.5.1. According to that design example, the maximum BW achieved with an IDCS LNA is less than 2 GHz and thus only one UWB band group can be covered, for example.

A basic CS-LNA with shunt-resistor or common-drain feedback can offer wideband input matching and output signal current performance. Compared to the IDCS stage, the maximum output signal current is achieved at the input matching frequency. In addition, because sufficient input matching is achieved without source inductance, the LNA occupies a small layout area. However, the use of a resistor-feedback CS stage is challenging, since both the gain and S_{11} depend on the actual values of all components and thus that topology is sensitive to component-value deviation. Similar performance to the resistor feedback CS-LNA can be achieved with a common-drain feedback. It is less sensitive to the component values, and similar gain performance compared to a resistor feedback CS LNA can be achieved with a lower current consumption.

A wide operational band can be achieved with a CG stage. The NF, however, is significantly higher compared to the IDCS LNA and therefore the usage of a CG stage is limited to applications that can tolerate high NF. A design example of a wideband CG LNA is presented in Section 6.5.2.

If multi-GHz BWs are required with a single LNA, an IDCS stage with Chebyshev input matching network is one possibility. Due to several on-chip inductors it consumes significant silicon area and suffers from higher NF than a basic IDCS LNA. This can be circumvented by using reactive feedback, for example. This can offer low NF simultaneously with a small die area and low power consumption. However, it is another matter how an appropriate and well-modeled transformer is realized in practice, since transformers typically are not available in foundry-provided design kits.

As a conclusion, none of the presented LNA structures cannot be declared as the winner, but all of them have the advantages and disadvantages of their own. Therefore, the choice of a proper LNA topology depends on the requirements and it can be limited by the technology used. For example, as presented in Section 6.6, the input stage for the LNA operating in UWB BG1 was realized with the IDCS stage having an additional CG path.

3.4 Effect of bonding pad

The integrated circuits are almost always mounted either in a package or connected on a PCB. An input pad is needed to provide the interface between the chip and the outside world. Typically, in direct-conversion and low-IF receivers, the LNA input is the first and only RF port having an off-chip interface. The typical pad structure consists of a metal plate and ESD protection, as is shown in Fig. 3.38a. The equivalent circuit shown in Fig. 3.38b is achieved by replacing the transistor M_1 with a simple small signal model consisting of gate-source capacitance C_{GS} and transconductance g_m. Bondwire L_{in} is needed to connect the pad to the package lead frame or to the PCB microstrip line.

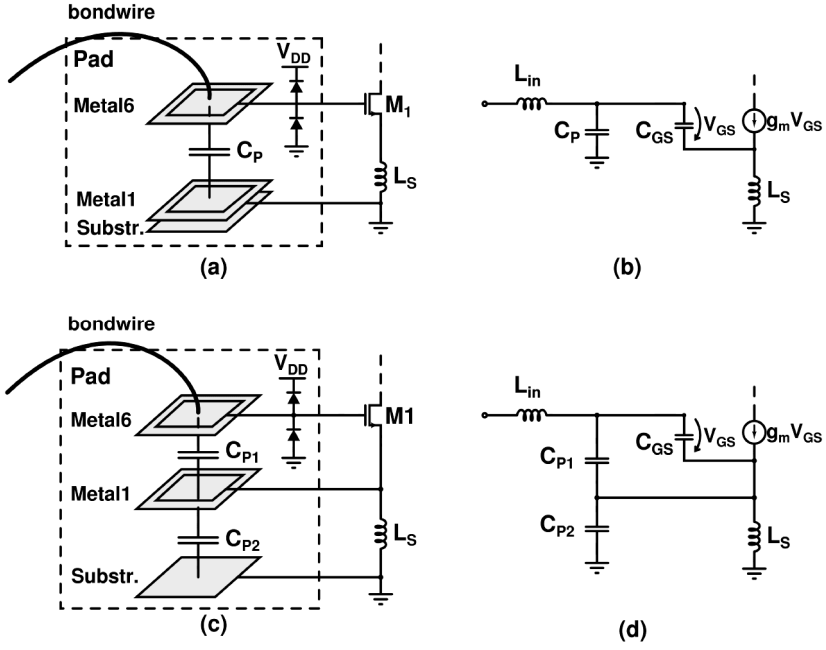

Fig. 3.38. a) Typical pad structure, b) simple equivalent circuit of a typical pad, c) modified pad structure, and d) simple equivalent circuit of a modified pad.

The capacitor C_P shown in Fig. 3.38b includes the parasitic capacitances at the gate node, i.e. capacitance caused by the bonding pads, ESD diodes, bondwire, and on-chip metal wiring. In a CG LNA, the parasitic capacitance can be included in a source resonator and therefore it can be resonated out with the source inductor. In a CS amplifier, the input parasitic capacitance has a more significant effect. The C_p transforms the real part of the LNA input impedance given by (3.2) downwards. Then, the real part of the impedance, shown in Fig. 3.38b, is approximately [31]

$$R_{in} \approx \left(\frac{C_{gs}}{C_{gs}+C_P} \right)^2 \underbrace{\frac{g_m L_S}{C_{gs}}}_{R_{eq}}, \tag{3.93}$$

where C_{gs}, C_p, g_m, and L_S can be identified from Fig. 3.38b and R_{eq} is the equivalent input resistance. Therefore, the R_{eq} should be designed to a higher level to maintain the overall optimal input impedance level. When the input reactive components values will not be altered, the higher R_{eq} is achieved by increasing the transconductance g_m. In addition, if the overdrive voltage is kept constant to maintain the linearity of the input stage, the increasing of g_m is mainly achieved with a larger drain current. The C_p should be minimized so as not to increase the current consumption. The on-chip metal wiring can be affected with a proper layout. The ESD diodes are typically provided by the foundry, and minimizing of C_p by modifying those is difficult.

A UWB front-end design example is presented in Section 6.6. When the LNA for BG3 was designed, it was found that the effect of parasitic capacitance can be minimized by connecting the lower pad metal layer (shield) to the source of the input transistor M_1, as is shown in Fig. 3.38c. The corresponding small-signal equivalent is shown in Fig. 3.38d. The parasitic capacitance C_{P1} is in parallel with the intrinsic C_{GS} capacitance and C_{P1} can be absorbed into the input matching network. When additional capacitances C_{P1} and C_{P2} are taken into account, the input matching criteria are modified to

$$R_{in} \approx \frac{g_m L_S \left[\left(L_{in}+L_S\right)\left(C_{gs}+C_{p1}\right)+C_{p2}L_S \right]}{\left(L_{in}+L_S\right)\left(C_{gs}+C_{p1}\right)^2} \approx \frac{g_m L_S}{C_{gs}+C_{p1}}, \tag{3.94}$$

$$\omega_0^2 \approx \frac{1}{\left(L_{in}+L_S\right)\left(C_{gs}+C_{p1}\right)+C_{p2}L_S} \approx \frac{1}{\left(L_{in}+L_S\right)\left(C_{gs}+C_{p1}\right)}, \tag{3.95}$$

when $(L_{in}+L_s)^2 >> 4C_{p2}L_{in}L_s$. When (3.94) is compared to (3.93) the real part value degradation is smaller. As a disadvantage, the capacitors C_{p1} and C_{p2} are not modeled in design kit and therefore capacitance extraction from the layout is required. Typically, the shield is realized with the lowermost metal layer and therefore the distance between pad contact (uppermost metal layer) and shield is much larger than the distance between the shield and substrate. Therefore, $C_{p2} > C_{p1}$. That is a desired result, since it is beneficial to have C_{p1} as small as possible to neutralize the effect of the pad.

It should be noted that the simple model shown in Fig. 3.38d ignores the influence of the ESD diode. Therefore, some parasitic capacitance to ground is still remaining, but its effect is significantly reduced. In addition, the simple model shown in Fig. 3.38d results also in another resonance at the frequency of

$$\omega_0^2 \approx \frac{(L_{in} + L_S)}{C_{p2} L_{in} L_S} \tag{3.96}$$

and at that frequency the input resistance is approximately

$$R_{in} \approx -\frac{g_m L_S}{C_{gs} + C_{p1} + C_{p2}}. \tag{3.97}$$

Since the input impedance is negative, the network input is unstable. In practice, however, other parasitic capacitors and resistors not included to the simple model have an affect on overall input impedance and attenuate the effect on negative resistance. In addition, the frequency of (3.96) is much higher than (3.3) and therefore its effect can be neglected.

The modified pad structure was used in the BG3 input of the UWB front-end design example presented in Section 6.6.

3.5 Load design

In this sub-chapter, different load structures are studied. For narrowband applications, sufficient performance is typically achieved either with a resistive or with a damped RLC resonator. Because the bandwidths of those loads are limited, different wideband structures are briefly discussed. The main interest is on the shunt-peak load and its alternatives. The wideband load design for two-stage amplifiers is also considered. The bandwidth shrinkage in such two-stage amplifiers, where both stages utilize separate shunt-peak loads, is discussed. Finally, a modified shunt-peak load using only single on-chip coil is proposed for two-stage amplifiers.

The different load alternatives described in this sub-chapter are not limited use with LNAs only. Obviously, same load structures can be utilized with local oscillator (LO) buffers or separate mixer transconductance stages as well. In a well-designed load, the effect of the following stage is also taken into account. For example, when a proper LNA or LO buffer load is designed, the loading effect of the mixer input stage and switch transistors should be considered, respectively.

3.5.1 Narrowband loads

The simplest load alternative is an ideal resistance, which has no parasitic capacitances thus being wideband by nature. In practice, however, all monolithic devices have parasitic capacitances and therefore the resistive amplifier output load is actually an RC-load. The capacitive part is the parasitic capacitance formed by the load resistance and the output (cascode) transistor and of the input parasitic capacitance of the following stage. At the RC-pole frequency, the impedance of the load is degraded by 3 dB from the low frequency value. Therefore, the resistive loads are typically restricted to applications, where the highest operational frequency is less than 2 GHz. Another disadvantage of the resistive load is the voltage drop, which can be problematic with low supply voltages.

The parasitic capacitance can be resonated out with a parallel inductor. Typically, the load inductor is an on-chip component, which requires a significant layout area compared to the resistor load only. The simplified schematic of the amplifier having a resonator load is shown in Fig. 3.39, where the input stage is replaced with a simple transconductance element. The output

resistance of the transconductance stage is assumed much larger than the load impedance. Taking into account the series resistance R_L of the load inductor L, the resonance frequency is

$$\omega_r = \frac{1}{\sqrt{LC}}\sqrt{1-\frac{R_L^2 C}{L}} = \frac{1}{\sqrt{LC}}\frac{Q_L}{\sqrt{1+Q_L^2}}, \tag{3.98}$$

where Q_L is the Q-value of the load inductor defined in (3.6) and all the parasitic capacitances are included into C. Due to finite Q_L, the resonance frequency is lower than with an ideal inductor but the resonance frequency is close to $\omega = 1/\sqrt{LC}$ when Q_L is large. At the resonant frequency (3.98), the impedance is

$$Z_{L,\omega=\omega_r} = \frac{1}{\frac{1}{R}+\frac{CR_L}{L}} = R \left\| (\omega_r Q_L L) \right. . \tag{3.99}$$

One measure of the resonator tank is its Q-value, which is usually determined with –3-dB bandwidth, i.e.

$$Q_r = \frac{\omega_r}{\Delta\omega_{-3dB}} . \tag{3.100}$$

For the resonator shown in Fig. 3.39, the Q-value is approximately [75]

$$Q_r \approx \frac{\omega_r RL}{\omega_r^2 L^2 + R_L R} = \frac{R}{\omega_r L + \frac{R}{Q_L}} . \tag{3.101}$$

The load impedance at resonant frequency can be expressed with (3.101) as

$$Z_{L,\omega=\omega_r} = \left(1-\frac{Q_r}{Q_L}\right) R = Q_r \omega_r L . \tag{3.102}$$

Therefore, when the desired bandwidth and impedance level of the resonator are known, the required component values can be calculated with (3.102). According to (3.99) and (3.101) the load resistor R and inductor L affect differently the impedance level and bandwidth of the resonator. The impedance level decreases when either the value of R or L is decreased. However, the Q-value of the resonator is lowered when the value of the load resistor R is decreased or the load inductor value is increased. In the latter case, the shunt-capacitance value needs to be decreased to keep the resonant frequency unchanged. The maximum bandwidth is obtained, when the load capacitor C consists only of the parasitic capacitance associated with the output node. In that case, the resonance frequency is susceptible to additional parasitics due to layout and the parasitics caused by metal wiring etc. should be extracted carefully.

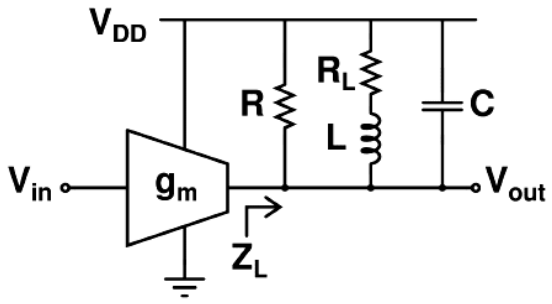

Fig. 3.39. Amplifier with a resonator load.

An example of RLC resonator impedance as a function of frequency is shown in Fig. 3.40. For the purpose of comparison, an actual and an ideal inductor were used. The Q-values are shown in Fig. 3.40. The response when an actual 5-nH on-chip inductor having Q_L of approximately 11 is used is shown with a solid line. The Q_L of practical on-chip inductors has a maximum value at self-resonant frequency. The response with an ideal 5-nH inductor, which has Q-value of 12 at 4 GHz, is shown with a dashed line. The center frequency is set with an ideal capacitor to 4 GHz and the impedance is damped with an ideal 300-Ω parallel resistor. When the impedances of loads using accurate and simple inductor models are compared, the difference is insignificant. Therefore, the resonator impedance and Q-value can be accurately predicted by knowing the Q_L at the resonance frequency. According to (3.99), the inductor impedance is approximately 1.5 kΩ, and the impedance of the whole resonator is 250 Ω at the resonance frequency. The –3-dB bandwidth is approximately 2 GHz ranging from 3.1 to 5.1 GHz. Thus, the resonator Q-value is about 2 and the value predicted by (3.101) is 1.99.

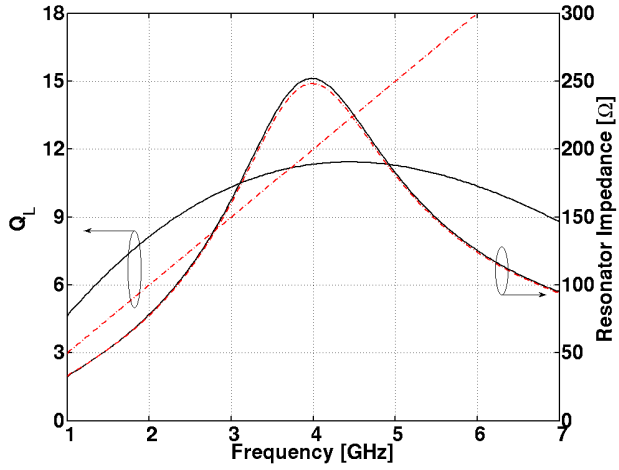

Fig. 3.40. Resonator load impedance and Q-value of the load inductor as a function of frequency. The values with an actual 5-nH on-chip inductor are shown with solid lines, while dashed lines show the responses with an ideal 5-nH inductor having Q-value of 12 at 4 GHz.

3.5.2 Wideband load structures

To design a wideband amplifier with a flat insertion gain response, both the output signal current of the input stage and the load should have wide enough bandwidths to achieve required gain deviation. In a narrowband amplifier, for example in an IDCS LNA, a resonator load is typically used. Although the RLC load of Fig. 3.40 has nearly 2-GHz BW, using it as a load for a maximally wide IDCS stage such as that presented in Section 3.3.1.2 would lead to an LNA that has approximately 6-dB gain variation over UWB BG1 band, for example. Generally, that is an undesirably large value. For low-frequency applications, which have a wide operation band, the resistive load could be a sufficient alternative if the voltage drop is tolerated. When the requirement of a wide relative wideband is combined with high center frequency, both the RLC and RC loads typically do not offer adequate performance.

For wideband and high-frequency applications, the shunt-peak load shown in Fig. 3.41 is a commonly used load structure. It consists of a series connection of inductance and L and resistor R with a shunt capacitor C. The frequency response is of the shunt-peak load is analyzed with the factor m, which is the ratio of L/R and RC time constants, i.e. $m = L/R^2C$ [76]. Then, the inductance value is expressed as

$$L = mR^2C \,. \tag{3.103}$$

The load impedance Z_L of a shunt-peak load is

$$Z_L(s) = \frac{R + sL}{1 + sCR + s^2CL} = R\frac{1 + smCR}{1 + sCR + s^2mC^2R^2} = R\frac{1 + m\dfrac{s}{\omega_0}}{1 + \dfrac{s}{\omega_0} + m\dfrac{s^2}{\omega_0^2}}, \tag{3.104}$$

where $\omega_0 = 1/RC$ is the RC pole frequency.

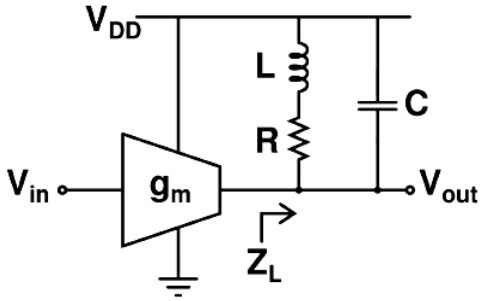

Fig. 3.41. Amplifier with a shunt-peak load.

The magnitude of the load impedance scaled to 0 dB is illustrated in Fig. 3.42 with several m values. When $m = 0$, there is no shunt peaking, and the response has a –3-dB corner frequency at a scaled frequency of 1. With $m = \sqrt{2} - 1 \approx 0.414$, the maximally flat response is achieved, and then the normalized –3-dB corner frequency is approximately 1.72. In the following, the term bandwidth extension ratio (BWER) is used. This is the ratio of the –3-dB corner frequency to the unity RC pole frequency [59]. The maximum BWER is achieved with $m = 1/\sqrt{2} \approx 0.707$, and then the normalized –3-dB corner frequency is approximately 1.85. In that case, approximately 1.5 dB peaking occurs at 0.88 normalized frequency.

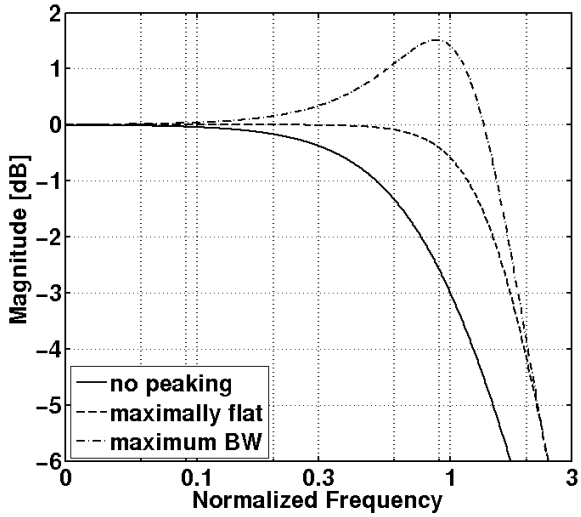

Fig. 3.42. Scaled magnitude of a shunt-peak load.

The performance of a shunt-peak load can be modified by adding an additional capacitor C_B in parallel with L, as is shown in Fig. 3.43. As a result, a bridged-shunt peaking load is formed [59].

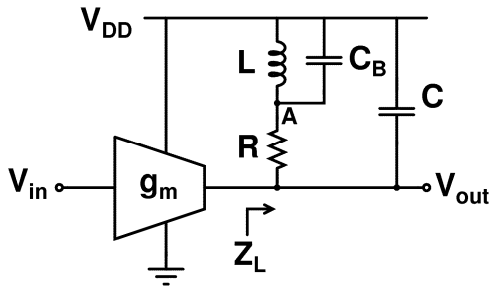

Fig. 3.43. Bridged-shunt peaking load.

The load impedance of a bridged shunt-peak load is

$$Z_L(s) = R\frac{1+m\frac{s}{\omega_0}+k_B m\frac{s^2}{\omega_0^2}}{1+\frac{s}{\omega_0}+(k_B+1)m\frac{s^2}{\omega_0^2}+k_B m\frac{s^3}{\omega_0^3}}, \tag{3.105}$$

where $k_B = C_B/C$, $\omega_0 = 1/RC$, and m is evaluated with (3.103). The shunt capacitor C_B adds another pole and zero to Z_L. The –3-dB corner frequency and gain peaking are depicted in Fig. 3.44 as a function of m and with different k_B values. The RC-pole frequency is normalized to 1. Compared to the typical shunt-peak load ($k_B = 0$), the maximum –3-dB cut-off frequency is not increased (BWER ≈ 1.85) but is achieved with lower peaking. However, the maximum BWER is achieved with a smaller value of m, thus leading to a smaller inductance value. As a result, inductor L occupies a smaller die area and it has higher self-resonant frequency [59]. When high

ω_0 frequency is targeted, the load capacitance C should be small. The minimum value of C is achieved when it is formed by the capacitive load of the next stage and parasitic capacitances of monolithic components connected to the output node. In that case, the design of a small-value capacitor C_B can be challenging. In practice, the load resistor and inductor and a possible feedback path (for example, see Fig. 3.14b and Fig. 3.17a) add parasitic capacitance at node A and a small C_B is present even without a physical capacitor. The value of capacitor C_B (or the parasitic capacitance at node A) should be kept less than the value of load capacitance C, since the operation of the simple bridged shunt-peak load shown in Fig. 3.43 becomes sensitive to component values and the BWER starts to decrease if $k_B > 1$.

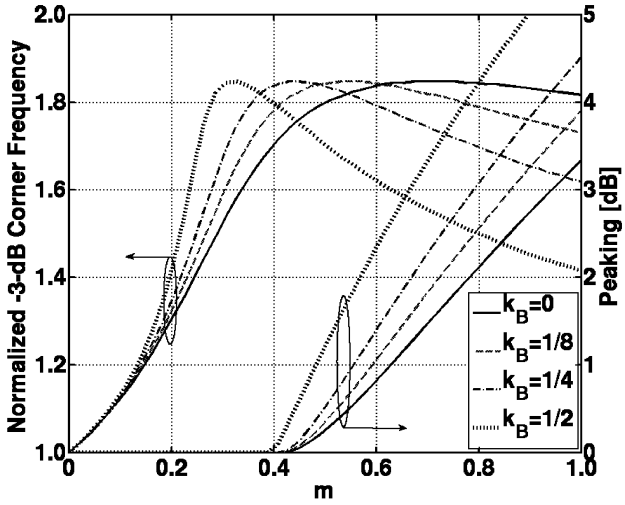

Fig. 3.44. –3-dB corner frequency and gain peaking of a shunt-peak load ($k_B = 0$) and a bridged-shunt load with $k_B = 1/8$, $k_B = 1/4$, and $k_B = 1/2$.

When an inductor is inserted such that the load capacitances are separated, the series-peaked load shown in Fig. 3.45a is formed [59]. The maximum –3-dB BW without peaking is approximately 2.52. In addition, the method is utilized, for example between the output of the CS input stage and a cascode stage as is shown in Fig. 3.45b, to minimize the effect of parasitic capacitances [77]. As a disadvantage, the transimpedance of the load shown in Fig. 3.45a is sensitive to the capacitor ratios, which define the BW and the ripple at the pass band.

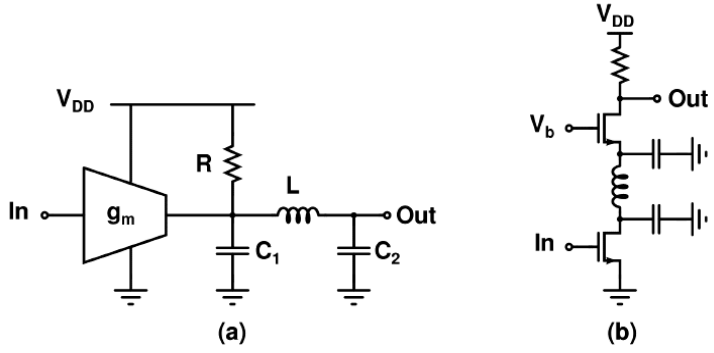

Fig. 3.45. a) Series peak load, b) a design example of series-peaking [77].

Other wideband loads can be designed by combining the presented structures, as is presented in [59] and [78], for example. Although BWERs higher than 4 can be reached with some of the techniques, there is also ripple at in-band frequencies. Clearly, complicated load impedance is challenging to realize in practice. A slight deviation from the nominal device values and the presence of parasitic components can significantly degrade the passband ripple and limit the –3-dB corner frequency. In addition, one disadvantage is the number of on-chip inductors, which is especially troublesome with balanced amplifiers. For example, balanced series-peaking loads cannot be realized with differential inductors. Thus, among various types of wideband load structures, shunt-peak loads are preferred in single-stage balanced amplifiers, since the number of on-chip inductors is small and its impedance is least sensitive to device values or ratios.

3.5.3 Load design for two-stage wideband amplifiers

With modern deep-submicron CMOS processes the intrinsic gain from a single transistor is only moderate. As a result, the gain achieved from a single-stage amplifier may not be sufficient and multi-stage amplifiers are needed to achieve adequate gain to suppress the noise of the following stages. The design of a two- or multi-stage amplifier is not so straightforward either. Although gain can be increased with cascaded amplifier stages, the overall bandwidth is limited by the stage that has the narrowest bandwidth. If the bandwidths of each stage are nearly equal, the overall bandwidth shrinks due to the cumulative roll-off of cascaded stages. Clearly, the number of on-chip inductors should be low to keep the layout area as small as possible. Next, the operation of a two-stage amplifier, where both stages utilize separate shunt-peak loads, is discussed. Then, a modified shunt-peak load using only single on-chip coil is proposed for two-stage amplifiers.

3.5.3.1 Cascaded shunt-peak loads

When two amplifiers are cascaded as shown in Fig. 3.46, the bandwidth typically shrinks compared to a single-stage amplifier. The bandwidth shrinkage of multiple-stage amplifiers is discussed in, for example, [78] and [79]. For example, when the amplifier is considered as having a single dominant pole, the normalized –3-dB frequency of the two-stage amplifier decreases to 0.643. Although the single dominant pole model is simple, the BW of the cascaded amplifier can be roughly estimated.

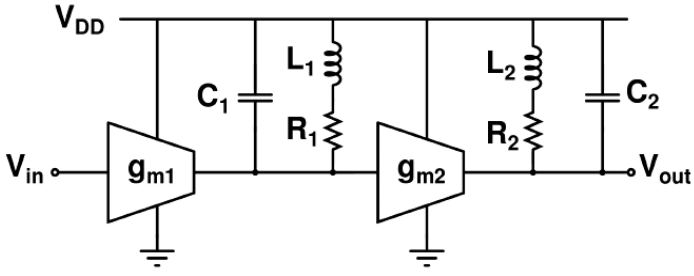

Fig. 3.46. Two-stage amplifier with shunt-peak loads.

In the following, the effective BW of a two-stage amplifier utilizing shunt-peak loads is analyzed. For simplicity, only the effect of the cascaded loads is considered and the bandwidth of the amplifier (i.e. g_m-stage in Fig. 3.46) is assumed infinite. Despite of the simplified model, since the impedance of the shunt-peak load consists of a zero and two poles, the analysis of cascaded shunt-peak loads is not so straightforward as it is for single-pole model. For example, dissimilar loads could be designed such that the other load peaks at a certain frequency, which compensates the droop caused by the other load. Thus, higher BWER could be obtained than with a single-stage shunt-peak load. The analysis of two-stage amplifiers having dissimilar shunt-peak loads with closed-form equations is tedious. Therefore, the –3-dB corner frequency is simulated and presented in Fig. 3.47. In that figure, m_1 in the x-axis is the design parameter of the first shunt-peak load and the values from 0 to 1 with incremental steps of 0.2 are values of the design parameter m_2 of the second stage. The order of shunt-peak loads can be interchanged without altering the –3-dB corner frequency. The maximum corner frequency of approximately 1.61 is achieved, when m_1 and m_2 values are around 0.8 … 0.9. If $m_1 = m_2 = m$, the accurate values for m and BWER are $1/\sqrt{\sqrt{2}} \approx 0.84$ and $\sqrt{2^{1/4}+\sqrt{2}} \approx 1.61$, respectively. Therefore, the m-value, which yields the maximum BWER, is slightly different from the single-stage shunt-peak load. Eventually, the maximum corner frequency starts to decrease, when m_1 and m_2 are larger than 1. Therefore, the BWER of the two-stage amplifier utilizing shunt-peak loads is limited to 1.61.[6] Compared to the single-stage case, the BWER is decreased by approximately a factor of 1.15. Clearly, taking into account the effect of the finite BW of the input stage, the bandwidth shrinkage can be significantly worsened.

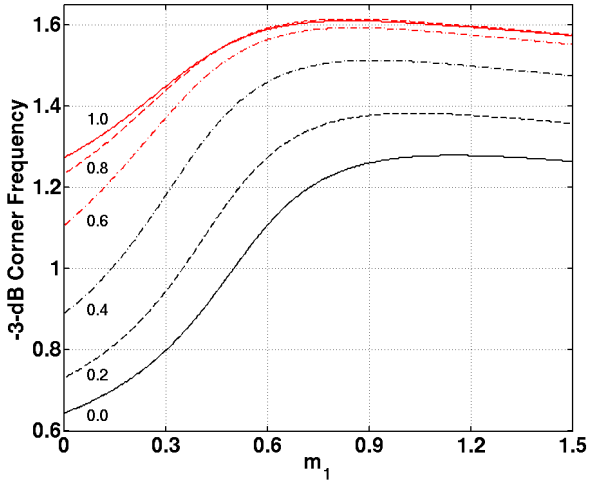

Fig. 3.47. –3-dB corner frequency of a two-stage amplifier having dissimilar shunt-peak loads. The shunt-peak load design parameter m_1 is shown in x-axis, and values from 0 to 1 with steps of 0.2 are values of the design parameter m_2 of the second stage.

[6] In this case, it would be possible to define the BWER of a two-stage amplifier as a ratio of –3-dB corner frequency to the cascaded RC-pole frequency (0.643). However, in this thesis, the BWER is always rationed to the unity normalized frequency for the sake of clarity.

The use of large m values significantly increases the gain peaking as is presented in Fig. 3.48. For example, with maximum BWER ($m_1 = m_2 = 0.84$), the gain peaking is 4.7 dB, while with $m_1 = m_2 = 1/\sqrt{2}$, the gain peak is only 3 dB, and the BWER of a two-stage amplifier would be 1.60. Hence, the difference to maximal –3-dB corner frequency is insignificant, but is achieved with smaller peaking.

The maximally flat response can be achieved with several m_1 and m_2 combinations. However, according to simulations, the maximally wide response without peaking is achieved when m-values of both loads are identical. The maximally flat response is achieved with $m = \sqrt{2} - 1 \approx 0.414$, which is the same result as with a single-stage shunt-peak load. Then, the resulting normalized –3-dB corner frequency is approximately 1.33. Compared to the single-stage case, the BWER is decreased by approximately a factor of 1.3.

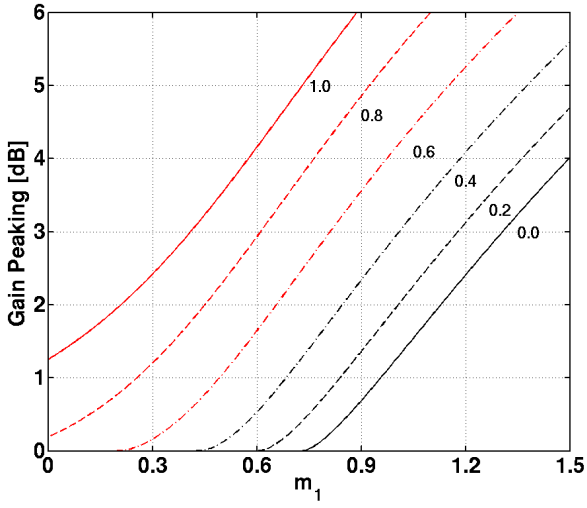

Fig. 3.48. –3-dB corner frequency of a two-stage amplifier having dissimilar shunt-peak loads. The shunt-peak load design parameter m_1 is shown in x-axis, and values from 0 to 1 with steps of 0.2 are values of the design parameter m_2 of the second stage.

3.5.3.2 Cross-connected shunt-peak load

As presented earlier, the maximum –3-dB normalized corner frequency of a two-stage amplifier utilizing shunt-peak loads is limited to 1.6. The BWER could be enhanced with the more complex load presented in Section 3.5.2. However, the number of differential inductors should be as small as possible for a compact layout. Therefore, a structure where the load inductor is re-used in cascaded stages is shown in Fig. 3.49. The resulting transimpedance of the modified shunt-peak load is

$$Z_L(s) = \frac{g_{m2}\left(R_1R_2 + sR_1L + sR_2L\right) - sL}{1 + s\left[g_{m2}L + C_1R_1 + C_2R_2\right] + s^2\left[L\left(C_1 + C_2\right) + C_1C_2\left(R_1R_2 + sR_1L + sR_2L\right)\right]}. \quad (3.106)$$

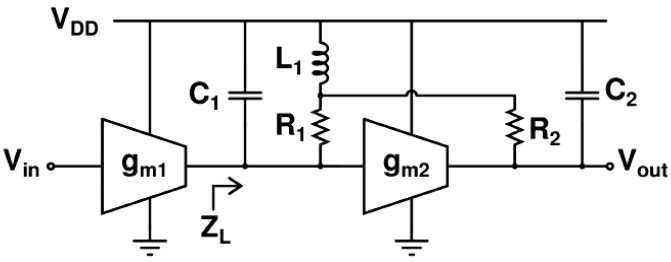

Fig. 3.49. Two-stage amplifier with a cross-connected shunt-peak load.

For simplicity, resistors and capacitors are assumed identical, i.e. $R_1 = R_2 = R$ and $C_1 = C_2 = C$, and L is replaced with (3.103). In addition, the g_{m2} is assumed to be constant as a function of frequency, i.e. it has infinite BW. Then, (3.106) can be modified to the form

$$Z_L(s) = R \cdot \frac{G_2 + (2mG_2 - m)\frac{s}{\omega_0}}{1 + (2 + mG_2)\frac{s}{\omega_0} + (1 + 2m)\frac{s^2}{\omega_0^2} + 2m\frac{s^3}{\omega_0^3}}, \tag{3.107}$$

where $\omega_0 = 1/RC$ is the RC pole frequency and $G_2 = g_{m2}R$ is the dc gain of the second stage. Compared to a typical shunt-peak load, there are now three complex poles and a zero. An example of characteristic impedance (3.107) is shown in Fig. 3.50, where $G_2 = 5$ and with m values of 0.5, 1, and 2. The impedance is scaled to 0 dB at unity frequency. By choosing component values appropriately, the two local points (i.e. the points where the derivative of the magnitude curve equals zero) can be equalized and thus flat band gain at the wanted frequency area can be achieved.

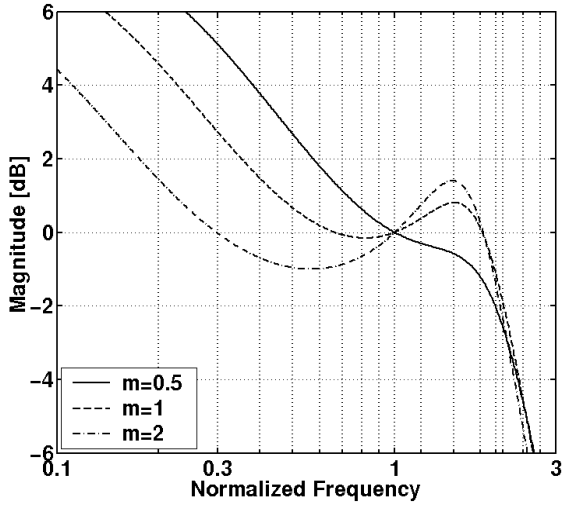

Fig. 3.50. Scaled magnitude of a modified shunt-peak load with $G_2 = 5$ and with several m values.

The analysis of the operation of a modified shunt-peak load with closed-form equations is complicated. The target is to equalize the gains at two local points to have flat gain over a wide operation frequency. Therefore, a design value for m is sought as a function of G_2. The first-order formula could not sufficiently model the behavior of the modified shunt-peak load. Therefore, an approximate second-order formula is given to achieve a simple design criterion for m:

$$m = \frac{1}{0.2 + 0.3G_2 - 0.005G_2^2} \,. \tag{3.108}$$

The operation of the modified shunt-peak load is shown in Fig. 3.51 with different G_2 values and (3.108) is used to calculate m. At low frequencies, the frequency response shows the roll-off due to the first pole. The transimpedance is scaled to 0 dB in the flat band area. With larger G_2 values, the bandwidth of the flat gain area increases and the band of interest shifts to a higher frequency.

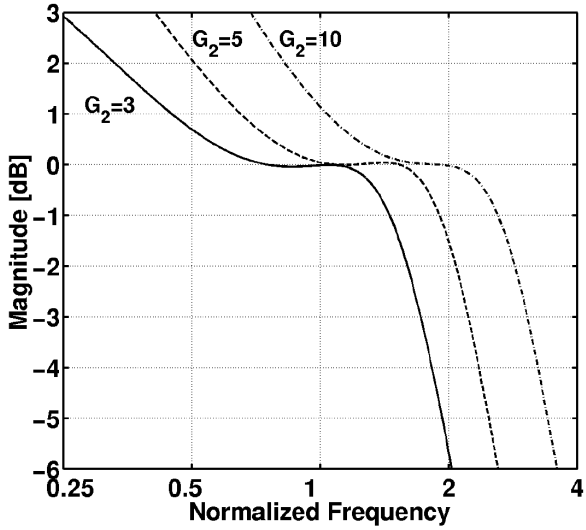

Fig. 3.51. Magnitude of the modified shunt-peak load with different G_2 values.

The performance of the modified shunt-peak load with G_2 = 5 is compared to a two-stage amplifier utilizing identical shunt-peak loads in Fig. 3.52. The modified shunt-peak load is shown with a solid line, while the traditional shunt-peak load with maximally flat and maximally wide bandwidth are presented with dashed and dashed-dotted lines, respectively. Due to quite different frequency behavior, comparison of all three cases is not trivial. The magnitudes of the traditional shunt-peak load are scaled to 0 dB at zero frequency and the magnitude of the modified shunt-peak load is scaled to 0 dB in the flat band area. The gain flatness of the modified shunt-peak load is better in the normalized frequency area of 1–1.5. The corner frequency, where the gain is decreased by 3 dB from the band of interest, is approximately 2.23. As a result, the modified shunt-peak load offers a trade-off between the gain level and having flat frequency response over a wide bandwidth with a single coil. The design example and usage of such circuit is shown later in Section 6.6.2.5.

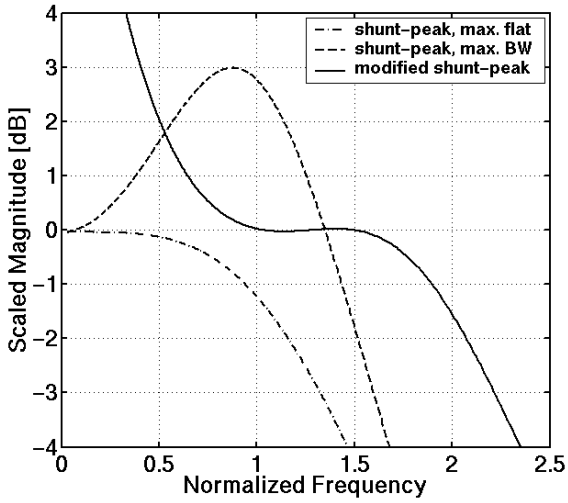

Fig. 3.52. Frequency response of two-stage amplifier. A solid line shows the response of a modified shunt-peak load (G_2 = 5). Dashed and dashed-dotted lines present the responses of a typical shunt-peak load with maximally flat and maximally wide bandwidths, respectively.

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4 Downconversion mixer design

The mixer is required in almost all receiver and transmitter topologies. It is a nonlinear circuit, the primary target of which is to perform frequency translation. In principle, that can be accomplished with either nonlinear devices (diodes, transistors) or time-varying elements (switches). Mixers can in general be categorized as passive or active mixers. Typically, active mixers can provide conversion gain, while the passive mixers are lossy but more linear. In addition, mixers can be divided into double-balanced, single-balanced, and unbalanced designs [1]. The kind of mixer required depends on the related application and system requirements.

This chapter deals with the design of the downconversion mixers for DCRs. First, general mixer design guidelines are discussed. In this thesis, only active mixers were implemented. Therefore, the detailed analysis of passive mixers is omitted from this thesis and only a short overview is given in Section 4.2. After that, the most common active mixer topology, the Gilbert cell mixer, is described and the issues related to the mixer input stage, switch quad, load design, and interfaces with other blocks are discussed. Finally, different mixer design aspects, such as folded mixers, mixers utilizing current boosting, and quadrature mixer design alternatives are considered. In addition to the mixer structures presented in this chapter, there are different kinds of mixers, which are not covered in this thesis. For example, switched transconductance mixers [2] and bulk driven mixers [3] can be found in the literature.

4.1 General mixer design aspects

To design a proper downconversion mixer for a receiver, the most important specifications are gain, noise, and linearity. In DCRs, the mixer interfaces are usually not matched. Therefore, the conversion gain (or loss) is measured with voltage gain. Typically, a wireless front-end should provide approximately 25-35 dB voltage gain to suppress the noise of the following stages. Because the practical voltage gain achieved from the LNA(s) is normally 15-25 dB, the mixer should provide the rest of the needed gain.

The design of a proper mixer is challenging due to linearity and noise requirements. In a DCR, dc offsets and $1/f$ noise of the mixer can severely degrade the sensitivity of narrow band systems, where most of the useful signal is located close to dc. The wide bandwidth of the communication system, e.g. WCDMA or UWB, reduces the influence of the flicker noise. Because the mixer handles the output signal of the LNA, its linearity (both ICP and IIP3) should be higher than the LNAs linearity by the gain of the LNA in order not to become a bottleneck in the front-end. In practice, high linearity is challenging to achieve without consuming a substantial amount of current. Thus, the mixer typically dominates the whole front-end linearity. In addition to the ICP and IIP3 requirements, the mixer is usually a dominant source for the second-order nonlinearity [4]. The IIP2 is especially problematic if a direct-conversion or low-IF architecture is used. The analysis and calibration of the second-order intermodulation is comprehensively studied in the literature, for example, in [5] – [8].

4.2 Passive mixers

A typical passive commutating mixer utilizing four NMOS transistors as analog switches is shown in Fig. 4.1. It does not need bias current and therefore it would be an ideal low-power circuit. Since there is no dc current flowing thorough the mixers, passive mixers are often claimed to be free of 1/*f* noise. This is not completely true, since flicker noise can be observed with passive mixers also [9], [10]. Its magnitude is proportional to the input signal amplitude and inversely proportional to the slope of the gate voltage waveforms at LO transitions [10]. Nevertheless, the level of flicker noise of the passive mixers is substantially lower than that of the active ones.

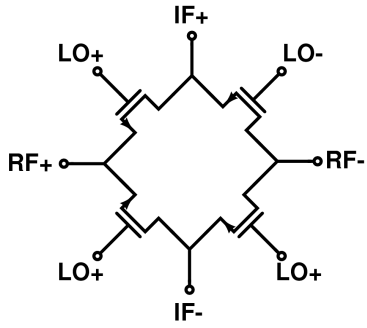


Fig. 4.1. Passive mixer.

The dc bias level of the switch gate plays a significant role in mixer performance. Typically the gate voltage is set close to the threshold of conduction to achieve the lowest on-resistance. As a result, noise from the switch quad is minimized and good linearity (IIP3) is achieved [11]. In addition, overlapping on-periods are prevented [12]. The overlapping on-periods result in decreased conversion gain and increased noise from the LO port [12]. The conversion gain can be increased with overlapping off-periods but, in that case, the linearity suffers [13]. Furthermore, linearity performance (both IIP2 and IIP3) is maximized, when the voltage swing across the switch transistors is kept as small as possible. Such passive mixer topology is discussed, for example, in [14].

Due to their flicker noise and linearity properties, passive mixers are potential alternatives. The disadvantage of the mixer shown in Fig. 4.1 is its non-unilateral nature, i.e. the signal flows bi-directionally from input to output, thus causing several problems. First, when a passive mixer is connected to the output of the LNA, the circuits after the mixer can load the LNA and degrade its gain and selectivity [15]. In addition, two mixers downconverting a common input by quadrature LO signal phases would tend to load each other's outputs during the overlap period when switches are on [16]. As a result, the output impedance of the mixers is lowered, which increases the noise contribution of the first baseband stage. The overlap time can be minimized by increasing the LO amplitude, as discussed later in Section 4.3.3.1. In addition, there is a second mechanism, which lowers the mixer's output impedance. The parasitic capacitances at the switch source and drain nodes lower the mixer output impedance [9]. With larger switches, there will be larger source/drain-junction capacitances, which results in larger amounts of stored noise. Due to the switched capacitor effect, these capacitances cause equivalent resistor, the value of which is inversely proportional to the LO frequency and the value of parasitic

capacitance [9], [11]. Therefore, from the noise point of view, there is a trade-off between having a switch transistor that is large enough for low on-resistance but small enough to achieve good noise performance.

An additional example of a passive mixer is presented in Fig. 4.2 [17]. Compared to the passive mixer shown in Fig. 4.1, the RF signal is fed to the switch transistors' gates and V_{DS} varies with the LO signal. The transistors are in the triode region and therefore resistance is inversely proportional to the RF signal. The capacitors C_V are needed to filter out the high-frequency currents injected into the virtual ground nodes. Thus, the op-amp needs only to have enough bandwidth to handle the low-frequency components [17]. The IF voltage signal is available at the output of the feedback resistors. The mixer shown in Fig. 4.2 has excellent linearity, but also a disadvantage in the form of large required LO swing and the rather poor noise performance.

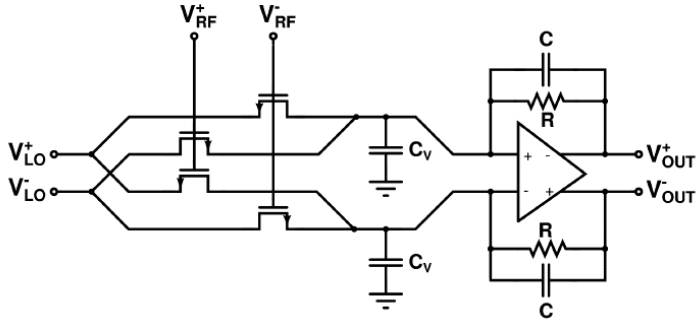


Fig. 4.2. Highly linear passive mixer [17].

4.3 Active downconversion mixers

The most common mixer for IC designers is probably the Gilbert-cell mixer and its variants. It was originally proposed by Barrie Gilbert as a four-quadrant multiplier in 1968 [18]. The schematic of a typical CMOS Gilbert mixer is shown in Fig. 4.3a. It consists of a balanced grounded transconductance stage, which converts the input voltage signal to current-mode. A differential pair could be used as a transconductance stage as well. After the input transconductor, the signal is fed to the switching quad, which is driven by a large (i.e. several 100 mV_{pp}) LO signal. The output current of the mixer is typically driven to either resistive, reactive, or active load.

Usually the Gilbert-cell mixer is driven with balanced RF and LO signals, i.e. it is a double-balanced structure, as is shown in Fig. 4.3a. If either of the RF or LO signals is supplied alone, there is no output signal. However, either of the input signals can be inputted single-endedly. Then, the other side of the input or switch quad is ac-grounded. For example, the output signal of the single-ended LNA can be brought to the mixer in that way [19]. Then, the mixer conversion gain is decreased, because only half of the mixer input stage transconductance is utilized. Double-balanced mixers are usually preferred in DCRs because they generate less even-order distortion, provide high port-to-port isolation, and usually have better noise performance than their single-balanced counterparts.

A single-balanced mixer is shown in Fig. 4.3b. It does not require a differential RF input signal and requires only half of the current of a balanced topology. The main problem in using single-balanced mixers is the large LO signal feedthrough at its output that may saturate the following stage [16]. Single-balanced mixers are suited for the first downconversion in receivers utilizing multi-step downconversion, see, for example, [15]. Next, different parts of the downconversion mixer and interfaces to other blocks are discussed.

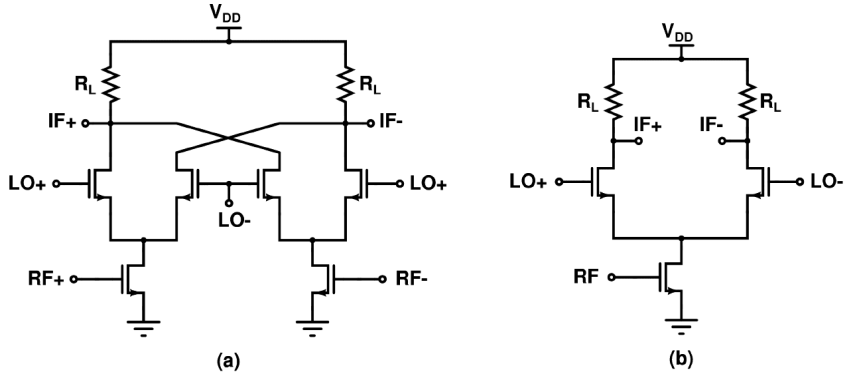


Fig. 4.3. a) Double-balanced mixer, b) single-balanced mixer.

4.3.1 Interface to LNA

The LNA output is usually ac coupled to the mixer input. Typically, the load of the LNA is a resonator and therefore the dc level of the LNA output is close to the positive supply voltage (when NMOS transistors are used as LNA input devices and resonator is connected towards positive supply). Thus, the LNA output dc level is not sufficient for the mixer input stage and with ac-coupling the mixer can be biased independently. In addition, due to ac-coupling, the second-order distortion generated by the LNA is filtered out, and the main IIP2 source of the front-end is the mixer itself.

4.3.2 Mixer input stage

Since the noise performance of mixers is generally rather poor, the transconductance is needed for signal amplification. In addition, a separate input stage improves the reverse isolation and separates the switch transistors from the LNA output. In the following, different possibilities to implement the mixer input stage are discussed. It should be noted that downconversion mixers without a separate transconductor stage are published as well, for example, in [P1], [P2], [20], and [21]. Such structures, where the LNA is merged with the downconversion mixer, are briefly introduced in Section 4.4.4.

In this thesis, stand-alone mixers were not implemented but the mixers were implemented together the LNA. Therefore, input matching techniques for mixers are not discussed. Nevertheless, there may be a need to match the mixer input to a certain impedance, for example due to the interstage SAW filter, for example. In that case, input matching methods similar to those presented for the LNA, would, in general, be applied to mixers as well.

Usually, the mixer input stage is composed of a balanced grounded CS amplifier or a differential pair with a tail current source, as shown in Fig. 4.4a and Fig. 4.4b, respectively. Both cases have their benefits and drawbacks. With the grounded CS stage, the available voltage headroom is relaxed by V_{DS}. This is crucial, especially in low-voltage designs. The third-order nonlinearity of both common-source and differential pair transconductors generally improve with larger overdrive voltages. In addition, when biased at the same current and device dimensions, the grounded CS stage has better third-order nonlinearity performance than the differential pair with a tail current source [22], [23]. However, a tail current source offers a common-mode rejection ratio, and the trade-off of the grounded CS stage is greater sensitivity to supply noise [22]. The tail current source can be replaced with an LC resonator tuned at the fundamental frequency to achieve high impedance to ground [24]. The LC resonator can also be tuned at the second harmonic to suppress common mode and second harmonic signals [25]. The inductor provides a dc bias path and thus dc voltage drop is avoided. As a drawback, an on-chip inductor consumes significant silicon area.

The linearity of the input stage can be improved by source degeneration. Degeneration can be implemented with resistive or reactive components. Using resistors leads to small layout area, but resistors are noisy and cause a voltage drop. If inductors are utilized instead, better noise performance is achieved, but at the cost of increased layout area. In addition, the transconductance stage with inductive degeneration has better IIP3 than those with resistive degeneration [26]. In a case of quadrature mixers, the source inductor can be shared between I- and Q-input stages to save the valuable silicon area [27].

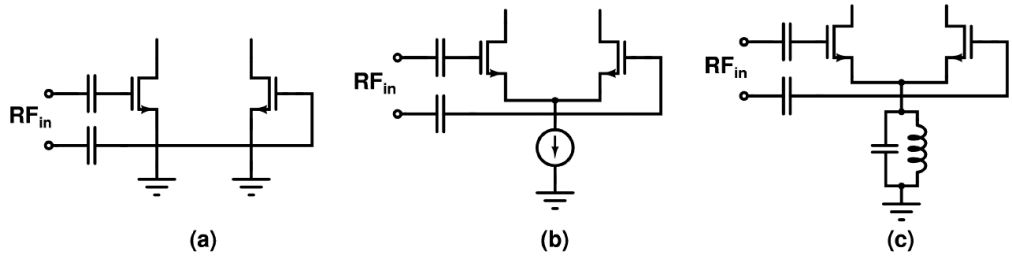


Fig. 4.4. Mixer transconductance stage utilizing a) grounded CS stage, b) differential pair with a tail current source, or c) source-coupled pair with a narrow-band LC resonator.

The noise due to the mixer transconductor stage is briefly discussed at a general level. The thermal noise due to the transconductance stage is at the same frequency as the input RF signal and, in DCRs, it will be downconverted to dc frequency, just like the useful signal [28]. It should be noted that any periodic LO waveform downconverts the noise from the odd-harmonics of the LO signal also. The noise at each frequency is uncorrelated and the noise contributions are added as the mean square [28]. However, the noise at the fundamental frequency accounts for a major part of the noise, even if the noise from the input stage is wideband [29]. If inductive source degeneration or input matching is used, the frequency response of the transconductance stage becomes frequency selective. In that case, noise from fewer harmonics should be taken into account [29]. The flicker noise of the transconductance transistors is up-converted to LO frequency and its harmonics. Typically, the flicker noise corner frequency of the transconductance MOSFETs is much lower than the LO frequency. Thus, they contribute only thermal noise at the mixer output [28].

When second-order intermodulation is taken into account, the fully differential transconductor (Fig. 4.4b) has higher second-order linearity than the grounded CS transconductor [5]. The second-order nonlinearity is mainly determined by threshold voltage mismatch. It improves with increasing biasing currents and decreasing device widths, i.e. for larger overdrive voltages [5]. Alternative input stage possibilities minimizing the second-order intermodulation are shown in Fig. 4.5. Figure 4.5a presents a mixer where the transconductance stage is ac-coupled to the switch quad to filter out the IM2 distortion generated by the input stage. The achieved IIP2 improvement is only moderate [30]. Moreover, the transconductance stage and switch quad require different quiescent current levels for optimal performance. With separate dc paths, the performance of both stages can be optimized separately, but more current is consumed compared to the conventional structure [31]. Figure 4.5b presents a transconductor that simultaneously obtains large degeneration at low frequencies and low degeneration at RF frequencies [32]. As a result, high IIP2 and IIP3 are achieved. Figure 4.5c shows a simple biasing technique that cancels the IM2 distortion in the CS transconductor [33]. Ideally, if the transconductor is excited differentially and all the devices are matched, no IM2 distortion is generated. Based on Monte Carlo mismatch simulations, a mixer with an IIP2 over +70 dBm was achieved in [33] with actual components. In addition, the transconductor of Fig. 4.5c is suitable for low supply voltages. However, it has slightly lower IIP3 compared to the conventional CS transconductor, but the difference decreases with large overdrive voltages [33].

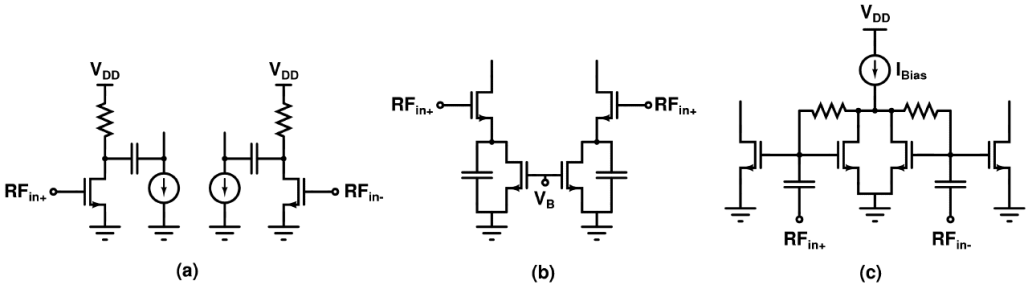


Fig. 4.5. Mixer inputs to minimize the second-order intermodulation: a) ac-coupled input stage, b) degeneration with triode-region FET [32], and c) biasing technique for IM2 cancellation [33].

4.3.3 Switch quad

After the input transconductance stage, the RF signal is fed to a switching quad, which performs the frequency translation. The performance of the switch quad is crucial with regard to the gain and noise of mixers. A switch quad typically causes additional loss due to frequency conversion. In addition to loss, the switch transistors generate thermal noise in a way similar to other active components [29]. In DCRs, where the signal is directly transferred to the intermediate frequency, the challenge of CMOS switching transistors is the high intrinsic flicker noise [23], [29]. Furthermore, although the linearity of the input transconductor is typically the dominant nonlinearity source of the mixer, also the switch quad nonlinearity should be taken into account [34].

4.3.3.1 Conversion gain

An example of a simple mixer LO pair and transistor M_1 and M_2 currents versus LO voltage are shown in Fig. 4.6. When there is no LO signal, i.e. $V_{LO} = 0$, the bias current is evenly shared between M_1 and M_2. When the switch pair is excited by an LO voltage V_{LO}, the tail current is steered to either of the branches. For the following simulation example, the transistors M_1 and M_2 are replaced with voltage-controlled current sources obeying classical long-channel transistor equations, i.e.

$$I_D = \begin{cases} k_n \left(V_{GS} - V_T\right)^2, V_{GS} > V_T, V_{DS} \geq V_{GS} - V_T \\ 2k_n \left[\left(V_{GS} - V_T\right) V_{DS} - \frac{1}{2} V_{DS}^2 \right], V_{GS} > V_T, V_{DS} \leq V_{GS} - V_T \\ 0, V_{GS} < V_T \end{cases} \quad (4.1)$$

The design values of $k_n = 30$ mA/V^2 and $V_T = 0.4$ V were chosen[7]. The drain current of LO pair transistor M_1 is shown in Fig. 4.6 relative to I_{bias} for cases, where the overdrive (V_{gs}–V_T) voltages are set to 50 mV, 100 mV, and 200 mV and the LO signal amplitude is swept. The drain-source voltage is approximately 600 mV. As can be seen, the required differential LO amplitude should be at least $\sqrt{2}$ times the overdrive voltage to completely drive the bias current to either of the branches. In that case, the other transistor of the LO pair acts as a cascode device and the other transistor is switched off.

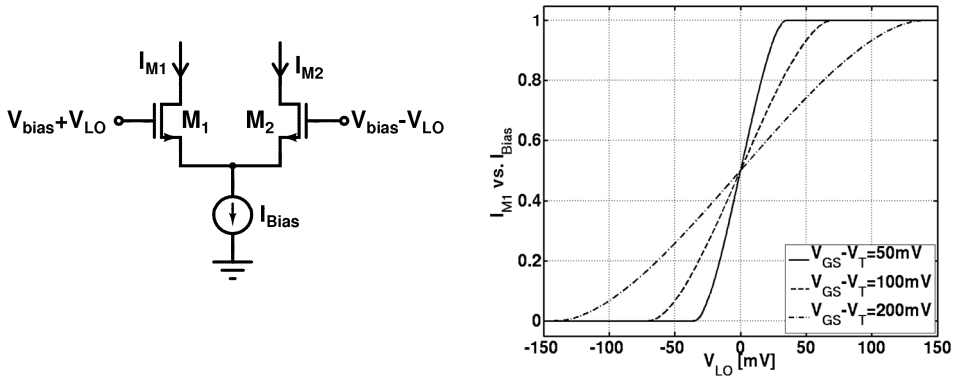


Fig. 4.6. Mixer LO pair and transistor M_1 and M_2 currents relative to I_{bias} versus LO amplitude.

The quiescent current of switch transistor M_1 is shown in Fig. 4.7 in cases where the LO pair is driven with a sinusoidal LO signal having different amplitudes. The overdrive voltage is set to 100 mV. A solid line shows switching, which is performed with LO signal amplitude that is too low. The transistor is not off at any moment and incomplete switching occurs. With dashed and dashed-dotted lines are shown switching with larger LO voltages. The transition from on to off state is sharper with larger LO amplitude. Fast switching is required to keep the time period, when both transistors are on, as short as possible.

[7] These values do not accurately model any particular transistor in deep submicron CMOS processes. The only purpose of using them is to achieve a simple and useful transistor model for simulation purposes.

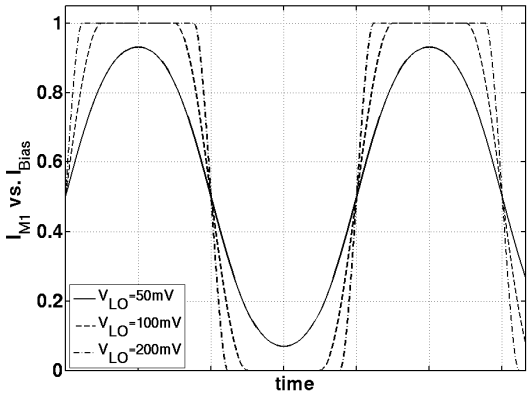


Fig. 4.7. Quiescent current of LO pair transistor M_1 with different LO signal amplitudes.

The conversion gain of the switching quad is calculated by averaging the gain over one period of the LO signal. This is analyzed in literature, for example, in [35] – [38]. For a fundamental RF frequency the conversion gain of a single-balance and double-balanced mixers are given by

$$G_{conv} = \frac{1}{\pi}\sin\left(\frac{\pi\Delta T}{T}\right)\frac{T}{\Delta T}, \tag{4.2}$$

where T is the LO signal period and ΔT is the turn on time. When the LO signal has a typical 50-% duty cycle, i.e. $\Delta T = 0.5T$, the voltage gain of a mixer is given by

$$A_V = \frac{2}{\pi} g_m R_L, \tag{4.3}$$

where g_m is the transconductance of the single input transistor and R_L is the load resistance [23]. As a result, the switching causes conversion loss of 3.9 dB. Equation (4.3) assumes that the LO signal amplitude is large enough for complete switching. A too-low LO signal causes incomplete switching, which increases the conversion loss and noise. Next, the conversion loss of an ideal double-balanced mixer is simulated as a function of LO signal level. The input transistors of a mixer shown in Fig. 4.3 are replaced with ideal voltage-controlled current sources having a constant transconductance and the switch transistors are replaced with voltage-controlled current sources obeying (4.1). The switch quad conversion gain is shown as a function of LO signal amplitude for different overdrive voltages. With increasing overdrive voltages, larger LO amplitude is required to approach the theoretical limit of 3.9 dB loss. When the single-ended LO signal amplitude is equal to overdrive voltage, the conversion loss is approximately 5 dB in this example. Furthermore, as is observed from Fig. 4.8, when the differential LO signal amplitude is $\sqrt{2}$ times the overdrive voltage, the achieved conversion loss is approximately 0.5 dB from the theoretical limit.

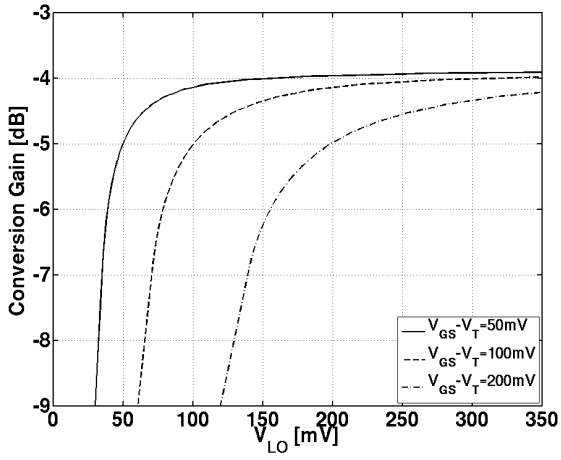


Fig. 4.8. Conversion gain vs. LO signal amplitude with several switch transistor overdrive voltages.

4.3.3.2 Noise and linearity

The noise of commutating mixers is widely presented in the literature, for example, in [28], [29], and [37] – [39]. In the following, the common methods of minimizing the noise of the mixer apply to the LO signal amplitude and shape, device sizing and type, and quiescent current. Clearly, trade-offs between mixer noise and linearity and overall front-end power consumption are encountered.

LO signal amplitude: The noise of the switch transistor can be decreased by raising the amplitude of sinewave LO, which sharpens the transition and minimizes the time when both switches are on [23]. In addition, transition time can be shortened replacing the sine-waveform by a more square-like one [37]. However, if the LO voltage drives the switch transistor deep into triode region, mixer nonlinearity worsens because of the nonlinear output resistance of the transconductance FETs [40]. The rail-to-rail LO signal with short rise and fall times can be achieved by driving the sinusoidal signal through an inverter chain. This, however, can consume a substantial amount of current in the LO signal chain.

Switch sizing: The choice of the size of the switch transistors is a trade-off between the parasitic capacitance for the LO buffers and switching time. For a given LO swing, switch transistors are simultaneously on for a shorter period of time as their width increases [22]. In addition, the spectral density of input-referred noise goes down linearly with MOS transistor gate area [28]. However, increasing the switch transistor gate area is impractical due to the higher parasitic capacitances, which increase the current consumption of the LO buffer. In addition, the capacitance at the source of the switch transistor slows down the switching speed and degrades the SNR [37], [28]. The tail capacitance can be tuned out with the inductor between the transconductor stage and switch quad. As a result, the resonator lowers the effect of the mixer noise [20].

Quiescent current: To minimize the 1/*f* noise, the drain current of the switch transistor should be decreased [28]. However, when the switch transistor drain current is reduced, the impedance seen at the switch transistor sources increases. As a result, more RF current will be shunted by

the parasitic capacitance at the switch transistors' source node, which degrades the signal-to-noise ratio [28]. Therefore, there exists a certain drain current level for 1/*f* and thermal noise optimum, which depends on the used technology and baseband bandwidth. Finally, although the switch quad usually has a minor effect on overall mixer linearity, the linearity of the switch transistor typically worsens along with small quiescent currents [34].

Device type: The 1/*f* noise can also be mitigated by using PMOS switches instead of NMOS ones, as is achieved, for example, in [41] – [44]. The PMOS switch quad is usually used in folded mixers, where the transconductor stage uses NMOS devices. The folded mixers are briefly discussed in Section 4.4.2.

4.3.4 Load design and interface to the baseband

The design of mixer load is important, since in DCRs the mixer load forms the interface to the baseband. The typical voltage-mode load for the mixer is realized with an RC-impedance, as is shown in Fig. 4.9a. The load also acts as a first filtering stage for baseband. The pole improves the mixer out-of-band blocking performance and reduces the out-of-band linearity requirements of the following baseband channel. The mixer and the first stage of the baseband circuitry are usually dc coupled. The ac-coupling between the mixer and baseband is possible in those communications systems where the modulation method allows high-pass filtering. When the dc coupling is utilized, the dc level of the mixer output must be adequate for the following baseband stage. In the case of a double-balanced mixer, if resistive load is used, the switch transistor's dc current I_{swi} and the value of the load resistor R_L are related, i.e.

$$V_{dc,out} = V_{DD} - 2I_{swi}R_L \tag{4.4}$$

To improve the voltage gain of the mixer, for example to suppress the noise contribution of the following blocks, the load resistor value can be increased by adding parallel current sources with the resistors loads as presented in Fig. 4.9b. It should be noted that, in practice, the linearity of the analog baseband circuit limits the value of R_L [45]. In addition, the largest voltage swing in the front-end is typically achieved at the mixer output node (assuming a voltage mode operation). Thus, the maximum achievable voltage swing can be limited by the available voltage headroom and the signal clipping at the mixer output can dominate the front-end compression point. The mixer load can be also realized with floating resistors, as is shown in Fig. 4.9c [36]. The PMOS current sources provide the dc current to the mixer. The current sources, however, add new noise sources to the mixer output. The optimum resistor value and mixer load design is analyzed in, for example, [45].

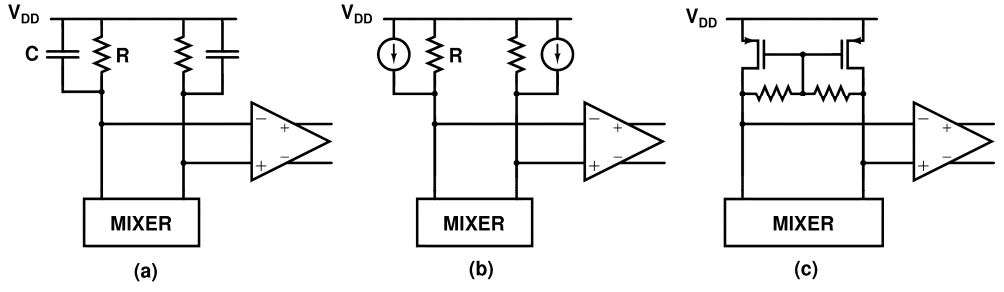


Fig. 4.9. Different voltage-mode mixer load structures, a) RC-impedance, b) parallel resistor and current source, and c) floating resistors with PMOS current sources.

The mixer can be designed in current mode, i.e. to drive low-impedance node, as is shown in Fig. 4.10. This can be achieved by connecting the mixer outputs to the virtual grounds of the operational amplifier (op-amp), as is shown in Fig. 4.10a [44], [47], [48]. Then, the IF output operates in current-mode instead of voltage mode and the voltage swing at the output is very small. Since the output voltage signal modulating the switch transistor is significantly decreased, the nonlinearity of the switches is minimized and the blocking performance of the mixer is improved. The current-mode interfaces are suitable for low-voltage applications, since there is no voltage signal at the mixer output [45].

The cascode or folded cascode transistors can be used to implement a current-mode interface [45]. An example of such an interface is shown in Fig. 4.10b [P1]. Compared to the topology shown in Fig. 4.10a, the folded cascode topology requires larger current through the current source I_B, thus increasing noise. However, the structure shown in Fig. 4.10b is implemented without op-amp and low power consumption can be achieved in mixer-baseband interface.

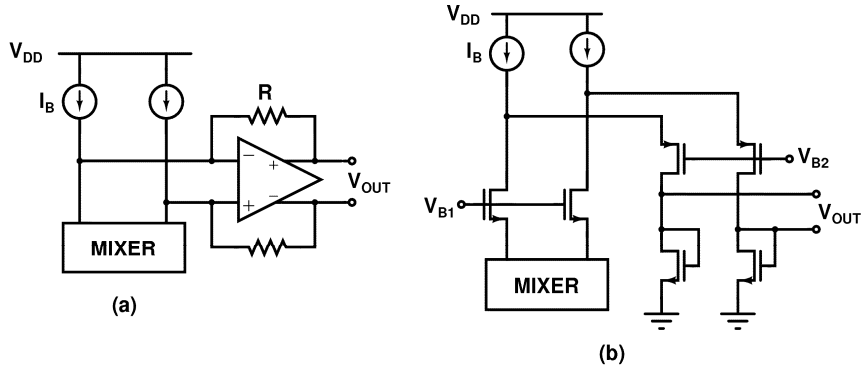


Fig. 4.10. Current-mode interfaces using a) an op-amp [47] and b) folded cascode transistors [P1].

4.4 Active mixer design techniques and alternatives

In the following, several mixer design options are presented. First, two alternatives to realize the quadrature mixer are presented and compared. Then, folded mixers and a mixer utilizing current boosting are discussed. Finally, mixers merged with the LNA are briefly described.

4.4.1 Quadrature mixers

In typical receivers, the downconversion to zero or IF frequency is usually performed with quadrature (I/Q) mixers. For I/Q-mixers, there are different possibilities to implement the interface between input transconductor and switch quad. The first topology is shown in Fig. 4.11. The RF signal is inputted to two separate input stages, which drive the switch quads of their own. Another possibility is to utilize a single input stage, which drives both switch quads, as is shown in Fig. 4.12.

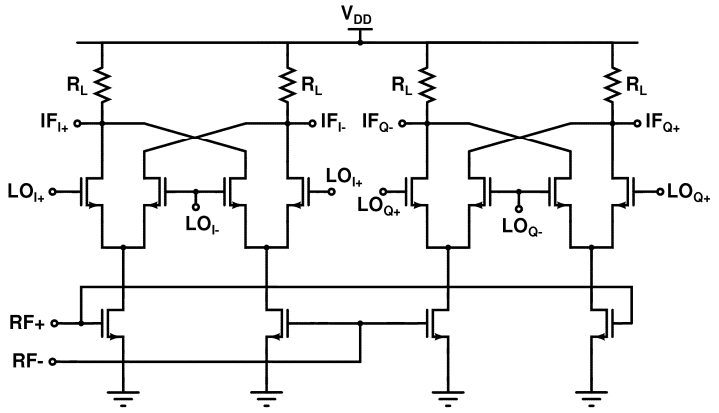


Fig. 4.11. Two separate Gilbert mixers driven by quadrature LO signals.

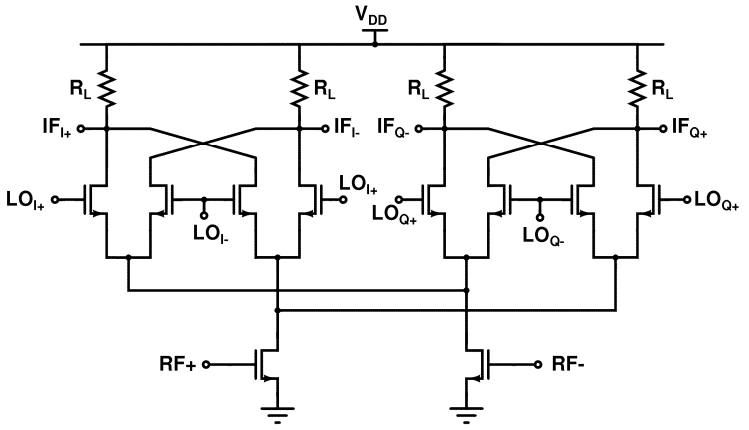
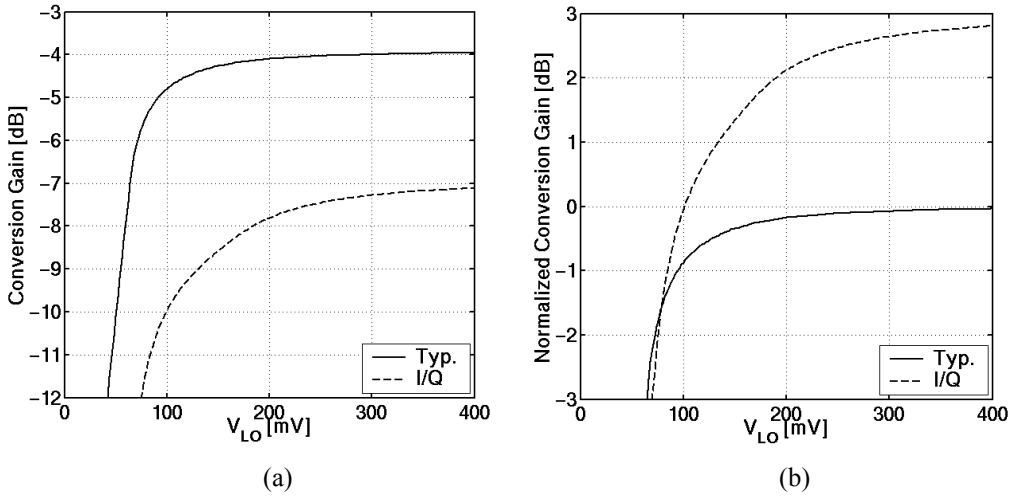


Fig. 4.12. Quadrature mixer with single input stage.

The conversion loss of a typical mixer and the one driving quadrature switch quads is shown in Fig. 4.13a. For that simulation, ideal mixers having an ideal input transconductor and switch transistor obeying (4.1) were used. The quiescent current of the switch transistor is 250 μA. The conversion loss is plotted as a function of the LO amplitude. The value of the input transconductance is equal for both mixers. Since the transconductor of the mixer shown in Fig. 4.12 drives both switch quads, the conversion gain is by $\sqrt{2}$, i.e. 3 dB lower than the that of a basic Gilbert cell mixer of Fig. 4.11. In addition, complete switching requires larger LO amplitude when quadrature switch quads are driven from a single transconductor.

However, the comparison shown in Fig. 4.13a is not fair, since the drain current of the input stage of I/Q mixer of Fig. 4.12 is double compared to the ones of Fig. 4.11. Therefore, with reasonable accuracy, the size of the input transistor can be doubled to achieve equal capacitive loading for the preceding stage and overdrive voltage equal to the ones in Fig. 4.11. As a result, the transconductance of input devices in Fig. 4.12 can be doubled. The corresponding comparison is shown in Fig. 4.13b. The conversion gains are normalized such that the conversion gain of a typical switch quad is 0 dB. As a result, with equal current consumption and capacitive loading for the preceding stage, the better conversion gain can be achieved with the quadrature mixer.

When the noise of the transconductors is considered, the quadrature mixer has a 3-dB advantage over a pair of typical mixers [49]. However, the quadrature mixer probably has a noise disadvantage due to the noise of the switch quads, i.e. noise from Q-branch can be observed at the output of I-branch, and vice versa. In addition, parasitic capacitance at the node between the transconductor and switch quad is expected to be larger in Fig. 4.12 than in Fig. 4.11 resulting in worsened SNR. The fair comparison of noise and linearity performance of mixers shown in Fig. 4.11 and Fig. 4.12 is nontrivial, since the mixing performance depends on the dimensioning and biasing of switch transistors, used LO signal level, and device matching. Which mixer structure alternative should be chosen depends heavily on the used circuit configuration and requirements.



(a) (b)

Fig. 4.13. a) Conversion gain of a typical Gilbert cell mixer (solid line) and the mixer driving quadrature switch quads (dashed line). b) Conversion gain of a typical mixer is normalized to 0 dB and the transconductance of I/Q mixer is doubled compared to a).

For extremely low-power applications, for example [21] and [P1], the quadrature mixer shown in Fig. 4.12 is a preferred option, since the desired conversion gain is achieved with the smaller current consumption. In addition, on-chip inductors can be used as a part of downconversion mixers, for example to optimize the noise of the mixer [20] or to realize the high-impedance LC resonator load for the folded mixer (see, for example, Fig. 4.14b). Then, separate transconductor stages would require on-chip inductors of their own, which would result in increased layout area and complicated floor planning.

4.4.2 Folded mixers

In a typical Gilbert cell mixer, input stage, switching stage, and load are stacked. Due to shrinking supply voltages, the implementation of such a mixer is challenging, because all stages require sufficient voltage headroom to achieve adequate performance. This can be mitigated by using folded mixer structures, as shown in Fig. 4.14. In addition, since the dc current of both the transconductor and switch stages can be adjusted separately, the gain, linearity, and noise performance of both stages can be optimized separately.

High impedance needed for folding is obtained either with current sources, as in [50] and [51] (Fig. 4.14a), or by LC resonator tuned at the center frequency [24], [44], [52] (Fig. 4.14b). The current sources require voltage headroom for a proper operation and they add noise, but the LC resonator occupies layout area. Since the resonator has high impedance at the wanted frequency and low impedance at other frequencies, the frequency selective performance of the resonator can be used to improve the linearity of the mixer. For example, the standing wave at double LO frequency produced by the mixing pair is attenuated [24]. Thus, the voltage swing across the drain-source terminals of both mixer input stage and switch transistors is lowered, which results in improved IIP3 [44]. Since the resonator has low impedance at the frequency of $|f_{RF1} - f_{RF2}|$, the second-order intermodulation generated by the input stage of the mixer is attenuated. As a result, the IIP2 of the mixer is also improved [52]

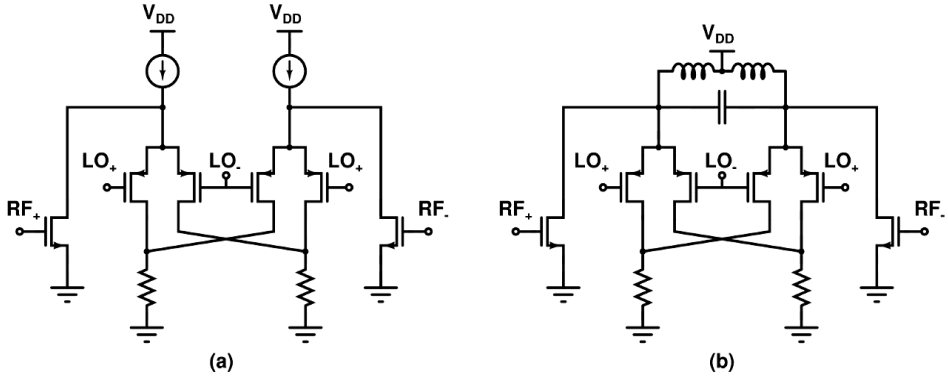


Fig. 4.14. Folded mixer realized with a) current sources, b) LC resonator.

4.4.3 Mixers with current boosting

A current boosting method is utilized in a mixer presented in Fig. 4.15a [53]. The optimum bias for the input stage and switching stage can be optimized separately with current boosting. Due to proper gain and linearity performance, the input transconductance stage should be biased with rather higher current. However, the performance of the switch quad may require quite low current level for optimum operation. With smaller quiescent current, the flicker noise of the switch transistors is lowered, which is important in DCRs. To reduce the LO overdrive required for complete switching, the drain current of switch transistors is reduced. The conversion gain is increased for two principal reasons: the mixer requires a lower LO swing to switch completely and a larger load resistor value can be used to increase the voltage gain. Alternatively, if the load resistor value is kept unchanged, mixer design for lower supply voltages is alleviated with current boosting, since the voltage drop at the resistive load is reduced.

The disadvantage of the switch transistor current reduction is that the impedance seen at the switch transistor sources is raised, which degrades the signal-to-noise ratio, as has been discussed earlier in Section 4.3.3.2. In addition, the boost current source adds noise of its own and increases the mixer white noise figure. However, the overall mixer performance usually benefits from properly designed current boosting.

The current boosting technique can be modified in such a way that the PMOS boost source is used as an additional transconductor, as is shown in Fig. 4.15b [54]. Then, the effective trans-

conductance of the mixer input stage is the combination of transconductances, $g_{m,n1} + g_{m,p2}$. As a result, slightly improved gain and noise properties can be achieved. However, the gain and noise performance improvement depends heavily on the used circuit configuration.

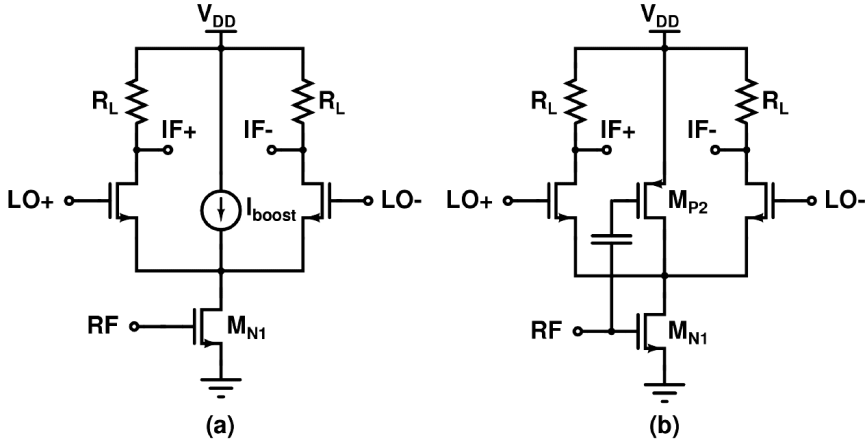


Fig. 4.15. a) Current boosting with constant current source, b) current boosting comprising additional transconductance.

In [55], a mixer with dynamic current injection was presented. Instead of feeding a fixed dc current, the dynamic PMOS current sources inject current only at the switching events. As a result, the flicker noise is reduced. That technique, however, requires a large LO signal swing and good matching between the NMOS dc current sources and PMOS dynamic current sources.

The additional capacitance due to current boosting can be avoided by feeding the boost current through the differential inductor, as shown in Fig. 4.16. In addition, the noise contribution of the boost current source is minimized, since its noise is common mode at the mixer output [P1]. The dc current source I_{boost} can be replaced with active blocks utilized in the receiver, as is discussed in Section 6.3. As a result, the overall current consumption can be reduced efficiently.

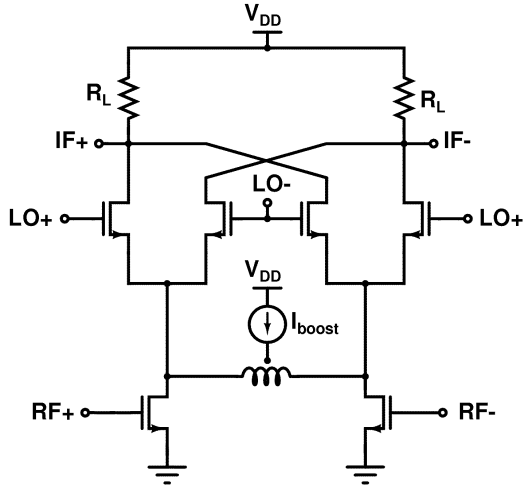


Fig. 4.16. Current boosting to inductor center tap [P1].

4.4.4 Merged LNA and mixer

Fig. 4.17 shows a structure where the LNA and mixer are merged. Compared to separate LNA and mixers, the number of nodes operating at RF frequency can be reduced, which minimizes the current consumption [20]. However, due to the Miller effect, the reverse isolation of this topology is poor and the drain node of the LNA is susceptible to the double-frequency LO beat typically generated by a quadrature switch quad [20]. The reverse isolation can be improved by adding a cascode stage or by using a CG input stage instead [21], [P1]. The problem of the CG input is the high noise figure, since switch transistors act as a low impedance load for the input transistors, and therefore there is only small voltage gain provided before the switch quad. However, the merged CG-LNA and mixer topology is suitable for applications requiring extremely low power consumption.

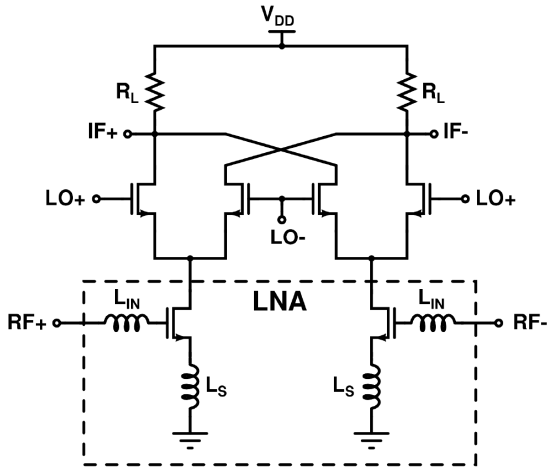


Fig. 4.17. LNA merged with a mixer.

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5 Quadrature signal generation

This chapter concentrates on circuit techniques for quadrature (I/Q) local oscillator (LO) signal generation. The chapter is organized as follows. First, general quadrature signal generation aspects are discussed. Then, the design of frequency dividers is briefly presented. Next, the passive quadrature signal generation structures are described. The main emphasis of this chapter is on the analysis and design of polyphase filters. Since the input LO signal in the experimental circuits presented in Chapter 6 was external, the design aspects of the VCO and PLL are beyond the scope of this thesis. The quadrature LO signal generation by cross-connected VCOs or ring oscillators are directly related to VCO design, and therefore those I/Q signal generation methods are left out of this thesis as well.

5.1 General quadrature signal generation aspects

Quadrature local oscillator signals are required in direct-conversion (and low-IF) receivers to drive downconversion mixers. Most of the modern communication standards utilize phase or frequency modulated signals, which require mixing with in-phase and quadrature signals to prevent information overlapping [1]. Therefore, the generation of quadrature signals is an essential part of the front-end design. In typical receivers, the quadrature phasing is performed on the LO signal path. Quadrature phasing can be implemented on an RF signal path as well [2] – [4]. That method, however, inevitably increases the noise figure of the receive path due to loss caused by the passive network.

There are several techniques to generate the 90° phase shift [5]. Commonly, the in-phase (I) and quadrature-phase (Q) signals are generated with passive phase shifter [6], divide-by-two circuit [7], or cross-coupled VCOs [8]. The selection of the applied quadrature signal generation method depends on the targeted system, selected radio architecture, and applied IC process. The quadrature signals always experience some imbalance due to mismatches among the active and passive components and due to the layout of the circuit as well. Amplitude and phase balance of the generated I and Q signals affect the image rejection of the receiver and thus the quality of reception.

Despite the applied quadrature signal generation method, the LO buffers are typically needed to drive the mixers. LO buffers are used to minimize the amplitude imbalance between I and Q LO signal branches and to compensate for loss caused by passive phase shifters, for example. In addition, the frequency dividers usually are sensitive to capacitive loading and cannot directly drive the gate capacitance of the mixer switch transistor. There are several ways to implement LO buffers. For example, an LO signal having a large swing can be achieved by using simple CMOS inverters. In general, the typical amplifier structures presented in LNA and mixer chapters apply as LO buffers, as well. The design of LO buffers is not covered in detail in this thesis. Nevertheless, a couple of implemented LO buffers are presented in Chapter 6. In a well-designed LO buffer special attention is paid to guaranteeing operation with large-amplitude signals. When the signal at the LO buffer input is increased, the LO swing will be eventually saturated to a certain level either due to compression of the transconductance stage or signal clipping at the buffer output. The achieved LO buffer output swing should be large enough for

proper mixer switching performance. This can be challenging to achieve with low current levels and thus the LO buffers can carry a significant part of the whole receiver current consumption.

5.2 Static frequency dividers

The frequency dividers (divide-by-2) are widely used to generate quadrature signals. The static divide-by-2 circuits are based on the cross-connected master-slave D-latch configuration presented in Fig. 5.1, see, for example, [7], [9] – [20]. When the differential input signal has a 50-% duty cycle, the output signals have 90° phase difference.

The advantage of the frequency dividers as quadrature generation circuits is that they provide a large output amplitude swing. In addition, static frequency dividers can operate from dc to the maximum toggle frequency. The maximum operation frequencies of different frequency dividers are studied in, for example, [10]. By using a frequency divider the LO signal is not at the same frequency as the RF signal, which reduces the LO leakage and LO pulling in DCRs [7]. As a drawback, the current consumption of the divider becomes large if high operational frequency is needed. Due to device mismatches the output swings of the I and Q branches may have amplitude and phase imbalance.

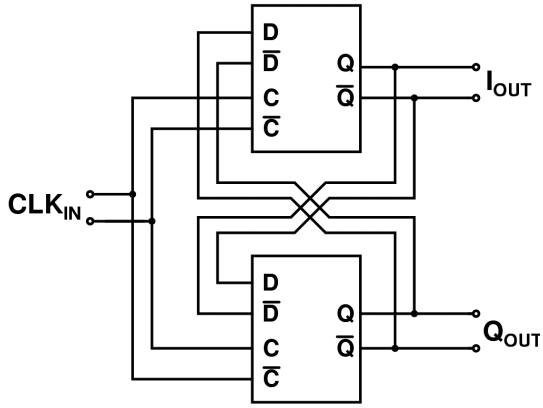

Fig. 5.1. Block diagram of static divide-by-two circuit.

5.2.1 D-latch structures

A typical D-latch circuit diagram is presented in Fig. 5.2a. A source-coupled logic (SCL) latch consists of an input tracking stage, where M_{N1} and M_{N2} are utilized to sense and track the data variation, while a cross-coupled regenerative pair formed by M_{N3} and M_{N4} is used to store the data [11]. The operation mode of the latch is determined by the input signal (CLK_{IN}) driving the input differential pair M_{N5} and M_{N6}. With a high clock period, the tail current entirely flows to the tracking circuit and vice versa. Typically, NMOS devices are utilized because of their higher speed compared to PMOS transistors [12].

Nowadays, the realization of the latch presented in Fig. 5.2a can be challenging with the low supply voltages, since three transistors and a resistive load are stacked. The supply voltage limitation can be mitigated by removing the tail current source M_{N7} as shown in Fig. 5.2b [13].

In that case, however, the drain currents of the clocked transistors are defined by the clock signal. Without a constant current source, the amplitude of the clock signal decides the currents in the latch circuit, which also affect the output voltage swing and power consumption [13]. Since the static dc point is not well defined, the total current of the divider fluctuates in time and unpredictable output swings can result [7], [14]. In addition, one possibility to design a low-voltage latch is to utilize inductive loading instead of resistive load [15].

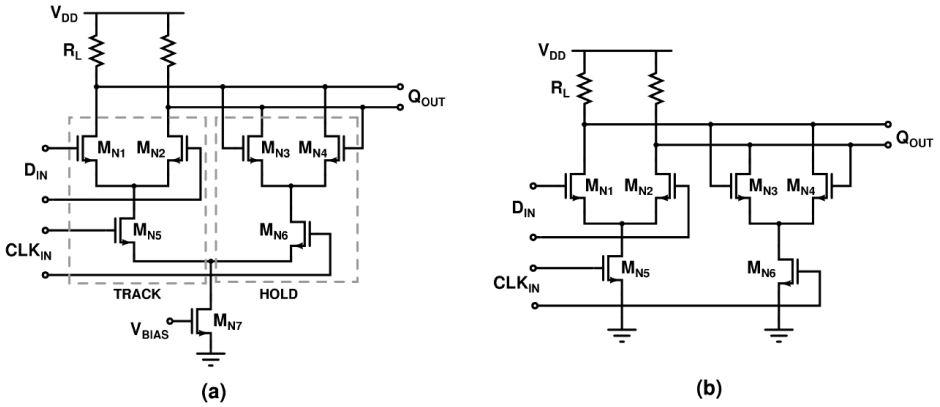

Fig. 5.2. Schematic of a CMOS latch a) with tail current source, b) without tail current source.

A low-voltage D-latch can also be implemented by shifting the clocked transistors as shown in Fig. 5.3a [16]. Due to tail current sources, the operation of the clocked transistors M_{N5} and M_{N6} and tracking (M_{N1}, M_{N2}) and holding (M_{N3}, M_{N4}) transistors is better controlled than the latch of Fig. 5.2b. When CLK is high, M_{N5} steers all the tail current from M_{N7}. Then, M_{N1} and M_{N2} are off and the latch is in the hold mode. When CLK signal is low, the reverse occurs. However, when CLK is low, M_{N5} is not completely off, and part of the tail current of M_{N7} flows through M_{N5} and loading of the output RC node through M_{N1} or M_{N2} is insufficient. To improve the operation in tracking mode, resistor R_{L2} shown in Fig. 5.3b can be added to steer a larger part of the tail current to either M_{N1} or M_{N2}.

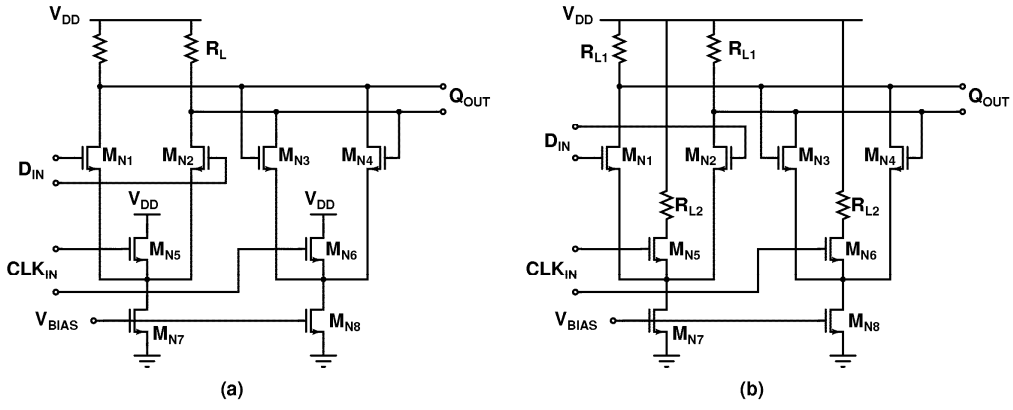

Fig. 5.3. a) Low-voltage latch, b) low-voltage latch with improved tracking mode operation.

The maximum operational speed of a latch shown in Fig. 5.2a is limited by tracking mode, and therefore the tail current must be sufficiently high [11]. The performance of the latch can be improved, for example, by using separate tail currents for tracking and latching circuits [11]. In addition, the divider speed can be improved with the dynamic loading shown in Fig. 5.4 [17], [18]. The PMOS transistors M_{P1} and M_{P2} are used as dynamic loads by varying their resistance with clock signals [18]. When the CLK signal is high, M_{N5} is turned on and PMOS load devices are operated in the linear region and have small impedance. As a result, the output RC time constant is small and the tracking speed is maximized. When CLK is low, PMOS devices have a small gate-to-source voltage (cut-off region) thus having larger impedance. Then, the RC time constant is large and maximum gain is achieved for latching mode.

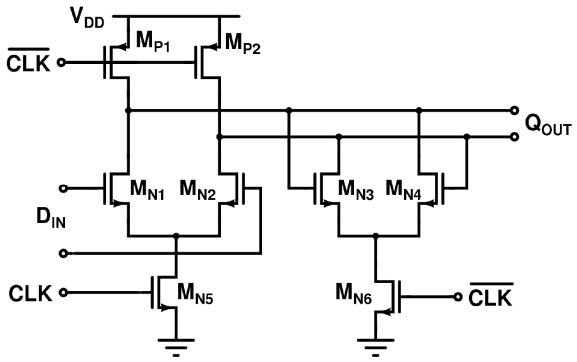

Fig. 5.4. Latch utilizing dynamic load [18].

Another resistorless frequency divider utilizing only two stacked transistors is presented in Fig. 5.5a [19]. When CLK is high, M_{N5} and M_{N6} are off and the master latch is in the sense mode and the slave is in the store mode. Having only two stacked transistors, this topology can be useful in designs with low supply voltage. Since all devices are connected to the output node, the maximum operational frequency is limited. To improve the toggle speed, the store transistors M_{N3} and M_{N4} can be stacked above data transistors M_{N1} and M_{N2} as is shown in Fig. 5.5b [20].

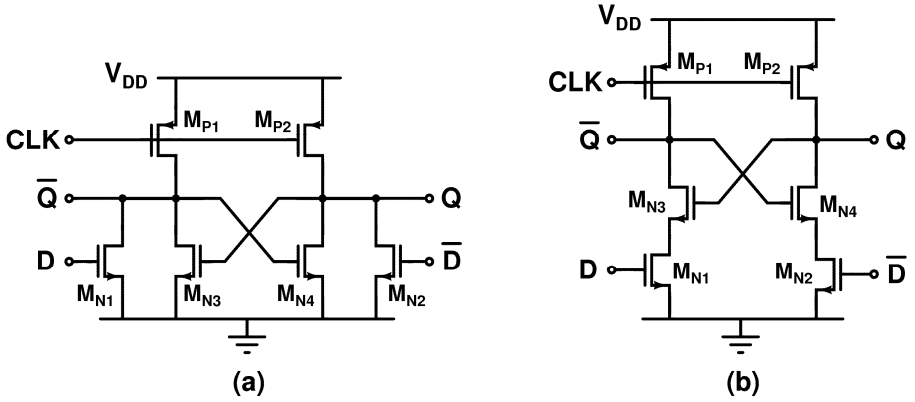

Fig. 5.5. a) Schematic of a low supply voltage D-latch [19], b) D-latch with smaller output capacitance [20].

5.3 Dynamic frequency dividers

In addition, a class of dynamic or regenerative dividers is presented in the literature, for example in [21] – [26]. The principle of regenerative frequency division is shown in Fig. 5.6 [21]. The double-frequency input signal is fed to the mixer, which is followed by a low-pass filter and an amplifier. The output signal of the mixer contains the frequency f_{LO} and its harmonics $3f_{LO}$, $5f_{LO}$, … [10]. When the input frequency f_{in} is high enough, the lowpass filter removes the high-order components and the output signal f_{LO} is fed back to the second mixer input. Without low-pass filtering the divider could lock to an undesired frequency. However, since the frequency response of the active mixer conversion gain shows low-pass behavior, an additional filter is not required [22]. The maximum toggle frequency of a dynamic divider is higher than that of a static frequency divider [10]. The disadvantage of regenerative frequency dividers is that they have a minimum operation frequency. This is determined by the input frequency at which the sum frequency at the mixer output, $f_{in} + f_{out}$, passes the low-pass filter [23].

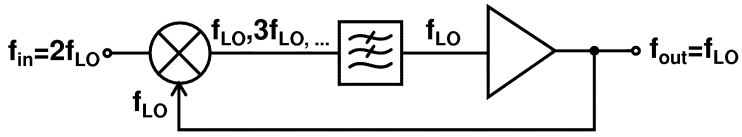

Fig. 5.6. Principle of regenerative frequency divider.

The basic regenerative divider shown in Fig. 5.6 does not provide quadrature outputs. To achieve divide-by-2 with quadrature outputs, the regenerative divider requires two mixers connected as shown in Fig. 5.7a. A positive feedback loop is created such that each multiplier stage contributes 90 degrees of phase shift to the divided output signal [24]. Although higher toggle frequency can be achieved with dynamic dividers with lower power consumption compared to static dividers [10], they are quite seldom used as quadrature signal generators. A few design examples can be found, for example in [25] and [26]. In both designs, bias tuning is needed to control the phase difference between I- and Q-outputs. The schematic of a CMOS dynamic divider similar to the one designed with bipolar devices in [25] is shown in Fig. 5.7b.

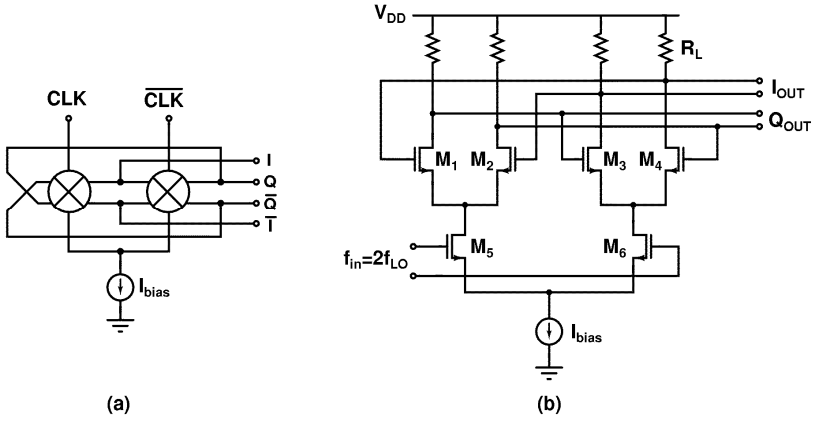

Fig. 5.7. a) Dynamic divider with quadrature outputs [24], b) its CMOS implementation example.

5.4 First-order RC-CR networks

The first-order RC-CR network capable of providing 90° phase shift is presented in Fig. 5.8a. The ratio of the I and Q output signals is

$$\frac{\Delta V_{Iout}(s)}{\Delta V_{Qout}(s)} = \frac{1}{sRC}. \tag{5.1}$$

Therefore, the phase difference between I and Q outputs is exactly 90° with all frequencies, but the outputs are balanced only at a single frequency of $\omega = 1/RC$. Thus, the equal amplitude frequency shifts if the absolute value of RC varies due to process and temperature.

Another RC-CR network is shown in Fig. 5.8b [30], [31]. The ratio of I and Q outputs is

$$\frac{\Delta V_{Iout}(s)}{\Delta V_{Qout}(s)} = \frac{1-sRC}{1+sRC}. \tag{5.2}$$

Thus, the amplitude balance is unity at all frequencies, but the phase has exactly 90° difference only at $\omega = 1/RC$. In practical RF IC realizations, both networks are quite useless due to the limited amplitude or phase accuracy. The amplitude balance can be improved by, for example, using a limiting amplifier after the RC-CR networks. A better amplitude or phase balance can be achieved by cascading polyphase filters, as is discussed in the next section.

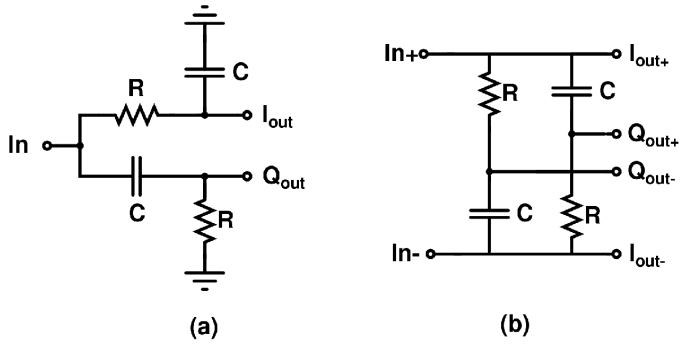

Fig. 5.8. a) Constant phase RC-CR network, b) constant amplitude RC-CR network.

5.5 Passive polyphase filters

Passive polyphase RC filters for quadrature generation was originally proposed by Gingell in the 1970s [32]. Passive polyphase filter (PPFs) IC realizations have been published since 1995 [6]. However, their detailed analysis in the literature is still limited [32] – [43] and explicit formulas given do not cover all relevant issues. In this section, the characteristics of an *n*-stage polyphase RC network are thoroughly discussed. For example, the transfer functions, frequency responses, image rejection, and loss are analyzed in detail. Based on this analysis design guidelines for optimum configuration and dimensioning will be presented. In addition, the impact of device tolerances and the effect of parasitic capacitance will be considered. The presented analysis is mainly focused on PPFs with a maximum of three stages, because the PPFs implemented on IC seldom have more stages. The equations can be derived for higher order PPFs too with the methods presented in this section.

Based on the input signal feeding technique two variants of PPFs can be separated. These are depicted in Fig. 5.9 and Fig. 5.10. In this thesis, these variants are called Type I and Type II PPF, respectively[8]. Since this slight change on input feeding has significant impact on the PPF performance, the analysis of both variants is carried out throughout the text. The material presented here is based on publication [P7].

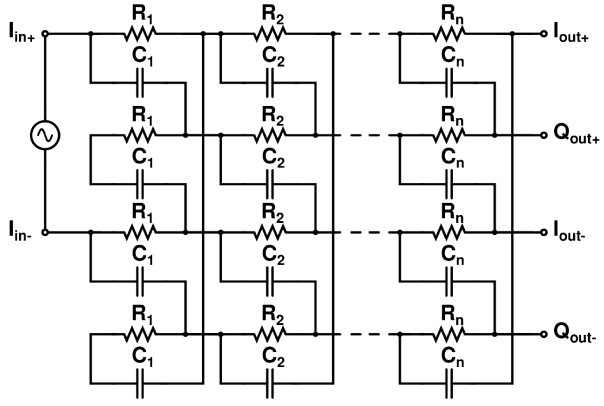

Fig. 5.9. Type I polyphase filter.

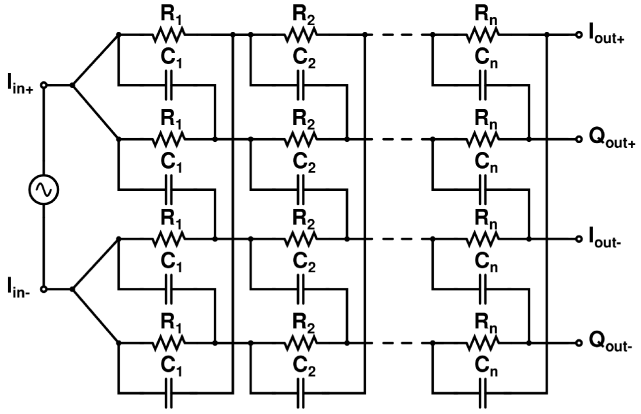

Fig. 5.10. Type II polyphase filter.

5.5.1 Introduction to the analysis of polyphase filters

The analysis of polyphase filters starts by calculating the output signals and the frequency responses of a single PPF stage. An n^{th} stage of a polyphase filter is shown in Fig. 5.11a. The output is loaded with impedance Z_{Ln} representing the input impedance of the following stage. This can be a next PPF stage, a mixer switch, or an amplifier input.

[8] As far as the author is aware, there are no standard names for the PPF structures. The purpose is not to give names for the two PPF topologies, but a short legend is needed to be able to separate the two structures in some way.

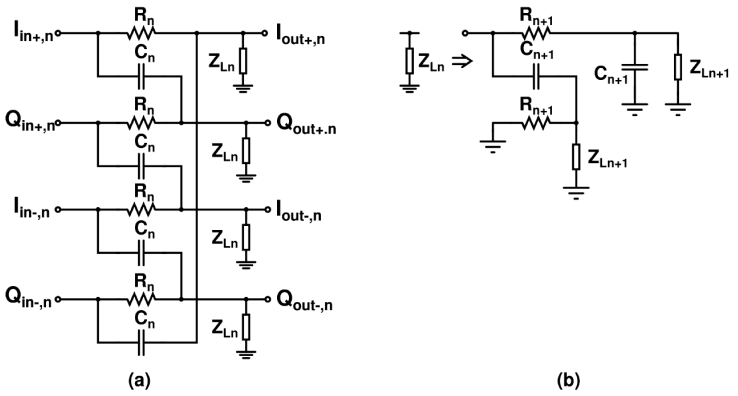

Fig. 5.11. a) An n^{th} PPF stage with output load impedance Z_{Ln}, b) load impedance of n^{th} PPF stage, when the load is a next PPF stage. Z_{Ln+1} represents the loading of the n+1th stage.

When a balanced input signal is applied to I input, the Q input nodes are virtual grounds whatever the source impedance is, and vice versa. When the load is the next PPF stage, the load impedance Z_{Ln} is presented with an equivalent circuit shown in Fig. 5.11b. The output voltages of n^{th} PPF stage shown in Fig. 5.11a can be calculated by voltage division and superposition rules. For example, the output node voltage $I_{out+,n}$ is calculated as follows

$$V_{Iout+,n} = V_{Iin+,n}\frac{\left(sC_n\right)^{-1} \| Z_{Ln}}{R_n + \left(sC_n\right)^{-1} \| Z_{Ln}} + V_{Qin-,n}\frac{R_n \| Z_{Ln}}{\left(sC_n\right)^{-1} + R_n \| Z_{Ln}}. \tag{5.3}$$

The first right-hand side term is achieved by applying the voltage signal to the input node $I_{in+,n}$ and grounding all the other inputs. Thus, the capacitor C_n connected to the input node $Q_{in-,n}$ is in parallel with the load impedance Z_{Ln} of the output node $I_{out+,n}$. The resulting output signal is calculated with voltage division. The other output voltages can be calculated similarly. In the general case, when each output node is loaded with impedance Z_{Ln}, the differential I- and Q-output signals are

$$\Delta V_{Iout,n} = \frac{Z_{Ln}}{R_n + Z_{Ln} + sR_nC_nZ_{Ln}}\left(\Delta V_{Iin,n} - sC_nR_n\Delta V_{Qin,n}\right), \tag{5.4}$$

$$\Delta V_{Qout,n} = \frac{Z_{Ln}}{R_n + Z_{Ln} + sR_nC_nZ_{Ln}}\left(sC_nR_n\Delta V_{Iin,n} + \Delta V_{Qin,n}\right), \tag{5.5}$$

respectively. Equations (5.4) and (5.5) are then represented in an useful matrix notation.

$$\begin{bmatrix}\Delta V_{Iout,n}\\ \Delta V_{Qout,n}\end{bmatrix} = \frac{Z_{Ln}}{R_n + Z_{Ln} + sC_nR_nZ_{Ln}}\begin{bmatrix}1 & -sC_nR_n\\ sC_nR_n & 1\end{bmatrix}\begin{bmatrix}\Delta V_{Iin.n}\\ \Delta V_{Qin.n}\end{bmatrix} \tag{5.6}$$

When the n^{th} PPF stage is followed by a subsequent PPF stage, the input impedance of stage n+1 acts as the load Z_{Ln}. From Fig. 5.11b, the equivalent load impedance Z_{Ln} for stage n can be calculated as

$$Z_{Ln} = \frac{R_{n+1} + Z_{Ln+1} + sC_{n+1}R_{n+1}Z_{Ln+1}}{1 + sC_{n+1}\left(R_{n+1} + 2Z_{Ln+1}\right)}. \tag{5.7}$$

R_{n+1}, C_{n+1}, and Z_{Ln}+1 are the resistor values, capacitor values, and the load impedance of the n+1th stage, respectively.

5.5.2 About PPF topologies, terminology, and notation

The manner of feeding the input signal to the first stage affects the operation of the PPF. In the case shown in Fig. 5.9, the Q-inputs of the first stage are signal grounds, i.e. $\Delta V_{Qin,1} = 0$. In Fig. 5.10 the input signal is injected in a dual-feed manner, i.e. $\Delta V_{Qin,1} = \Delta V_{Iin,1}$. For the rest of this paper, the former topology is referred to as Type I PPF and the latter topology as Type II PPF. In the following equations, the upper index $(\,)^{I}$ or $(\,)^{II}$ is used to indicate the type of the PPF.

5.5.3 PPF frequency responses and balances

The output voltages of an n-stage PPF can be calculated by multiplying the matrix (5.6) of each PPF stage, and by using (5.7) when taking into account the effect of the load of the next stage. At first, differential output voltages of a single-stage PPF Type I are calculated as

$$\Delta V_{Iout}^{I}(s) = \frac{Z_{L1}}{R_1 + Z_{L1} + sR_1C_1Z_{L1}} \Delta V_{Iin}^{I}(s), \tag{5.8}$$

$$\Delta V_{Qout}^{I}(s) = \frac{sR_1C_1Z_{L1}}{R_1 + Z_{L1} + sR_1C_1Z_{L1}} \Delta V_{Iin}^{I}(s). \tag{5.9}$$

The ratio between I and Q output signals is

$$\frac{\Delta V_{Iout}^{I}(s)}{\Delta V_{Qout}^{I}(s)} = \frac{1}{sR_1C_1}. \tag{5.10}$$

According to (5.10), the output signals have exactly the same magnitude at the single angular frequency of $\omega_1 = 1/R_1C_1$. Furthermore, (5.10) is purely imaginary ($s = i\omega$). Thus, the phase difference between I and Q outputs is exactly 90° with all frequencies and with all R_1 and C_1 values. In addition, the result is independent of the load impedance if identical load impedance at every output node is assumed.

A wider amplitude balance with Type I PFF is achieved by cascading several stages. For example, the transfer functions of I and Q channels of a two-stage Type I PPF are calculated with (5.6):

$$H_{2-stg,I}^{I}(s) = \frac{\Delta V_{Iout}^{I}}{\Delta V_{Iin}^{I}} = \frac{Z_{L1}Z_{L2}\left(1 - s^2C_1R_1C_2R_2\right)}{\left(R_1 + Z_{L1} + sC_1R_1Z_{L1}\right)\left(R_2 + Z_{L2} + sC_2R_2Z_{L2}\right)}, \tag{5.11}$$

$$H_{2-stg,Q}^{I}(s) = \frac{\Delta V_{Qout}^{I}}{\Delta V_{Iin}^{I}} = \frac{Z_{L1}Z_{L2}s\left(C_1R_1 + C_2R_2\right)}{\left(R_1 + Z_{L1} + sC_1R_1Z_{L1}\right)\left(R_2 + Z_{L2} + sC_2R_2Z_{L2}\right)}. \tag{5.12}$$

The amplitude balance then becomes

$$A_{bal,2-stg}^{I} = \frac{\left|H_{2-stg,I}^{I}(s)\right|}{\left|H_{2-stg,Q}^{I}(s)\right|} = \frac{1 + \omega^2R_1C_1R_2C_2}{\omega\left(R_1C_1 + R_2C_2\right)}. \tag{5.13}$$

Thus, unity gain balance is achieved at $\omega_1 = 1/R_1C_1$ and $\omega_2 = 1/R_2C_2$. In addition, the phase balance is always 90° at all frequencies, R and C values, and load impedances. For higher order PPFs the transfer functions can be calculated similarly.

Next, we will repeat the previous analysis for Type II PPF. The output voltages can be calculated in a manner similar to that for Type I PPF but, in this case, the Q input signals are

$V_{Qin+} = V_{Iin+}$ and $V_{Qin-} = V_{Iin-}$ for the first stage. The transfer functions of the single-stage Type II PPF are

$$H_{1-stg,I}^{II}(s) = \frac{Z_{L1}}{R_1 + Z_{L1} + sR_1C_1Z_{L1}}\left(1 - sC_1R_1\right), \tag{5.14}$$

$$H_{1-stg,Q}^{II}(s) = \frac{Z_{L1}}{R_1 + Z_{L1} + sR_1C_1Z_{L1}}\left(1 + sC_1R_1\right). \tag{5.15}$$

The ratio of I and Q outputs is

$$\frac{H_{1-stg,I}^{II}(s)}{H_{1-stg,Q}^{II}(s)} = \frac{1 - sR_1C_1}{1 + sR_1C_1}. \tag{5.16}$$

Thus, the amplitude balance is unity with all component R_1 and C_1 values, all frequencies, and load impedances, but the phase is exactly 90° only at $\omega_1 = 1/R_1C_1$. For a two-stage Type II PPF, the transfer functions are

$$H_{2-stg,I}^{II}(s) = \frac{Z_{L1}Z_{L2}\left(1 - s\left(C_1R_1 + C_2R_2\right) - s^2C_1R_1C_2R_2\right)}{\left(R_1 + Z_{L1} + sC_1R_1Z_{L1}\right)\left(R_2 + Z_{L2} + sC_2R_2Z_{L2}\right)}, \tag{5.17}$$

$$H_{2-stg,Q}^{II}(s) = \frac{Z_{L1}Z_{L2}\left(1 + s\left(C_1R_1 + C_2R_2\right) - s^2C_1R_1C_2R_2\right)}{\left(R_1 + Z_{L1} + sC_1R_1Z_{L1}\right)\left(R_2 + Z_{L2} + sC_2R_2Z_{L2}\right)}. \tag{5.18}$$

The ratio between I and Q outputs is

$$\frac{H_{2-stg,I}^{II}(s)}{H_{2-stg,Q}^{II}(s)} = \frac{1 - s\left(R_1C_1 + R_2C_2\right) - s^2R_1C_1R_2C_2}{1 + s\left(R_1C_1 + R_2C_2\right) - s^2R_1C_1R_2C_2}. \tag{5.19}$$

The previous analyzes can be extended for higher order PPFs as well. It turns out that Type II PPF has always unity amplitude balance and the phase is 90° only at each RC pole. Respectively, Type I PPF has ideal phase balance and amplitude balance is unity at each RC pole frequency.

5.5.4 Image-reject ratio

In this section, image-rejection ratios (IRR) of both PPF topologies are studied. In a receiver context, the IRR is defined as the relation of the desired sideband to the suppression of the image sideband. The IRR was first calculated by Norgaard [43] and it is expressed as

$$IRR = \frac{1 + 2A_{bal}\cos\left(\Delta\theta\right) + A_{bal}{}^2}{1 - 2A_{bal}\cos\left(\Delta\theta\right) + A_{bal}{}^2}. \tag{5.20}$$

In (5.20), A_{bal} and $\Delta\theta$ define the amplitude ratio of I and Q outputs and phase deviation from an ideal 90° between I and Q branches, respectively. The IRR contours (in decibels) are plotted as a function of A_{bal} and $\Delta\theta$ in Fig. 5.12. For example, to achieve an IRR better than 30 dB, A_{bal} and $\Delta\theta$ should be better than 0.55 dB and 3.6°, respectively.

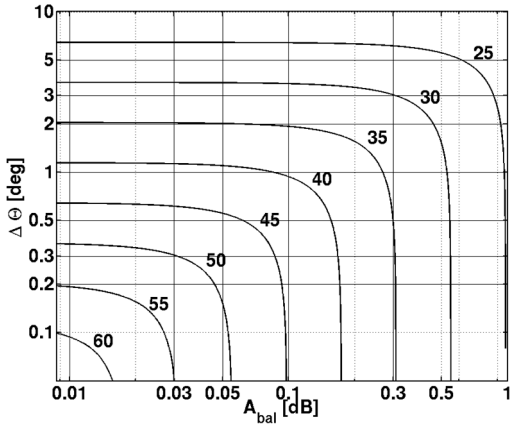

Fig. 5.12. IRR contours (in decibels) as a function of A_{bal} and $\Delta\theta$.

If the IRR is separately defined with magnitude balance (IRR_{gain}) and phase deviation (IRR_{phase}) factors, (5.20) simplifies to

$$IRR_{gain} = IRR_{\Delta\theta=0} = \left(\frac{1+A_{bal}}{1-A_{bal}}\right)^2, \tag{5.21}$$

$$IRR_{phase} = IRR_{A_{bal}=1} = \cot^2\left(\frac{\Delta\theta}{2}\right). \tag{5.22}$$

Thus, the amount of phase and amplitude imbalance provided by a PPF can be converted into equal IRR. Such an IRR is a figure-of-merit for a PPF used for I/Q generation.

This section is divided into two parts. The IRR performances of both PPF topologies with equal and unequal RC pole frequencies are studied separately. In the former case, equal component values are utilized in all filter stages, while, in the latter, the resistor and capacitor values of different stages are adjusted separately.

5.5.4.1 Equal RC poles

Type I PPF has ideal phase response resulting in IRR = IRR_{gain}. Based on (5.10), the amplitude balance is simply $A_{bal} = \omega_1/\omega$, where $\omega_1 = 1/R_1C_1$. According to (5.21), the IRR_{gain} becomes

$$IRR^{I}_{gain,1-stg} = \left(\frac{\omega+\omega_1}{\omega-\omega_1}\right)^2. \tag{5.23}$$

Respectively, Type II PPF has ideal gain balance. Therefore, IRR = IRR_{phase}, and solving the phase of (5.16) and using the definition of (5.22), the IRR_{phase} becomes

$$IRR^{II}_{phase,1-stg} = \cot^2\left[\tfrac{1}{2}\arctan\left(\frac{(\omega-\omega_1)(\omega+\omega_1)}{2\omega\omega_1}\right)\right]. \tag{5.24}$$

It can be proven with trigonometric functions that (5.24) equals (5.23), i.e. the IRR performance is equal for both PPF types. That holds for multi-stage PPFs, too. Although both PPF topologies have equal IRR performance, the choice of PPF type may be eventually constrained by amplitude and phase imbalance specifications required by the system.

According to (5.23) and (5.24), the IRR depends only on pole frequency. Therefore, the IRR of a passive polyphase network cannot be improved by the choice of topology. For the following IRR analysis, (5.23) is used.

PPF stages with equivalent R_1 and C_1 values can be cascaded. The IRR of an n-stage PPF with equal poles is

$$IRR_{gain,n-stg} = \left(\frac{\omega + \omega_1}{\omega - \omega_1} \right)^{2n} . \tag{5.25}$$

The IRRs of PFFs with 1 to 4 stages are depicted in Fig. 5.13, where the frequency axis is scaled with respect to ω_1. The relative bandwidth BW_{rel}, which defines the ratio of maximum and minimum frequencies where a specific IRR is achieved, is shown in Fig. 5.13 and is defined as

$$BW_{rel} = \frac{\omega_{\max}}{\omega_{\min}} . \tag{5.26}$$

The BW_{rel} for an n-stage PPF is calculated as

$$BW_{rel,n-stg} = \left(\frac{IRR^{1/2n} + 1}{IRR^{1/2n} - 1} \right)^2 . \tag{5.27}$$

As a result, the IRR as a function of BW_{rel} becomes

$$IRR = \left(\frac{\sqrt{BW_{rel}} + 1}{\sqrt{BW_{rel}} - 1} \right)^{2n} . \tag{5.28}$$

Equation (5.28) directly relates the targeted IRR, BW_{rel}, and the number of PPF stages together. The IRRs of PPFs with 1 to 4 stages are shown in Fig. 5.14 as a function of relative bandwidth. For example, if the designed PPF should have a BW_{rel} of 2, the minimum IRR increases approximately 15 dB per PPF stage.

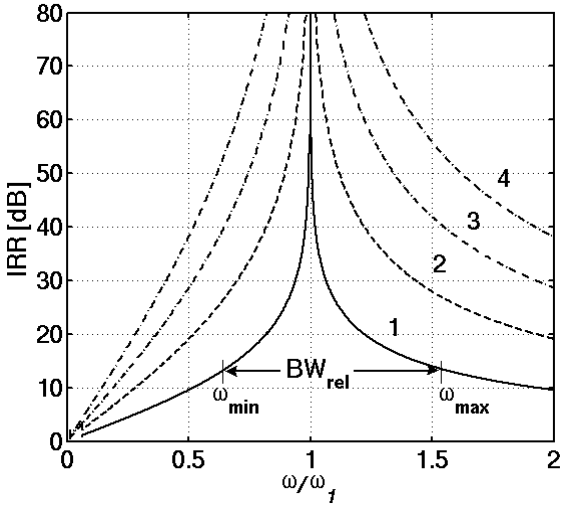

Fig. 5.13. IRR of equal RC pole PPFs with 1 to 4 stages as a function of frequency. The frequency axis is scaled with respect to $\omega_1 = 1/R_1C_1$.

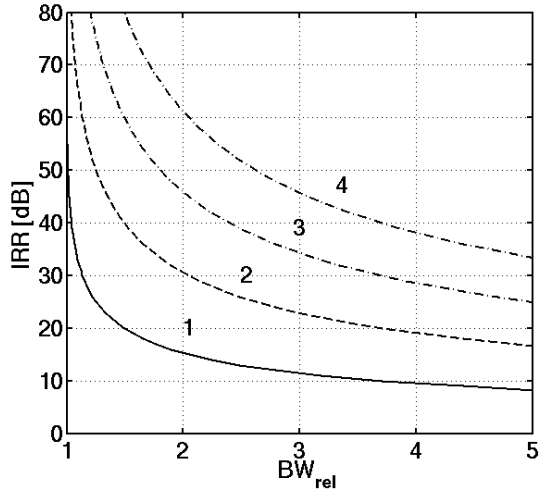

Fig. 5.14. IRR vs. relative bandwidth for 1- to 4-stage PPFs with equal RC pole frequencies.

5.5.4.2 Two-stage PPF with unequal RC poles

The IRR for a two-stage PPF calculated with (5.13) and (5.21) is given by

$$IRR_{2-stg} = \left(\frac{\omega+\omega_1}{\omega-\omega_1}\right)^2\left(\frac{\omega+\omega_2}{\omega-\omega_2}\right)^2, \tag{5.29}$$

where $\omega_1 = 1/R_1C_1$ and $\omega_2 = 1/R_2C_2$. The corresponding curve is plotted in Fig. 5.15.

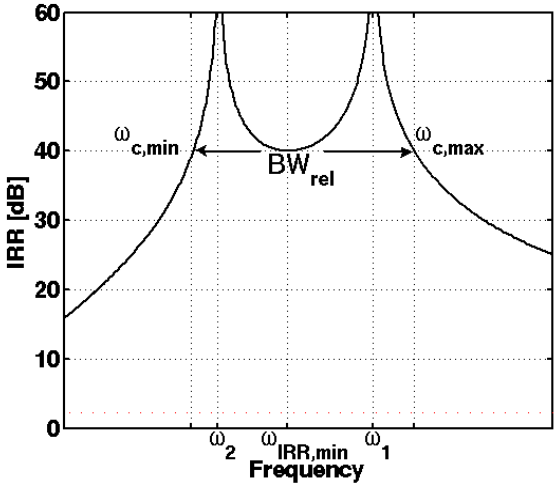

Fig. 5.15. IRR of a 2-stage PPF. According to (5.31), an IRR of 40 dB is achieved with pole-splitting factor $k_2 = 121/81$.

For the following analysis, without losing any generality, the pole frequency ω_1 is assumed to be higher than ω_2. Figure 5.15 depicts that with unequal RC poles there is a minimum IRR (IRR_{min}) locating between ω_1 and ω_2. The minimum IRR frequency is $\omega_{IRR,\min} = 1/\sqrt{R_1C_1R_2C_2}$.

To simplify the following calculations, the ratio of RC poles ω_1 and ω_2 is defined with a pole-splitting factor k_2 as follows:

$$k_2 = \frac{\omega_1}{\omega_2} = \frac{R_2 C_2}{R_1 C_1} > 1 . \tag{5.30}$$

Then, the minimum IRR of a two-stage PPF between ω_1 and ω_2 is expressed as

$$IRR_{\min,2-stg} = \left(\frac{\sqrt{k_2}+1}{\sqrt{k_2}-1} \right)^2 . \tag{5.31}$$

According to (5.29), the IRR depends only on the RC pole frequencies and, according to (5.31), the minimum IRR is defined by the ratio of RC pole frequencies. In the case of equal RC poles (k_2 = 1), (5.31) goes to infinity, since there is no inter-pole minimum. The corner frequencies $\omega_{c,min}$ and $\omega_{c,max}$ define points, where an IRR equal to IRR_{min} is achieved (see Fig. 5.15).

$$\omega_{c,\min\&\max} = \frac{\omega_1}{4} \frac{(k_2+1)^2 \pm (k_2-1)\sqrt{k_2^2+6k_2+1}}{k_2\sqrt{k_2}} \tag{5.32}$$

As a result, the relative bandwidth BW_{rel}, where the minimum IRR is reached, is given by

$$BW_{rel,2-stg} = \frac{\omega_{c,\max}}{\omega_{c,\min}} = \frac{(k_2+1)^2 + (k_2-1)\sqrt{k_2^2+6k_2+1}}{(k_2+1)^2 - (k_2-1)\sqrt{k_2^2+6k_2+1}} . \tag{5.33}$$

Therefore, if BW_{rel} is known, k_2 can be expressed as

$$k_2 = \frac{1 + BW_{rel} + \left(\sqrt{BW_{rel}}-1\right)\left(\sqrt{BW_{rel}+1}\right)}{\sqrt{BW_{rel}}} - 1 . \tag{5.34}$$

The relation between BW_{rel} and minimum IRR according to (5.31) for a two-stage PPF is

$$BW_{rel,2-stg} = \frac{\left(1+\sqrt{IRR}\right)^2 + 2\sqrt{2}IRR^{1/4}\sqrt{IRR+1}}{\left(1+\sqrt{IRR}\right)^2 - 2\sqrt{2}IRR^{1/4}\sqrt{IRR+1}} . \tag{5.35}$$

When comparing (5.35) to (5.27), it can be noted that the BW_{rel} of a 2-stage PPF with unequal poles is always wider compared to a PPF with equal poles. However, the difference decreases if a high IRR is required, because then small pole-splitting factor k_2 is required. For example, with an IRR target of 30 dB and 40 dB, the BW_{rel} of unequal poles is approximately 36 % and 18 % larger than with equal poles, respectively.

5.5.4.3 Three-stage PPF with unequal RC poles

For a three-stage PPF, the IRR as a function of frequency is

$$IRR_{3-stg} = \left(\frac{\omega+\omega_1}{\omega-\omega_1} \right)^2 \left(\frac{\omega+\omega_2}{\omega-\omega_2} \right)^2 \left(\frac{\omega+\omega_3}{\omega-\omega_3} \right)^2 . \tag{5.36}$$

As in the two-stage case, the following analysis assumes $\omega_1 > \omega_2 > \omega_3$. The RC poles ω_2 and ω_3 are related to ω_1 with pole-splitting factors k_2 and k_3. k_2 is defined as in (5.30) and k_3 is

$$k_3 = \frac{\omega_1}{\omega_3} = \frac{R_3 C_3}{R_1 C_1} > 1 \,. \tag{5.37}$$

When (5.36) is plotted, two IRR minimum notches between ω_3 and ω_1 are obtained, as is shown in Fig. 5.16. First, such a relation between k_2 and k_3 is calculated such that the minimum IRR of the two notches are equivalent. The IRR_{min}s are not located at geometric average frequencies of $\sqrt{\omega_1 \omega_2}$ and $\sqrt{\omega_2 \omega_3}$, but at

$$\omega_{IRR\min} = \frac{\omega_1}{\sqrt{2}} \sqrt{\frac{F_1(k_2,k_3) \pm \sqrt{(k_2+1)(k_2+k_3)(k_3+1)\left(F_1(k_2,k_3) - 6k_2k_3\right)}}{k_2 k_3 (k_2 + k_2 k_3 + k_3)}} \,, \tag{5.38}$$

where

$$F_1(k_2,k_3) = k_2(k_2k_3 + k_2 + 1) + k_3(k_2k_3 + k_3 + 1) \,. \tag{5.39}$$

To achieve equivalent IRR_{min}s at those frequencies, there are actually three optimum relations between k_2 and k_3:

$$k_3 = \frac{1}{k_2} \,,\; k_3 = \sqrt{k_2} \text{ , and } k_3 = k_2^2 \,.$$

Based on definitions of pole locations, $k_3 > k_2$ is required and only the last result always obeys this. From here on, the relation according to (5.40) is used in all calculations.

$$k_3 = k_2^2 \tag{5.40}$$

The exact IRR_{min} formula at frequencies according to (5.38) becomes far too complicated to present here, but it can be calculated and included into a design formula set. To simplify the calculations, the IRR minimum presented here is calculated at geometric average of RC poles to achieve a simpler equation. As a result, an IRR minimum of a three-stage PPF is

$$IRR_{\min,3-stg} = \left(\frac{\sqrt{k_2}+1}{\sqrt{k_2}-1}\right)^3 \left(\frac{k_2 - \sqrt{k_2}+1}{k_2 + \sqrt{k_2}+1}\right) . \tag{5.41}$$

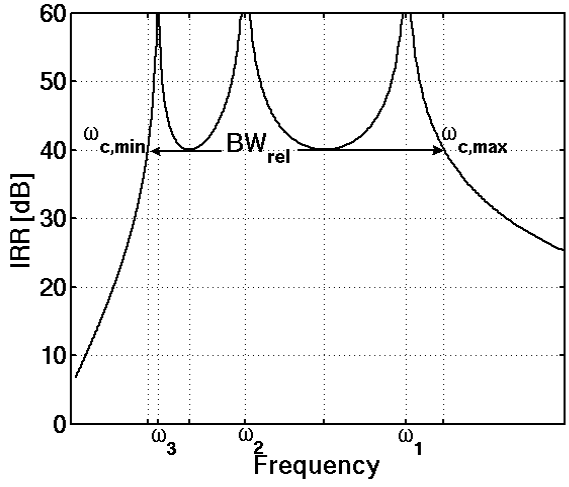

Fig. 5.16. IRR of a 3-stage PPF. An IRR of 40 dB is achieved with pole-splitting factor $k_2 \approx 1.84$ and $k_3 = k_2^2 \approx 3.39$.

Equation (5.41) slightly overestimates the IRR compared to the exact calculated IRR minimum. The maximum error is approximately 0.23 dB when k_2 is close to unity and decreases with a larger k_2. Thus, the error is insignificant and (5.41) can be used to calculate k_2 if the IRR target is known. Due to the lack of a closed-form solution of the quintic formula, k_2 cannot be analytically solved from (5.41). Therefore, a rough value for k_2 can be sketched from Fig. 5.17 or k_2 can be calculated numerically.

Next, the relative bandwidth of a 3-stage PFF is calculated. The frequencies $\omega_{c,min}$ and $\omega_{c,max}$ shown in Fig. 5.16 present corners frequencies, where the IRR_{min} is achieved and are given as

$$\omega_{c,\min} = \frac{\omega_3}{2\sqrt{k_2}} \frac{\left(1+k_2\right)^2\left(1+k_2^2\right) - \sqrt{F_2\left(k_2\right)}}{\left(2+k_2+k_2^2\right)}, \tag{5.42}$$

$$\omega_{c,\max} = \frac{\omega_1}{2k_2\sqrt{k_2}} \frac{\left(1+k_2\right)^2\left(1+k_2^2\right) + \sqrt{F_2\left(k_2\right)}}{\left(1+k_2+2k_2^2\right)}, \tag{5.43}$$

where $\omega_1=1/R_1C_1$, $\omega_3=\omega_1/k_2$, and

$$F_2\left(k_2\right) = 1+4k_2-10k_2^4+4k_2^7+k_2^8. \tag{5.44}$$

The relative bandwidth calculated with (5.42) and (5.43) is approximated with the following formula, so that k_2 can be easily solved if BW_{rel} is known.

$$BW_{rel,3-stg} \approx 2k_2^2 - 1.9k_2 + 0.9 \tag{5.45}$$

Equation (5.45) predicts the exact relative bandwidth with an accuracy better than 1.5 % when $k_2 < 2.8$. The IRR_{min} and the relative bandwidth, where IRR_{min} is covered, are shown as a function of k_2 in Fig. 5.17. For example, to achieve better than 40-dB IRR, k_2 should not exceed 1.84. Then, the BW_{rel} becomes approximately 4.2, which is a significant improvement compared to the BW_{rel} of a two-stage PFF (1.78) with the same IRR.

5.5.4.4 Optimal pole splitting of higher order PPFs

An n-stage PPF with unequal RC poles has n-1 IRR minimum notches. When equivalent IRR_{min}s are targeted, the optimum RC pole frequencies for PFFs having more than three stages are not achieved with a generic formula of $k_n / k_{n-1} = k_2$ (n>3). For example, the calculation of an optimal four-stage PPF is presented in Appendix B.

The IRR and relative bandwidth as a function of k_2 for optimal 2-, 3-, and 4-stage PPFs are presented in Fig. 5.17. Furthermore, the IRR as a function of relative bandwidth for 2-, 3-, and 4-stage PPFs is shown in Fig. 5.18.

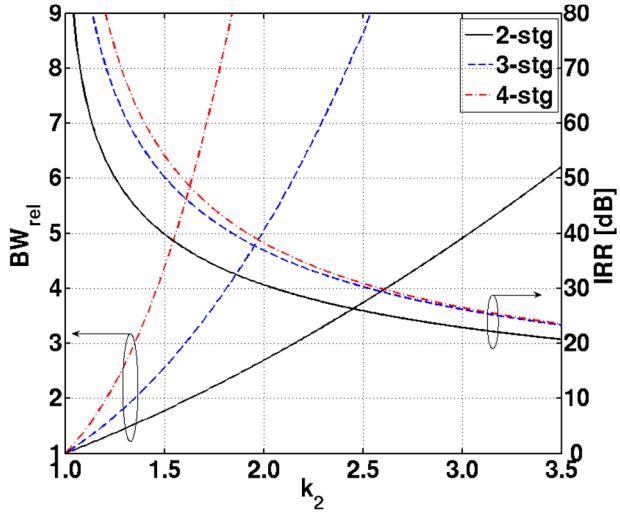

Fig. 5.17. IRR and relative bandwidth BW_{rel} as a function of pole-splitting factor k_2. The optimum pole splitting is calculated according to (5.40) and (B.5) for 3- and 4-stage PPFs, respectively.

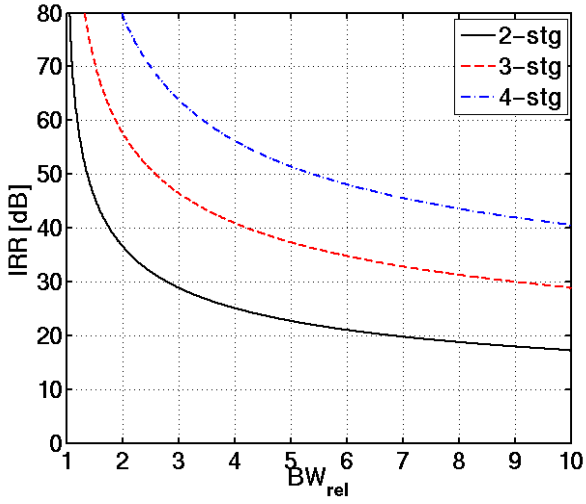

Fig. 5.18. IRR as a function of relative bandwidth BW_{rel} for 2-, 3-, and 4-stage PPFs with unequal RC pole frequencies.

5.5.5 Intrinsic PPF loss

When PPFs are used for quadrature signal generation in the LO signal path, the loss due to PPF is usually compensated with on-chip buffers. Often, the current consumption of the LO buffers becomes a remarkable part of RF front-end power budget. Therefore, it is crucial to be aware of the methods to minimize the PPF loss. As a rule of thumb the loss due to PPF is usually estimated to be 3 dB/stage. That holds when all PPF stages have equal RC poles, the loss is calculated at $\omega = 1/RC$, and the PPF is terminated with infinite load impedance.

The previous section described the optimization of IRR bandwidth. The analysis showed that there was no difference in IRR performance between Type I and II PPFs. In this section, the loss of both PPF types is analyzed as a function of the number of stages and pole-splitting factor. In addition, in the case of a multi-stage PPF, the optimal device scaling is discussed. In the following analysis, the source impedance is assumed zero and the termination impedance of the last PPF stage is infinite. This section discusses the loss caused by the PPF only, i.e. intrinsic loss. The effect of the finite input and output impedances are considered in Section 5.5.6.

5.5.5.1 Loss of single-stage PPFs

The differential output signals of a single-stage PPF is calculated from (5.6) by setting $Z_{L1} = \infty$. In the case of Type I PPF, I and Q output voltages have low-pass and high-pass frequency characteristics, respectively. The outputs have an equal magnitude at $\omega_1 = 1/R_1C_1$ calculated as

$$H^{I}_{1-stg,\omega_1} = \left|\frac{1}{1+sC_1R_1}\right|_{s=i/R_1C_1} = \frac{1}{2}\left|1-i\right| = \frac{1}{\sqrt{2}}, \tag{5.46}$$

which corresponds to 3-dB loss. For the Type II PPF the loss at ω_1 is given by

$$H^{II}_{1-stg,\omega_1} = \left|\frac{1-sC_1R_1}{1+sC_1R_1}\right|_{s=i/R_1C_1} = \left|-i\right| = 1, \tag{5.47}$$

which is 3 dB less than the loss of Type I PPF.

5.5.5.2 Loss of two-stage PPFs

The loss for two-stage Type I PFF can be calculated by cascading (5.6) for $n = 1$ and $n = 2$ and by applying

$$Z_{L1} = \frac{R_2 + Z_{L2} + sC_2R_2Z_{L2}}{1+sC_2\left(R_2+2Z_{L2}\right)} \xrightarrow[Z_{L2}\to\infty]{} \frac{1}{2}\left(R_2 + \frac{1}{sC_2}\right) \tag{5.48}$$

for the load impedance Z_{L1} of the first PPF stage. The last form of (5.48) is used in the following analysis because Z_{L2} is infinite. In the case of Type I PFF, the I-output has a loss maximum and the Q-output has a loss minimum at the geometric average of the RC poles, i.e. $\omega = 1/\sqrt{R_1C_1R_2C_2}$, as is shown in Fig. 5.19.

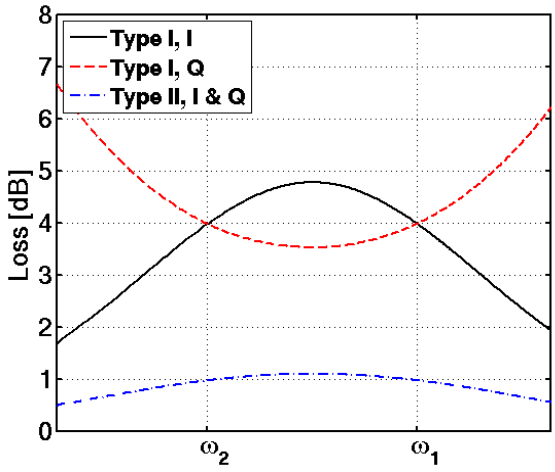

Fig. 5.19. Loss of two-stage PPFs as a function of frequency. The loss is shown for both PPF types. The pole-splitting factor $k_2 = 3$ ($k_{2R} = 3$ and $k_{2C} = 1$).

At that frequency, the I and Q output losses become

$$L^{I}_{2-stg,Iout,\max} = \frac{\left(C_1R_1 + 2C_2R_1 + R_2C_2\right)^2}{4C_1C_2R_1R_2}, \tag{5.49}$$

$$L^{I}_{2-stg,Qout,\min} = \left(\frac{C_1R_1 + 2C_2R_1 + R_2C_2}{C_1R_1 + C_2R_2}\right)^2, \tag{5.50}$$

respectively. In the case of equal RC poles, (5.49) and (5.50) will lead to 6-dB loss (i.e. 3 dB/stage) at both outputs. However, in the general case, RC poles are not equal. It is possible to design the pole ω_2 to the wanted frequency with the pole-splitting parameter k_2 by scaling either the value of R_2 or C_2 or both. Since the minimum (or maximum) loss is a function of R_1, C_1, R_2, and C_2 as is shown in (5.49) and (5.50), there are optimal component values, which minimize the PPF loss. To calculate the optimum device scaling, the parameter k_2 is further divided into two parts

$$k_2 = k_{2R}k_{2C}, \tag{5.51}$$

where k_{2R} and k_{2C} denote the ratio of the first- and second-stage resistors and capacitors, i.e. $k_{2R} = R_2/R_1$ and $k_{2C} = C_2/C_1$. Equation (5.49) can be modified into

$$L^{I}_{2-stg,Iout,\max} = \frac{\left(1 + 2k_{2C} + k_{2C}k_{2R}\right)^2}{4k_{2C}k_{2R}} = \frac{\left(1 + 2k_{2C} + k_2\right)^2}{4k_2}. \tag{5.52}$$

According to the last form, if k_2 is fixed, for example due to the IRR requirement, the loss is minimized when k_{2C} is as small as possible. In other words, when the component values of the lower pole ω_2 are chosen, the resistor value should be larger and capacitor value smaller compared to the component values of the higher pole ω_1 (i.e. $R_2 > R_1$ and $C_2 < C_1$). This holds also for higher order PPFs. In practice, when a PPF with unequal RC poles is designed, it is beneficial to dimension all the capacitors with a fixed value. Then, $k_{2C} = 1$ and the pole-splitting factor k_2 is defined by the resistor ratio k_{2R} only. The following analysis is performed for cases

where equal capacitor values are used in all stages, i.e. $k_{2C} = 1$ if not otherwise mentioned. Then, the losses for Type I PPF I and Q outputs as a function of k_2 are achieved by

$$L^{I}_{2-stg,\max,I} = \frac{(k_2+3)^2}{4k_2}, \tag{5.53}$$

$$L^{I}_{2-stg,\min,Q} = \left(\frac{k_2+3}{k_2+1}\right)^2, \tag{5.54}$$

respectively. The losses of both outputs are plotted in Fig. 5.20 as a function of k_2. With equal RC poles ($k_2 = 1$), both (5.53) and (5.54) lead to a loss of 6 dB. In addition, it is observed that $k_2 \geq 1$ is required to minimize the losses. Therefore, the RC poles should be placed such that the highest RC pole is the first stage in the signal path, i.e. the impedance level increases along with signal path. Then, the average loss is less than the 3 dB/stage.

Next, a similar analysis is carried out for Type II PPF. According to (5.19), I and Q outputs of a two-stage Type II PFF always have balanced amplitude. As is shown in Fig. 5.19, the maximum loss is achieved at $\omega = 1/\sqrt{R_1 C_1 R_2 C_2}$ and is

$$L^{II}_{2-stg,\max} = \frac{(C_1R_1 + 2C_2R_1 + R_2C_2)^2}{C_1^2R_1^2 + 6C_1R_1C_2R_2 + C_2^2R_2^2} = \frac{(1+2k_{2C}+k_2)^2}{1+6k_2+k_2^2}. \tag{5.55}$$

The loss is minimized by choosing the capacitor scaling factor k_{2C} as small as possible. The loss of Type II PPF is plotted in Fig. 5.20 as a function of k_2, and $k_{2C} = 1$. When $k_2 = 1$, the loss becomes 3 dB. The loss does not have an optimum point as a function of k_2 and it approaches 0 dB when k_2 increases.

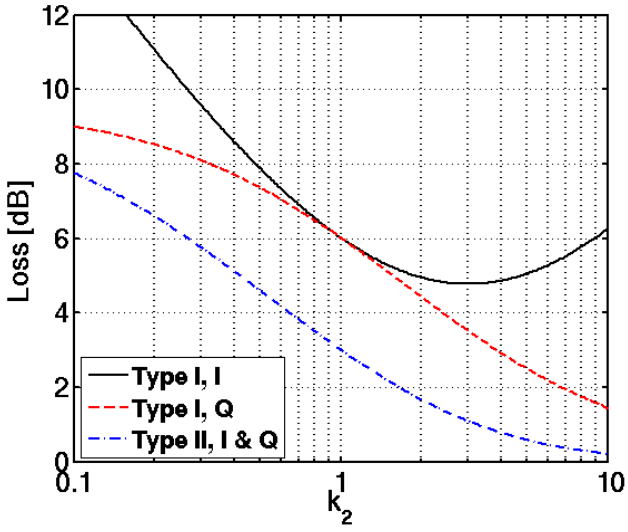

Fig. 5.20. Maximum loss of both PPF types (two-stage) as a function of pole-splitting factor k_2. For Type I PPF, both the I and Q outputs are shown separately.

5.5.5.3 Loss of three-stage PPFs

The losses of three-stage PPFs as a function of frequency are shown in Fig. 5.21, where $k_2 = k_{2R} = 2$, and $k_{3C} = k_{2C} = 1$. Both the I and Q outputs of Type I PPF have loss maximums between ω_1 and ω_3. The frequencies of loss maximums are too lengthy to present here as closed-form formulas. Therefore, the loss of a 3-stage PPF is calculated at $\omega_2 = 1/R_2C_2$, which is the geometric average of ω_1 and ω_3. At that frequency the loss becomes

$$L^{I}_{3-stg,\omega_2} = 2\left(1+\frac{4}{(1+k_2)^2}\right)^2. \tag{5.56}$$

The calculated and simulated loss maximums are plotted in Fig. 5.22 as a function of k_2. Loss is reduced with increased pole splitting. When $k_2 < 2$, (5.56) predicts the loss of Type I with an accuracy better than 0.1 dB.

PPF Type II has a loss maximum exactly at ω_2 and it is expressed as

$$L^{II}_{3-stg,\omega_2} = \left(1+\frac{4}{(1+k_2)^2}\right)^2. \tag{5.57}$$

Comparison of (5.56) and (5.57) reveals that the intrinsic loss of Type II PPF is 3 dB smaller than that of Type I at ω_2. The 3-dB difference in loss between PPF types is achieved at every pole frequency independent of the number of stages.

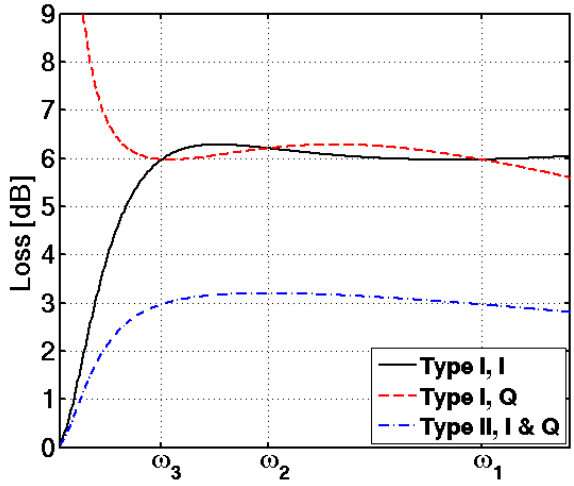

Fig. 5.21. Loss of three-stage PPFs as a function of frequency. Loss is shown for both PPF types. The pole-splitting factor $k_2 = 2$.

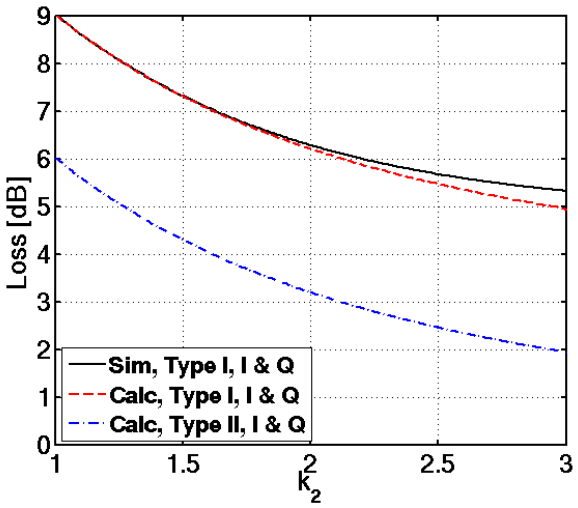

Fig. 5.22. Loss of three-stage PPF at ω_2 as a function of pole-splitting factor k_2. Loss of PPF types I and II are calculated according to (5.56) and (5.57), respectively. The simulated maximum loss of PPF Type I is also shown.

5.5.6 The effect of termination impedances

In this section the effects of input and output impedances on the PPF loss are analyzed. Finite termination impedances cause voltage division both at the input and output of the PPF. In previous sections, the optimal pole frequencies and device scaling were analyzed. The analysis so far, however, does not define the resistor and capacitor values that should be chosen for the PPF. This chapter shows how the impedance level of the PPF should be chosen to minimize the overall loss if finite source (Z_S) and load impedances (Z_L) are known a priori. In addition, the optimum impedance level depends on the PPF topology and on the number of stages.

5.5.6.1 Optimum component values for a single-stage PPF

The differential input impedance of a Type I PPF is

$$Z_{in,1-stg}^{I} = 2\frac{R_1 + Z_{L1} + sC_1R_1Z_{L1}}{1 + sC_1\left(R_1 + 2Z_{L1}\right)}, \tag{5.58}$$

where Z_{L1} is the load impedance of a single output node (see Fig. 5.11a). The output impedance can be calculated with (5.58) by replacing Z_{L1} with Z_S. In the case of PPF Type I, the differential input and output impedance simplifies to R_1+1/sC_1 at the pole frequency of $\omega_1 = 1/R_1C_1$. The result is independent of Z_{L1} or Z_S.

In the general case, the signal loss due to voltage division at the input and output are calculated as

$$L_{input} = \frac{V_{in,PPF}}{V_{source}} = \left|\frac{Z_{in,PPF}}{Z_{in,PPF} + Z_S}\right|, \tag{5.59}$$

$$L_{output} = \frac{V_{load}}{V_{out,PPF}} = \left| \frac{Z_L}{Z_{out,PPF} + Z_L} \right|, \tag{5.60}$$

where $Z_{in,PPF}$ and $Z_{out,PPF}$ are differential input and output impedances of the PPF and Z_S and Z_L are differential source and load impedances, respectively. When Z_S is finite, the voltage division at the input is minimized by maximizing the value of R_1. However, for the minimal voltage division at the output, the value of R_1 should be minimized when Z_L is finite. Thus, there is an optimum PPF impedance level, which minimizes the overall loss. The absolute values of Z_S and Z_L are related to the resistor value R_1 of the first PPF stage with parameters k_S and k_L:

$$|Z_S| = \frac{R_1}{k_S}, \tag{5.61}$$

$$|Z_L| = R_1 k_L . \tag{5.62}$$

A parameter k_Z is used to relate the output and input impedances.

$$\frac{|Z_L|}{|Z_S|} = k_S k_L = k_Z \tag{5.63}$$

As was shown earlier, the intrinsic PPF loss does not depend on the component values. Therefore, for a single-stage PPF, the optimum impedance level can be calculated by setting voltage divisions L_{input} and L_{output} equal. For Type I PPF the optimum output impedance relation k_L becomes

$$k^{I}_{L,opt,1-stg} = \sqrt{2\left|\frac{Z_L}{Z_S}\right|} = \sqrt{2k_Z} . \tag{5.64}$$

The optimum R_1 can then be calculated using (5.62). It should be noticed that $Z_{in,PPF}$, $Z_{out,PPF}$, Z_S, and Z_L are differential, when using equations above.

Due to the dual feed structure, the input impedance of the PPF Type II is half of input impedance of (5.58). When the analysis is repeated, the optimum k_L becomes

$$k^{II}_{L,opt,1-stg} = \sqrt{k_Z} . \tag{5.65}$$

The optimum impedance level of Type I PPF is $\sqrt{2}$ times larger than of Type II PPF. Therefore, if k_Z is known, the resistor value R_1 of Type II PPF should be $\sqrt{2}$ times larger than in PPF Type I. Accordingly, to maintain pole frequency ω_1, the capacitor value C_1 of PPF Type II is $\sqrt{2}$ smaller than in PPF Type I.

The total losses of single-stage Type I and Type II PPFs taking into account both the intrinsic PPF loss and termination losses are expressed as a function of k_Z as

$$L^{I}_{tot,1-stg} = \left(\frac{\sqrt{2} + 2\sqrt{k_Z} + \sqrt{2}k_Z}{k_Z} \right)^2, \tag{5.66}$$

$$L^{II}_{tot,1-stg} = \left(\frac{2 + 2\sqrt{k_Z} + k_Z}{k_Z} \right)^2, \tag{5.67}$$

respectively. The total losses and the difference of the losses are plotted as a function of k_Z in Fig. 5.23. Due to finite input and output impedances, the difference between loss performance of PPF types is less than 3 dB.

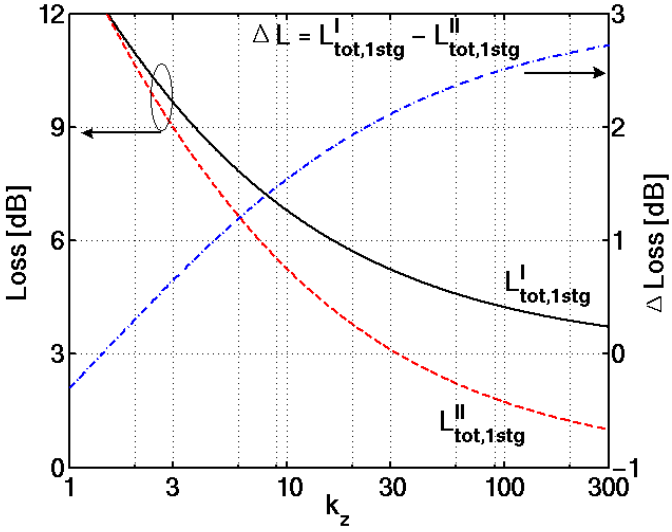

Fig. 5.23. Overall loss of a single-stage PPF. Loss is shown for both PPF types as a function of k_Z (ratio of output and input impedances). In right y-axis, the difference of the losses is shown.

5.5.6.2 Optimum component values for multiple-stage PPFs

The optimization of a two-stage Type I PPF is first considered. When the input and output impedances are calculated, it turns out that the differential input impedance of PPF Type I at ω_1 is R_1+1/sC_1 regardless of the number of PPF stages. With multi-stage PFF, the input impedance at ω_2 is

$$Z_{in,\omega_2} = \frac{R_2\left[\left(C_1R_1+C_2R_2\right)^2+2R_1R_2\left(C_1^2+C_2^2\right)\right]}{C_1^2\left(R_1+R_2\right)^2+R_2^2\left(C_1+C_2\right)^2} - i\frac{R_2\left[\left(C_1R_1+C_2R_2\right)^2+2C_1C_2\left(R_1^2+R_2^2\right)\right]}{C_1^2\left(R_1+R_2\right)^2+R_2^2\left(C_1+C_2\right)^2} \quad (5.68)$$

At ω_2, the output impedance of PPF Type I ($Z_{out,\omega 2}$) is R_2+1/sC_2 and, at ω_1, the output impedance $Z_{out,\omega 1}$ can be achieved with (5.68) by switching $R_1 \leftrightarrow R_2$ and $C_1 \leftrightarrow C_2$.

In the analysis of intrinsic PPF loss, we learnt that it is favorable to perform the pole splitting by scaling the resistor values to minimize the loss. Therefore, k_2 is again divided into two parts ($k_2 = k_{2R}k_{2C}$) to find both optimal component values and scaling ratio when finite termination impedances are taken into account. The optimum loss is found by making overall input and output voltage divisions at ω_1 and ω_2 equal. This results in the following equation:

$$\left|\frac{Z_{in,\omega_1}}{Z_{in,\omega_1}+Z_S}\right|\left|\frac{Z_L}{Z_L+Z_{out,\omega_1}}\right| = \left|\frac{Z_{in,\omega_2}}{Z_{in,\omega_2}+Z_S}\right|\left|\frac{Z_L}{Z_L+Z_{out,\omega_2}}\right|. \quad (5.69)$$

For simplicity, termination impedances Z_S and Z_L are assumed frequency independent. Equation (5.69) results an optimum k_L as

$$k_{L,opt,2-stg}^{I} = \sqrt{2k_{2R}k_Z} \ . \tag{5.70}$$

A similar analysis can be derived for Type II PFF too, and then

$$k_{L,opt,2-stg}^{II} = \sqrt{k_{2R}k_Z} \ . \tag{5.71}$$

When the overall PPF loss is calculated with the result given by (5.70) or (5.71), the analysis again shows that pole splitting is beneficial to perform by increasing the resistor values. Therefore, the loss of the whole two-stage PPF is shown in Fig. 5.24 in a case where $k_{2C} = 1$ and resistor values (k_{2R}) are increased from 1 to 3. The Type II PPF has typically 1-2 dB lower loss than Type I PPF and the difference between PPF losses decreases with small k_Z values.

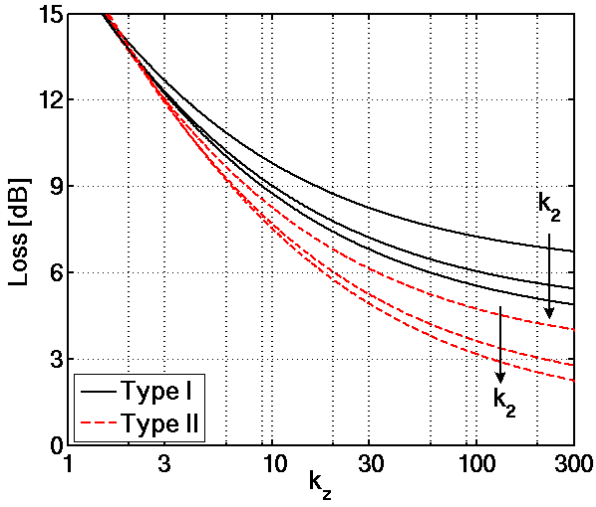

Fig. 5.24. Overall loss of a two-stage PPF. Loss is shown for both PPF types as a function of termination impedance ratio k_Z. The pole-splitting factor k_2 has values of 1, 2, and 3. The arrow shows the direction of increasing k_2.

Finally, the loss of a three-stage PPF is considered. For a Type I PPF, the I and Q outputs signals are balanced at ω_1, ω_2, and ω_3. The optimum component values are achieved when voltage divisions due to termination impedances are equal at ω_1 and ω_3, as they are in (5.69). Then, the optimum k_L values for Type I and II PPFs are calculated with

$$k_{L,opt,3-stg}^{I} = k_{2R}\sqrt{2k_Z} \ , \tag{5.72}$$

$$k_{L,opt,3-stg}^{II} = k_{2R}\sqrt{k_Z} \ , \tag{5.73}$$

respectively. Therefore, the optimum input impedance of PPF Type II is $\sqrt{2}$ smaller than that of Type I PPF for 1-, 2-, and 3-stage PPFs. The optimal total loss of a 3-stage PPF as a function of k_Z is shown in Fig. 5.25 for both filter types. The loss is shown in a case where $k_{2C} = 1$ and resistor values ($k_2 = k_{2R}$) are 1, 2, and 3.

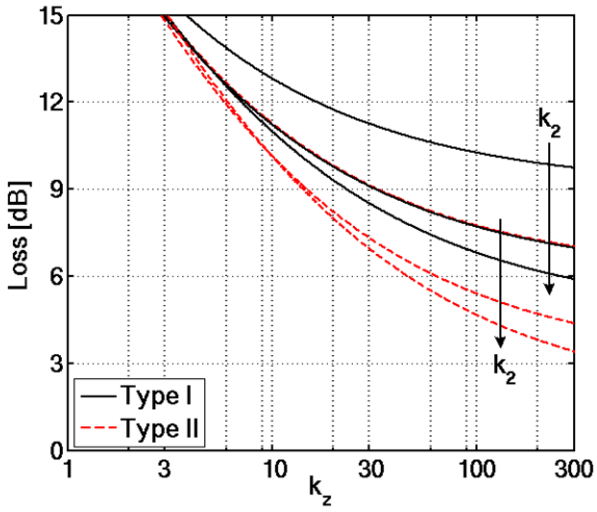

Fig. 5.25. Overall loss of a three-stage PPF. Loss is shown for both PPF types as a function of k_Z. The pole-splitting factor k_2 has values 1, 2, and 3. The result $k_2 = 1$ for Type II overlaps with $k_2 = 2$ for Type I. The arrow shows the direction of increasing k_2.

5.5.7 The effect of parasitic capacitance

The realistic monolithic components always have parasitic capacitance to the substrate. For simplicity, in the following analysis, the parasitic capacitances of the PPF components are combined into a single parasitic capacitor C_{par}. In addition, it is assumed that the value of C_{par} is equal for each PPF node. Precisely speaking, this is not exactly true since larger resistors of small-valued devices implemented using several parallel resistors introduce more parasitic capacitance. However, the main contributors of parasitic capacitances are the capacitors attached to corresponding node, not the resistors. In a well-designed PPF, capacitor values are equal in all PPF stages. Thus, the error introduced by setting C_{par} fixed is small.

The output signals of n^{th} PPF stage are now expressed as

$$\begin{bmatrix} \Delta V_{Iout,n} \\ \Delta V_{Qout,n} \end{bmatrix} = \frac{Z_{Ln}}{R_n + Z_{Ln} + sR_n Z_{Ln}\left(C_n + C_{par}\right)} \begin{bmatrix} 1 & -sC_nR_n \\ sC_nR_n & 1 \end{bmatrix} \begin{bmatrix} \Delta V_{Iin,n} \\ \Delta V_{Qin,n} \end{bmatrix}. \quad (5.74)$$

The load impedance Z_{Ln} is calculated from a network depicted in Fig. 5.26 and the corresponding formula is given in (5.75).

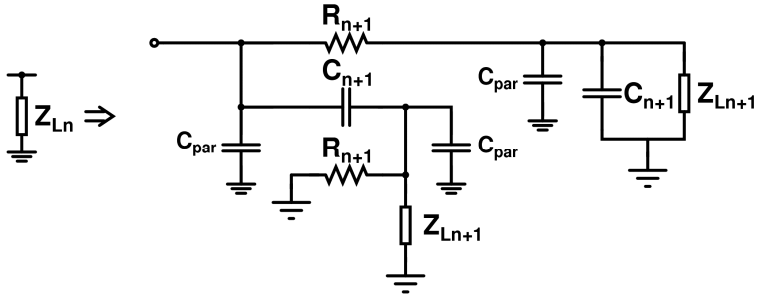

Fig. 5.26. The equivalent load network for calculation of PPF with parasitic capacitance.

$$Z_{Ln,Cpar} = \frac{R_{n+1} + Z_{Ln+1} + sC_{n+1}R_{n+1}Z_{Ln+1} + sC_{par}R_{n+1}Z_{Ln+1}}{1 + sC_{n+1}\left(R_{n+1} + 2Z_{Ln+1}\right) + sC_{par}\left(R_{n+1} + 2Z_{Ln+1} + s2C_{n+1}R_{n+1}Z_{Ln+1} + sC_{par}R_{n+1}Z_{Ln+1}\right)} \tag{5.75}$$

The C_{par} is in parallel with the load impedance Z_L. As was calculated in (5.10) and (5.16), the load impedance does not have an effect on IRR. If the value of C_{par} is equal at each PPF node, it does not affect the IRR either. Therefore, only the loss caused by the parasitic capacitance C_{par} needs to be studied in this section. The amount of extra loss due to C_{par} is similar for both I and Q outputs of Type I PPF. It can be noted that C_{par} causes the same amount of loss for both PPF types, too. The effects of C_{par} on intrinsic loss and voltage division due to finite termination impedances are considered separately. Furthermore, how the C_{par} affects optimal device values is briefly discussed.

5.5.7.1 Single-stage PPF

For a single-stage PPF the additional intrinsic loss at $\omega_1 = 1/R_1C_1$ is

$$L_{Cpar,1-stg} = \frac{1}{2}\left(\frac{C_1^2 + \left(C_1 + C_{par}\right)^2}{C_1^2}\right) = \frac{1}{2}\left(1 + k_{par}^2\right), \tag{5.76}$$

where

$$k_{par} = \frac{C_1 + C_{par}}{C_1} = 1 + \frac{C_{par}}{C_1}. \tag{5.77}$$

For example, a 10-% relative parasitic capacitance causes approximately 0.45-dB additional loss. In addition, C_{par} decreases the input impedance of PPF at ω_1. Due to lower PPF input impedance, the voltage division at the input increases. Additional loss caused by voltage division at the input is

$$L_{Cpar,in} = 1 + \frac{C_{par}}{2C_1^2} \cdot \left(\frac{2C_1 + C_{par}}{1 + 2k_2 + 2k_S^2}\right) = 1 + \frac{k_{par}^2 - 1}{2\left(1 + 2k_2 + 2k_S^2\right)}, \tag{5.78}$$

where k_S denotes the relation between R_1 and differential source impedance according to (5.61). For example, with k_S=1, a 10-% relative parasitic capacitance causes less than 0.1 dB additional loss at input. In practice, $k_S > 1$, and therefore $L_{Cpar,in}$ has an insignificant effect compared to (5.76).

The parasitic capacitance decreases also the output impedance, which improves the voltage division at the output. The additional output voltage division due to C_{par} is less than 1 according to

$$L_{Cpar,out} = 1 - 2\frac{k_{par}^2 - 1}{k_{par}^2 + 1} \cdot \frac{1 + k_L}{2 + 2k_L + k_L^2}. \tag{5.79}$$

In (5.79), k_L is defined according to (5.62). Also (5.79) is quite insignificant compared to (5.76) if $k_L > 10$. Actually, by using optimal k_L values given by (5.64) and (5.65), it can be shown that, when the effect of losses $L_{Cpar,out}$ and $L_{Cpar,in}$ are combined, the result is always less than unity, i.e. parasitic capacitance decreases the termination losses. Therefore, as a worst case, the loss due to C_{par} can be predicted by (5.76).

5.5.7.2 Effect on optimal device values

In addition to the increased loss, the C_{par} modifies the optimal component values calculated with (5.64) and (5.65). The analysis of the optimal component values due to C_{par} using closed-form expressions is complicated. Therefore, the effect of C_{par} is presented by simulation results. First, the C_{par} is divided into dependent and independent parts of C_1 as

$$C_{par} = \theta C_1 + C_{fixed} \,. \tag{5.80}$$

θ denotes the relative parasitic capacitance of C_1 (per plate) and C_{fixed} presents the fixed parasitic capacitance of resistors and metal wiring of the layout etc. The effect of C_{par} was studied in two extreme cases: C_{par} is dependent only on C_1 or C_{par} is independent of C_1. In the former case, decreasing the value of C_1 and increasing the value of R_1 minimizes the overall PPF loss. This is quite understandable because then C_{par} minimizes along with C_1. In the latter case, it is optimal to increase the value of C_1 and decrease the value of R_1. This results from (5.76), which suggests that the value of C_1 should be increased compared to C_{par} to minimize the k_{par} and additional intrinsic loss. In a realistic case, C_{par} has both independent and dependent parts of C_1 and thus a starting point for finding the optimal component values is given by (5.64) and (5.65). This holds for the higher order PPFs, too.

5.5.7.3 Multi-stage PPFs

The loss caused by parasitic capacitance to a two-stage PPF is considered next. Only the intrinsic PPF loss is analyzed. As was shown for the single-stage PPF, it gives the worst case assumption. The additional loss as a function of frequency can be calculated with

$$L_{Cpar,2-stg}(\omega) = 1 + \frac{\left(k_{par}^2 - 1\right)\left(\frac{\omega}{\omega_1}\right)^2 \left(9 + 2k_2 + k_2^2 + 4k_2^2 k_{par}^2 \left(\frac{\omega}{\omega_1}\right)^2\right)}{1 + \left(9 + 4k_2 + k_2^2\right)\left(\frac{\omega}{\omega_1}\right)^2 + k_2^2 \left(\frac{\omega}{\omega_1}\right)^4}, \tag{5.81}$$

where $\omega_1 = 1/R_1C_1$ and k_{par} is calculated according to (5.77). In Fig. 5.27, (5.81) is plotted in two cases as a function of frequency. In the first case, no pole splitting is utilized ($k_2 = 1$, double RC pole at ω_1) and, in the second case, pole splitting with $k_2 = 3$ was utilized. Figure 5.27 was plotted with C_{par} values being 5 %, 10 %, 15 %, and 20 % of C_1. The figure depicts that the additional intrinsic loss of the PPF increases along with the frequency. In addition, the pole splitting enhances the additional loss.

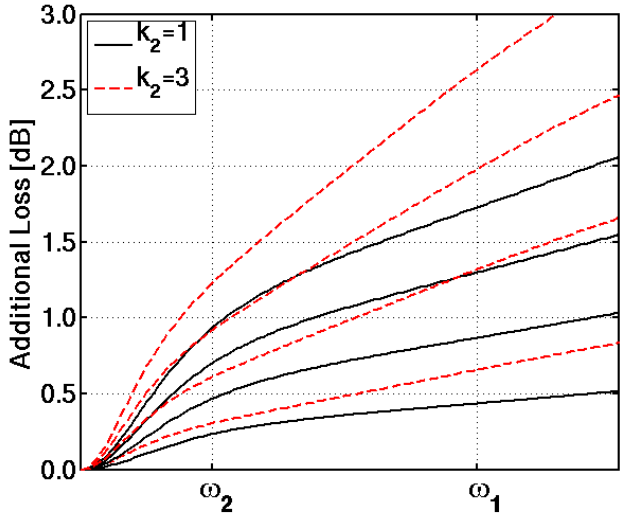

Fig. 5.27. Additional loss due to C_{par} of a two-stage PPF as a function of frequency. In the first case, no pole splitting is utilized (double RC pole at ω_1) and, in the second case, PPF was designed with pole splitting of $k_2 = 3$. The C_{par} values used in plotting were 5 %, 10 %, 15 %, and 20 % of C_1.

The following analysis concentrates on calculating the loss at the highest pole ω_1, where the worst-case results are achieved. At ω_1 and without pole splitting ($k_2 = 1$) the additional loss due to C_{par} is

$$L_{Cpar,2-stg,\omega=\omega_1,k_2=1} = \frac{1}{4}\left(1+k_{par}^2\right)^2, \tag{5.82}$$

which is familiar from (5.76). Actually, it can be calculated that the loss of an n-stage PPF at ω_1 and with equal RC poles is

$$L_{Cpar,n-stg,\omega=\omega_1,k_2=1} = \frac{1}{2^n}\left(1+k_{par}^2\right)^n. \tag{5.83}$$

Taking into account $k_2 > 1$, the additional loss for a two-stage PPF at ω_1 can be calculated as

$$L_{Cpar,2-stg,\omega=\omega_1,k_2>1} = 1+\frac{1}{2}\left(k_{par}^2-1\right)\left(1+\frac{4+4k_{par}^2k_2^2}{5+2k_2+k_2^2}\right). \tag{5.84}$$

For the higher order PPFs, similar equations become quite lengthy and only a simulated result is presented. The additional loss due to C_{par} at ω_1 is shown in Fig. 5.28 as a function of k_2 for 2- and 3-stage PPFs. The parasitic capacitance has values of 5 %, 10 %, 15 %, and 20 % of C_1. The loss of 3-stage PPF worsens quite dramatically along with pole splitting.

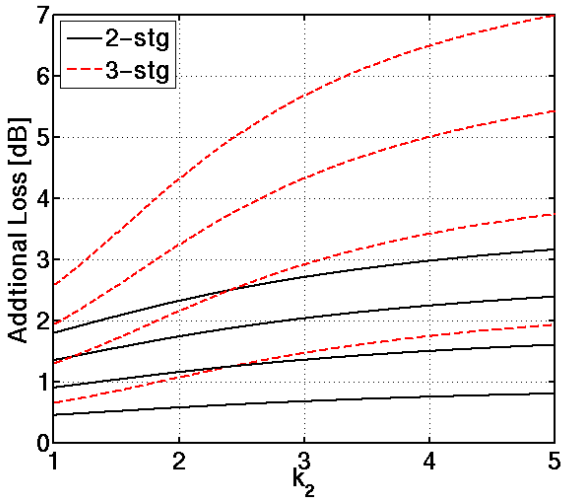

Fig. 5.28. Additional loss due to C_{par} of a 2- and 3-stage PPFs at ω_1 as a function of pole-splitting factor k_2. The parasitic capacitances used in figure were 5 %, 10 %, 15 %, and 20 % of C_1.

5.5.7.4 Summary of effect of parasitic capacitance

In this section, the effect of parasitic capacitance is analyzed with some simplifying assumptions. It is found that, if there is equal parasitic capacitance at each PPF stage output node, it does not affect the IRR performance. Because C_{par} modifies the input and output impedances of PPF, the optimal component values also change in a minor way. In addition, C_{par} increases the intrinsic loss, which worsens at higher frequencies and with pole splitting.

5.5.8 Component value deviation

This section analyzes the effect of the resistor and capacitor value deviation. In a typical PPF, the resistors and capacitors are in close proximity and the mismatch among resistor and capacitor values is usually well controlled in most IC processes. Therefore, the component mismatch is neglected in this analysis and only the minimum and maximum component deviations are considered. The effect of component mismatch is analyzed in [34] and [35], for example.

The relative maximum (ΔR_{max}) and minimum (ΔR_{min}) resistor value deviation from the typical value (R_{typ}) are defined in the following way:

$$\Delta R_{\max} = \frac{R_{\max} - R_{typ}}{R_{typ}} \rightarrow R_{\max} = R_{typ}\left(1 + \Delta R_{\max}\right), \tag{5.85}$$

$$\Delta R_{\min} = \frac{R_{typ} - R_{\min}}{R_{typ}} \rightarrow R_{\min} = R_{typ}\left(1 - \Delta R_{\min}\right). \tag{5.86}$$

The capacitor deviation is defined in a similar manner. Typically, the component deviation is symmetrical, i.e.

$$\Delta R_{\max} \approx \Delta R_{\min} = \Delta R\,. \tag{5.87}$$

Therefore, the resistor R_n of the n^{th} PPF stage could be replaced with $R_n \rightarrow R_n(1\pm\Delta R_n)$ in all presented equations. The same can be done for the capacitors, too, $C_n \rightarrow C_n(1\pm\Delta C_n)$. Clearly, the pole frequencies shift due to the device-value variation.

$$\frac{1}{R_n C_n} \rightarrow \frac{1}{R_n\left(1\pm\Delta R_n\right)}\frac{1}{C_n\left(1\pm\Delta C_n\right)} \tag{5.88}$$

It is possible that the pole frequency remains unchanged because resistor and capacitor variations do not track each other. In the worst case, both the capacitor and resistor values vary in the same direction, i.e. only '+' or '−' signs apply. However, the pole-splitting factor remains nearly unchanged if the relative deviation is independent of the original component value. That holds when all the devices are made of the same material and have similar geometry. For example, in the case of a two stage-PPF, if $\Delta R_1 \cong \Delta R_2$ and $\Delta C_1 \cong \Delta C_2$, the pole-splitting factor k_2 is

$$k_2 = \frac{R_2 C_2}{R_1 C_1} \rightarrow \frac{R_2\left(1\pm\Delta R_2\right)}{R_1\left(1\pm\Delta R_1\right)}\frac{C_2\left(1\pm\Delta C_2\right)}{C_1\left(1\pm\Delta C_1\right)} \approx k_2 . \tag{5.89}$$

The unchanged pole-splitting factor holds for the higher order PPFs, too. As a result, the overall IRR remains unchanged but shifts in the frequency domain. To achieve the required IRR over the whole wanted bandwidth, and taking into account the device variation, the relative frequency BW_{rel}, defined as $\omega_{max}/\omega_{min}$, as in (5.27), (5.35), and (5.45), should be multiplied by bandwidth deviation factor (BW_{dev}) defined as:

$$BW_{dev} = \frac{R_{\max} C_{\max}}{R_{\min} C_{\min}} = \frac{\left(1+\Delta R_{\max}\right)}{\left(1-\Delta R_{\min}\right)}\frac{\left(1+\Delta C_{\max}\right)}{\left(1-\Delta C_{\min}\right)} . \tag{5.90}$$

Therefore, the efficient relative factor $BW_{rel,eff}$ is defined:

$$BW_{rel,eff} = BW_{rel} BW_{dev} . \tag{5.91}$$

For example, a typical 25 % ΔR and ΔC variation leads to $BW_{dev} = 2.78$. Therefore, the required relative bandwidth BW_{rel} nearly triples.

5.5.8.1 Geometric center frequency deviation

When the PPF minimum (ω_{min}) and maximum (ω_{max}) operational frequencies are known, the geometric center frequency ω_c can be calculated as

$$\omega_c = \sqrt{\omega_{\min}\omega_{\max}} = \sqrt{BW_{rel}}\,\omega_{\min} = \frac{\omega_{\max}}{\sqrt{BW_{rel}}} . \tag{5.92}$$

The center frequencies of 1-, 2-, and 3-stage PPFs are $\omega_{c,1\text{-}stg} = \omega_1$, $\omega_{c,2\text{-}stg} = \omega_1/\sqrt{k_2}$, and $\omega_{c,3\text{-}stg} = \omega_1/k_2 = \omega_2$, respectively.

IRR performance of a 2-stage PPF (k_2=2) with minimum (RC_{min}), typical (RC_{typ}), and maximum (RC_{max}) component values ($\Delta R = \Delta C = 0.25$) are plotted in Fig. 5.29. The frequency where IRRs with minimum and maximum deviations overlap slightly differs from the geometric center frequency of a PPF with typical values. In the general case, the relative center frequency deviation can be calculated as

$$\Delta\omega_{RCdev} = \frac{\omega_{c,RCtyp}}{\omega_{c,RCdev}}. \tag{5.93}$$

In (5.93), $\omega_{c,RCtyp}$ is the geometric center frequency of the PPF with typical component values, $\omega_{c,RCdev}$ is the geometric center frequency due to device variations, and thus $\Delta\omega_{RCdev}$ becomes

$$\Delta\omega_{RCdev} = \sqrt{(1-\Delta R_{\min})(1+\Delta R_{\max})(1-\Delta C_{\min})(1+\Delta C_{\max})} \approx \sqrt{(1-\Delta R^2)(1-\Delta C^2)}. \tag{5.94}$$

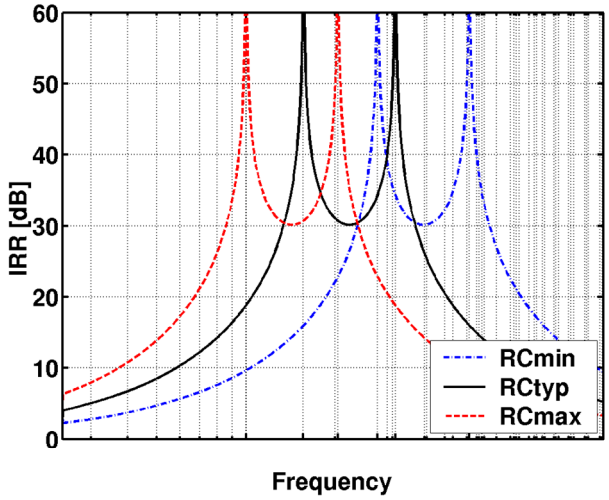

Fig. 5.29. IRR of a two-stage PPF with 25 % component variation.

The last form of (5.94) holds when device-value deviation is symmetrical according to (5.87). For example, with 25 % device variation, $\Delta\omega_{RCdev}$ is approximately 0.94. All the original pole frequencies ω_n of a PPF with nominal device values should be multiplied by a factor $\Delta\omega_{RCdev}$ to achieve the required IRR over the whole wanted bandwidth and taking into account the device variation.

5.5.9 Summary and design example

In this section the results are summarized and a design example is provided to clarify the PPF design procedure. Below is a list of major design principles of an optimum PPF. Reasoning for each item is given in the analysis, but for sake of brevity is not repeated here. A well-designed multi-stage PPF obeys the following rules:

- RC poles are split.
- Optimal pole splitting is calculated according to $BW_{rel,eff}$.
- The capacitors are of equal value in each stage.
- The impedance level (i.e. resistor values) increase along the signal chain.
- Component value deviation is taken into account when the effective relative bandwidth $BW_{rel,eff}$ is calculated.
- The resistor values are calculated taking into account the termination impedances.
- Parasitic capacitance is kept equal in each node of a PPF stage.

For the design example given next, an IRR of 40-dB is required, the wanted relative bandwidth BW_{rel} is 1.5, and component deviation $\Delta R = \Delta C = 0.25$. The source impedance ($Z_S$) is 100 Ω differentially and the load (Z_L) is a buffer with differential input impedance of 2 kΩ. The maximum corner frequency $\omega_{c,max}$ is scaled to 1. Then, the minimum corner frequency $\omega_{c,min} = 0.666$.

The design of a PPF starts by checking the needed number of stages. That depends on the IRR requirement and device-value variation.

1. *Effective relative bandwidth*: According to (5.90), the bandwidth deviation BW_{dev} is 2.78. Therefore, the effective required bandwidth (5.91) becomes 4.17.
2. *Equal RC poles*: According to (5.28), when $BW_{rel,eff} = 4.17$, the n-stage PPF with equal RC poles offers approximately $n \cdot 9.31$-dB IRR performance. Therefore, a 5-stage PPF would be needed.
3. *Unequal RC poles*: According to (5.34), in a two-stage PPF $k_2 = 2.69$ is needed to fulfill $BW_{rel,eff}$ requirement leading to less than 25-dB IRR (5.31). When a 3-stage PPF is utilized instead, with (5.45) k_2 can be solved to be 1.838. Equation (5.41) gives an IRR of 40.2 dB, which is adequate. The requirement for the number of stages could be quickly checked from Fig. 5.17.

When the number of PPF stages is known, the pole frequencies are calculated. The effect of component deviation is also taken into account.

4. *Pole frequencies*: The geometric center frequency ω_2 can be calculated with (5.92), $\omega_2 \approx 0.816$. The other poles, ω_1 and ω_3, are achieved with (5.30), (5.37), and (5.40): $\omega_1 \approx 1.501$, $\omega_3 \approx 0.444$.
5. *Pole shifting*: The device-value deviation causes the geometric center frequency deviation. According to (5.93), the relative center frequency shift factor $\Delta\omega_{RCdev} = 0.9375$. Therefore, all the pole frequencies are shifted to lower frequencies by that factor. The final pole frequencies are therefore $\omega_1 \approx 1.407$, $\omega_2 \approx 0.765$, and $\omega_3 \approx 0.416$.

When termination impedances are known, the optimal device value can be calculated. In addition, the choice of PPF type is made.

6. *Optimal device values*: Based on termination impedance relation (5.63) $k_Z = 20$. The capacitor values are assumed to have only one value through the whole PPF, and therefore pole splitting is performed by scaling the resistor values only. The optimum k_L-values are given by (5.72) and (5.73), and they are $k_{L,opt}^{I} = 9.714$ and $k_{L,opt}^{II} = 6.869$ for Type I and Type II PPFs, respectively. Therefore, the R_1 values calculated with (5.61) and (5.62) are 233 Ω and 330 Ω for Type I and Type II PPFs, respectively. The other resistor values are calculated with (5.30) and (5.37), i.e. R_2 and R_3 are 429 Ω and 788 Ω for Type I PPF, and 606 Ω and 1115 Ω for Type II PPF, respectively. The capacitor values are finally dimensioned with the pole frequencies

defined in Step 5. $C_1 = C_2 = C_3 = 1/\omega_1 R_1$ i.e. 3.05 mF and 2.15 mF for Type I and Type II, respectively.

7. *Loss*: The loss without the effect of parasitics can be checked from Fig. 5.25. When $k_Z = 20$ and $k_2 \approx 1.838$, the overall loss of Type I and Type II PPFs are approximately 10 dB and 8.4 dB, respectively. Therefore, it is optimal to choose Type II PPF to minimize the LO signal loss if the system allows frequency deviation of 1.15°.

8. *The effect of parasitics*: With modern IC processes, the bottom plate capacitance of capacitors is rather small, less than 10 %. According to Fig. 5.28, the additional loss at ω_1 is approximately 2 dB with a three-stage PPF with k_2 of 1.838 regardless of PPF type.

5.6 Comparison of frequency dividers and polyphase filters for quadrature signal generation

In this chapter, the presented quadrature signal generation methods were mainly concentrated on static frequency dividers and passive polyphase filters. The advantages and disadvantages of both methods are briefly summarized and compared.

The main advantage of the passive polyphase filter is its simplicity. The bandwidth, where required amplitude and phase balance are achieved, can be increased by cascading several RC-CR stages. That, however, comes at the cost of increased LO signal loss, which needs to be compensated with amplifiers before the downconversion mixers. Therefore, to keep the signal loss at reasonable limits, in practical realizations, the number of PPF stages is typically two or three. To keep the required BW as narrow as possible, the passive components having as small deviation as possible are wanted. Clearly, the component deviation is set by the used technology and typically the resistors have stronger dependence on process parameters than the capacitors. The resistors should have well-controlled sheet resistance, which can lead to the need for additional process masks, and that is not always a desired option.

Passive phase shifters operate at the VCO frequency. Therefore, in DCRs the PA can disturb the VCO running at the same frequency, thus resulting in an effect known as LO pulling [7]. That can be avoided by using frequency dividers in quadrature signal generation, since VCO operates at double frequency. Divide-by-two circuits typically have a wide operational band and can provide a large output swing. However, the current consumption of the divider can become large if operation at high frequency is targeted. Although amplifiers are not needed to compensate the LO signal loss, the frequency dividers may require buffering before mixers as well. When the overall power consumption is considered, there is no general rule by which a quadrature signal generation method leads to an optimal result. From the layout size point of view, passive components such as resistors and capacitors usually consume more die area compared to MOSFETs. Thus, the area consumed by the PPFs typically is larger than that of frequency dividers. However, when the die area of the power supply stabilization capacitors especially required by divide-by-two circuits is taken into account, the overall layout areas of these two alternatives are comparable.

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6 Design examples

In this chapter, design examples concerning the design of the LNA, downconversion mixers, LO buffers, and 90-degree phase shift circuits are presented. The main interest is the circuit design for sensor systems and the ultrawideband system (UWB). The design examples are given mainly as they were published in the original manuscripts listed in Chapter 1. The first design examples are involved in the design of a sensor radio IC. The two experimental receivers were presented in [P1] and [P2]. The baseband circuit design details are partially omitted from those two papers, since the author's contribution is not significant in that research area. Some material related to baseband design is nevertheless included here for the sake of the clarity and to gain a better understanding of the whole receiver operation. In Section 6.3, a current reuse method for transceivers is presented. In addition, a design example, where the proposed technique is used, is shown. Then, a design example of a 2.4-GHz RF front-end simulated with a 65-nm CMOS process is given [P3]. The rest of the chapter is devoted to the design of RF circuits for WiMedia UWB receivers. The wideband LNA design examples given in publications [P4] and [P5] are included in Section 6.5. Next, an experimental front-end IC designed and published in [P6] is presented. Finally, the summary of the design examples and comparison to the other published designs is given at the end of this chapter.

6.1 2.4-GHz receiver for sensor applications

This section describes a receiver designed to meet the stringent power consumption requirements for sensor radio, which operates in the 2.4-GHz ISM band with Bluetooth. To enable the reusability of the Bluetooth system, slight changes are made in the radio parameters. The details of the radio system concept can be found in [1].

The block diagram of the fabricated direct-conversion receiver (DCR) is presented in Fig. 6.1. The direct-conversion demonstrator receiver includes a low-noise amplifier, which is merged with quadrature downconversion mixers, local oscillator buffers, and one analog baseband (BB) channel with 1-bit limiter for analog-to-digital conversion. The measured active current consumption of the whole RX with a single baseband channel is 2.75 mA from a 1.2-V supply. With two BB channels, the current consumption would be 2.83 mA.

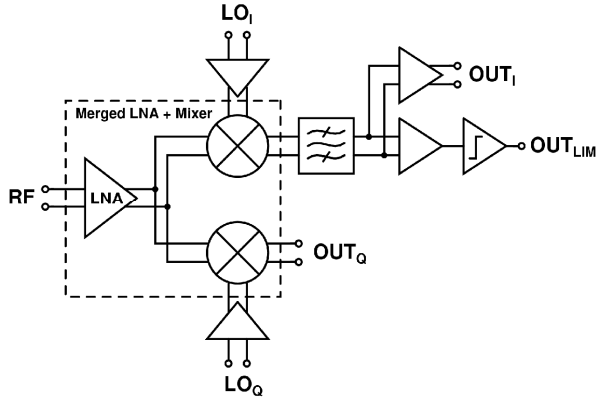

Fig. 6.1. Block diagram of the receiver.

6.1.1 RF front-end

6.1.1.1 LNA and quadrature mixers

The LNA, which is merged with I/Q-mixers, is shown in Fig. 6.2. The I-mixer is followed by a baseband channel, while the Q-channel mixer is loaded with resistors, which enables the separate characterization of the RF front-end in a dc operation point equal to the I-channel mixer. Compared to the solution where separate LNA and mixers are used, the current consumption of a merged structure with the same performance can be decreased by the amount of the dc current, which flows through the mixer switch transistors. In this receiver, the simulated current consumption of the combined LNA and mixer including the biases is 1.4 mA. If separate LNA and mixers were used, the current consumption would be at least 30 % higher.

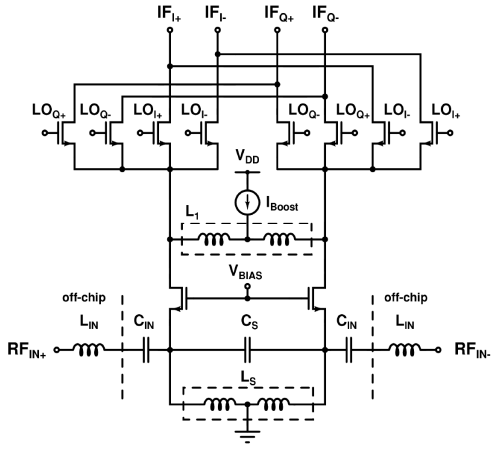

Fig. 6.2. LNA and I/Q-mixers.

The LNA is a balanced common-gate (CG) amplifier with a moderate-Q inductor load (L_1). The CG configuration is used instead of the common-source topology because of the improved reverse isolation. In addition, in the CG configuration the Miller effect is avoided. Therefore, no cascode stage is needed, which is crucial in low-voltage applications. The differential input matching to 100 Ω is implemented with two LC resonators. To save the silicon area, the value of the source inductor L_S is decreased with shunt capacitance C_S. Furthermore, a small area inductor structure was chosen for L_S. When the area of L_S is decreased, the series resistance R_{Ls} increases, resulting in the lower quality value Q_{Ls}. As a consequence, part of the input signal leaks into the source resonator, thus worsening the signal-to-noise ratio (SNR). The R_{Ls} also contributes a noise of its own, as is predicted by (3.85). In addition, the value of L_S defines the source impedance level Z_{LC} and Z_{rel} according to (3.61) and (3.62), respectively. According to (3.88), Z_{rel} together with Q_{Ls} define the minimum achievable noise figure of a CG stage. Therefore, both parameters should be decreased carefully so as not to degrade the overall noise performance, but still some trade-off between sufficient noise performance and small die area can be made.

In addition, the finite Q-value of the inductor L_S affects the input matching. Because the drain-source resistor r_{ds} of the input transistor is much larger than the impedance of the load of the LNA, the load has an insignificant effect on the input matching. Thus, the input matching is

$$Z_{IN} = \left(sL_{IN} + \frac{1}{sC_{IN}} \right) + \left(\frac{sL_S + R_{Ls}}{sL_S \left(sC_T + g_m \right) + R_{Ls} \left(sC_T + g_m \right) + 1} \right), \tag{6.1}$$

where

$$C_T = 2C_S + C_{gs} + C_{par} . \tag{6.2}$$

C_{gs} is the gate-source capacitance of the input transistor, g_m is the effective transconductance of the input transistor, and C_{par} is the capacitance at the source of the input transistor including all parasitic capacitances. At the resonance frequency, the input resistance R_{in} becomes

$$R_{in} = \frac{L_S}{L_S g_m + C_{tot} R_{LS}} = \frac{1}{g_m + \frac{1}{Z_{LC} Q_{Ls}}} . \tag{6.3}$$

According to (6.3), the optimum S_{11} is achieved with a g_m having a value of less than $1/R_{in}$ due to its term, which is defined by the finite Q-value of the source inductor Q_{Ls} and the source resonator characteristic impedance level Z_{LC}. The width of the LNA transistor is chosen to optimize the g_m by using as small a dc current as possible. The simulated effective transconductance of a single input transistor as a function of the transistor width and drain current (I_D) is shown in Fig. 6.3. The transistor length is selected as the minimum needed to maximize the transistor f_T and g_m. The drain-source voltage (V_{DS}) of the input transistor was set to 300 mV. As can be seen in Fig. 6.3, to reach a g_m of 20 mS, which corresponds to 50 Ω, a current of at least 0.75 mA is needed, even with a wide input device. Because of a stringent current budget and a non-zero resistance R_{Ls}, the g_m of less than 20 mS was chosen, which is shown with a dot in Fig. 6.3. When optimizing for a small current consumption, the subthreshold region in Fig. 6.3, where the g_m/I_D ratio is at the maximum, can be exploited. The input referred third-order intercept point (IIP3) of the input transistor improves with a higher overdrive voltage. However, in this design, the input transistor linearity is not critical because the out-of-channel IIP3 is limited by the baseband.

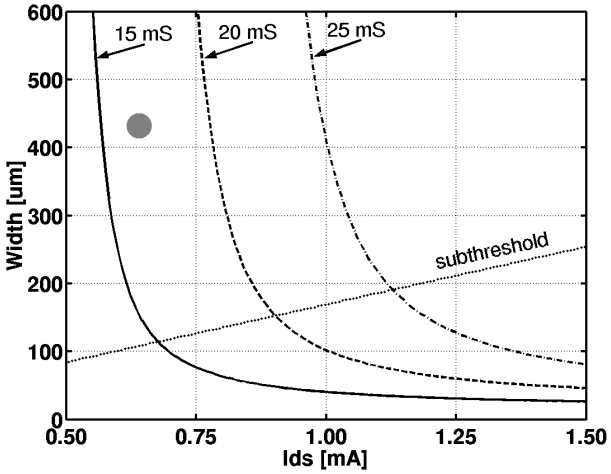

Fig. 6.3. The effective transconductance (15 mS, 20 mS, and 25 mS) of the input transistor as a function of transistor width and drain current. The selected width and I_{ds} of the input transistor are shown with a dot.

The disadvantage of CMOS switching transistors is the high intrinsic flicker noise, which is the largest noise contributor in this design. According to simulations, the flicker noise of the switching transistors increases the NF of the whole receiver by 6 dB. To minimize the 1/*f* noise, the drain current of the switch transistor should be minimized, the active gate area of the mixer switch should be maximized, and the LO amplitude should be maximized [2], [3]. However, not all of these methods are suitable for a low-power low-voltage realization. For example, achieving a large LO swing with a sharp slope is current consuming in a DCR due to the high frequency of the LO signal. In addition, increasing the switch transistor gate area is impractical due to the higher parasitic capacitances, which increases the current consumption of the LO buffer [4]. Thus, the minimum gate length was chosen to keep the mixer gate capacitance small. In addition, the capacitance at the source of the switch transistor degrades the SNR [3]. The tail capacitance can be tuned out with the moderate-Q inductor L_1 between the LNA and the mixer. As a result, the resonator lowers the effect of the mixer flicker noise [5]. According to simulations, the inductor improves the NF and the voltage gain of the receiver by approximately 7-8 dB.

The mixer noise performance can be additionally improved by minimizing the drain current of the switch transistors, because the mixer output noise is directly related to the amount of the dc current of the switches [3]. Typically, the voltage gain and linearity improve with a larger switch current but, in this design, the noise of the switches is the most critical parameter because of the low gain of the LNA. As a result, very different currents are required in the switch transistors and in the LNA transistors to optimize the performance of the front-end and the whole receiver. In this design, the dc current that flows through the switch transistors is reduced with an additional current source I_{Boost}, which is approximately 70 % of the total drain current of the LNA input transistors. Compared to existing solutions [6] and [7], where separate current boosts are used, this design has a single boost current at the center tap of the load inductor L_1, which is a virtual ground. As a result, the thermal noise generated by the boost current source I_{Boost} will cause only common-mode noise at the output of the mixer. If separate boost current sources were used at the output nodes of the LNA, the parasitic capacitance would increase in that node. As a result, the Q-value of the LC resonator would be lower. It follows that the voltage gain would degrade and the following stages would have more effect on the output noise. In addition, separate current sources would cause an output noise voltage, which is comparable to the noise generated by the input transistors. Because the NF in this design is dominated by the flicker noise of the switches, the current boost to the center tap of L_1 has a relatively small effect on the total performance. However, the significance of the presented current boost method on the total output noise depends heavily on the selected process technology and the topology of the receiver.

6.1.1.2 LO buffer

The LO signals are amplified and buffered using balanced LO buffers of the kind shown in Fig. 6.4. The input stage of the LO buffer is a combination of NMOS and PMOS transistors. With typical LO input signal levels (i.e.> –10 dBm), the buffer operates in the large signal region. When the large LO signal has the maximum or minimum amplitude, it latches the input transistors such that the cascoded input transistors are not on simultaneously. The output signal is a sum of V_{DS} voltages of the complementary transistors (M_{N1} and M_{P2}, or M_{N2} and M_{P1}). When

compared to a conventional NMOS differential pair, the presented structure offers an approximately 4-5 dB larger voltage signal to the mixer gates with the same dc current. The NMOS-PMOS transistor pairs between the input and output are used for biasing.

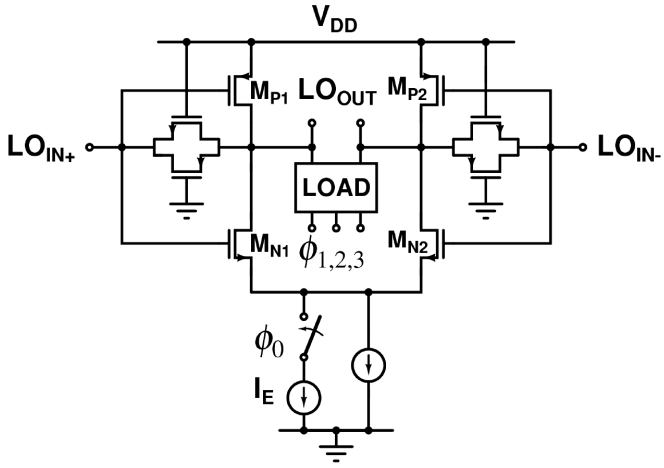

Fig. 6.4. LO buffer.

The load of the LO buffer, which consists of an inductor L, a capacitor C, and capacitors $C_1 - C_3$, is shown in Fig. 6.5. The resonator having a high Q-value was designed to achieve a sufficient LO signal swing with a small current consumption. As a result, the bandwidth of the LO buffer is narrow and the center frequency is sensitive to process variations. With a tunable capacitor load, the LO signal can be adjusted. Three-bit tuning with a range of ±13 % covers all process corners. The tuning was realized by adding capacitors $C_1 - C_3$ to the LC resonator. When the maximum capacitance setup is used, the Q-value of the resonator is lowered, which degrades the available signal swing. Thus, an extra current source I_E was added to increase the output signal swing of the LO buffer when the maximum capacitance setup is used. As a result, the LO signal amplitude variation can be kept within three decibels. The simulated total current consumption of one LO buffer including biases is 0.4 mA. With the additional current source I_E the current consumption increases to 0.6 mA.

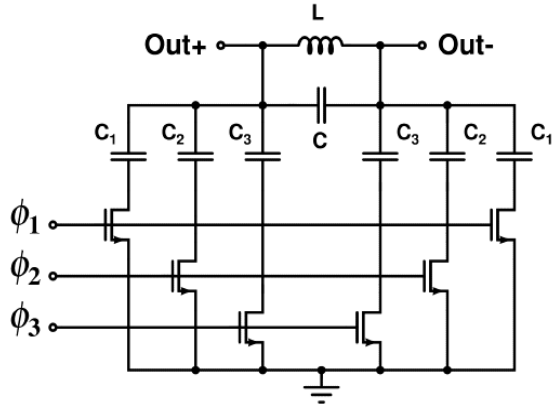

Fig. 6.5. Load of the LO buffer.

6.1.2 Analog baseband circuit

6.1.2.1 Channel-select filter

The realized channel-select filter is a third-order all-CMOS filter. Figure 6.6a shows one half of the filter. The filter is realized with two single-ended circuits, which is also called a pseudo-differential structure. This structure does not need a common-mode feedback circuit, which helps the design when using low supply voltages [8]. When low power consumption and low power supply is targeted, a simple realization of the filter is preferred [9]. The third-order filter can be separated into a real and imaginary part [10]. First, there is a mixer-baseband interface with a real pole and servo loop. The real pole is followed by a biquad stage. The filter was designed for a –3-dB frequency of 550 kHz. The total current consumption of the filter including biases is 65 μA.

6.1.2.2 Mixer-baseband interface

The mixer-baseband interface shown in Fig. 6.6a is the most critical part at baseband since it limits the dynamic range and dominates power dissipation of the baseband. The effective transconductance of the RF front-end is low. Thus, the noise contributed by the interface becomes significant. In addition, the output impedance of the mixer is small whereas a higher impedance level is preferred in the filter to minimize power dissipation. Because of the low transconductance of the RF front-end, small load impedance at the mixer output would require a high supply current in the following baseband stage to keep the input-referred noise of that stage sufficiently small. Another possibility is to increase the mixer output impedance by using cascode devices. Hence, compared to the commonly used resistive mixer load, an interface based on cascode transistors was used. An NMOS cascode device M_1 stacked with the mixer increases the mixer output impedance without additional current. Another cascode stage implemented as a folded PMOS transistor M_4 is needed to achieve sufficiently high output impedance to the NMOS load M_6. The bias current of the PMOS cascode must be larger than the peak signal current caused by any out-of-channel interfering signal to avoid clipping. Steering some of the bias current through the NMOS current source M_5 increases the gain. The load transistor M_6 and the NMOS-capacitor M_7 form the real pole of the filter.

6.1.2.3 Biquad

The biquad stage of the channel-select filter shown in Fig. 6.6a is derived from a g_mC biquad prototype of the kind shown in Fig. 6.6b. To enable the use of low supply voltages, the transconductors are replaced with common-source NMOS transistors instead of using, for example, differential pairs. This filter structure is suitable for applications requiring moderate linearity. MOS capacitors are used because they provide a high capacitance per unit area and sufficient linearity [11].

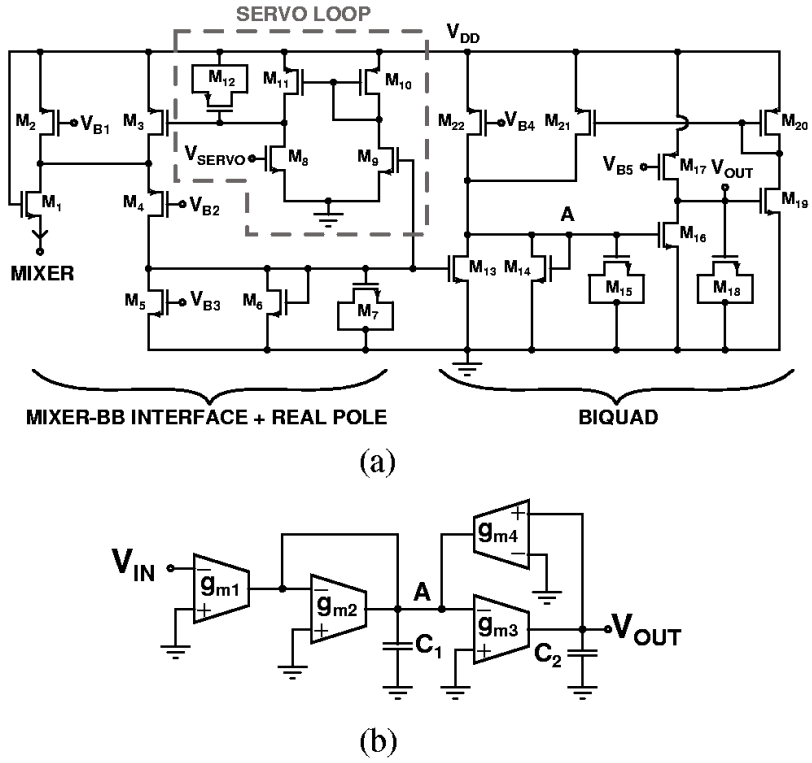

Fig. 6.6. a) 3rd-order all-CMOS channel-select filter and b) a prototype g_mC biquad.

6.1.2.4 Limiter

The 1-bit analog-to-digital conversion is realized with a limiter shown in Fig. 6.7. It consists of five stages, which give a total voltage gain of 47.5 dB. The differential signal at the channel-select filter output is transformed to a single-ended signal with a differential-to-single-ended converter. The single-ended limiter follows the differential-to-single-ended converter. The limiter consists of similar cascaded amplifier stages. By selecting a proper number of amplifiers, the power dissipation of the limiter can be minimized [12].

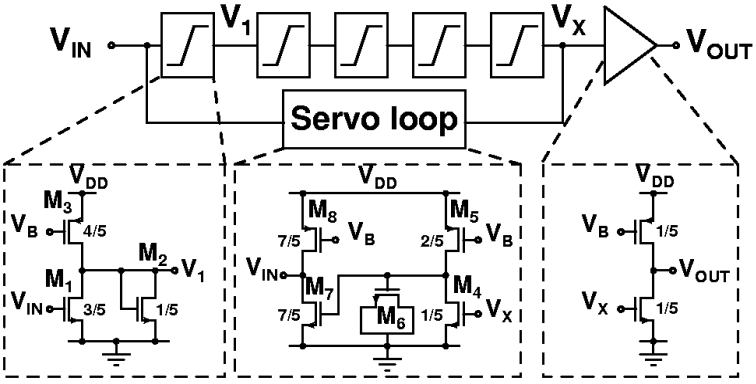

Fig. 6.7. Limiter.

6.1.3 Experimental results

The chip was fabricated with a 0.13-µm CMOS technology. The active chip area is 1.0 mm^2. In addition to the actual receiver, the chip includes test structures and additional test pads that increase the total chip area to 3.3 mm^2. The chips were bonded directly onto a printed circuit board (PCB). The chip micrograph is shown in Fig. 6.8.

The measured active current consumption of the whole receiver with one baseband channel is 2.75 mA from a 1.2-V supply. The measured and the simulated input matchings are shown in Fig. 6.9. The measured S_{11} is better than –10 dB within the wanted frequency band. The simulated S_{11} agrees well with the measured one. The voltage gain, NF, linearity (IIP3, IIP2), and receiver start-up time were measured from the analog test output of the baseband channel. During the measurements, it was found that the LO tuning was sensitive to noise and glitches generated on the chip and PCB. Thus, to confirm the validity of the results, the receiver measurements were primarily performed with the setup where the LO resonator is at the lowest frequency of operation (LO buffer in reset mode). As a result, the maximum performance could not be obtained. The measured RF response is shown in Fig. 6.10. The maximum voltage gain of 47 dB is achieved at 2.0 GHz. The corresponding frequency response of the channel-select filter is shown in Fig. 6.11 where the measured and simulated maximum voltage gains are scaled to 0 dB for the purpose of comparison. The NF measured from the analog test output is 28 dB. In addition, the receiver gain and NF were measured at 2.0 GHz as a function of supply voltage and the result is shown in Fig. 6.12. The measurement shows that the receiver operates down to 1.0-V supply. The minimum supply voltage is limited by the mixer-baseband interface, where four transistors are stacked.

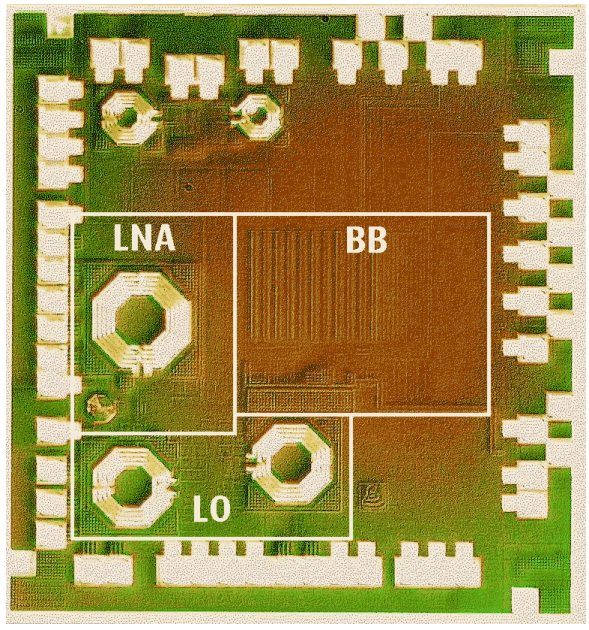

Fig. 6.8. Chip micrograph.

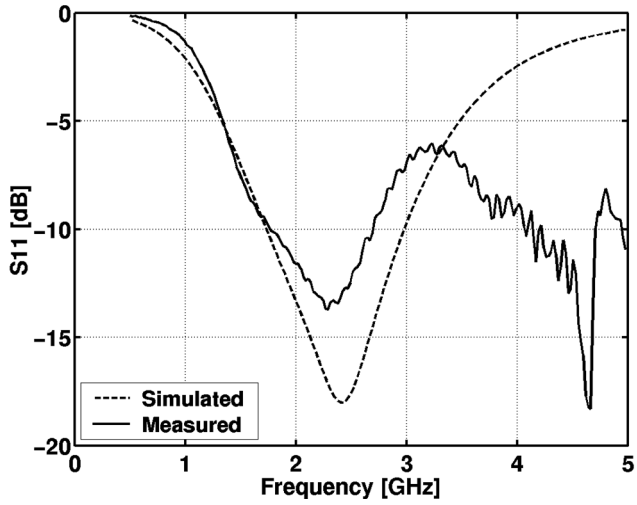

Fig. 6.9. Measured and simulated input matching.

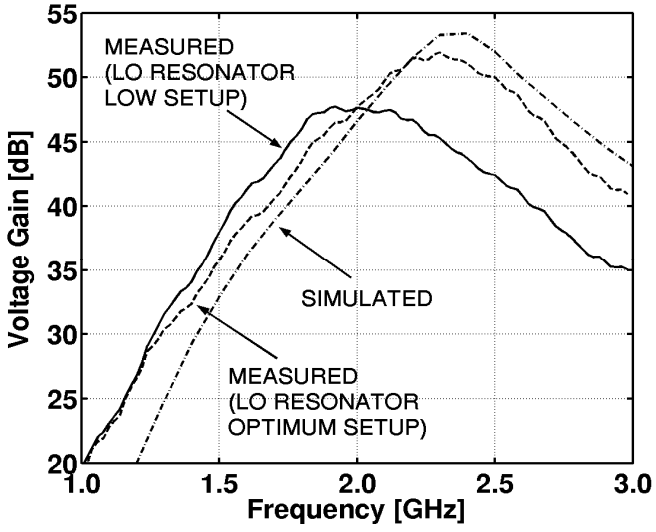

Fig. 6.10. Measured and simulated RF responses.

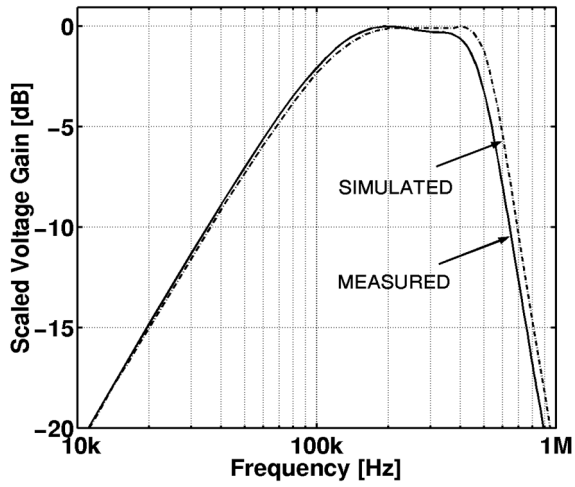

Fig. 6.11. Measured and simulated frequency responses of the channel-select filter.

The receiver IIP3 was measured by using test signals at 3.0-MHz and 5.8-MHz offsets from a 2-GHz LO. The measured IIP3 is –21 dBm at the 100-Ω input impedance. The IIP2 was measured with test tones having 2.8-MHz and 3.0-MHz frequency offsets from the LO, and the results varied between +18 and +26 dBm. For the purpose of comparison, the measured voltage gain with the optimum LO buffer setup and the simulated result are also shown in Fig. 6.10. With the optimum LO buffer setup, the maximum voltage gain is achieved at 2.35 GHz. The measured voltage gain is 52 dB and the NF is 24.5 dB. The start-up time plays an important role in sensor systems when the target is to minimize power consumption. The channel select filter output has settled after 50 μs. The start-up time is limited by the charging of the large capacitance at servo loop of the mixer-baseband interface. The measured duty cycle is given in Table 6.1. The measured group delay with a 200-kHz input signal is 105 ns.

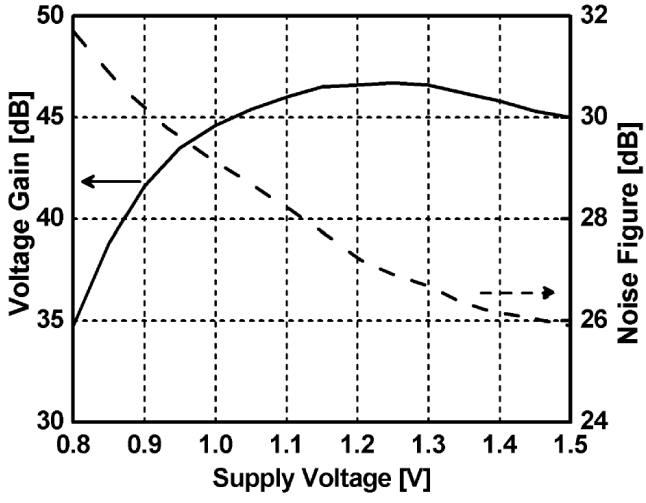

Fig. 6.12. Measured receiver voltage gain and NF vs. supply voltage.

The merged LNA and mixer with the LO buffers consume approximately 94 % of the receiver supply current. In stand-by mode, the measured current consumption is 18 μA. According to simulations, this is mainly due to the leakage current of the bonding pad ring. Table 6.1 summarizes the measured performance of the demonstrator. The measured performance with the optimized LO signal is given in parenthesis.

Table 6.1. Summarized performance of the receiver.

Parameter	Unit	Result
Supply voltage	V	1.2
Supply current (active)	mA	2.75
Supply current (stand-by)	μA	18
Voltage gain, RF + BB	dB	47 (52)
Voltage gain, LNA + Mixer	dB	12.5 (14.5)
Maximum gain frequency	GHz	2.0 (2.35)
NF	dB	28 (24.5)
Out-of-channel IIP3	dBm	–21
Out-of-channel IIP2	dBm	+18
S_{11}	dB	–10
Filter –3-dB corner frequencies	kHz	86, 493
Start-up time	μs	~50
Limiter group delay @ 200 kHz	ns	105
Duty cycle (Up/Period) @ 100 kHz 300 kHz 500 kHz	%	49.0 47.5 46.5

6.2 Direct-conversion receiver for ubiquitous communications

6.2.1 Introduction

A direct-conversion receiver (RX) for a 2.4-GHz sensor network is described in this section. The receiver includes an LNA, downconversion mixers, a 90-degree phase shift circuit, analog filters, a 1-bit analog-to-digital converter, and a received signal strength indicator (RSSI). Compared to the previous prototype [P1], the separate LNA and mixers are used and a 90-degree phase shift circuit is added. In addition, the RX includes two baseband channels with improved selectivity. The wake-up logic and RSSI are added and limiters are fully differential. Biasing is implemented by using an on-chip current reference. The receiver consumes 4.1 mA from a 1.2-V power supply and it achieves 43-dB voltage gain, 25-dB noise figure, –22-dBm IIP3, and +11-dBm IIP2.

The RX is part of a single-chip transceiver circuit, which was fabricated with a 0.13-μm CMOS process. The RX block diagram is presented in Fig. 6.13. The RX has a shared RF input/output port with the transmitter (TX). In addition, the RX and TX use the same VCO circuit for the local oscillator (LO) signal generation.

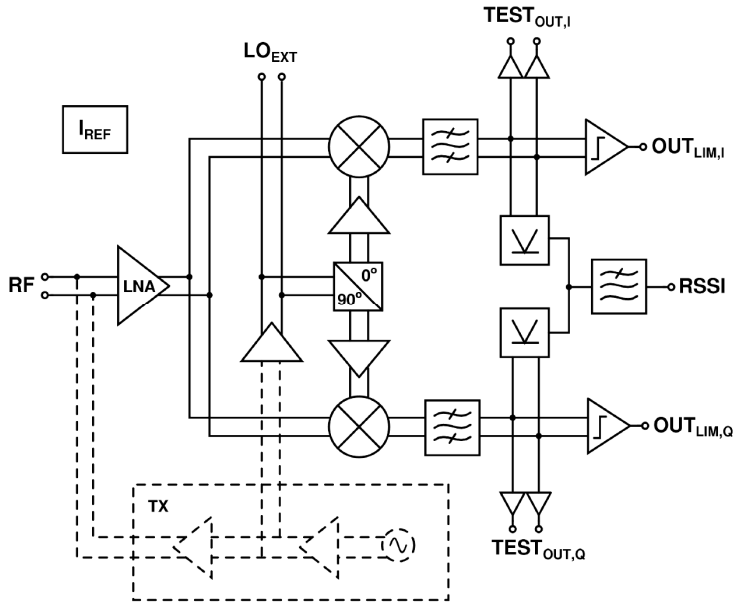

Fig. 6.13. Block diagram of the fabricated receiver (RX). Part of the transmitter (TX) and the RX interface with the TX are shown with a dashed line.

6.2.2 RF front-end design

6.2.2.1 Low-noise amplifier

The low-noise amplifier shown in Fig. 6.14a uses a common-gate (CG) topology with a cascode stage. The input transistors are biased into the subthreshold region to maximize the transconductance versus drain current ratio. The LNA uses an LC resonator tuned at 2.45-GHz center frequency as a load. The RX shares the same time-divided RF input-output port with the TX. The CG input allows a high impedance path towards RX in the transmit mode. Thus, a proper matching performance is achieved without using the switches in the signal path.

In the previously published prototype receiver, the front-end and the baseband interface consisted of four stacked transistors [P1]. As a result, the drain-to-source voltage V_{DS} of the LNA was susceptible to the supply voltage V_{DD}. The deviation from the nominal V_{DD} changed the LNA drain current, which altered the bias condition of the mixers and the baseband interface. With a separate LNA and mixer, the performance dependence of the supply voltage is reduced. In addition, the input transistors of a separate LNA have a higher V_{DS}, which improves the gain and noise performance. However, with a separate LNA and mixer, the whole receiver consumes more current compared to [P1]. In this design, the LNA consumes approximately 2.3 mA including biasing, which is half of the total receiver current.

6.2.2.2 Downconversion mixer

The mixer schematic is shown in Fig. 6.14b. The mixer does not have a typical common-source (CS) input stage due to the strict current budget. The simulated current consumption of the whole mixer is 410 μA, which is 10 % of the receiver total current. With such a small current a

CS amplifier realized with deep submicron CMOS transistors would not improve the gain or noise performance. Hence, the LNA output signal is fed directly on the sources of the switch transistors to maximize the linearity. The switches are designed with minimum transistor length to minimize the load of the LO buffers [4].

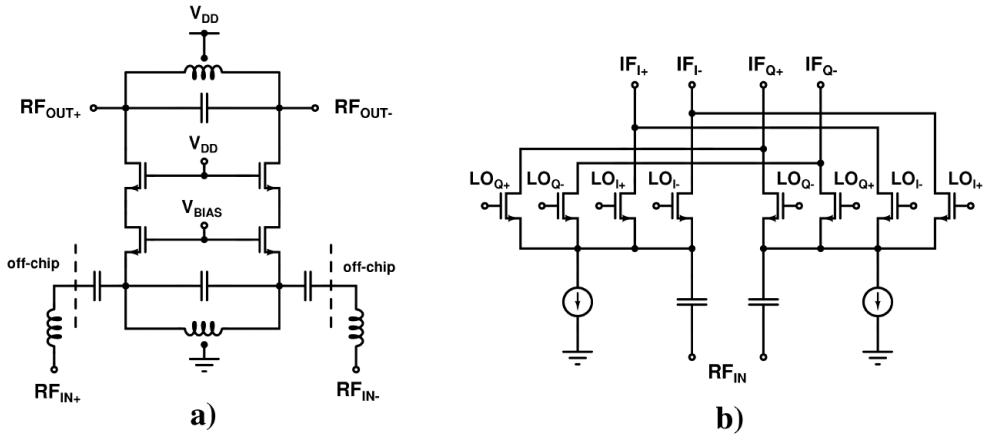

Fig. 6.14. a) LNA, b) mixer.

6.2.2.3 Quadrature LO signal generation

The quadrature LO signal generation circuit is shown in Fig. 6.15. When the transceiver operates normally, the LO signal is generated on-chip (LO_{VCO}) and is fed into the first buffer. However, in the receiver measurements the VCO is shut down to be able to measure the receiver performance only. Thus, an external LO signal (LO_{EXT}) is required. It is fed to the output of the first LO buffer. The first buffer uses an LC resonator as a load for better LO swing, but the buffers driving the mixers do not include inductors to save the silicon area.

The 90-degree phase shifting is realized with a single-stage polyphase filter (SPF). While the amplitude balance of the SPF is poor and susceptible to process variations, it was chosen to minimize the LO signal loss and hence the power consumption. According to the simulations, the loss due to the SPF was 5 dB in this design. The target current consumption for the LO buffers was approximately 1 mA only. Thus, the compensation of the LO signal loss caused by two or more filter stages would increase the current of LO buffers to an unacceptable level. The first buffer consumes approximately 0.46 mA and one second-stage buffer 0.33 mA supply current.

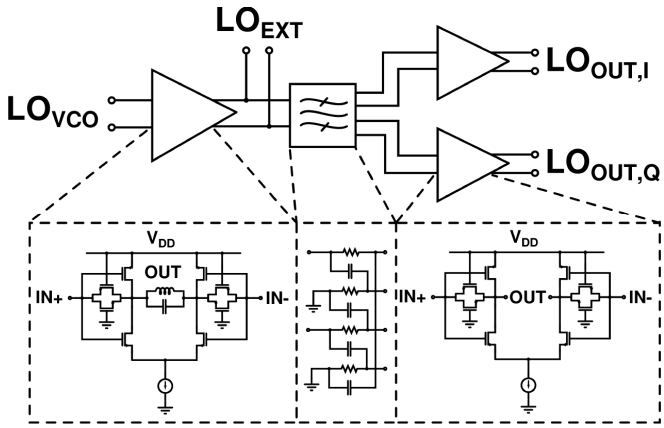

Fig. 6.15. Schematic of the LO buffers and 90-degree phase shifter.

6.2.3 Baseband design

6.2.3.1 Mixer-baseband interface and channel-select filter

The realized channel-select filter is a fourth-order all-CMOS filter with a –3-dB corner frequency of 600 kHz. Figure 6.16 shows one half of the filter. The selectivity of the filter is improved from [P1] by adding a 2nd real pole. Furthermore, the value of the servo capacitor M_{FB} was halved to decrease the silicon area. Since the dc gain of the servo loop was also halved with a constant current source M_1, the –3-dB frequency of the resulting highpass filter is unchanged.

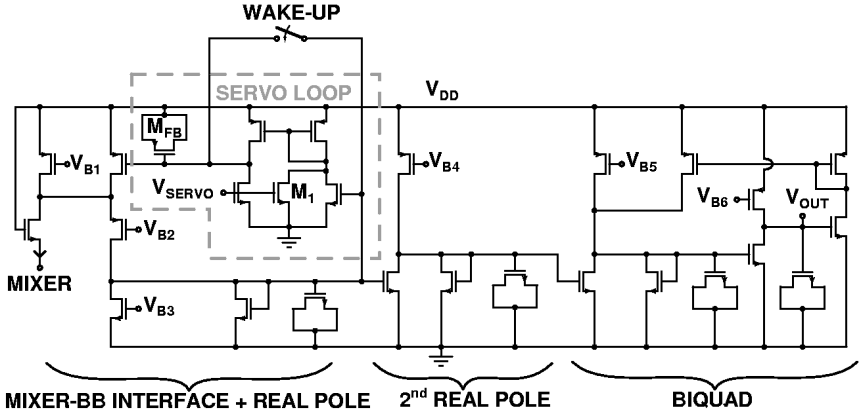

Fig. 6.16. Mixer-baseband interface and a channel-select filter (one half).

6.2.3.2 Limiting amplifier

The block diagram of the limiter is shown in Fig. 6.17. The limiter consists of a unity gain input stage, four cascaded amplifiers with a total small signal gain of 47 dB, a balun, and a flip-flop that samples the output signal. The limiter amplifier is a differential pair with PMOS input devices and cross-coupled NMOS devices in parallel with diode-connected NMOS transistors to increase the load impedance and thus the gain of the amplifier.

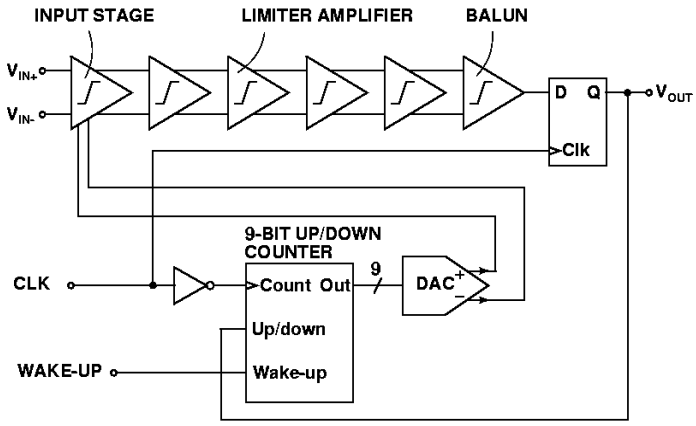

Fig. 6.17. Limiter architecture.

To reduce the limiter input-referred dc-offset, a dc feedback loop is required. To achieve a large time constant without large resistors and capacitors, the dc feedback loop is implemented by using digital circuitry. The dc feedback loop consists of a digital 9-bit up/down counter and a 9-bit current-steering DAC to filter out the dc-offsets [13].

6.2.3.3 Received signal strength indicator

The designed received signal strength indicator (RSSI) is shown in Fig. 6.18. The RSSI has separate full-wave rectifiers for I- and Q-branches, but the following two-stage filter and the latched comparator are common. The full-wave rectifier is designed to eliminate common-mode components at the input of the RSSI. For this purpose, a common-mode feedforward technique is utilized [14]. The ripple of the rectified signal is attenuated by using a two-stage low-pass filter formed by transistors $M_1 - M_4$. The targeted input signal level is –60-dBm.

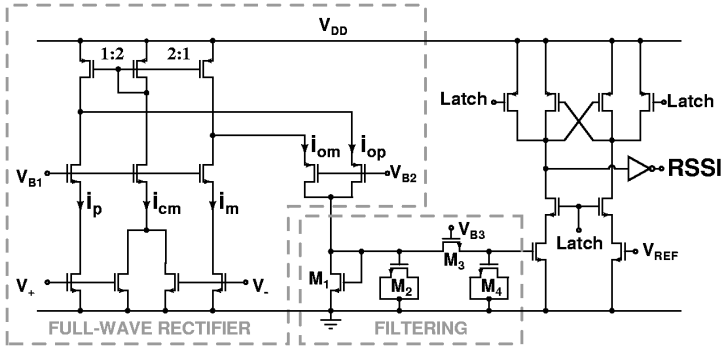

Fig. 6.18. Received signal strength indicator (RSSI).

6.2.4 Experimental results

The chip was fabricated with a 0.13-µm CMOS process. The active area of the RX is approximately 1.0 mm^2. The chips were directly bonded onto a printed circuit board (PCB) made of FR-4 substrate. Measurements were performed both from the analog test output of the baseband circuit and from the limiter output. The performance was characterized by using the

on-chip current reference. According to the measurements from several samples, the noise figure (NF) in the Q-channel was approximately 3 dB higher than in the I-channel. In addition, the IIP2 result of the Q-channel was degraded compared to the I-channel. The imbalance and the noise leakage are probably due to a systematic error in the layout. Thus, the NF and IIP2 performance of the receiver are determined according to the I-channel measurement results only. For the other measured parameters such significant performance difference between the I- and Q-branches was not observed.

The measured S_{11} is shown in Fig. 6.19. Since the circuit model from the latest TX output was not available, the resulting input matching of the RX was inadequate, as is indicated with the dashed line in Fig. 6.19. Thus, the S_{11} of the RX was improved by adding 2.2-nH series inductances on PCB. As a result, S_{11} better than –10 dB is achieved between 2.05–2.55 GHz. However, the input matching circuit and RX/TX interface suffers from the parasitic capacitances, which cause signal loss and most of the gain degradation. The parasitic capacitance also increases the NF, because the gain is lacking before the mixers, which have the largest effect on the total output noise.

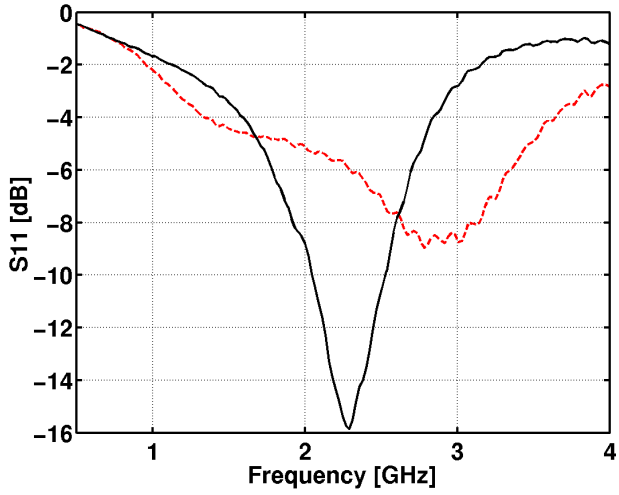

Fig. 6.19. Measured S_{11}. The dashed line shows the original S_{11} and the solid line presents the S_{11} after adding the 2.2-nH series inductors on PCB.

The measured original RF response and the one with the corrected input matching are depicted in Fig. 6.20. The input matching correction improves the gain by 1–2 dB in the wanted frequency area. The maximum voltage gain of 43 dB is achieved at 2.45 GHz. The NF measured from the analog test output is 25 dB. The measured voltage gain and NF versus the supply voltage are presented in Fig. 6.21, which shows that the receiver operates down to one-volt supply voltage. The mixer and the interface with the baseband set the limit because of four stacked transistors.

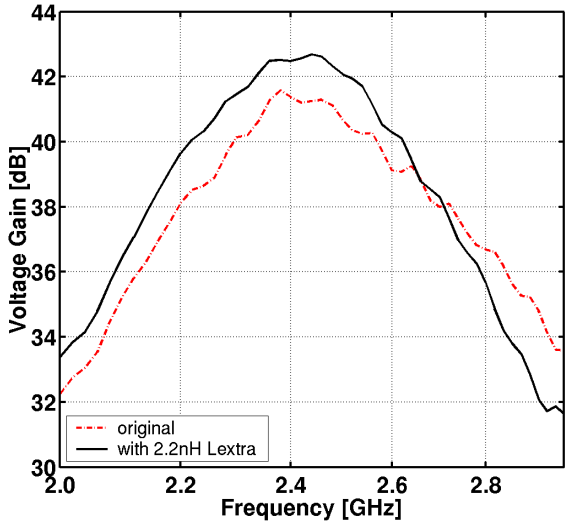

Fig. 6.20. Measured RF responses before (dashed line) and after (solid line) the correction of the RF input.

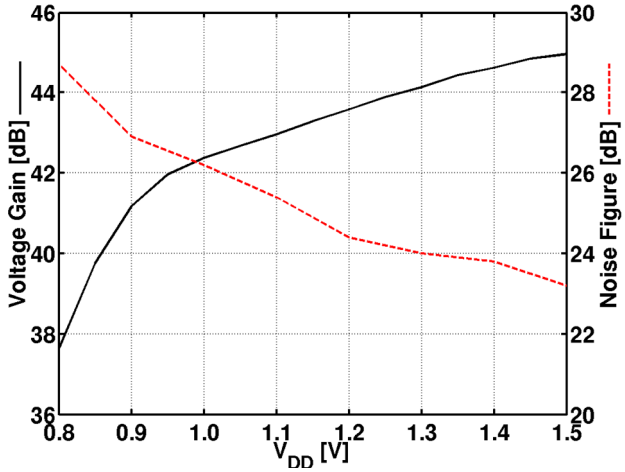

Fig. 6.21. Measured voltage gain and NF versus supply voltage.

The measured IIP3 of the receiver is –22 dBm with the test tones at 3-MHz and 5.8-MHz offsets from the LO. Because the linearity is dominated by the mixer-baseband interface, the measured IIP3 is 3 dB higher than simulated due to the lower gain at RF. The IIP2 was measured with 5.8-MHz and 6-MHz test signals. The IIP2 result varied between +11…+21 dBm in the I-channel. The Q-channel IIP2 was approximately 0 dBm.

The simulated and measured frequency responses (three samples, six channels) of the channel-select filter are shown in Fig. 6.22, where the measured and simulated maximum voltage gains are scaled to 0 dB for the purpose of comparison. The measured –3dB-corner frequency variations are within the specified ±10 %.

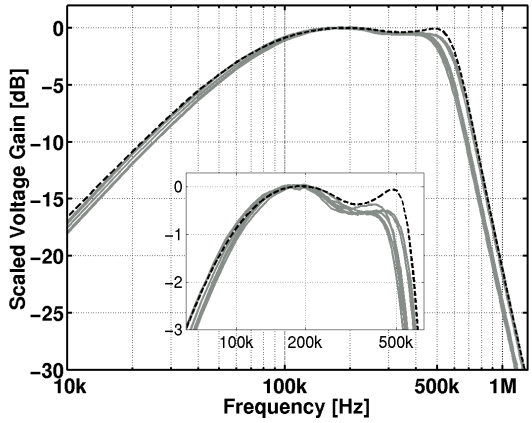

Fig. 6.22. Measured and simulated channel-select filter responses.

The measured wake-up times of the whole receiver with and without the wake-up logic were 15 μs and 80 μs, respectively. The measured RSSI threshold varied between –59…–55 dBm. The threshold is larger than the designed value due to the lower voltage gain of the front-end. The limiter was characterized by measuring the duty cycle with input signal frequencies from 100 kHz to 600 kHz, and input signal levels from –77 dBm to –27 dBm. In all cases, the duty-cycle variation was between ±1 % from the nominal value of 50 %. The measured limiter group delay at 200 kHz input signal frequency was 82 ns.

The measured current consumption of the whole receiver was 4.1 mA. Although the RX was measured alone, the whole transceiver could not be completely shut down due to the TX on the same chip. Thus, the measured stand-by current consumption of 440 μA is arbitrarily high compared to the simulated value of 20 μA, which includes the measured current consumption of the on-chip bias generator (6.2 μA). The measured receiver performance is summarized in Table 6.2. The chip micrograph is shown in Fig. 6.23.

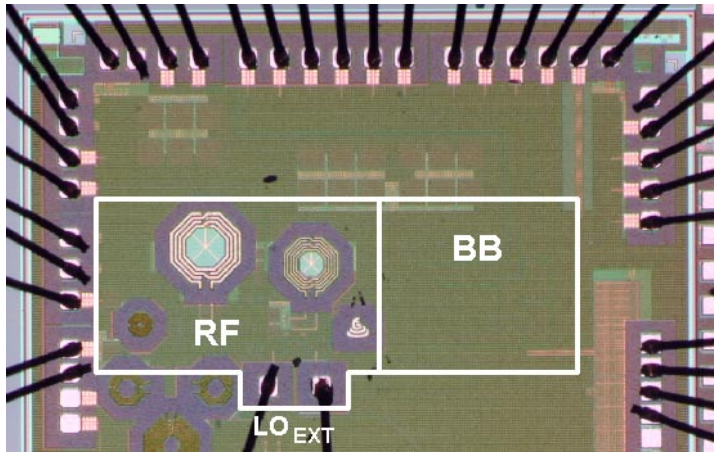

Fig. 6.23. Chip micrograph.

Table 6.2. The measured receiver performance.

Parameter	Unit	Result
Supply voltage	V	1.2
Supply current (active)	mA	4.1
Supply current (stand-by)	μA	440
Voltage gain	dB	43
NF	dB	25
Out-of-channel IIP3	dBm	-22
Out-of-channel IIP2	dBm	+11
ICP	dBm	–35
S11	dB	< –10
Filter high-pass –3-dB frequency	kHz	66
Filter low-pass –3-dB frequency	kHz	546
Wake-up time	μs	15
Duty cycle	%	49
Limiter group delay @ 200kHz	ns	82
RSSI threshold	dBm	–55

6.3 Efficient current reuse for low-power transceivers

Current boosting is a method where the performance of an active circuit block is optimized by placing a constant current source in parallel with the active signal path to provide optimal biasing for different components. In this sub-section, a technique to replace the constant dc current source with active building blocks typically required in transceivers is proposed. By using this method the total current consumption of the transceiver can be efficiently reduced without modifying its performance. A design example where the proposed technique reduces the receiver current consumption by 45 % is given.

6.3.1 Introduction

In a sensor radio, the RF circuits are usually in the dominant role when it comes to the current consumption. For example, in the design examples presented in Sections 6.1 and 6.2, the current consumption of the RF parts is approximately 90 % of the total receiver current consumption. For that reason, power optimization should be concentrated on the blocks and elements operating at the RF. In [5] and [15], the downconversion mixer is stacked on top of the LNA such that the same dc current is re-used in both blocks, thus reducing the total power consumption. However, the stacking of individual blocks is difficult in modern deep submicron CMOS processes due to decreased supply voltages.

The current in the different circuit blocks or stages can be separately adjusted with current boosting, which enables the optimization of the overall noise, linearity, and gain performance [6]. For example, the optimum performance of Gilbert cell downconversion mixers is typically achieved by biasing the switch quad with smaller quiescent current than the transconductance

input stage. In a merged LNA and mixer topology shown in Fig. 6.2, the constant boost current I_{boost} is approximately 70 % of the dc current of the input stage [P1]. A possible way to exploit the PMOS boost source is to use it as an additional transconductance stage [16]. If that method was utilized for the design shown in Fig. 6.2, the boost current source would have been split into two separate devices. As a result, the capacitive loading at the source of the switch transistor increases, which degrades the signal-to-noise ratio [3]. In addition, the gain and noise performance improvement depends heavily on the used circuit configuration. To use the current source more efficiently, a technique where the constant current source is replaced with active blocks used elsewhere in the receiver is described. Compared to the other published current boost solutions, the active blocks used as boost current source are not related to the block having the current boosting. With the proposed solution, the current consumption is efficiently reduced while still maintaining the original performance.

6.3.2 Current boosting with active elements

The LNA merged with a downconversion mixer is shown in Fig. 6.24. Compared to the one presented in Fig. 6.2, the dc current boosting source is replaced by active circuits, which can be any other blocks typically used in a receiver, i.e. LO buffers or baseband circuitry. Because the dc current fed by the active circuits flows to the center tap of the inductor L_1, the possible interference or noise coming from the active boosting will be common-mode at the output nodes of the inductor and thus will not deteriorate the performance of the LNA or mixer. A stabilization capacitor to ground can be included in the center tap of the L_1 to further minimize the interference. In addition, the RF signal at the output of the LNA will be zero at the L_1 center tap, because it is a virtual ground. Therefore, the disturbance between active elements operating in both sides of L_1 center tap is insignificant.

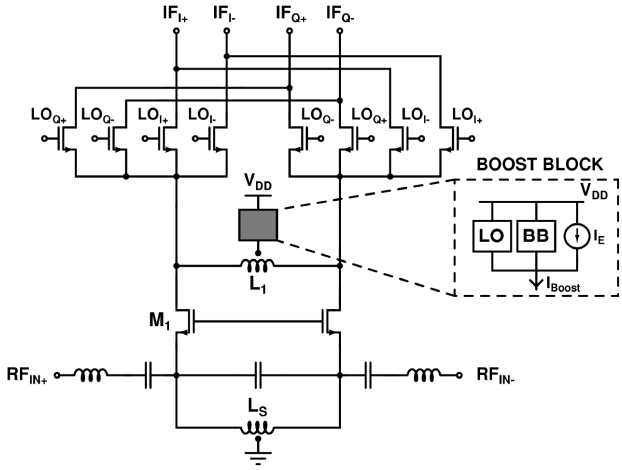

Fig. 6.24. Current boosting with active elements.

The drawback of the solution is that the effective supply voltage of the blocks used in active boosting is reduced by the drain-source voltage (V_{DS}) of input transistor M_1. In addition, the finite series resistances of the inductors L_1 and L_s cause a slight voltage drop. Thus, only those blocks of which the performance does not significantly degrade due to a decreased supply voltage should be placed within the boost block. Furthermore, the total dc current consumption

of the boosting blocks should not exceed the value of the corresponding dc current source I_{boost}. An additional current source I_E shown in Fig. 6.24 can be added to maintain the original biasing of the LNA and switch transistors. Taking into account the process, temperature, and supply voltage (PTV) variations, the dc operation point of different blocks can be adjusted with I_E. Furthermore, it is possible to trade the dc current between the boosting blocks and additional current source I_E. The proposed method is not limited to be used in mixers and receivers only. It can be used in all circuits that use current boosting, while the boost current is injected into the node that is a signal ground.

6.3.3 Design example

The RF front-end presented in Section 6.1 was the basis for this design example. The simulated current consumptions of the merged LNA and mixer and LO buffers were approximately 1.4 mA and 1.1 mA, respectively. The quadrature downconversion mixers are resistively loaded in this design example. The resistor values were chosen such that the dc level at the output node is compatible with the mixer/baseband interface [P1]. Two LO buffers driving quadrature mixers are used as active boosting elements, as is shown in Fig. 6.25.

The design of the LNA is not changed due to the new boosting principle. However, the dc operation point deviation from the nominal state due to process variations requires more attention. If the V_{DS} of the input transistors deviates significantly from the nominal state due to process variations, both the biasing of the input transistors and the operation of the switching stage and boosting blocks may be altered. The quiescent current of the mixer should be accurately controlled, since it also affects the properties of the baseband interface. Because the center tap of the inductor L_1 is a signal ground, a switch transistor can be biased with a current mirror using the center tap of L_1 as a reference node as is shown in Fig. 6.25. As a result, the gate-source voltages of the diode-connected current mirror ($M_{bias,SWI}$) and switch transistor (M_{SWI}) are equal (except the minor voltage drop due to finite series resistance on L_1). The transistors $M_{bias,SWI}$ and M_{SWI} have equal aspect ratios. The slight deviation from 1-to-1 current mirroring is due to non-equal drain voltages. According to the simulations, the drain current variation of a switch transistor in different process corners is less than 7 % from the nominal value and thus the mixer performance is not significantly altered. Thus, the biasing method alleviates the problem related to adequate biasing of the merged LNA and mixer structure described in Section 6.2.2.1.

The LO buffers driving the quadrature mixers are similar to the ones used in [P1] except the tail current sources are omitted. Because both the LNA and mixer switch transistors are biased by current mirrors, the dc current through one LO buffer (I_{LO}) is achieved by subtraction:

$$I_{LO} \approx \frac{1}{2}\left(2I_{LNA} - 9I_{SWI}\right). \tag{6.4}$$

I_{LNA} and I_{SWI} are the dc currents of a single LNA and a switch transistor, respectively, as shown in Fig. 6.25. Because the LO buffers are identical, the dc current is evenly divided between them. If an additional block was placed in parallel with the LO buffers, a serial dc current source would be required to control its current independently. The LO buffer utilized in this design is a self-biasing structure and therefore a separate bias circuit is not needed. In addition,

with the proposed biasing method the operational points of LO buffer devices are nearly unchanged and the performance is not degraded compared to that of the original design.

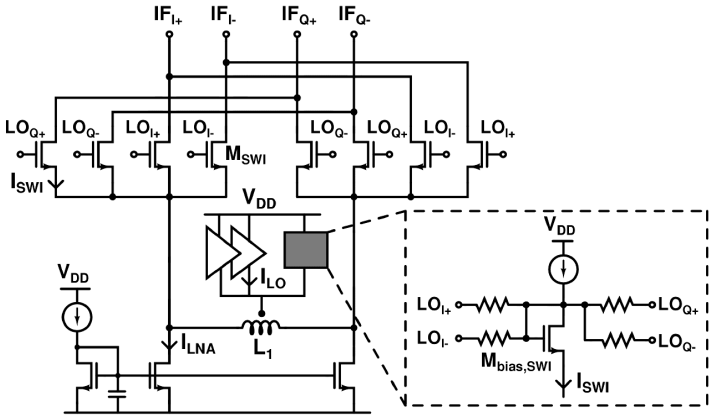

Fig. 6.25. Simplified biasing scheme for the LNA, the switch quad, and the LO buffers.

6.3.4 Simulation results

The total dc current of the LNA was kept at 1.4 mA from a 1.2-V supply. Two LO buffers consume approximately 1.1 mA, which corresponds to nearly 75 % of LNA current. Taking into account the biasing currents, the total current consumption of the design with the active current boosting method is 1.5 mA. If "traditional" dc current boosting was used having LO buffers at a separate dc current path, the total current consumption would be 2.7 mA. Therefore, 45 % current saving is achieved in this design example. The biasing of all blocks and component dimensions remained nearly unchanged compared to the original design [P1]. As a result, according to simulations, a significant difference in conversion gain, input matching, or noise performance is not observed. In addition, no remarkable difference was observed in linearity (IIP3, IIP2) performance, either. While the measurement results are not provided, the simulation results of this and [P1] are comparable, since device sizing, biasing, and modeling are nearly unchanged.

Two LO buffers are operating in a 90-degree phase shift, and a double LO frequency signal is observed at the center tap of L_1 when all the components in LNA, LO buffers, and mixers are fully matched. The signal is at such a high frequency and has such a small amplitude (<1mV$_p$) that its effect on the circuit operation is insignificant. However, in the case of finite device matching in switch quad or LO buffers, a small current signal leaks to the center tap of the inductor at the fundamental LO frequency and causes a several mV signal at the center tap of L_1. That can be attenuated to a negligible level by stabilizing the center tap with a capacitor to ground, as mentioned earlier. The common-mode rejection ratio (CMRR) of the LO signal path is checked because the tail current sources of LO buffers are now omitted. The simulated CMRR in the LO signal path is reduced by only 3 dB, this being negligible degradation compared to the original design.

6.4 A direct-conversion RF front-end in a 65-nm CMOS

This sub-section demonstrates 65-nm CMOS RF circuit design for wireless applications operating in the 2-GHz frequency area. It should be noted that the presented design example is not directly related to the subject of the other two main applications (short-range sensors or UWB). However, it contains slightly different, but nevertheless relevant, circuit design details compared to the other design examples. It therefore completes the material presented in this chapter.

The simplified block diagram of the direct-conversion RF front-end is shown in Fig. 6.26. The RF front-end consists of a low-noise amplifier (LNA), folded quadrature mixers, a local oscillator (LO) divider, and LO buffers. The front-end consumes 29.3 mA from a 1.2-V power supply and, according to simulations, it achieves 39-dB voltage gain, 1.5-dB minimum spot noise figure, and –17-dBm IIP3. Because of the low-resistivity CMOS substrate, all the signal paths are balanced to achieve immunity to the substrate noise and interferers.

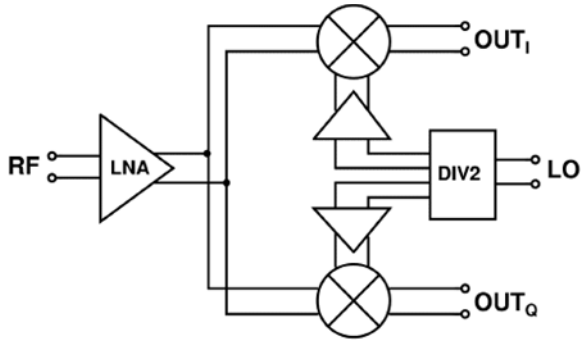

Fig. 6.26. Block diagram of the RF front-end.

6.4.1 RF front-end design

6.4.1.1 Low-noise amplifier

The LNA shown in Fig. 6.27 is a balanced inductively degenerated common-source amplifier with a cascode stage. The LNA consumes 5.4 mA without biasing. The minimum channel length was chosen for the LNA input transistors to optimize the f_T of the transistor and to test the process gain and noise performance. The input matching of the LNA is realized with an on-chip source inductor L_S and shunt capacitor C_S between the gate and source of the input transistor, and an off-chip capacitor C_{in} and inductor L_{in}. The input matching better than –10 dB is achieved in the band of 2.1 GHz – 2.6 GHz. The load of the LNA is a resonator consisting of a 1.9-nH differential inductor and 2-pF capacitance. Two separate 1-pF capacitors units were used in parallel to achieve symmetrical parasitics at output nodes. In addition, the resonator Q-value is decreased with a shunt resistor to widen the bandwidth of the resonator.

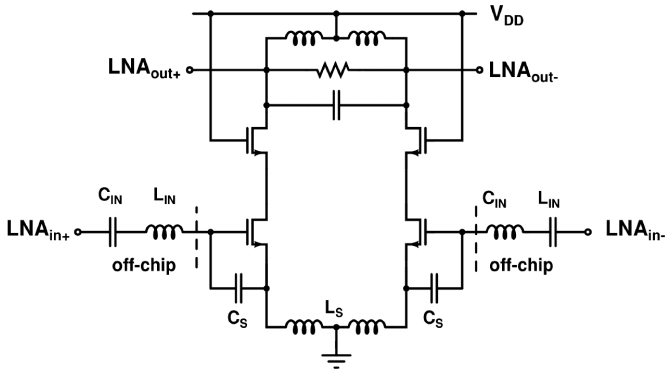

Fig. 6.27. Simplified schematic of the LNA.

The voltage gain and noise figure (NF) of the LNA are shown in Fig. 6.28. According to simulations, a 1.2-dB noise figure is achieved with 22-dB voltage gain at 2.45-GHz frequency. The simulated IIP3 and ICP of the LNA are approximately 0 dBm and –5 dBm, respectively. According to simulations, no severe noise, gain, or linearity penalty was incurred due to minimum channel length devices when using this topology.

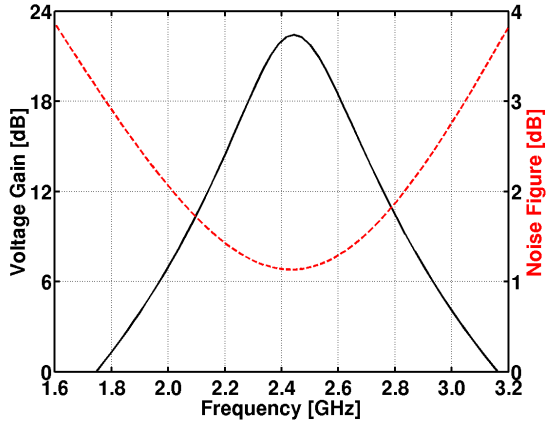

Fig. 6.28. Simulated LNA voltage gain and noise figure.

6.4.1.2 Quadrature mixers

The folded structure shown in Fig. 6.29 was chosen to avoid the stacking of different mixer blocks. As a result, sufficient voltage headroom was achieved for input stage, switch stage, and load. In addition, to optimize the gain, linearity, and noise performance, the dc current of both the mixer input and switch stages can be adjusted separately.

The input stage of the mixer consists of a common-source amplifier. Both the amplifier and cascode stages have 140-nm channel length to achieve better linearity performance compared to minimum length devices. The input stage consumes 13 mA without biasing. A pretty large dc current is needed to achieve a sufficient linearity and voltage gain before the switching stage.

The high impedance needed for folding could be obtained with current sources, but due to limited supply voltage device stacking should be avoided, thus leading to the use of an LC

resonator. The resonator consists of an on-chip 1.9-nH inductor, 1.2-pF shunt capacitance between the outputs (two 600-fF capacitor units in parallel for symmetrical parasitics), and two 1.2-pF capacitors from the output to the V_{DD}. With the latter capacitors, the effect of the parasitic capacitance of the following switching stage is not dominating. The inductor tunes the resonator to the wanted frequency and it also minimizes the noise contributed at the source node of the switch transistors [3].

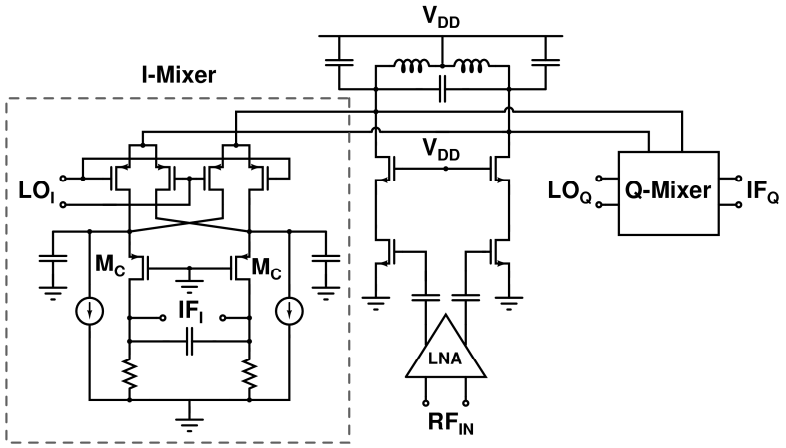

Fig. 6.29. Simplified schematic of the quadrature mixer.

The scaled RF response at the mixer resonator output is shown in Fig. 6.30. The resonator has high impedance at the wanted frequency, but the impedance is lower at other frequencies. As a result, the standing wave at double LO frequency produced by the mixing pair is attenuated. Thus, the voltage swing across the drain-source terminals of both mixer input stage and switch transistors is lowered which results in improved IIP3 [17]. In addition, also IIP2 of the mixer is improved, because the resonator has low impedance at the frequency of $|f_{RF1} - f_{RF2}|$, thus attenuating the second-order intermodulation generated by the input stage of the mixer [18].

The PMOS transistors are used as switches to minimize the flicker noise. The $1/f$ noise is further optimized by using as small a quiescent current as possible. However, too small a dc current can degrade the linearity performance. Eventually, for a single switch transistor, the nominal dc current of approximately 320 μA was chosen. In addition, the channel length of the switch transistors was optimized as 220-nm to improve the $1/f$ noise performance but to not deteriorate the operation of the LO buffers. Furthermore, device matching is better with non-minimum channel length transistors.

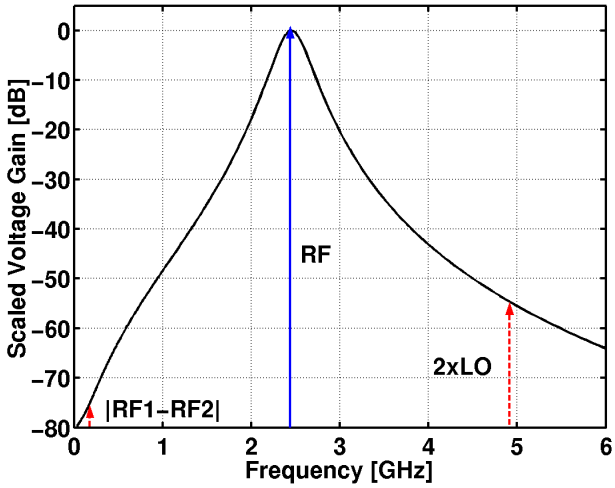

Fig. 6.30. Scaled voltage gain at the mixer resonator output.

This mixer was designed to drive voltage mode output. Therefore, RC-impedances are used as a load to improve the mixer out-of-band blocking characteristics and to relax the linearity requirements for the following blocks. The floating capacitor is used to minimize the value and the area of the load capacitor. The RC pole frequency is approximately 10 MHz. It was chosen pretty arbitrarily, because this prototype chip is not intended for any particular application. For better isolation and larger voltage gain, the RC-loads were separated from the switch transistors with PMOS cascode transistors M_C. The cascode devices have negligible effect on overall noise performance. In transient simulations, it was found that the double-frequency LO signal at the drain node of the switch transistors modulates the V_{DS} voltage of the cascode transistor. For that reason, an additional capacitor was added before the cascode stage. As a result, the double-frequency LO signal over the drain-source terminals of cascode stage is attenuated by 10 dB.

Finally, part of the quiescent current of the switch transistors is removed before the cascode stage with NMOS current sources. As a result, the load resistor value can be chosen more freely to have a sufficiently large voltage gain but not to cause voltage drop. In addition, according to simulations, also the IIP3 and NF results are improved. The length of the current source transistors was set to 4 μm so that the effect of the 1/*f* noise is insignificant. In this design, a 1.2-kΩ load resistor value was chosen to achieve adequate gain, noise, and linearity.

6.4.1.3 Quadrature LO signal generation

The quadrature LO signal was generated from an external LO source by using the frequency divider presented in Fig. 6.31 [19]. With a double-frequency LO signal, several problems related to direct-conversion, such as LO leakage to the RF input, can be minimized. The divider topology was chosen in this design because only two transistors are stacked and a large 1.8-V_{pp} differential LO-signal swing is achieved. In addition, it does not require resistors, thus being more tolerant to process variations. The minimum length was chosen to maximize the speed of transistors. The nominal current consumption of the divider is 3.2 mA. In typical use (f_{in}<5GHz), the divider requires a rather small (<50mV_{pp}) input signal for injection locking. By

increasing the current consumption by 65 % and LO input signal amplitude to 170 mV_{pp}, the divider can operate with input frequencies as high as 9 GHz.

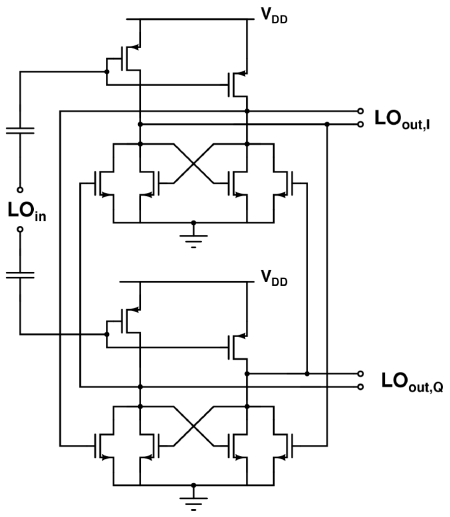

Fig. 6.31. Schematic of the LO divider.

The divider is sensitive to capacitive load. Usually, it cannot directly drive the gate capacitance of the switch transistor and therefore LO signals need to be buffered before mixers. In this design, the balanced LO buffers shown in Fig. 6.32 were used [P1]. The transistors M_n and M_p have minimum channel length to minimize the parasitics. Due to relatively high V_T, careful optimization is required not to force the current source M_5 into linear region. The capacitor C_2 is required to decrease the effect of the noise of the LO buffer. Otherwise, the buffer upconverts the low-frequency noise coming from the bias circuit to the LO frequency. The current consumption of one buffer is nominally 0.5 mA without biasing.

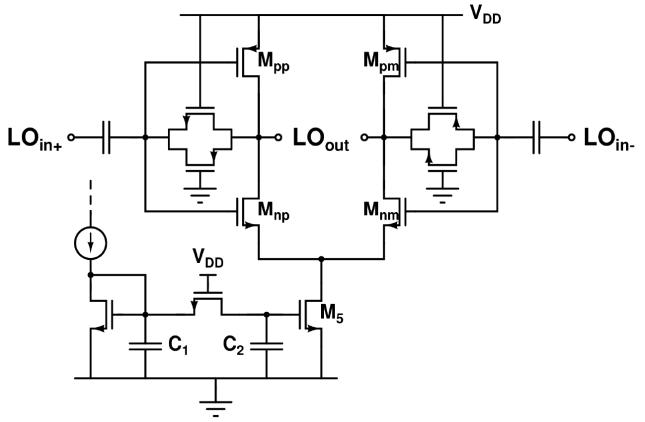

Fig. 6.32. Schematic of the LO buffer.

6.4.1.4 Simulation results

The voltage gain, IIP3, and ICP of the whole front-end simulated from the mixer output are approximately 39 dB, –17 dBm, and –29 dBm, respectively. The spot noise figure as a function of intermediate frequency (IF) is shown in Fig. 6.33 with a solid line. The minimum noise figure is 1.5 dB. The 1/*f* noise corner frequency is approximately 400 kHz, and thus it can increase the total NF in narrowband applications. For a comparison, an integrated NF starting from 100 Hz is shown with a dashed line in Fig. 6.33. As can be seen, a sub-3dB total NF, for example, is achieved with applications having an IF bandwidth of approximately 4.7 MHz. The summary of the front-end performance is given in Table 6.3.

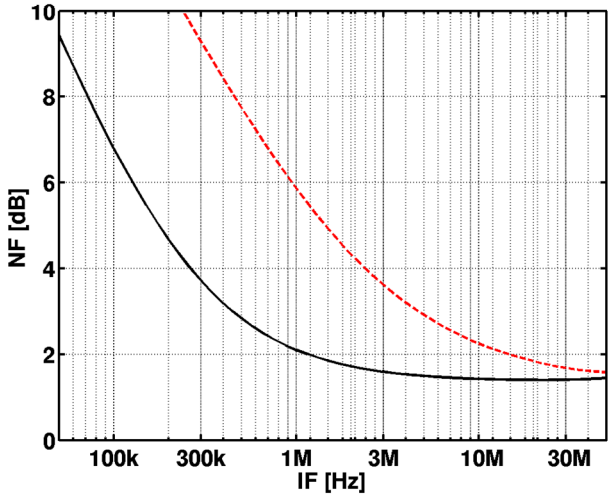

Fig. 6.33. NF as a function of IF frequency. The spot NF is presented with a solid line and the integrated NF starting from 100 Hz is shown with a dashed line.

Table 6.3. The simulated front-end performance.

Parameter	Unit	Result
Supply voltage	V	1.2
Supply current	mA	29.3
Voltage gain	dB	39
NF (minimum)	dB	1.5
NF (100 Hz … 2.5 MHz)	dB	3.9
NF (100 Hz … 4.7 MHz)	dB	3.0
1/*f* noise corner frequency	kHz	400
Out-of-channel IIP3	dBm	–17
ICP	dBm	–29
S_{11}	dB	< –10

6.5 Low-noise amplifiers for UWB

In this sub-section design examples of low-noise amplifiers for UWB are given. The first design example is based on inductively degenerated common-source (IDCS) LNA. The LNA operates in the 3.1 – 4.7 GHz band. The purpose of this design example is to compare the basic IDCS topology to the two alternatives presented in Section 3.3.2 and 3.3.3. The second design example covers the design of a common-gate LNA. The center frequency is set to 5 GHz and the target is to cover the frequency band of 3 – 8 GHz. The CG LNA theory presented in Section 3.3.7 was utilized to design the input matching resonators.

6.5.1 Inductively degenerated CMOS low-noise amplifiers for BG1

Fig. 6.34 shows three balanced IDCS LNAs designed for BG1: i) without any feedback, ii) with RC feedback, and iii) with an additional CG signal path. The balanced structure was chosen to achieve immunity to the substrate noise and interferers. The simulations were performed with a 0.13-µm CMOS process. The input and cascode transistor size, biasing, and the value of inductors were kept unchanged to achieve comparable results. The LNA core consumes approximately 7 mA from a 1.2-V supply. In case iii) the CG transistor has approximately 3-mS g_m. The feedback resistor in case ii) was chosen as 700 Ω to obtain a comparable NF with case iii). The bonding pads were also included in the simulations to achieve realistic parasitic capacitance at the input node.

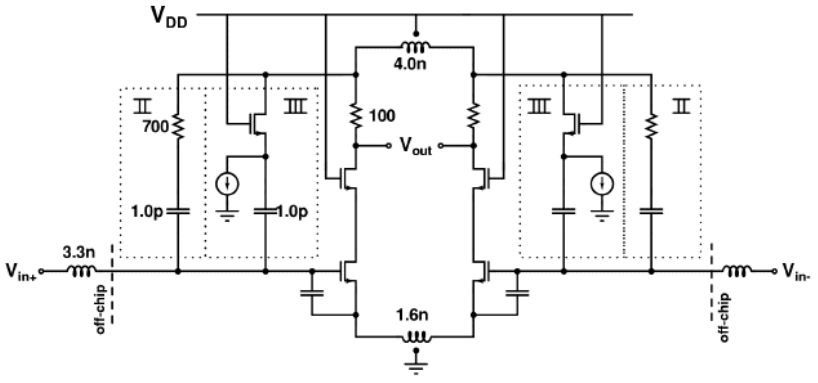

Fig. 6.34. IDCS LNA i) without any feedbacks, ii) with RC-feedback, iii) with additional CG signal path.

The S_{11}, insertion gain, and NF were simulated and the results are shown in Fig. 6.35 and Fig. 6.36. It can be seen from the results that the basic IDCS LNA without any feedback has the narrowest BW_{S11}. In addition, it is the most sensitive to the parasitic capacitance of the input pad. The LNA with additional CG path or RC feedback have approximately 30 % wider BW_{S11} compared to the basic IDCS LNA. In addition, both topologies cover the whole BG1. However, the RC feedback reduces the reverse isolation by 5-6 dB compared to the basic IDCS topology with these component values. The LNA with CG path does not suffer from reverse isolation degradation.

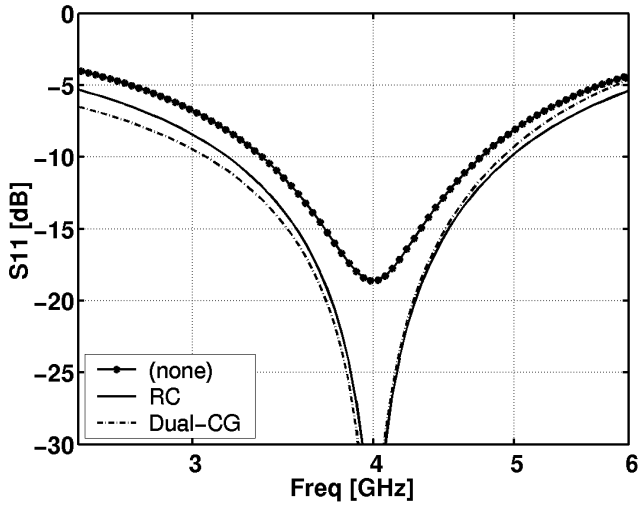

Fig. 6.35. S_{11} with different input matching setups.

The effect of the input matching circuit to the gain BW can be observed from Fig. 6.36. The S_{11} mismatch for the basic topology causes a slight gain peaking compared to other two topologies. That also affects the NF, but the NF difference of the basic IDCS LNA compared to two variants is small. The LNA with RC-feedback has the narrowest BW. To achieve wider operation, the feedback resistor should be larger, but that would cause narrower BW_{S11}. The LNA with an additional CG path has the best gain flatness over BG1 frequencies. In addition, its maximum insertion gain frequency is closer to the input matching frequency when compared to the other two LNAs. That was also detected in Section 3.3.3, where IDCS LNA variants were simulated with ideal components.

In this design example, the LNA with dual CG path gives the most promising performance, when S_{11}, gain, and NF should cover the BW between 3.1 – 4.7 GHz. Finally, with component values used in this example all cases had similar IIP3 performance.

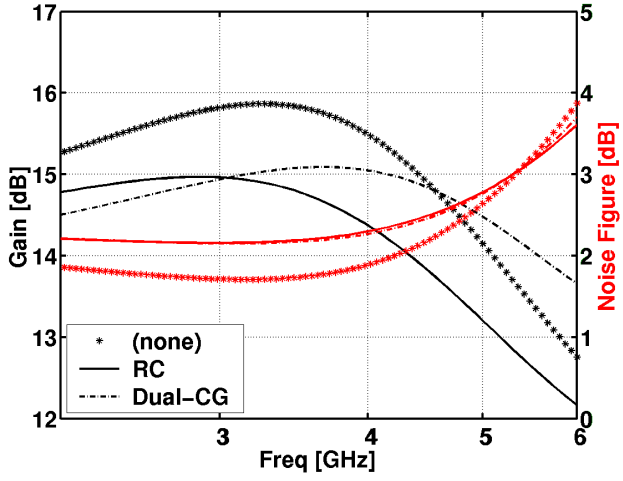

Fig. 6.36. Insertion gain and NF with different input matching setups.

6.5.2 Common-gate LNA for BG1 and BG3

The design of a CG LNA, which covers the UWB band groups #1 and #3, i.e. 3 – 8 GHz, is presented. For simplicity, a single-ended structure was chosen, but the analysis presented in Section 3.3.7 can be utilized for a balanced CG LNA, too. The schematic of the LNA is shown in Fig. 6.37. The bonding pad was included in the simulations to achieve realistic parasitic capacitance at the input node. The transistor M_1 was biased with a 1.2-mA current from a 1.2-V supply voltage. The source impedance Z_0 was 50 Ω. The simulations were performed with a 0.13-μm CMOS process.

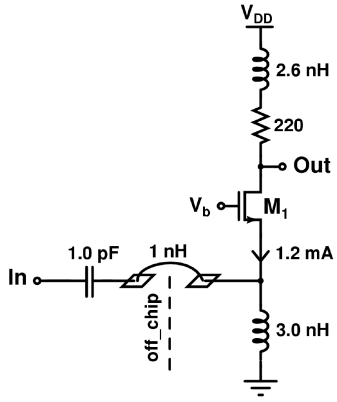

Fig. 6.37. Simplified schematic of CG LNA.

The desired band is 3 – 8 GHz and the center frequency is approximately 5 GHz. Therefore, the relative bandwidth is 1. First, the design criteria for source and input resonators are estimated from Fig. 3.27 and Fig. 3.28. To achieve better than –10 dB S_{11}, which covers the whole band with some design margin, the required minimum relative impedance Z_{rel} for the source resonator is 1.5. The input series resonator should be dimensioned with a p value higher than 2.

According to (3.61), the source resonator tuned at 5 GHz frequency should have at least a 2.4-nH inductor for the desired Z_{rel}. The source resonator was realized without additional shunt capacitance and the resonance at 5 GHz frequency was achieved with a 3.0-nH inductor. The input matching without the series input resonator is shown in Fig. 6.38 with a solid line. The source resonator gives S_{11} better than –10 dB from 2.7 GHz to 8.8 GHz. The relative bandwidth is 1.22, which is close to the theoretical value 1.26 given by (3.61). The Z_{rel} of the source resonator is evaluated with (3.68): $Z_{rel} = 1.83$.

According to (3.74), the optimal value for p would be 6.7 to maximize the overall $BW_{rel,S11}$. Because the Z_{rel} was slightly overdesigned, a smaller p value can be chosen and still achieve the required S_{11}. The S_{11} of the whole LNA was simulated with the p values of 2, 3, and 4. The results are shown in Fig. 6.38 with dashed lines. The BW_{rel} increases along with p according to the theory. The p value between 2.5 to 3 gives the required S_{11} bandwidth. With larger p values, the BW_{S11} is improved, but the value of the input inductor L_{in} gets smaller. Therefore, it is possible that optimal L_{in} is not reached due to limitations set by the bond wire inductor to package or PCB.

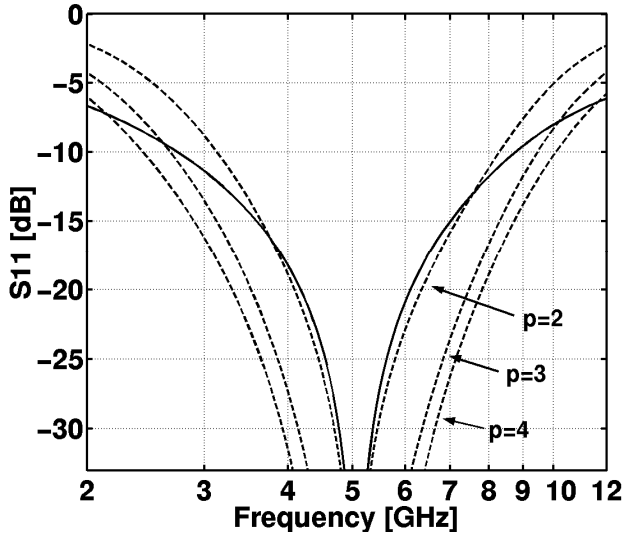

Fig. 6.38. Simulated S_{11}. The effect of the source resonator is shown with a solid line. The dashed line shows the whole S_{11} with several p values.

The insertion gain and NF are shown in Fig. 6.39 with p values of 2, 3, and 4. The gain and NF are approximately 12 dB and 4 dB over the whole wanted band. Both the gain and NF bandwidths increase along with p. However, the highest operational frequency is limited by the shunt-peak load and the parasitic capacitance at the output node. Therefore, scaling the p does not improve the BW at high frequencies. The gain is decreased at 8 GHz frequency by approximately 1 dB from the maximum value. To increase the operational BW at high frequencies, the value of the load resistor should be lower. As a result, the gain would degrade as well.

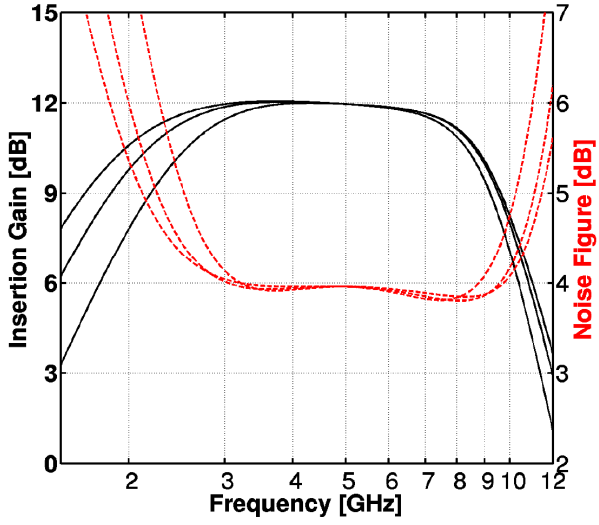

Fig. 6.39. The solid line presents the simulated insertion gain and the dashed line shows the NF with p values of 2, 3, and 4. Both the gain and NF BW increase along with p.

The Q-value of the input circuit and the IIP3 of the LNA is presented in Fig. 6.40. Both parameters are given with p values of 2, 3, and 4, and the results are shown with solid, dashed, and dashed-dotted lines, respectively. As can be seen, with p value of 2, the additional gain due to input matching resonators is low, which is predicted by (3.66). The Q_{in} increases along with larger p values. This also decreases the IIP3 by about the same amount.

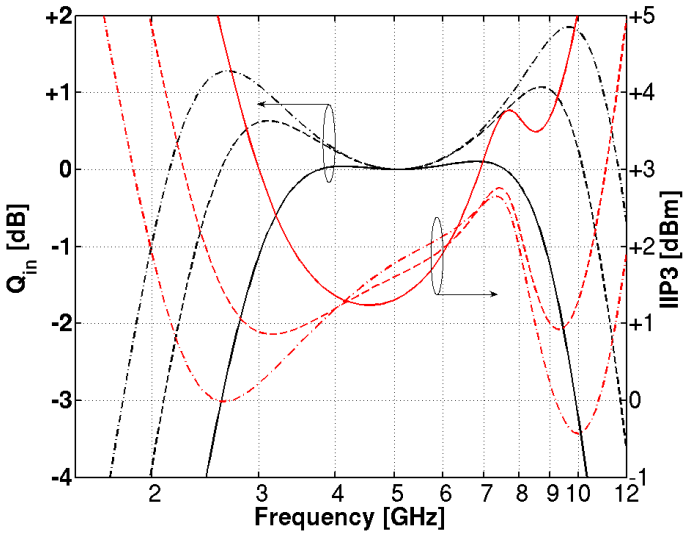

Fig. 6.40. Simulated Q-value of the input resonators and IIP3 with p values of 2 (solid line), 3 (dashed line), and 4 (dashed-dotted line).

In this design example, the implementation of a sufficient input matching network was limited by the minimum length of the input bond wire. The upper limit for the gain was set by the parasitic capacitance of the output node. According to the design example, it is possible to achieve a unity relative BW at 5 GHz center frequency with a simple CG LNA. The simulation results are in good agreement with the theory.

6.5.3 Conclusions

According to the two presented LNA design examples, several points can be noted. The design of a wide input matching circuit is easier with a CG topology, because wider bandwidth can be achieved and the parasitic capacitance associated with the input node can be embedded in the input matching network. The current consumption of a single branch of the balanced IDCS LNA was roughly triple compared to the single-ended CG LNA. The major disadvantage of the CG LNA is the higher noise figure compared to IDCS LNA. In addition, the gain of the CG LNA is several dBs lower, which can increase the noise contribution of the following stages. Therefore, if the target is to cover just a single BG, the IDCS LNA usually offers better NF and gain performance.

6.6 A dual-band direct-conversion RF front-end for WiMedia UWB receiver

6.6.1 Introduction

This section describes a direct-conversion RF front-end designed for dual-band WiMedia UWB receiver. The front-end operates in band groups BG1 and BG3, i.e. 3.1 – 4.8 GHz and 6.3 – 7.9 GHz, respectively. The UWB receiver is targeted for a mobile handset, where several other radios can be simultaneously on. Therefore, special attention was paid to minimizing the interference from different wireless systems. The front-end achieves approximately 26-dB gain and 4.9 – 5.6-dB noise figure across three sub-bands of BG1. In BG3 mode, it obtains 23 – 26-dB gain and 6.9 to 7.7-dB NF. The front-end consumes 48.1 mA and 42.7 mA from a 1.2-V supply voltage in BG1 and BG3 operation modes, respectively.

6.6.2 Front-end design

The block diagram of the direct-conversion front-end is presented in Fig. 6.41. It includes low-noise amplifiers (LNA), quadrature downconversion mixers, a passive polyphase filter for quadrature local oscillator (LO) signal generation, and LO buffers. All the signal paths are balanced to achieve immunity to substrate noise and interferers. The front-end is targeted to co-operate with the analog baseband filter similar to the one presented in [20].

The use of a wideband LNA covering the whole UWB band is questionable in a multi-system environment, since a strong unwanted signal at any frequency in the reception band can desensitize the whole front-end. In this design, the first LNA stages are separate for BG1 and BG3 operation modes. The significant benefit achieved at the cost of individual pre-selection filters utilized for both inputs is the improved suppression of strong interferers. The other radios operating in the 5-GHz frequency band and at lower frequencies (common RF systems around and below 2 GHz) are more efficiently attenuated than with a single wideband pre-filter covering the whole UWB reception band. In addition, since the systems operating around 2.4 GHz are relatively close to the lowest frequency of BG1, the LNA1 includes a high-Q 2.4-GHz notch filter to further improve the attenuation.

With modern deep-submicron CMOS processes it is challenging to design wideband amplifiers with several GHz bands. The intrinsic gain from a single transistor is moderate and typical resonator loads used in narrowband applications must be replaced with wideband structures. As a result, the gain achieved from a single-stage amplifier may not be sufficient. Therefore, multi-stage LNAs were implemented to have adequate bandwidth and gain before the mixers.

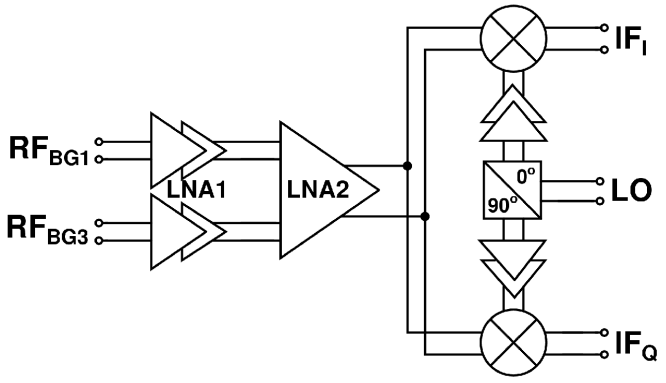

Fig. 6.41. Block diagram of the UWB front-end.

6.6.2.1 First LNAs (LNA1)

The schematic of the BG1-LNA1 is shown in Fig. 6.42. The LNA core is based on a typical inductively degenerated common-source (IDCS) structure. It was chosen because it offers satisfactory noise, linearity, and gain performance. However, it is challenging to achieve proper input matching for a UWB system with this topology, even though the matching would be only needed for one BG at time, as in this design. As was shown in (3.33), the achievable input matching bandwidth (BW_{S11}) is proportional to the source impedance Z_0 and inversely proportional to the sum of input (L_{in}) and source inductor (L_S) values. The input is matched to 100 Ω differentially, and therefore Z_0 cannot be altered. When the effect of process deviation and practical component values are taken into account, an S_{11} sufficiently wide for the BG1-LNA with IDCS topology could not be obtained. Therefore, an additional common-gate (CG) transistors (M_{CG}s) connected to the LNA input were added. As was shown in Section 3.3.3 and in the design example presented in Section 6.5.1, the transconductance of M_{CG}s improve BW_{S11}, but the cost is slightly increased noise. In addition, due to the low-impedance signal path caused by CG transistors, the resulting input matching circuit is less sensitive to the parasitic capacitance caused by the pad with ESD protection diodes than a basic IDCS input stage.

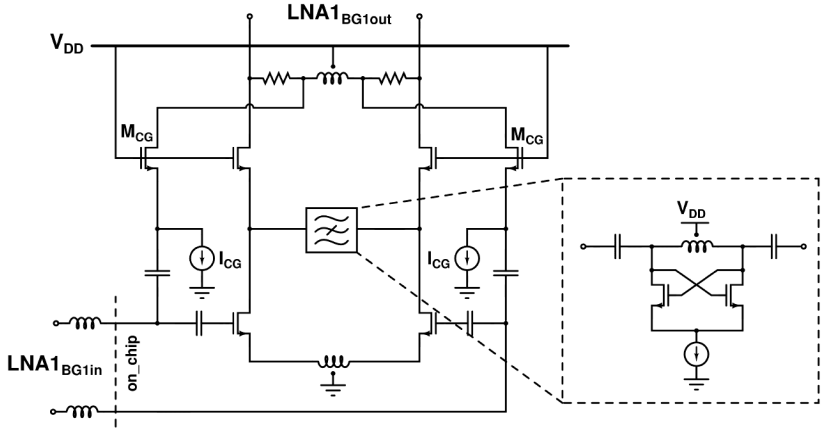

Fig. 6.42. Schematic of the BG1-LNA1.

The BG1-LNA1 includes an additional LC notch filter tuned at 2.45 GHz to further suppress interferers at this frequency. For example, due to the 3rd-order nonlinearity, the interferer at 2.4 GHz together with 900-MHz GSM can corrupt UWB signal reception. The notch includes a cross-connected NMOS pair to improve the Q-factor of the resonator [21]. The notch is connected at the IDCS stage, which is the main source of the nonlinearity. Thus, although the CG stage bypasses the notch filter, the interferers leaking through this path do not degrade the performance.

The BG3-LNA1 is also based on the basic IDCS topology. The additional CG signal path is not utilized in BG3 because the parasitic capacitance at the input would become too large, thus deteriorating the input matching. The sum input bond wire and source inductor values are less than 3 nH per input. As a result, according to (3.33), the input matching bandwidth is approximately 2 GHz. Thus, BG3 input can be covered without any feedback or additional signal paths. However, the BG3 input is rather sensitive to the parasitic capacitance at the input node. To minimize the capacitance caused by the bonding pad, the modified pad structure presented in Section 3.4 was utilized.

Both BG1-LNA1 and BG3-LNA1 utilize a shunt-peak load. Different load structures were presented in Section 3.5.2. While various wideband load structures exist, a shunt-peak load is typically used in single-stage balanced amplifier since the number of on-chip inductors should be kept as small as possible.

6.6.2.2 Buffer

The LNA1 cannot provide enough gain before the mixers, and therefore a second amplifier (LNA2) is needed. The design of the LNA2 is a trade-off between having large enough input devices to achieve the required gain but not to cause capacitive loading for the LNA1. To maintain the freedom to optimize the performance of both LNA stages, a buffer shown in Fig. 6.44a is used between them.

The buffer has approximately unity voltage gain with a wide frequency band without inductors. The output impedance of the buffer is low, and therefore it can sustain large output capacitance. The voltage gain of LNA1 is moderate, and thus the linearity of the buffer is not the limiting factor on the whole signal chain. In addition, its contribution to the total front-end noise is less than 0.3 dB. The simulated buffer response is shown in Fig. 6.43. The response of the buffer is shown, with and without feedback capacitor C_{fb}, with solid and dashed lines, respectively. The gain is scaled to 0 dB at zero frequency for the purpose of comparison. Without the C_{fb}, the buffer is a traditional source follower and M_2 acts as a current source only. Then, the –3-dB band hardly exceeds 2.5 GHz frequency. The operational bandwidth is extended by several GHz by adding a feedback loop from the drain of M_1 to the gate of M_2.

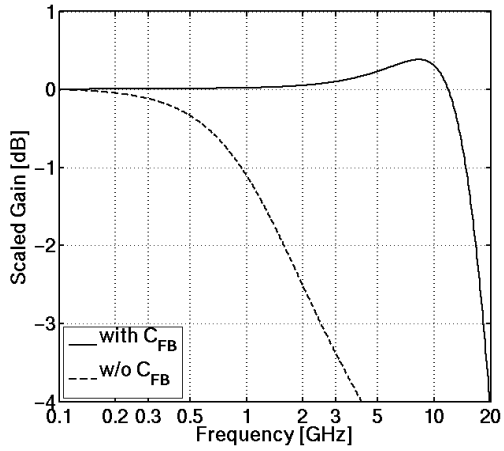

Fig. 6.43. Simulated frequency response of the buffer with and without capacitor C_{fb}.

6.6.2.3 Second LNA (LNA2)

The purpose of the LNA2 is to combine the signal paths and to provide the remaining gain before the mixers. The simplified schematic of a resistor-feedback LNA used as LNA2 is shown in Fig. 6.44b. The analysis of the basic operation principle of this type of amplifier is presented in, for example, [22] and [23]. This amplifier topology was chosen because it achieves wide operational BW and parasitic capacitance at the node $LNA2_{out}$ causes only slight gain degradation. Therefore, additional buffers before mixers are not needed.

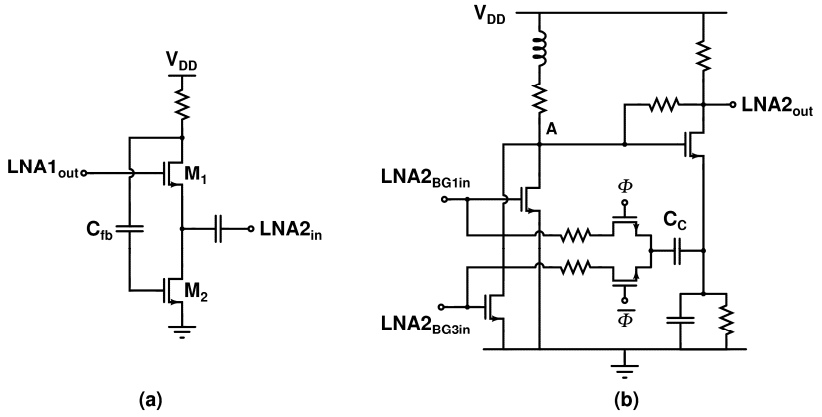

Fig. 6.44. a) Schematic of the buffer between LNA1 and LNA2 (single-side view only), b) schematic of the second LNA (single-side view only).

Compared to those presented in the literature, this design includes a shunt-peak load to widen the operational bandwidth of basic resistor-feedback LNA. In addition, the capacitor C_C was added to prevent the dc current flowing from input nodes to the feedback loop. Otherwise, the bias current of the input transistor would be sensitive to the process variations. The signal path is combined at the drains of the input devices and the feedback path from gate of the input device to the source of the output device has an additional switch to isolate the non-operational input from the operational one.

6.6.2.4 Downconversion mixers

The schematic of the downconversion mixers is shown in Fig. 6.45. The quadrature mixer is based on a basic Gilbert cell, where the output signal of the LNA2 is directly fed to the switching stage. Therefore, the quadrature mixer is a low-impedance load for the LNA2. With this kind of LNA/mixer interface, a wider operational BW is achieved compared to a mixer with a typical CS input stage.

The quiescent current of the switch transistors is set by current sources. The dc levels of the IF output nodes are set to 0.7 V such that the compatibility with targeted baseband filter [20] is achieved.

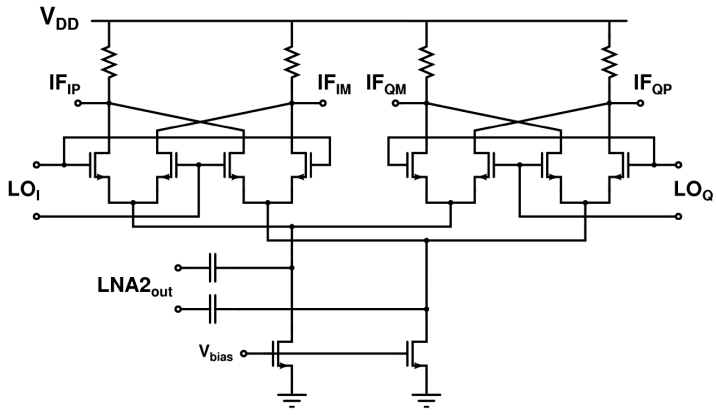

Fig. 6.45. Schematic of downconversion mixers.

6.6.2.5 LO signal generation

The local oscillator (LO) generation chain is designed such that the operational band uniformly covers the BG1 and BG3 frequencies, i.e. 3 – 8 GHz. The quadrature signal was generated from an external LO signal source with a three-stage passive polyphase filter (PPF). According to the simulations, the PPF causes approximately 8-dB loss for the LO signal. The losses were compensated with the LO buffer shown in Fig. 6.46. It consists of a two-stage amplifier, where the first stage is a CS amplifier with a cascode stage. Current source I_B was utilized to boost part of the cascode current. As a result, the dc drop at the output of the first stage is decreased and sufficient performance is maintained in process corners. If the switch transistors of the mixer were directly connected to the output of the first LO buffer stage, the capacitive loading would deteriorate the BW. Therefore, to be able to drive the mixer gate capacitances, buffer topology similar to that was used between LNA1 and LNA2 is utilized as the second stage of the LO buffer.

An LO signal with a constant level over a wide frequency band is required to achieve a flat conversion gain response from the mixers. However, only one differential inductor is wanted per buffer for a compact layout. Therefore, the differential inductor of the modified shunt-peak load presented in Section 3.5.3.2 is re-used in both stages. According to the simulations, the presented method increases the −1-dB band by 2 GHz at the band of interest when compared to a buffer where a single load inductor was used only for one or other of the stages. In addition,

the achieved bandwidth is wider even compared to a case when separate load inductors for both stages were used. Therefore, bandwidth extension is achieved with a single load inductor only.

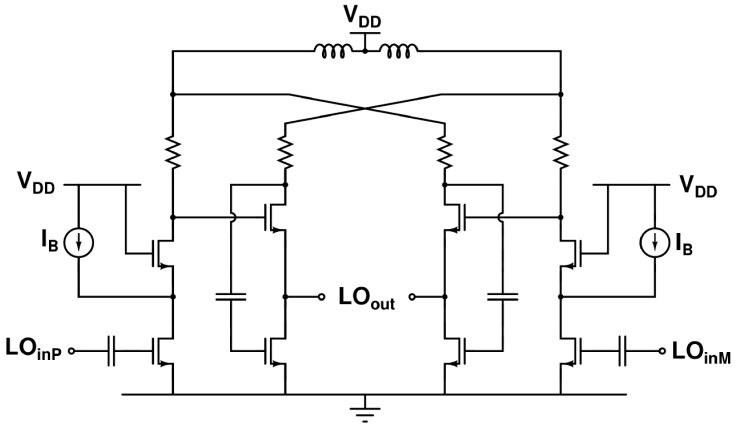

Fig. 6.46. Schematic of the LO buffer with bandwidth extension load.

6.6.3 Experimental results

The chip was fabricated in a 0.13-μm CMOS process and the chips were directly bonded onto a printed circuit board (PCB). The gain, noise, and linearity performances of the front-end were verified from IF outputs with an external high-impedance buffer.

The gain and input matching of the receiver in BG1 are shown in Fig. 6.47 with solid and dashed lines, respectively. The gain is approximately 26 dB and the gain deviation is less than 2 dB over the 3.1 – 4.8 GHz band. The gain starts to degrade after 5.4 GHz. The S_{11} at the BG1 band is better than –9 dB. The notches seen in S_{11} response are due to the PCB. The center frequency (f_C) of the LC notch filter is located at 2.3 GHz. Due to the slight deviation from the targeted f_C of 2.45 GHz, some of the linearity tests are performed at 2.3 GHz as shown later. The $1/f$ noise corner frequency is approximately 2 MHz. Because the BW of the external buffer utilized in measurements is limited, the output noise is integrated from 2 MHz to 30 MHz. That will give a result comparable with the other reported designs, because the flicker noise averages along with increasing IF frequency. The measured noise figures of different BG1 sub-bands are 4.9 – 5.6 dB. When the additional CG path of the BG1-LNA1 was shut off, the gain increased approximately by 1 dB and the NF lowered to 3.6 – 4.7 dB. The S_{11}, however, degraded to –6 dB in the worst case, which shows the effectiveness of the CG transistors.

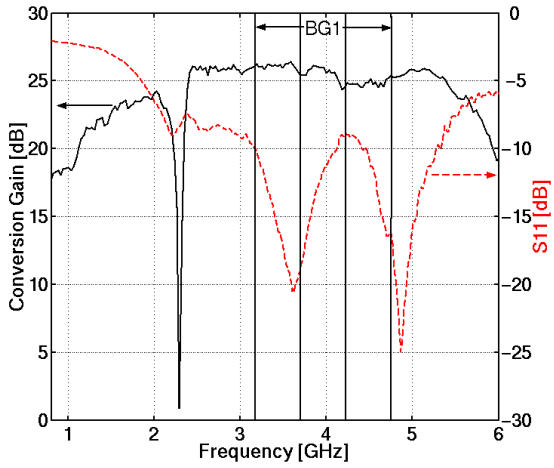

Fig. 6.47. Conversion gain and S_{11} of the BG1.

The gain and S_{11} in BG3 mode are shown in Fig. 6.48 with solid and dashed lines, respectively. The maximum gain is approximately 26 dB and the gain deviation over 6.3 – 7.9 GHz band is approximately 4 dB. The measured NF of BG3 sub-bands are 6.9 – 7.7 dB. Due to the high operational frequency, the optimization of the PCB input was challenging. Despite the PCB modeling, the notches of S_{11} are nearly at a 1 GHz lower frequency than targeted. Therefore, even more effort should be applied to PCB design and modeling to achieve adequate performance at the wanted frequency band.

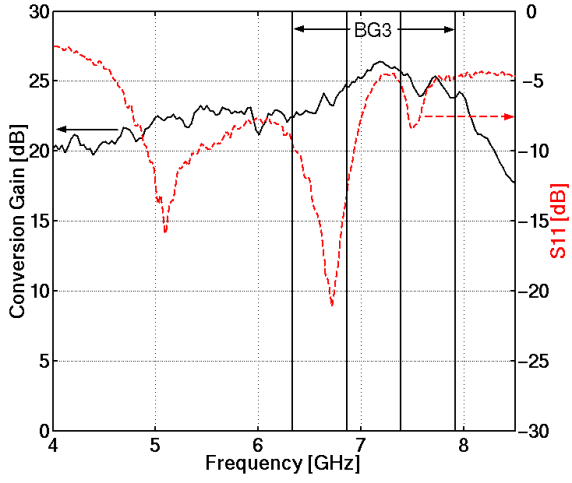

Fig. 6.48. Conversion gain and S_{11} of the BG3.

The front-end IIP3 performance was measured by using typical two-tone test signals at 20-MHz and 39.8-MHz offsets from the LO frequency. The in-band IIP3 result is approximately –16 dBm and –20 dBm in BG1 and BG3, respectively. The IIP2 was measured with test tones having 19.8-MHz and 20-MHz offsets from the LO frequency. The IIP2 result was approximately +20 dBm among BG1 and BG3 sub-bands.

The intermodulation caused by the GSM900 transmitter (f_{RF1}) and 2.4-GHz interferer (f_{RF2}) was measured by applying test signals at 880 MHz and 2.25 – 2.33 GHz into BG1 input, such that the latter signal is 15 dB stronger than the former. The most harmful interferers locating at UWB BG1 band were downconverted from the frequencies of 2 x $f_{RF1} + f_{RF2}$ and 2 x $f_{RF2} - f_{RF1}$. The corresponding out-of-band IIP3 result is +1 dBm for both cases. The measured result at the latter frequency is presented in Fig. 6.49.

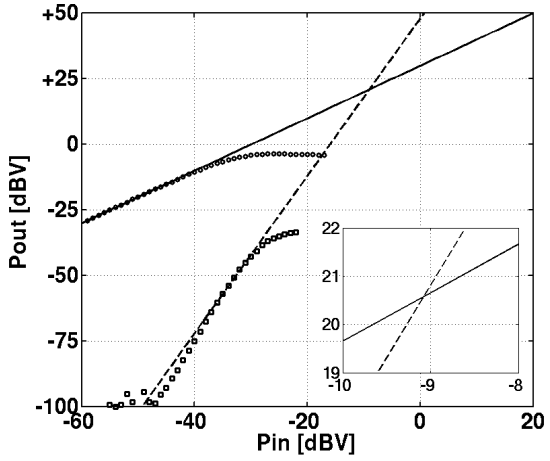

Fig. 6.49. Intermodulation caused by GSM900 transmitter and 2.4-GHz interferer.

The in-band input compression point (ICP) is better than –27 dBm and –29 dBm in BG1 and BG3, respectively. The desensitization of the front-end was characterized by supplying a strong interferer at frequencies below 3 GHz such that the wanted weak signal is at BG1. The level of the interferer, which causes the gain of the wanted signal at BG1 band to be decreased by 1 dB, is depicted in Fig. 6.50. For example, at 2.25 – 2.33 GHz frequencies, which cover the 80-MHz BW allocated for 2.4-GHz systems, the –1-dB desensitization is achieved when the level of the interferer at BG1 input was approximately –20 dBm. Compared to in-band results, the filter improves the performance at the notch by 6 – 7 dB.

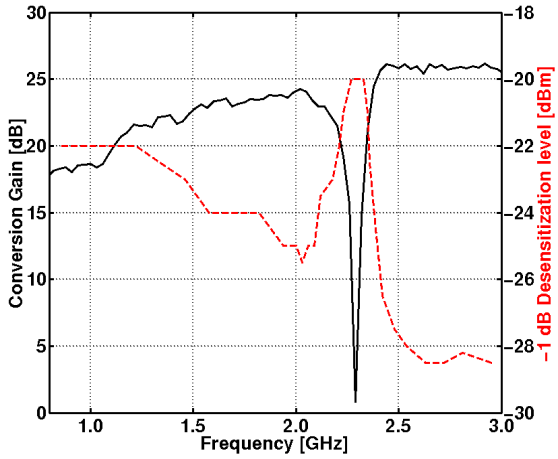

Fig. 6.50. Desensitization of BG1.

The measured current consumptions of the front-end were 48.1 mA and 42.7 mA for BG1 and BG3 operation modes, respectively. The measured gain and linearity results match well with the simulations. However, the measured NF deviates moderately from the simulated one. The measured front-end performance is summarized in Table 6.4. The chip micrograph is shown in Fig. 6.51. The active chip area is 0.73 mm^2.

Table 6.4. The measured front-end performance.

Parameter	Unit	BG1 (GHz)			BG3 (GHz)		
		3.432	3.960	4.488	6.600	7.128	7.656
Supply voltage	V	1.2					
Current cons.	mA	48.1			42.7		
Gain	dB	26.1	26.0	25.0	23.4	25.8	24.6
Noise figure [1)]	dB	4.9	5.0	5.6	7.3	6.9	7.7
IIP3 [2)]	dBm	–15.8	–15.8	–14.8	–17.4	–20.1	–18.8
IIP2 [3)]	dBm	+21	+19	+18	+19	+23	+19
ICP	dBm	–26.3	–26.5	–25.8	–25.8	–28.8	–27.5
Active area	mm^2	0.73					

1) Integrated from 2 MHz to 30 MHz
2) Measured with 20-MHz and 39.8-MHz offsets from the LO
3) Measured with 19.8-MHz and 20-MHz offsets from the LO

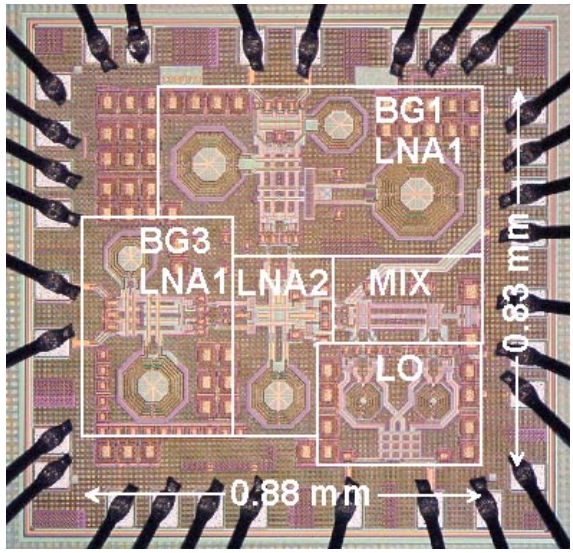

Fig. 6.51. Chip micrograph.

6.7 Summary and comparison to other published designs

In Sections 6.1 and 6.2, two direct-conversion receivers for wireless sensor applications operating in the 2.4-GHz ISM band were presented. Both design examples use a modified Bluetooth system that has optimized radio parameters for low power applications. The first demonstrator receiver consists of a merged LNA and mixers, LO buffers, and one baseband channel. It achieves 47-dB voltage gain, 28-dB NF, –21-dBm IIP3, and +18-dBm IIP2. The second prototype receiver includes an LNA, downconversion mixers, a 90-degree phase shift circuit, analog filters, a 1-bit analog-to-digital converter, and a received signal strength indicator (RSSI). The receiver consumes 4.1 mA from a 1.2-V power supply and achieves 43-dB voltage gain, a 25-dB noise figure, –22-dBm IIP3, and +11-dBm IIP2. The active silicon area was not increased, although several blocks were added. In addition, improvement in the overall performance was achieved. Both ICs were processed in same 0.13-μm CMOS process.

In those designs, approximately 90 % of the total receiver power is consumed in the RF blocks, i.e. in the LNA, mixer, and the LO buffers. Thus, several circuit design techniques were developed to minimize the power consumption. For the first low-power receiver prototype, a topology, where the LNA and mixer were merged, was chosen. A current boosting was utilized to separately optimize the performance of the LNA input devices and mixer switch transistors and the following baseband interface. A method to connect the boost current to the center tap of the load inductor was proposed. The benefit of the presented current boosting method was that the noise from the boost current source is common-mode at the mixer outputs. Therefore, the contribution to the overall front-end noise is insignificant. In addition, the effect of the parasitic capacitance caused by the boost current transistor is alleviated. Furthermore, a current boosting alternative, where the constant current source was replaced with other active blocks used in the receiver, was presented in Section 6.3. A design example, where the constant boost current source was replaced with LO buffers, was shown. In that case, the presented current reuse method decreased the front-end current consumption by 45 % without performance degradation. For the second low-power receiver prototype, the LNA and mixer were on separate dc paths. Due to the extremely stringent power budget, the separate transconductor input stage was not beneficial to the design of the mixer. Therefore, the output signal of the LNA is directly fed to the switching stage and the quadrature mixer is a low-impedance load for the LNA. The quadrature LO signal was generated with a single-stage polyphase filter. Although it has poor amplitude balance performance, it was chosen to minimize the LO signal loss and hence the power consumption.

Table 6.5 contains recently published CMOS RF front-ends and receivers for 2.4-GHz wireless sensor systems found in the literature. All the designs use either direct-conversion or low-IF architecture. The power consumption comparison is not trivial because some of the design examples collected in Table 6.5 include RF front-end (i.e. LNA and mixer) only, but some of them include baseband filters and ADCs as well, such as [P2]. In addition, the other designs apply higher supply voltage due to larger channel length. In general, the power consumption of the presented circuits is equal or lower than that of the circuits developed for ZigBee.

The measured NF in RF front-ends presented in [P1] and [P2] is high and deviates from the simulated one. The discrepancy is briefly discussed and improvements are considered. Firstly, since the target was to minimize the die area, a custom-designed source inductor having small area was used in the CG-LNA input matching. It is possible that the Q-value of the source

inductor is lower than predicted. According to (3.88), a source inductor having a large value and high Q-value should be used to minimize the noise figure, although the penalty is the increased layout area. Secondly, since the current consumption budgeted for LO buffers was small, the amplitude of the LO signal driving the mixer was moderate and the signal waveform was sinusoidal rather than square wave. Thus, the overlapping on-state of the switch transistors may be longer than predicted, resulting in worsened mixer noise performance. Since the voltage gain before the mixers is low, the switch stage noise is not adequately suppressed and improper switching has a significant influence on the overall RF front-end noise. In addition, the LO buffers used in [P1] and [P2] did not include the capacitor C_2 shown in Fig. 6.32, which filtered the noise coming from the bias circuit. Since there is some imbalance in the mixers, the noise coming from the LO port is not perfectly rejected but it nevertheless enhances the mixer output noise as well. Thus, even more attention should be paid to LO buffer design and interface with the downconversion mixer.

Table 6.5. CMOS RF front-ends and receivers for 2.4-GHz wireless sensor systems.

Metric	Unit	[P1]	[P2]	[24]	[25]	[26]	[27]	[28]	[29]	[30]
V_{DD}	V	1.2	1.2	1.8	1.8	1.8	1.8	1.8	1.8	1.8
I_{DD}	mA	2.8	4.1	9 [1)]	n/a	n/a	14.7	6	n/a	11.5 [3)]
P_{DD}	mW	3.4	4.9	31 [2)]	6.3	9	n/a	n/a	4.8	31.7 [4)]
Gain	dB	47	43	91	30	30	n/a	n/a	23	n/a
NF	dB	28	25	8	7.3	n/a	5.7	10	8.1	25
IIP3	dBm	–21	–22	–15	–8	–4	–16	–15	–15	–11
IIP2	dBm	+18	+11	n/a	+40	n/a	+6	n/a	n/a	n/a
ICP	dBm	n/a	–35	n/a	–18	n/a	n/a	n/a	n/a	–18
Techn. [μm]		0.13	0.13	0.18	0.18	0.18	0.18	0.18	0.18	0.18
Topology		DCR	DCR	Low-IF	DCR	Low-IF	Low-IF	Low-IF	DCR	Low-IF

1) current consumption of the RX chain only
2) power consumption of the whole receiver including the synthesizer
3) current consumption of analog parts only, digital part consume 7.4 mA from a 1.4-V supply
4) total power consumption (analog+digital)

A direct-conversion RF front-end designed in a 65-nm CMOS was presented in Section 6.4. Transistors having minimum channel length are utilized whenever possible, e.g. LNA input stage, LO divider, and LO buffer, for maximum device speed and minimum parasitics. The simulated performance of the presented LNA is comparable with other CMOS LNAs designed with longer channel lengths. In downconversion mixer design, however, transistors with non-minimum channel lengths were used to optimize the linearity, 1/*f* noise, and device matching. Due to limitations caused by low supply voltage, satisfactory mixer performance was achieved by using folded structure. To minimize the 1/*f* noise, PMOS transistors with small quiescent current were used as switches.

This RF front-end operates at 2.4-GHz center frequency. Performances of recently published RF front-ends realized in 90-nm to 150-nm CMOS are shown in Table 6.6. The comparison is nontrivial due to requirements of different applications and when comparing simulation results to measured ones. This design example has an excellent minimum noise performance and moderate linearity vs. dissipated power. To improve the 1/*f* noise corner frequency and linearity, methods presented in [17], for example, could be investigated.

Table 6.6. The comparison of recently published 1.8 – 2.4 GHz CMOS RF front-ends.

	Tech.	f_C	V_{DD}	I_{DD}	P_{DD}	Gain	NF	IIP3	IIP2	ICP
Ref.	[nm]	[GHz]	[V]	[mA]	[mW]	[dB]	[dB]	[dBm]	[dBm]	[dBm]
[31]	150	2.4	1.8	65	n/a	96	4.4	–19	n/a	–4 *
[17]	130	1.9	1.2	n/a	105	50	3.9	–9	+30	n/a
[32]	130	2.4	1.2	20	n/a	23.4	5.8	–4.8	+54	n/a
[33]	90	2.1	1.5	12.7	n/a	9.0	9.4	+8.9	+55	–3.3
[34]	90	1.8	1.4	n/a	75	37	2.9	–11	+63	n/a
[35]	90	1.9	0.75	15	n/a	31.5	3.5	–10.5	+51	–18
[P3]	65	2.4	1.2	29.3	35.2	39	3.0	–17	n/a	–29

*) measured with 0 dB gain setting

An RF front-end targeted for a dual-band UWB receiver operating at BG1 and BG3 was presented in Section 6.6. The prototype chip was realized in a 0.13-μm CMOS. Because the target is a mobile environment, special attention was paid to interference issues. Therefore, separate inputs and on-chip filtering were designed for sufficient suppression against narrowband systems. The efficient component sharing and small die area were achieved by combining the input signals in the second LNA and by designing the LO buffers to uniformly cover both BGs. Furthermore, special emphasis was given to the optimization of interfaces between different blocks.

The performance of the presented front-end is compared to the other CMOS UWB receivers and front-ends found in the literature mentioned in Table 6.7. Most of the UWB receivers are targeted for BG1 and BG3. The overall performance comparison is nontrivial, because some of the receivers include more circuit blocks than the others. For example, both the current consumption and layout area are significantly increased if the on-chip synthesizer is included [38], [39].

The gain, which is given in Table 6.7, is the maximum gain achieved at the operational band. The gain itself is not a relevant figure-of-merit to be compared, since it is affected by the blocks included. More interesting merit would be the gain variation within a single bandgroup or subband. Since the gain responses are not always shown and the detailed information is seldom given for separate sub-bands, this gain deviation is omitted from the table. In the publications where the gain deviation is mentioned, the in-band gain ripple within a single BG is typically less than 2 dB. The NF results are typically separately mentioned for each sub-band. The minimum and maximum NFs within the whole operational band are collected in Table 6.7. For BG1 devices, the typical NF is 4 – 6 dB, while in the case of BG3 UWB ICs, the NF is approximately 2 dB higher. The NF of [P6] is comparable with the other published BG1 and BG3 designs.

All the linearity performances (IIP3, IIP2, and ICP) are given as in-band results if not otherwise mentioned. If the results are separately published for different sub-bands or BGs, the worst-case linearity results are included in Table 6.7. It should be noted that some of the linearity results are achieved with minimum gain setup. Because no specification for input test signals exists for UWB, the variety of test signal frequencies is found in the published designs, but inconveniently, they are not always mentioned. Although the linearity performance comparison is not straightforward, the in-band linearity performance of [P6] is in line with the other

designs. A more relevant measure of the UWB receiver linearity is the robustness against the interference caused by other active radios, i.e. GSM900, GSM1900, and systems operating at 2.4-GHz and 5-GHz ISM and in U-NII bands. Such intermodulation measurements are performed in, for example, [P6], [41], [43], and [45]. For example, [P6] has a measured IIP3 of +1 dBm when the interference is caused by a GSM900 transmitter and 2.4-GHz system.

Table 6.7. Recently published CMOS UWB receivers and RF front-ends.

Metric	Unit	[P6]	[36]	[37]	[38]	[39]	[40]	[41]
f_C	GHz	3.1 – 7.9	3 – 5	3.1 – 9.5	3.1 – 8	3 – 5	3 – 5	3 – 8
V_{DD}	V	1.2	1.5	1.1	1.5	1.8	1.5	1.2
I_{DD}	mA	48	n/a	n/a	81.5	n/a	34 [1]	43 [1]
P_{DD}	mW	57	105	224	n/a	412	237 [2]	114 [2]
Gain	dB	26	73	64	32.3	63.8	37	24
NF	dB	4.9 .. 7.7	6.5 .. 8.4	6.3 .. 7.8	6.5 .. 7.9	4.0 .. 4.7	3.6 .. 4.1	5 .. 5.5
IIP3	dBm	–20	n/a	–17 [3]	–12.6 [3]	–0.8 [3]	–22	+5 [4]
IIP2	dBm	+18	n/a	n/a	+21.6 [3]	+22 [3]	n/a	+24 [4]
ICP	dBm	–29	–27.5	n/a	–24.5	–9 [3]	n/a	n/a
Area	mm^2	0.76	1	3.5	7.25	15.96	6.6	0.4 [5]
Technology		0.13-µm	0.13-µm	90-nm	0.18-µm	0.18-µm	0.13-µm	65-nm

1) receiver chain without LO generation
2) whole receiver
3) with minimum gain setup
4) intermodulation measured with out-of-band interferers
5) active area of the whole transceiver

Table 6.8 shows the UWB receivers implemented with SiGe process. Compared to CMOS designs, the NFs of SiGe UWB receivers are typically 1-2 dB better. The supply voltages of SiGe circuits are higher due to technology limitations, but the overall power consumption is typically comparable with CMOS designs. All published UWB receivers and front-ends utilize direct-conversion architecture except [38], which uses low-IF topology.

Table 6.8. Recently published SiGe UWB receivers and RF front-ends.

Metric	Unit	[42]	[43]	[44]	[45]	[46]	[47]
f_C	GHz	3.1 – 8.2	3.1 – 4.8	3.1 – 10.6	3 – 5	3.1 – 10.6	3 – 10
V_{DD}	V	2.7	2.5	2.7	2.7	1.8	2.5
I_{DD}	mA	88	78	31	47 [1]	30	114
P_{DD}	mW	n/a	n/a	n/a	n/a	53.7	n/a
Gain	dB	52	59	21.8	59	39	78
NF	dB	3.3 ... 4.1	4.5	4.1 … 6.2	4.5	3.3 ... 5	5 … 10
IIP3	dBm	–4.5 [2]	–6 [3]	–12.7	–6 [3]	n/a	–9
IIP2	dBm	+37.2 [2]	+25 [3]	+29	+25 [3]	n/a	n/a
ICP	dBm	–10.2 [2]	n/a	–23.5	n/a	–46	–27
Area	mm^2	7.0	4	2.7	4	2.3	5.6
Technology		0.18-µm	0.25-µm	0.25-µm	0.25-µm	0.18-µm	0.25-µm

1) receiver chain without LO generation
2) with minimum gain setup
3) intermodulation measured with out-of-band interferers

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7 Conclusions

In this thesis, RF circuit techniques for short-range direct-conversion receivers were presented. The two main target applications were low-power sensor radio and WiMedia UWB BG1 and BG3. The targeted operational frequencies were 2.4 GHz and 3.1 – 4.7 GHz and 6.3 – 7.9 GHz, respectively. Two prototype circuits for sensor radios and one IC realization for UWB systems were presented. The demonstrated direct-conversion front-ends included LNAs, down-conversion mixers, and LO generation circuits. The front-ends presented in papers [P1] and [P2] have been a part of a whole receiver including baseband amplifiers and filters and 1-bit analog-to-digital converters.

Several LNA topologies were first studied and analyzed in this thesis. Typically, the input matching circuit provides additional voltage gain, which is measured with Q-value. It affects the noise performance, linearity, and current consumption of the LNA. The input matching circuit also has an impact on the achievable input matching and output current bandwidths. The input matching circuit design parameters were derived for different LNA topologies. The presented calculations were adapted to several wideband LNA design examples and good agreement with the theory was observed.

The IDCS LNA input is typically sensitive to the parasitic capacitance associated with the input node. In contrast to the common-gate LNA, the parasitic capacitance at the IDCS stage cannot be absorbed into the input matching network. Therefore, the parasitic capacitance associated with the typical bonding pad can limit the achievable input matching performance. To mitigate that problem, a simple modification to the pad usage was proposed and analyzed. The presented pad structure was used at UWB BG3 LNA input, where benefit was gained due to high operational frequency.

The different amplifier load structures were discussed. A typical RLC resonator load is applicable for narrowband applications. In addition, shunt-peak load and its alternatives were briefly presented and compared. Such load structures are needed, when the target is to cover wide bandwidths simultaneously with high center frequency, in the case of UWB, for example. The bandwidth shrinkage of two cascaded shunt-peak loads was briefly described. An alternative wideband load, which was targeted for two-stage amplifiers but contained only a single on-chip inductor, was proposed and analyzed.

The presented work also includes a theoretical analysis of passive polyphase filters. A general method with which to calculate the transfer functions of cascaded PPF filter stages is presented. According to the analysis, design guidelines for two- and three-stage PPFs, which are the most typical PPF structures encountered in practical RF IC design, are provided. Whenever it was reasonable, formulas for general *n*-stage PPFs are given. Based on the input signal feeding technique, two variants of PPFs can be separated. The analysis of both variants was carried out and a performance comparison between the PPF types was made.

The main targets of the presented application examples were quite separate from each other due to power consumption, operational frequency, and bandwidth points of view. From the sensor applications, the primary goal was to design a complete receiver with current consumption of only a few mWs. The challenge of the low power consumption is to achieve sufficient performance for RF blocks, which dominate the total receiver current consumption. On the other hand, the challenge of the UWB design example was to design LNAs having sufficient

input matching and gain response over the 1.6-GHz band and to optimize the interface between different blocks, still bearing mind the power consumption. For both applications, one relevant criterion was to keep the number of on-chip inductors as low as possible. Although the focus of the design examples was on these systems, the circuit presented and analyzed in this thesis can be utilized in other kinds of applications as well.

Three experimental circuits presented in this thesis were fabricated in a 0.13-μm CMOS. Part of the theory here was validated with design examples where actual IC component models were used. In addition, circuit design examples in 0.13-μm and 65-nm CMOS processes were included. Technology scaling allows an extensive use of digital signal processing and there is ever increasing pressure to replace analog parts with digital ones. Nevertheless, radio communication is still based on transmitting and receiving signals in the analog domain and some analog blocks will remain in forthcoming transceivers as well. It is feasible to design RF front-end in the analog domain, even with deep-submicron process, as was presented in this thesis.

Appendix A: General common-source LNA

A general common-source (CS) LNA is presented in Fig. A.1. The CS-LNA includes gate and source impedances Z_g and Z_s, gate-to-drain and gate-to-source impedances Z_{gd} and Z_{gs}, and a load impedance Z_L. The general CS LNA circuit is used to analyze the input matching and gain of the several LNA topologies shown later in this thesis. It should be noted that, when using the following equations, the intrinsic gate-source and gate-drain capacitors C_{gs} and C_{gd} of M_1 are included in Z_{gs} and Z_{gd}, respectively.

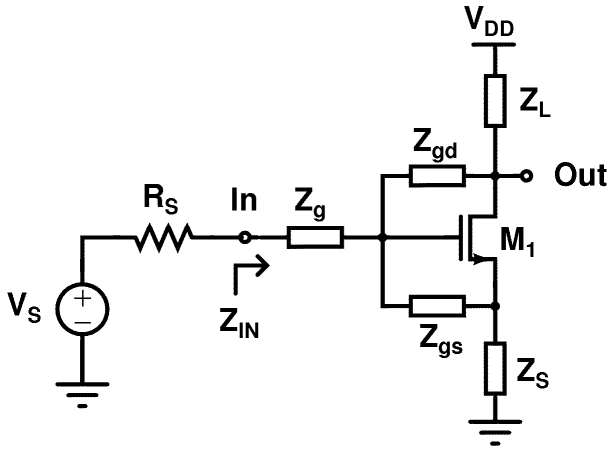

Fig. A.1. General common-source stage.

The input impedance of the common-source LNA of Fig. A.1 is

$$Z_{in} = Z_g + \frac{\left(Z_{gd}+Z_L\right)\left[Z_{gs}+Z_S\left(1+g_m Z_{gs}\right)\right]}{Z_{gd}+Z_{gs}+\left(1+g_m Z_{gs}\right)\left(Z_L+Z_S\right)}, \tag{A.1}$$

where the components can be identified from Fig. A.1. An equation similar to (A.1) is also given in [1], where bulk conductance and source-bulk and drain-bulk impedances are also taken into account. If Z_{gd} is infinite, i.e. there is no feedback or a unilateral transistor model is assumed, (A.1) simplifies to

$$Z_{in} = Z_g + Z_{gs} + Z_S\left(1+g_m Z_{gs}\right). \tag{A.2}$$

The insertion gain of a CS LNA shown in Fig. A.1 is

$$A_i = \frac{2Z_L\left(1-\dfrac{g_m Z_{gd} Z_{gs}}{Z_S+Z_{gs}+g_m Z_S Z_{gs}}\right)}{Z_{gd}+Z_L+\left(R_S+Z_g\right)\left(1+\dfrac{Z_L+Z_{gd}+g_m Z_L Z_{gs}}{Z_S+Z_{gs}+g_m Z_s Z_{gs}}\right)}. \tag{A.3}$$

If Z_{gd} is infinite, (A.3) simplifies to

$$A_{i,Z_{gd}\to\infty} = -\frac{2g_m Z_{gs} Z_L}{R_S+Z_g+Z_{gs}+Z_S+g_m Z_{gs} Z_S}. \tag{A.4}$$

The voltage gain, neglecting bulk conductance and source-bulk and drain-bulk impedances, is given by [1]

$$A_v = \frac{Z_{in} - Z_g}{Z_{in}} \cdot \left(Z_L \parallel Z_{gd} \right) \cdot \left[\frac{1}{Z_{gd}} - \frac{g_m Z_{gs}}{Z_{gs} + Z_S \left(1 + g_m Z_{gs} \right)} \right]. \tag{A.5}$$

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Appendix B: Analysis and optimization of 4-stage PPF

The optimum pole splitting is calculated for a four-stage PPF. First, the pole-splitting factor k_4 is defined as the ratio of the pole frequencies ω_1 and ω_4. Due to symmetry reasons, the pole ratio between ω_3 and ω_4 is the same as the pole ratio between ω_1 and ω_2. Thus, k_4 is determined by k_2 and k_3

$$k_4 = \frac{\omega_1}{\omega_4} = \frac{\omega_1}{\omega_3}\frac{\omega_3}{\omega_4} = k_3 k_2 \,. \tag{B.1}$$

The minimum IRRs are achieved at three frequencies given by

$$\omega_{IRR,\min 2} = \frac{\omega_1}{\sqrt{k_2 k_3}}\,, \tag{B.2}$$

$$\omega_{IRR,\min 1,3} = \frac{\omega_1}{\sqrt{2}k_2 k_3}\sqrt{F_3\left(k_2,k_3\right) \pm \sqrt{F_3\left(k_2,k_3\right)^2 - 4k_2^2 k_3^2}}\,, \tag{B.3}$$

where

$$F_3\left(k_2,k_3\right) = k_2\left(1-k_3\right)^2 + k_3\left(1-k_2\right)^2 + 2k_2 k_3\,. \tag{B.4}$$

The IRR minimums at $\omega_{IRR,min1}$ and $\omega_{IRR,min3}$ are always equal. To achieve equal IRR with $\omega_{IRR,min2}$, too, k_3 is calculated as

$$k_3 = \frac{1}{3k_2}\left[k_2\left(k_2^2 + k_2 - 1\right) + F_4\left(k_2\right)\cos\left(\frac{1}{3}\arccos\left(\frac{F_5\left(k_2\right)}{F_4\left(k_2\right)^3}\right)\right)\right], \tag{B.5}$$

where

$$F_4\left(k_2\right) = 2\sqrt{k_2\left(k_2^5 + 2k_2^4 - k_2^3 - 5k_2^2 + 4k_2 + 3\right)}\,, \tag{B.6}$$

$$F_5\left(k_2\right) = 4k_2^2\left[-9 + k_2\left(-9k_2^3 + 2\left(-1 + k_2 + k_2^2\right)^3\right)\right]. \tag{B.7}$$

Equation (B.5) is quite tedious for hand calculations. Therefore, an approximate formula for k_3 calculation given as

$$k_3 \approx 1.2k_2^2 + 0.17k_2 - 0.37 \tag{B.8}$$

will predict (B.5) with an maximum error of 1.1 % when k_2<3. At $\omega_{IRR,min,2}$, the amplitude balance becomes

$$A_{bal,4-stg} = \frac{k_2\left(1+k_3\right)^2 + k_3\left(1+k_2\right)^2}{2\sqrt{k_2 k_3}\left(k_2+1\right)\left(k_3+1\right)}\,, \tag{B.9}$$

from where the IRR can be calculated with (5.21). The corner frequencies $\omega_{c,min}$ and $\omega_{c,max}$, where the minimum IRR is achieved, can be calculated with

$$\omega_{c,\min\&\max} = \frac{\omega_1}{\left(4k_2 k_3\right)^{3/2}}\left[F_6^+\left(k_2,k_3\right) + F_6^-\left(k_2,k_3\right) \pm 2\sqrt{F_6^+\left(k_2,k_3\right)F_6^-\left(k_2,k_3\right)}\right], \tag{B.10}$$

where the '+' or '–' -sign of F_6 is chosen according to

$$F_6^{\pm}(k_2,k_3) = k_2(k_3 \pm 1)^2 + k_3(k_2 \pm 1)^2 . \tag{B.11}$$

The relative bandwidth, where the IRR_{min} is achieved, is

$$BW_{rel,4-stg} = \frac{F_6^+(k_2,k_3) + F_6^-(k_2,k_3) + 2\sqrt{F_6^+(k_2,k_3)F_6^-(k_2,k_3)}}{F_6^+(k_2,k_3) + F_6^-(k_2,k_3) - 2\sqrt{F_6^+(k_2,k_3)F_6^-(k_2,k_3)}} . \tag{B.12}$$

Equation (B.12) can be approximated with better than 1.0-% accuracy with

$$BW_{rel,4-stg} \approx 2.73k_2^3 - 3.63k_2^2 + 2.9k_2 - 1 , \tag{B.13}$$

when $k_2 < 3$. The minimum IRR and relative bandwidth with optimum pole splitting are shown in Fig. 5.17.

If the IRR is calculated for the 4-stage PPF by using (B.5), quite complicated equations are achieved. To get a simple equation for 4th-order PPF IRR, the generic formula $k_{n+1}/k_n=k_2$ is used to calculate pole-splitting factors k_3 and k_4. As a result, the IRR at the frequency given by (B.2) becomes

$$IRR_{\min,4-stg} = \left(\frac{\sqrt{k_2}+1}{\sqrt{k_2}-1}\right)^4 \left(\frac{k_2-\sqrt{k_2}+1}{k_2+\sqrt{k_2}+1}\right)^2 . \tag{B.14}$$

Compared to the other two IRR minimums at frequencies given by (B.3), the IRR of (B.14) is approximately 5 dB higher when k_2 is close to unity. This is shown in Fig. B.1, where the IRR of a 4th-order PPF is shown. A BW-optimized PPF is shown with a solid line. In that case, k_3 is calculated with (B.5). The dashed line presents a PPF where k_3 is calculated as k_2^2. In both cases k_2 = 1.6 and k_4 is calculated as in (B.1).

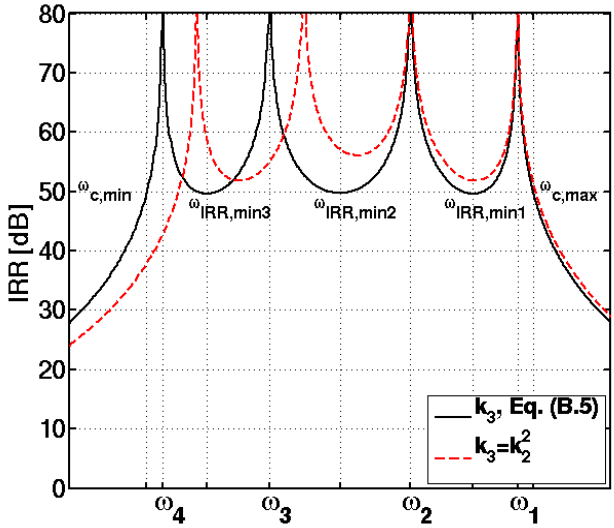

Fig. B.1. IRR of a 4th-order PPF. The solid line presents a BW-optimized PPF. In that case, k_3 is evaluated with (B.5). The dashed line presents a PPF, where k_3 is evaluated as k_2^2. In both cases, k_2 = 1.6.

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