Helsinki University of Technology
Faculty of Electronics, Communications and Automation
Department of Electronics
Espoo, Finland

TKK-EVT-18

HIGH FREQUENCY SIGNAL INTEGRITY IN HIGH-DENSITY ASSEMBLIES

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Dissertation for the degree of Doctor of Science in Technology to be presented with the due permission of the Faculty of Electronics, Communications and Automation, Helsinki University of Technology, for public examination and debate in Auditorium S5 at Helsinki University of Technology (Espoo, Finland) on the 18th of April, 2008, at 12 noon.

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TKK-EVT-18
ISSN 1797-5824 (print)
ISBN 978-951-22-9345-2 (print)

ISSN 1797-5816 (pdf)
ISBN 978-951-22-9346-9 (pdf)

Abstract

The demand for faster, portable and reliable electronic devices is increasing the pressure on the development of assembly techniques for signal integrity (SI). The advance of integrated circuits toward a large number of Input/Output (I/Os), a high number of operations and up to microwave communication frequencies, is behind the drive for the search for new packaging solutions. The materials and assembly techniques have an important impact on the propagation of high speed signals. Signal integrity issues emerge due to the electrical losses of materials, reflections from impedance discontinuities in the signal path and fast transitions of the signals. For these reasons, signal integrity in lead-free connections of WLCSP, flip chip (FC) and Integrated Module Board (IMB) assemblies were investigated up to 50 GHz.

The increase of conductor loss resulting from the presence of thick oxide layers on the surface of solder bumps of hot running components was experimentally studied for the first time. Utilizing theoretical calculations, a design rule was developed to account for the 40 % increase in losses due to the presence of oxide layers at high frequencies. The research into the influence of solder microstructure on signal quality showed that it did not negatively affect the wave propagation. Experimental results proved that the presence of underfills and high density routing on printed wiring boards (PWBs) under theWLCSP components, detuned the components and the connections. The effects of three different underfills on signal propagation were studied. It was proven that the changes resulting from the rheology and parameters of curing process influence the losses and reflections of circuits.

The analysis of microwave performances of flip chip (FC) and Integrated Module Board (IMB) assembly techniques demonstrated that they are well suited to Radio frequency (RF) and high speed applications. Comparison showed that IMB performed better as the wave encountered smaller discontinuities and had an optimized propagation path. Full wave simulations of IMB assemblies were performed considering finite ground coplanar waveguide (FGCPW), microstrip and stripline connections with stack-ups that included high dielectric constant materials and four connection possibilities. The research was carried out in the domains of both frequency and time to rigorously determine the sources of signal reflections. The results emphasized that in the design for match impedance and optimal current return path, discontinuities and reference planes had significant impact on signal integrity.

Preface

This doctoral thesis is a result of the work carried out in the Department of Electronics at the Helsinki University of Technology. The research has been part of the projects financially supported and supervised by the Academy of Finland, Semiconductor Research Corporation and National Semiconductor Corporation.

I am most grateful to my supervisor Professor Jorma Kivilahti and my mentor Dr. Luu Nguyen for their guidance, time and support. Also, I wish to thank all the colleagues at the department for their contribution to this work: Dr. Tomi Laurila, Dr. Vesa Vuorinen and Dr. Toni Mattila. Special thanks go to the co-authors of this work, Dr. Hao Yu and Lic. Tuomas Waris.

Additionally, appreciation goes to Pia Holmberg for helping me through the jungle of bureaucracy and M.Sc. Pirjo Kontio for her assistance in achieving reliable fabrication processes. I am also grateful to the team from the Radio Laboratory, Lic. Leonardo Azzinari, Dr. Klemens Ichlem, and M.Sc. Viktor Sibakov for their support in making it possible to carry out the high frequency experiments and to M.Sc. Tommi Riekkinen (VTT) for the fabrication of Si test coupons.

Finally, I am deeply grateful and dedicate this thesis to my parents, Viorica and Cristache Burlacu, as well as my brother, Mihai Burlacu, for their love and irreplaceable support. Sunt profund recunoscator si dedic aceasta lucrare parintilor mei, fratelui precum si celor care m-au sustinut in acest timp, multumindu-le pentru dragostea daruita si suport. I am grateful to my partner Helena Faust and all my dear friends for providing encouragement and support that will never be forgotten.

Espoo, October 2007,
Dragos Burlacu

Symbols and Abbreviations

Symbols

α	Attenuation constant of transmission line (dB/m)
α_c	Conductor loss of transmission line (dB/m)
α_{cr}	Conductor loss of rough transmission line (dB/m)
α_d	Dielectric loss of transmission line (dB/m)
α_r	Radiation loss of transmission line (dB/m)
α_s	Surface waves and high order wave loss (dB/m)
α_T	Total losses of transmission line (dB/m)
β	Phase constant of transmission line (rad/m)
C	Capacitance (F)
Δ	Roughness (m)
δ_s	Skin depth (m)
ε	Permittivity of material (F/m)
ε_0	Permittivity of free space ($8.8541878176 \times 10^{-12}$ F/m)
ε_r	Relative permittivity or dielectric constant
L	Inductance (H)
λ	Wavelength (m)
G	Conductance (S)
γ	Propagation constant
i	Instantaneous current (A)
ω	Angular frequency (rad/sec)
σ	Conductivity of metal (S/m)
σ_d	Conductivity of dielectric (S/m)
f	Frequency (Hz)
f_r	Resonant frequency (Hz)
η	Wave impedance in vacuum (Ω)
μ	Permeability of material ($N \cdot A^{-2}$)
μ_0	Permeability of free space ($\mu_0 = 4\pi \times 10^{-7}$ $N \cdot A^{-2}$)
μ_r	Relative permeability
Γ	Reflection coefficient

ρ_c	Resistivity of conductor (Ωm)
τ	Transmission coefficient
q	Standard deviation
R	Resistance (Ω)
R_s	Surface resistivity (Ω/m)
S_{11}, S_{21}, S_{12}, S_{22}	Scattering (S) parameters
t	Thickness (m)
t_d	Time delay (sec)
t_r	Rise time (sec)
tanδ	Loss tangent of dielectric material
v	Instantaneous voltage (V)
W	Width of transmission line (m)
Z_0	Characteristic impedance (Ω)
Z_{11}, Z_{21}, Z_{12}, Z_{22}	Impedance(Z)-parameters

Abbreviations

BBUL	Bumpless build-up layer packaging
BGA	Ball grid array
BW	Bandwidth
CAD	Computer aided design
CiB	Chip-in-Board assembly technique
CPW	Coplanar waveguide
DC	Direct current
DCA	Direct chip attachment
DUT	Device under test
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
FC	Flip chip
FD	Finite difference
FE	Finite element
FDTD	Finite-difference time-domain
FFT	Fourier transformation
FGCPW	Finite ground coplanar waveguide

IC	Integrated circuit
IFFT	Inverse Fourier transformation
IMB	Integrated Module Board
I/O	Input / Output
JEDEC	Joint Electron Device Engineering Council
LCP	Liquid crystal polymer
MCM-D	Multi-chip-module dielectric
MoM	Method of Moments
PCB	Printed circuit board
PDN	Power distribution network
PGA	Pin grid array
PTFE	Polytetrafluoroethylene (Teflon)
PWB	Printed wiring board
QFP	Quad flat pack
RF	Radio frequency
RoHS	Restriction of the use of Certain Hazardous Substances
RLC	Resistance-Inductance-Capacitance
SEM	Scanning electron microscope
SI	Signal Integrity
SIA	Security Industry Authority
SoP	System on package
SMT	Surface mount technology
TEM	Transverse electromagnetic wave
TDR	Time domain reflectometry
TDT	Time domain transmission
UTF	Universal test fixture
VNA	Vector network analyzer
WL-CSP	Wafer Level Chip Scale Package
XT	Crosstalk

1. Introduction

High-density interconnections and packaging technologies for high-frequency and high-speed digital applications are becoming more challenging as new applications push up wireless communication frequencies and digital clock rates [1 - 5]. The number of functions performed by integrated circuits and the number of I/O counts is increasing while the pitch and dimensions of the interconnections are shrinking. Moore's law states that the sizes of transistors will continue to shrink and their transition times decrease, doubling the clock frequencies every 2 years [5, 6]. In this high speed environment, the package of electronic devices represents the bottlenecks of high frequency signals as they utilize largest part of the noise budget of systems [7, 8]. The miniaturization of packages and the use of new low loss, low dielectric constnat materials both help to improve signal quality [9]. Chip scale packages, direct chip attachments and embedded active and passive components are viable solutions that improve the noise budget. By embedding components into substrates, the functionality of modules is increased considerably as in each dielectric layer are integrated a few active and passive components. A good understanding of high-frequency conditions, new lead-free assembly materials, as well as assembly technologies, requires further investigation and is, however, essential as on July 1st, 2006, the RoHS directive for lead-free implementation came into force [10].

The packaging of electronics is a complex field that requires the combined expertise of material science and electrical design for signal integrity and reliability. The impacts of assembly design, materials and fabrication technologies, all have to be considered side by side in the future development of electronic devices. High speed, high density assemblies require special consideration as at high frequencies the interconnections are no longer transparent to signals, being electrically long. Performing as transmission lines, their characteristics are influenced by the electrical properties of the nets, the surrounding environment and physical geometries. In the case of hot running components, thick layers of oxides form on the surface of the solder connections. These change the surface resistivity and dielectric constant of the medium. The underfill materials utilized to increase the mechanical reliability of packages detune the interconnections and the circuitry of assembled components. The

degree of change of the electrical parameters is influenced not only by the underfill but also by the transmission line type utilized in the design of the circuits. The appropriate selection of materials, fabrication processes and designs are an important step in the development of electronic applications which utilize embedded components. A rigorous control of assembly process is essential as the thickness and properties of materials affect the electrical characteristics of interconnections and electrical performances of integrated active and integral passive components. In the design process, the fabrication issues such as assembly space between PWB and component, molding epoxy, drilling and artwork alignment accuracy, together with electrical solutions for current return paths and signal and reference layers distribution all have to be carefully considered.

The noise from packages cause false logic switching and signal delays that affect significantly the functionality of electronic devices [11]. The attenuation and reflections of signals resulting from material losses and impedance mismatches are the main causes of parasitic noise [12, 13]. In the packages characterization, a considerable amount of attention was paid to the effects of the geometry of interconnections and their parasitics on signal quality [14 - 16]. The influences of assembly materials were researched for microwave applications in order to study the distortions due to amplitude attenuation as well as to the phase shift of the signals' harmonics with frequency [17, 18]. For faultless functionality, the amount of distortions introduced by interconnections' parasitics to signals and the power supply must be kept to a minimum [19, 20]. Typical signal integrity issues at the package level, such as signal reflection, delay, crosstalk, ground bounce, and voltage drop are reduced by careful consideration of the geometries and materials of interconnections [7, 13, 16]. Power distribution network noise is minimized with the help of short, low-resistance, low-inductance connections to the reference planes [20, 21]. Signal reflections due to characteristic impedance mismatches in packages account for up to 50% of the total power loss of the signal [12, 22]. Careful design of the nets, current return paths, and assignment of the bumps all help decrease the reflection noise. Concerns over power loss in assembly materials are increasing with higher frequencies as resistivity, roughness and the surface finish of conductors, dielectric loss, and manufacturing tolerances have important effects on high-speed signals [23]. The current trend in the electronics industry to utilize low voltage levels pushes the

development of low noise packages because the consequent decrease in the voltage-to-noise ratios increases the communication errors [8].

Interconnections operating at high frequencies have large resistive losses as the skin effect prevents the current from penetrating deep into the conductor metal [17]. The skin effect, together with the roughness and bump shape, add to the losses in the interconnections [18, 24, 25]. Moreover, high temperatures of hot running components create favorable conditions for the growth of thick oxide layers on the surface of solder bumps that perform as an n-type semiconductor [26 - 28]. The presence of thick oxide layers is of concern for the integrity of high frequency signals since the harmonics of the signal are differently attenuated and delayed. The effect of thick oxide on a bump surface is similar to the effect of a high-resistivity metal layer deposited on conductors to improve adhesion - previously described by Denlinger *et al*, Sobol, and Staiculescu [25, 29, 30]. They demonstrated that thick layers of higher resistivity materials deposited on the surface of a conductor increase the conductor loss from 30 to 50 %, as a high portion of the power flow is conducted through the outermost part of the material. The presence of multi-layer dielectric materials also increases the dielectric constant of the transmission line, thereby detuning the electrical circuit [31].

The mechanical reliability of the flip chip and some WLCSP assemblies, and consequently the lifetime of electronic devices, is improved with the help of underfill materials [32, 33]. The properties and the rheology of underfills are adjusted according to the reliability requirements and assembly types by changing the average size, type and quantity of filler particles. The dielectric constant and loss tangent of materials change with the distribution and electrical parameters of the fillers [34]. Having a higher dielectric constant and loss tangent than air, the underfill increases the dielectric losses and detune the circuits of the components and package interconnections [35 - 37]. The effects of the anisotropy caused by the differences between the fillers and the polymers, the orientation of the non-spherical fillers, the volume fraction of filler and uneven filler distribution due to settling time and viscosity were all investigated for Polytetrafluoroethylene (PTFE) with fused silica filler [38, 39]. The anisotropy of the material further detune the components as it increases the value of the square root of the dielectric constant by up to 3% for narrow

lines and by up to 9% for wide lines. The corner underfills affect the signal integrity only of the neighboring connections as they disperse around the corner bumps [33, 40].

Signal reflections and power distribution issues are minimized utilizing the packages having small size connections [7]. Flip chip, WLCSP and Ball grid array BGA are the main packages utilized for high speed / high frequency applications as the size of their bumps are as small as 50 μm [41 - 44]. Another way to improve signal integrity, homogeneity, and the reliability of component-board interconnections, while increasing the functionality of modules, is to utilize chip-in-board (CiB) techniques. Helsinki University of Technology (HUT) developed the IMB assembly technology based on CiB [45 - 48]. Utilizing short Cu-Cu interconnections and low-loss assembly materials reduces the insertion loss. Signal reflections are better controlled as the discontinuities of the connections are small and a good control of characteristic impedance of signal lines and their current return paths is achieved.

In this study, three fields of expertise, electronic design, material science and manufacturing, will be employed to analyze the effects of the assembly materials (solder and underfills) and of the assembly techniques (WLCSP, FC and IMB) up to 50 GHz. The research will be carried out with the help of the transmission line theory and with specially designed and fabricated test boards. This work will focus on both experimental and theoretical simulation approaches. The effect of the microstructure and oxide layers of Sn and Sn3.8Ag0.7Cu (SnAgCu) interconnections on signal integrity will be analyzed for the first time at microwave frequencies. The design rules will be determined from theoretical calculations having as reference the experimental results. The effects of the presence of three underfills and high density circuitry routed on PWB under WLCSP components on signal integrity will be studied by comparing the electrical characteristics of the underfilled test coupons to the reference ones. The results will emphasize the influence of rheology and the curing parameters of materials on the change of electrical parameters of components and interconnections. With the help of full wave electrical simulations, the analysis will also be extended to include microstrip line designs. The effects of new assembly techniques on signal quality will be investigated with the help of the FC and IMB techniques. Special test

coupons will be fabricated and tested at microwave frequencies. Based on the positive correlation between experimental and calculation results, the IMB analysis will be extended to microstrip and stripline connections. Four interconnection possibilities will be analyzed for each type of transmission line and part of the stack-ups will also be considered for high dielectric materials to study their influence on performances of IMB connections. The circuit models with bandwidths of up 50 GHz will be determined for stripline connections. The analysis will be carried out in both frequency and time domains.

This research does not solve all the signal integrity issues in assemblies, yet the subject of this work is technologically important for the electronic industry which considers more than ever that future increases in the functionality of devices can be achieved by increasing operating frequency and embedding active and passive components into substrates. This work is also interesting on a theoretical level as design rules have been developed for the interconnection losses of hot running components and IMB assemblies realized with different transmission lines.

2. Signal integrity

Signal integrity (SI) is a general term that refers to the timing and quality of signals in electronic devices. The quality of signals is affected by noise generated in one net, multiple nets, a power distribution network, electromagnetic compatibility (EMC) and electromagnetic interference (EMI). Most noises are electromagnetic waves triggered by the propagation of signals from driver to receiver along the net and at the discontinuities. The origins of noise in packages are caused by: the transition rates of signals, impedance mismatch, the length of traces, and coupling [49 - 51]. The miniaturization of transistors to increase the functionality of components and count of interconnections is the main cause for the advanced signal integrity issues in the assemblies. The advances in SI processing had made possible Faster switching times are achieved not only by scaling down the gate of transistors but also by changing the operating voltage. Therefore, the SI issue has become even more challenging as the noise budget decreased with the voltage levels of systems. The increases in functionality and speed have made the systems more prone to failure caused by noise from the packages. The size of the interconnections is now comparable to the wavelength of frequencies from the spectrum of signals. In this chapter, the causes of noise in assemblies are presented together with techniques for analysis as well as possible solutions to the problems.

2.1 Signal integrity in assemblies

The functions of electronic packages are to protect the fragile components from mechanical shocks and the environment while ensuring good heat dissipation paths and electrical connections. Solder balls, wire bonds, vias, and traces are combined to create electrical connections to link the wirings of PWBs to the circuits from components (Fig. 2.1). The three main factors driving changes in electronics packages are high speed/high frequency operation, power dissipation and functionality. The short rise times and high communication frequencies demand new packages and assembly techniques to be developed. Small discontinuities and an optimized

propagation path for signals are required to decrease the package impact on the noise budget [12, 52 - 54]. The power distribution network (PDN) and the number of connections must follow the high diversity in functionality of assembled components. The PDN had to deliver more noise free power while fast switching signals introduce complex noises. The augment in the number of connections, concurrent with the decrease in the size of the package, results in a smaller pitch and size of interconnections. The mechanical reliability of connections is affected together with the signal integrity as one return path connections have to be allocated for more signals and the tight coupling increases the switching noise.

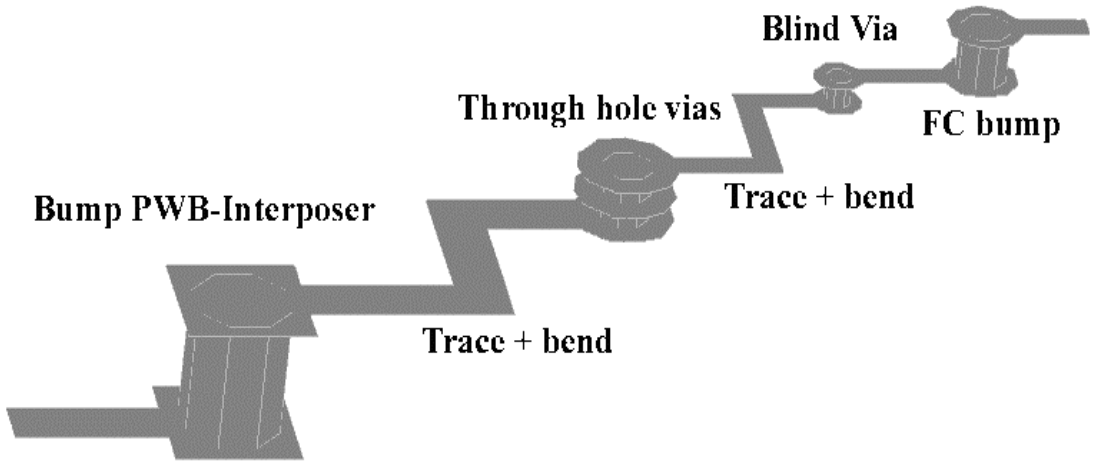


Fig. 2.1 Schematic representation of a BGA trace.

In order to build an electronic system different assembly solutions are employed to cope with the specific requirements of interconnecting dissimilar materials. A hierarchy of packaging is defined, as materials and bonding are very different for each level of assembly [8]. The zero level packaging defines the connections inside components. The first level packaging accounts for the interconnections of components to packages. The second level represents the package to PWB connections. The third level is the substrate to board, the fourth is board to motherboard and the fifth level represents the connection between physically separate units. The first and second level packaging are the most challenging as they make the physical connections of the sub-micron circuitry of components to the PWBs. The electrical connections on the first level packaging are realized with the help of wire bonds, tape-automated bonds or solder balls. Inside one package are enclosed one (single chip module), or more chips (multi chip modules). The integrated circuits (ICs) are mounted on a special carrier substrate, which is ceramic or organic

according to the requirements of the circuits. The attachment of packages to boards is realized with solder connections or anisotropic conductive adhesives. To achieve smaller devices and increase functionality density, the first level packaging is ruled out and bare chips are directly attached to the PWB by wire bonding, flip chip solder balls or by integrating them into the boards (CiB). The main issues of the second level packaging are the mechanical reliability resulting from the CTE mismatch of materials and large electrical noise caused by discontinuities in the signal trace and its return path.

To reduce the cost and weight of packages and signal integrity issues direct chip attach (DCA), chip scale package (CSP), and wafer level CSP (WL-CSP) assemblies are being developed. These solutions support high frequency applications, but with a limited number of connections due to the small surface area of components and offer limited mechanical reliability. To increase the reliability and cope with the high count of I/Os, new packages such as multiple line grid array (MLGA), pin grid array (PGA) and ball grid array (BGA) are employed [44, 55, 56]. The components are mounted on a large interposer whose size is calculated considering the number of I/Os and the size of bumps. To improve the signal quality of the long connection, critical signal lines are designed to have constant impedance and power planes and filtering capabilities are integrated in the interposers [57, 58]. Moreover, the interposer is utilized to integrate passive components, this expand further the functionality of packages as some RF functions such as matching and filtering are performed outside the components (Fig. 2.2).

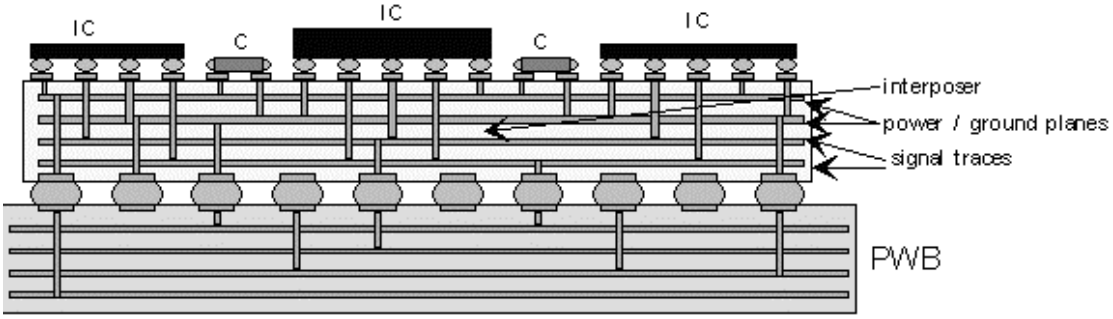


Fig. 2.2 Schematic representation of an assembly with interposer.

Recently, the chip-in-board assembly (CiB) technology has been developed to increase further the functionality per module, to reduce the number of discontinuities, to improve the signal integrity, homogeneity, and reliability of component-board

interconnections (Fig. 2.3). This manufacturing technique provides smaller interconnections, better control of geometries and materials, as well as a short connection to PDN and PWB circuitry. Developed for multi chip modules (MCM-D), these days is utilized for system on package (SoP) and lately for PCB (IMB) applications [47, 59 - 62]. The experimental and theoretical results indicated that this technique is well suited to both RF and digital applications with frequencies ranging up to 100 GHz, and low noise connections for a power distribution network [20, 63].

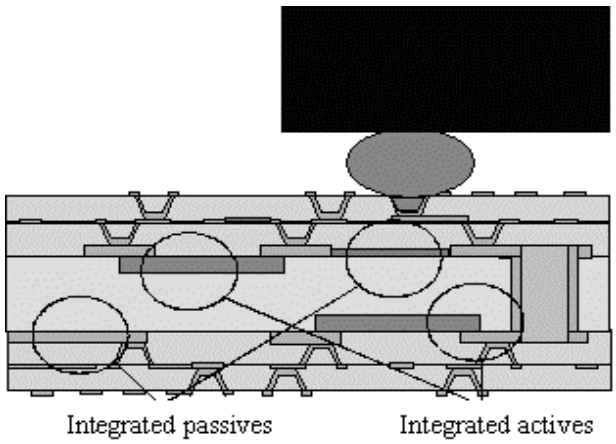


Fig. 2.3 Schematic presentation of IMB assembly technique

The rapid development of mixed signal applications on the chip or in the package increases the signal integrity concerns [64, 65]. With the harmonics of digital communications reaching microwave domains, the packages must perform very well over a large bandwidth. The package design for microwave applications is not easy to implement into digital assemblies and often is overlooked the fact that the bandwidth of the connection depends on the rise time of the signal and not on the frequency. The signal integrity in assemblies has been studied extensively over the last years and often the failures have been associated with the noise from the packages [4, 7, 11, 12]. An important issue in the analysis of digital signal represents the spectrum of the signal necessary to pass undistorted through the interconnection. A square wave is described using the Fourier series (2.1) [66]. A reasonable reconstruction of the signals at the receiver requires that at least the fundamental, third, and fifth harmonics must pass undistorted. The bandwidth of interconnection is determined by considering the power spectrum of the fastest signal that flows over the connections. It is calculated from the rise or fall time of the signals traveling through the connection.

$$x_{sq} = \frac{4}{\pi} \sum_{k=1}^{\infty} \frac{\sin\left((2k-1)2\pi ft\right)}{(2k-1)} \tag{2.1}$$

A proper understanding of RF and digital noise is necessary because the circuits, situated in close proximity to each other, interact and affect the electrical functionality of one another. The noise in an electronic system can be divided in four main groups: noise resulting from one net, multiple nets, power distribution networks, and EMC / EMI [7]. The signal quality in one net is influenced by the reflection and distortion noise which causes attenuation, dispersion, time delay, overshoot, undershoot and ringing. Reflections occur due to impedance mismatches in the signal path and discontinuities in the current return paths [67 - 69]. The electrical losses induced by assembly materials are the main source of distortion noise. The dispersion of electrical properties of materials with frequency cause different levels of attenuation and phase shift for signals having different frequencies [17, 29, 70]. Noise levels in one net are reduced by controlling the impedance of the lines and utilizing low loss, low dispersion materials [9].

The energy transfers between adjacent lines influence the signal quality of multiple nets. The electromagnetic coupling - also known as crosstalk (XT) - between nets, vias and connections occurs by two mechanisms: mutual inductance and mutual capacitance [8]. The amplitude of XT noise depends on the values of mutual inductance and capacitance, the length of interconnections and the transition times of the signals. When multiple lines are strongly, inductively coupled the switch noise is significant and is referred to as simultaneously switching noise, ΔI noise, or dI/dt noise [71, 72]. To minimize the crosstalk, one or more of the following measures are adopted: increasing the distance between nets, adding guarding traces, reducing the length of the interconnections, decreasing the distance between nets and their reference planes and using low dielectric constant materials.

Noise in the power distribution networks result from parasitic inductance and the resistance of the connections. The resistance causes IR drops that decrease the levels of voltage at different points of the module [73]. The ground bounce or rail collapse is a typical noise for high speed assemblies without ground planes [52, 72, 74]. The noise is triggered when the ΔI noise is large in the PDN and mutual coupling between

many switching I/Os is strong. Due to the finite impedance value of the PDN, a voltage drop occurred when the IC current switches over inductive interconnections. Consequently, the rails of IC bounce -with respect to the ones of the PWB -according to the activity of the output buffers [75, 76]. This noise is becoming an important issue as the power consumption increases while the drive voltages decrease and signals switch faster. To minimize the rail collapse noise, the impedance of the PDN needed to be small and the connections had low inductance. These are achieved by utilizing low inductance decoupling capacitors, adjacent power and ground planes separated by thin, high dielectric constant material, and a large number of power and ground connections with small inductance [57].

The EMI/EMC noise represents lost energy in the communication process that is radiated into the neighboring environment. The noise levels increase with the operation frequencies and affect not only the signal integrity of the systems but also interfere with other devices as noise spreads over into the communication bands of neighboring electronic devices [8]. EMI/EMC regulations had been set for all electronic applications in order to permit the operation of different devices in close proximity without interferences. With the increase in the operating frequencies each small stub, through hole via, or open line become an antenna that radiates the energy from the assembly into the surrounding medium. The EMI/EMC issues are overcome through careful design which minimizes the return current loops, avoids open ends of traces, reduces the common mode noise from the PDN, increases the transition times of signals and uses a larger number of reference planes with a thinner separation layer between them [49, 77]. The ultimate and most expensive solution is to shield the noisy parts.

To overcome the noise in packages, high density interconnections principles are implemented in the design and fabrication process of assemblies [9]. Short interconnections and low dielectric constant materials help improve the signal quality of one net and decrease the XT noises. Low dielectric constant materials are preferred because of the shorter the time of flight of signals. The time delay is a wire is direct proportional with the square root of the dielectric constant of materials it propagates through. Moreover, the capacitive coupling between two adjacent lines is reduced when low dielectric constant materials are utilized; thus reducing the crosstalk

between lines. Fine lines and thin dielectric reduce the XT and EMI noise levels, while small vias and short connections reduce the PDN noise and improve the quality of the signal.

2.2 Signal integrity of one net

The allocation of the noise budget of systems shows that rigorous designs of each net considerably improve the noise figure of systems (Fig. 2.4) [7]. Ringing, reflections, discontinuities and crosstalk account for about 51 % of the noise while power distribution network noises, rail collapse and simultaneously switching output (SSO) noise account for about 49 % of the total noise budget.The design and fabrication processes are the two mechanisms that define the electrical characteristics of each line. The solder connections of vias, package leads, stubs, bends, gaps and splits in reference planes, changes of signal layers and reference planes of current return are some of the discontinuities encountered by the flow of the signal down the traces [12, 78]. The fabrication process affects the thickness and homogeneity of materials and the geometries of the lines [7]. Studies of signal integrity of one net are carried out in both the frequency and time domains. Utilizing the frequency domain it is possible to predict accurately the effects of discontinuities and materials losses. The time domain analysis helps to identify the discontinuities that introduce the highest power loss of signals.

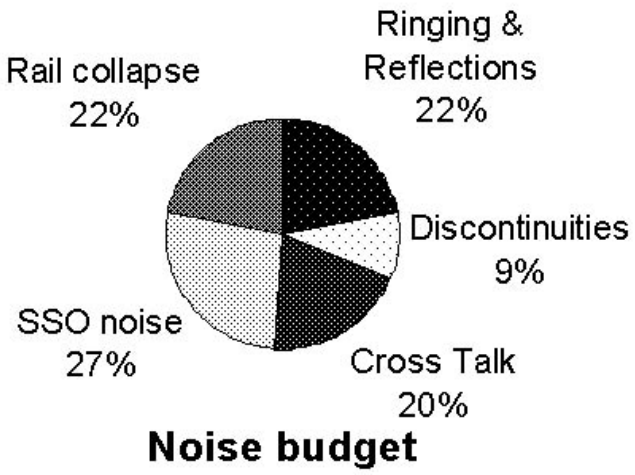


Fig. 2.4 Noise budget of a typical electronic assembly.

2.2.1. Transmission line theory

The transmission line theory has been developed to bridge the gap between the complex electromagnetic field theory (Maxwell's equations) analysis and circuit theory [17, 79]. Circuit theory is utilized mainly for low frequency applications where the size of the circuit is more than 10 times smaller when compared to the wavelength of the highest harmonic from the spectrum of the signal that is counted [12]. Currently, complex solutions are being developed to utilize the circuit models for high frequencies [63, 80 - 82]. These models are, however, employed only for limited bandwidth applications as the dispersion of materials is highly complex – and therefore, extremely difficult to be modeled. Utilizing the transmission line theory, the dimensions of the structures can range from a fraction of a wavelength up to a few wavelengths. In high-speed packages, the length of interconnections is comparable to the wavelength of the waves that compose the spectrum of the signal. For this reason the interconnections needed to be studied and designed as electrically long circuits utilizing the transmission line theory.

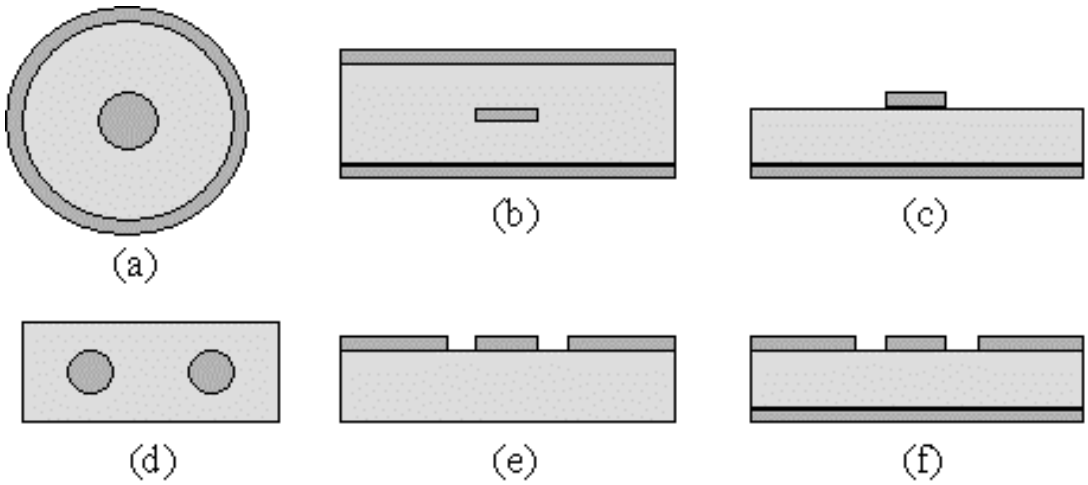


Fig. 2.5 Schematic presentations of the transmission lines: (a) coaxial line, (b) stripline, (c) microstrip line, (d) twin line, (e) coplanar waveguide (CPW), (f) finite ground coplanar waveguide (FGCPW).

Transmission line is a broad term that describes a material medium or structure that forms a path to direct the energy of signals from driver to receiver [17]. It consists of two parts, the signal trace and its return path that close the electrical circuit. There are a high number of transmission lines that are commonly utilized in assemblies: microstrip lines, striplines, coplanar waveguides, coaxial lines, twin lines and finite ground coplanar waveguides (Fig. 2.5). The type of the transmission line utilized in a

circuit is chosen based on the requirements of the system and stack-up configuration. The microstrip and coplanar waveguides are preferred for fast signals as the velocity of signals is comparable to the speed of light and the phase shift of different harmonics is small. When the noise budget is tight, good shielding and accurate communication are required. They are characterized by the unit-length time delay (t_d) (2.2) and characteristic impedance (Z_0). The time delay is the amount of time it takes the signal to propagate from the driver to the receiver. It depends on the speed of the wave propagation in the assembly media (v), the length of the trace (Δz), the parasitics from path discontinuities and the reactance of the load [17]. The characteristic impedance represents the ratio of voltage-to-current for a traveling wave in either direction at any point of the line.

$$t_d = \Delta z * \frac{\sqrt{\varepsilon_r}}{c} \tag{2.2}$$

A small segment of a transmission line is modeled utilizing ideal lumped components R (resistance), L (inductance), G (conductance) and C (capacitance) if the voltage drop between input and output is considered to be insignificant (Fig. 2.6). The R represents the series resistance per unit length due to the finite conductivity of the metal and the skin effect, for both conductors (Ω/m). The L is the sum of the total self-inductance of both conductors (H/m) and of the loop inductance. The shunt conductance per unit length is produced by the dielectric loss in the material between lines, (S/m). The shunt capacitance per unit length represents the energy stored in-between the lines (F/m).

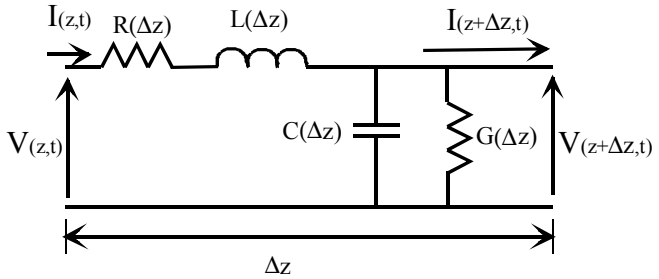


Fig. 2.6 The lumped element equivalent circuit of a part Δz of the transmission line.

The values of the voltage and current of the waveform are determined at each point of the trace with the help of the Telegrapher's equations. The solutions to the problems are expressed in both time domain (2.3) and frequency domain forms (2.4) utilizing

ideal circuit elements [17]. They represent the fundamental formulas utilized in the calculations of the impedance of the lines, propagation constant, and parameters of waves along the trace (2.5). Solving the equations the characteristic impedance Z_0 of the transmission line is related to the primary constants R, L, C, and G (2.6). The propagation constant (γ) is a complex number, which depends on the attenuation constant (α) and phase constant (β) of the transmission line. The real part, the attenuation constant, accounts for all losses, while the imaginary part, the phase constant, represents the phase shift of the sine wave (2.7).

$$\frac{\partial v(z,t)}{\partial z} = -Ri(z,t) - L\frac{\partial i(z,t)}{\partial t}$$
$$\frac{\partial i(z,t)}{\partial z} = -Gv(z,t) - C\frac{\partial v(z,t)}{\partial t} \quad (2.3)$$

$$\frac{\partial V(z,\omega)}{\partial z} = -RI(z,\omega) - j\omega LI(z,\omega)$$
$$\frac{\partial I(z,\omega)}{\partial z} = -GV(z,\omega) - j\omega CV(z,\omega) \quad (2.4)$$

The solutions

$$V(z,\omega) = V^{+}(\omega)\exp(-\gamma z) + V^{-}(\omega)\exp(-\gamma z)$$
$$I(z,\omega) = \frac{1}{Z_0(\omega)}\left[V^{+}(\omega)\exp(-\gamma z) - V^{-}(\omega)\exp(-\gamma z)\right] \quad (2.5)$$

Where:

$$Z_0(\omega) = \sqrt{\frac{R(\omega) + j\omega L(\omega)}{G(\omega) + j\omega C(\omega)}} \quad (2.6)$$

$$\gamma(\omega) = \alpha + j\beta = \sqrt{[R(\omega) + j\omega L(\omega)][G(\omega) + j\omega C(\omega)]} \quad (2.7)$$

2.2.2. Signal attenuation and dispersion

The conductors and dielectric materials of assemblies are not ideal. The interaction of their inner structure with the propagating electromagnetic waves causes attenuations and distortions of signals. The mechanisms of signal attenuation are: conductor loss (α_c), dielectric loss (α_d), radiation loss (α_r) and surface waves and high order modes loss (α_s) (2.8) [18, 78]. The losses are specific to each type of transmission line. They depend on the distribution of the electromagnetic field, cross-sectional dimensions of

traces and electric parameters of conductor and dielectric materials. The distortions occur due to the dispersion of electrical properties of materials with frequency. The values of attenuation and phase shift are characteristic to each harmonic of the signal.

$$\alpha_T = \alpha_c + \alpha_d + \alpha_r + \alpha_s \tag{2.8}$$

The interaction of conductive materials on signal loss is estimated knowing the conductivity of the metal, the roughness, operation frequency and the electromagnetic field distribution [17, 18]. The losses induced by the bulk resistivity of the metal are significant at low frequencies. The DC resistance of one net is calculated as the sum of the resistances of the signal line and its return path. At higher frequencies the magnetic field induced inside the metal conductor by the time varying currents increase the inductive impedance of the core of the trace. As a result, the current is repealed toward the outer surface of the conductor, flowing mainly in a defined penetration depth (2.9). This phenomenon, called skin effect, becomes important at high frequencies where the penetration depth is only a few microns. The conductor attenuation constant is calculated utilizing either the perturbation method or incremental inductance rule of Wheeler. The Wheeler's method, utilized in this study, expresses the series surface resistance as part of the total inductance created by the skin effect. The roughness of lines together with the skin effect, augment the physical length of the structure, which increases the ohmic losses (2.10) [29]. The surface finish of the conductor and the combination of two or more layers of high resistive materials on the conductor is another mechanism that adds to the conductor loss of the structures [24, 83, 84]. When a high resistivity material is present on the outer surface of conductors, the skin effect repels a considerable amount of current into that layer. Depending on the thickness of the layer and the surface resistance, the conductor loss can increase with up to 50 % (2.11) [29]. Similar effects occur when oxide layers are present on the surface of the solder bumps.

$$\delta_s = \frac{1}{\sqrt{\pi f \mu \sigma}} \tag{2.9}$$

$$\alpha_{cr} = \alpha_c \left[1 + \frac{2}{\pi} \tan^{-1} \left(1.4 \left(\frac{\Delta}{\delta_s} \right)^2 \right) \right] \tag{2.10}$$

$$R_S = R_{S1}\frac{\left[1+\frac{R_{S2}}{R_{S1}}\right]^2 * e^{(4t/\delta_1)} + 2\left[\left(\frac{R_{S2}}{R_{S1}}\right)^2 - 1\right]\sin\frac{2t}{\delta_1} - \left[\frac{R_{S2}}{R_{S1}} - 1\right]^2}{\left[1+\frac{R_{S2}}{R_{S1}}\right]^2 * e^{(4t/\delta_1)} - 2\left[\left(\frac{R_{S2}}{R_{S1}}\right)^2 - 1\right]\sin\frac{2t}{\delta_1} + \left[\frac{R_{S2}}{R_{S1}} - 1\right]^2} \tag{2.11}$$

Where, R_{S1} – surface resistivity of the high resistivity (layer 1),R_{S2} – surface resistivity of the conductor (layer 2), t – thickness of layer 1, δ_1 – skin depth of layer 1, and δ_2 – skin depth of layer 2.

The dielectric losses are the second major attenuation factor in electronics assemblies. At high frequencies the attenuation due to dielectric loss can surpass that attenuation resulting from the conductor loss because it increases directly in proportion to the frequency (2.12) [23]. The energy loss in dielectric materials occurs due to two mechanisms: relaxation of the molecular dipoles and resonance of the atoms, ions or electrons. The electromagnetic energy lost in dielectric materials is transformed into heat. At low frequencies, however, the electric field moves slowly enough that polarized molecules reach equilibrium before it changes the polarity. At microwave frequencies the fast change of the polarity of the field does not to allow the dipoles to reach equilibrium. The spin motion induced is strong enough to break the molecular bonds increasing the losses. The resonance mechanism occurs in the neighborhood of characteristic absorption frequencies [34]. The dielectric attenuation constant of a transmission line is calculated knowing the loss tangent and the filling factor of the dielectric. For the microstrip, stripline, coplanar waveguide (CPW), and FGCPW lines utilized in this study, the effective dielectric constant needed to be determined for each frequency.

$$\alpha_d = \frac{1}{2}\sigma_d\eta = \frac{1}{2}\omega\varepsilon\eta(\tan\delta) \tag{2.12}$$

Radiation loss occurs mainly at the discontinuities of the lines, as some magnetic lines do not return to the source conductor when the cycle alternates. These lines are projected into space as radiation with resulting losses in power. At high frequencies the discontinuities in transmission lines are also sources of surface waves. The high order modes propagation occurs when the substrates are electrically large compared to the wavelength of the signal. These losses are small compared to the dielectric and

metal losses. Nonetheless, they are the major factor of EMI and crosstalk disturbances in the interconnections.

2.2.3. Signal reflections

Significant energy losses and communication errors occur due to the reflections of the waves when the signal encounters impedance mismatches in the signal and its current return path. At each discontinuity, a part of the energy of the signal is reflected back towards the source while the remainder continues propagating in the initial direction but is distorted. False switching, bit errors and power loss are the functionality effects of the initial wave reaching the driver very weakly. Moreover, the reflected wave combines with the following signal generating intersymbol interference. Each impedance discontinuity is electrically described with the help of a parasitic resistance-inductance-capacitance (RLC) equivalent network [79]. As a result, the time delay of the interconnections and the rise time increases.

The change of the local impedance is as a result of the routing solutions or manufacturing process. Usual impedance mismatches encountered in assemblies are: pins, solder balls, wire bonds, trace bends, steps, stubs, branching, vias, changes of the reference planes of the return path, gaps in the return path, loading of the receiver and presence of passive components in the signal path. The parasitic effects of the discontinuities in the signal path have been investigated for a long time, with design rules and close form formulas having been developed to counteract these effects [17, 79]. From the physical dimensions of discontinuities, the values of parasitic R, L and C are determined and a new Z_0 of the trace at the discontinuity has been calculated. The discontinuities in the current return path of the signal proved to have significant impact on the characteristics of the line as at higher frequencies, the return current followed closely the signal path [8, 67]. Splits or holes in reference planes forced the return current to take a longer path, increasing the local impedance. Another return path situation that was not ideal was encountered when the signal changed the reference planes. The return current had to also change the planes in order to follow the signal. To do this, it chose the lowest possible impedance path through the decoupling capacitors or coupling between the adjacent planes [7, 11]. The third major discontinuities in the signal return path occurred at the interconnections and

connectors. The signal and the return path had to flow through different connections, creating an inductive loop in the circuit. Frequently, the return path connection was sheared by multiple signals, resulting in signal attenuations.

The manufacturing process is the second mechanism that affects the characteristic impedance. The non-homogeneity of dielectric substrates, usage of mixed materials with different dielectric constant, the sidewall shape of conductors, and thickness of the solder mask all change the local value of the characteristic impedance. The underfills and globtops are one of the unstable materials. Their electrical parameters change with the variations of settling times, viscosity, content, shape and size of the filler particles, curing time and pot life. They detune the components, interconnections and traces routed in the vicinity of the components. Detailed discussion is presented in the next sub chapter.

The reflection phenomena are studied both in the time and frequency domains. In the time domain, a reflection coefficient is determined utilizing the Telegraph theory. In the frequency domain, the effects of discontinuities are investigated by comparing the decrease of the amplitude and the shift of the phase of the output and input sine waves. With the increase in frequency the impedance mismatch causes more energy to be reflected towards the source. To solve this problem, terminations are utilized to match the impedance of the line with the one of the driver or receiver. Five types of termination circuits can be utilized to address the problems: parallel, series, Thevnin, AC, diodes.

2.3 Electrical modeling of interconnections

The modeling of assemblies is an essential part in the design and integration of modern electronics. The electrical model of an interconnection accounts for all the discontinuities and materials present in the path of a signal. The model is, however, an approximation of electrical performance because not all physical features are included in the model for a number of reasons: the fabricated parts do not perfectly match the specifications of design, the properties of materials change with each fabrication process and frequency, the return path is assumed to be ideal, real structures are more

complex than described in the model, boundary conditions in the model do not perfectly match the real world ones and, typically, the bandwidth of the application is larger than the bandwidth of the model. The modeling process requires extensive consideration of the physical parameters of circuits, the properties of materials and system requirements. To predict the waveform of signals, noise levels and the timing budget of systems, two distinctive processes are employed: model development and simulation. The modeling translates the physical world into mathematical expressions and electrical circuits. The simulation process makes use of the electrical models to calculate the waveforms of voltages, currents and predict the performances of the circuit. Modeling and simulation are the first steps in signal integrity analysis. They are utilized to determine the best architecture of the package that, together with the performance of the circuits, fulfill the timing and noise budget requirements for each specific electrical device [85]. Modeling is extensively utilized to minimize the cost and time to market of products. Being such an important part in assembly characterization, the methods employed to determine the performances of interconnections are presented in greater detail in the next section.

2.3.1. Models of interconnections

The electrical model is a mathematical description or electrical equivalent circuit that represents the behavior of a device. The models of interconnections and the quality of packages are determined with the help of experimental measurements, electromagnetic calculations, or predefined close form formulas. A recurring issue in the development and application of models is the use of simplifying assumptions to allow a compromise between accuracy and complexity. The electrical models are divided into non-linear or large signal and linear or small signal. Each of these is divided further into time invariant and time or frequency dependent. Electrical models of connections are a single lumped element, a network of lumped elements, a distributed element circuit with per unit length parameters, a transmission line, a transfer function, a “black” box containing S, Z, Y, or H parameters or a behavior model such as Input / Output Buffer Information Specification (IBIS) [86 - 89].

The simplifying assumptions and rules of thumb utilized in the modeling process cover three parts: the dielectric materials, the shape of the metal circuitry and ports

and boundaries. The most common assumptions regarding the dielectric materials are: isotropic, homogen, the thickness is constant, and the stability of their electrical parameters with the frequency as the parameters varies very little. When 2.5D or 2D electromagnetic simulators are employer and the spatial distribution of the materials is very complex, based on the calculations some parts of materials can be allocated as their neighboring ones if their characteristics are close. The assumptions for the metal parts are that the corners and steps are 90 deg, which in reality is not possible, the circle arcs are segmented in a finite number, the thickness of the conductor is constant, and side walls are 90 deg. For the ports, it is assumed that they are the only source of radiation in the system, they can support polarized waves, and perfectly match the measurement devices. The boundary assumptions are made with regard to their status: close, open, perfect electric, perfect magnetic. The calculation time can be reduced if the structure is symmetric and correct boundary conditions are applied. Concerning the model the assumptions are: there are no other circuits in the vicinity that can influence the performances, the boundaries are far enough not to affect the electrical characteristics and for they are small compared to the wavelength. As a rule of thumb can be introduced that a model can be transformed into an electrical circuit model if its size is less than one tenth of the smallest wavelength.

2.3.1.(a) Modelling of the assemblies

Until quite recently, the models of packages have been determined mainly for RF assemblies, mostly coming from experimental measurements and electromagnetic simulations [90]. The output of analysis is presented as the S matrix, Z matrix, and reflection and transmission coefficients. Complex electromagnetic simulators make use of scattering parameters, while simpler circuit simulators require further processing to establish the circuit or IBIS models [37, 91]. The circuit models are utilized when the application has a narrow bandwidth and the interconnections are short. They are the preferred form for digital applications as they are well integrated into the simulations of digital circuits. Circuit model are a bridge between the results from EM simulators or experimental measurements and circuit simulators. Nevertheless, the development of mixed signal applications demanded that the interconnections models be utilized by both the RF and digital simulators. Considering the large bandwidth of the high-speed digital signals, frequency

dependent electrical models had to be developed for electrically long connections [7, 50]. The circuit models became increasingly complex, as they had to also account for the less than ideal current return paths.

The research into the effects of assemblies on signal integrity focused on three specific directions: the geometries of connections, materials losses and assembly techniques. For many years now, the electrical models of flip chip and wire bond connections have been widely researched, developed and implemented in simulators, as they are the most common connection methods in use [92 - 95]. Studies of solder bump connections have focused mainly on the effects of the geometry of connections on signal quality. The models developed consider the height and diameter of the bumps, the dimensions of the pads, the width of the connection lines, and the overlapping area [14, 96 - 98]. The flip chip connections are modeled as a π type RLC network having good accuracy up to 35GHz (Fig. 2.7b) [99]. The material losses of the PWB and component are simulated by adding three resistive elements to the π model [15]. In order to improve the electrical performances of the connections, further research focused on the shape of the bumps, the possibility of utilizing multiple bumps for signals and ground connections and their staggered displacement [20, 80, 82, 100]. Moreover, for some applications the pads of interconnections are designed as matching circuits to reduce the reflection losses [36, 101]. The RF performances and models of Anisotropic Conductive Adhesive bonds and connections utilizing Au and polymer bump materials have been researched and developed [102 - 104]. The wire bond connections are more complex to model, as each connection has a specific length of the wire, start and end angles and loop height [105 - 107]. Depending on the accuracy and bandwidth of the model, a wire bond is modeled as an inductor or a RLC network. The performances of the nets, their discontinuities, and vias had been extensively researched for RF and microwave applications. Close form formulas are and rules of thumb are determined to enable fast and accurate calculations [17, 18, 79, 108].

2.3.1.(b) Modelling of the materials

To date, studies of assembly materials have focused mainly on the expensive solutions utilized in analog applications such as low-temperature co-fired ceramics (LTCC) and

polymers. In more recent times as operating frequencies have increased up to a few GHz, the usual materials are accurately characterized at microwave frequencies to predict the amplitude attenuation and phase shift of signals [109 - 110]. This has helped in the development of accurate models of interconnection as they rely on the knowledge of the properties of materials [111 - 113]. Materials studies have shown that in addition to the dielectric constant and loss tangent of the dielectrics, it is also important to take into consideration also the smallest details such as the conductance/surface finish of conductors [30, 110]. The development of dielectric materials has been carried out in two directions: insulators with small ε_r for separation of digital signal layers and dielectrics with high ε_r for power layers and high density RF integrated components. Utilizing low ε_r as carrier substrates for digital signal layers, some of the signal integrity issues, such as coupling, delays and losses, are minimized [7]. Power distribution noise and the size of decoupling capacitors and RF integrated circuits are reduced when materials with high ε_r are utilized in the stack-up. Regardless of the dielectric constant, a common requirement of the materials is to have low loss tangent in order to avoid power losses in dielectrics. The characteristics of the materials are evaluated utilizing resonators and transmission lines. These methods provide accurate feedback on the properties of the dielectrics and conductors after the fabrication process. Moreover, utilized in mass productions they provide useful information on the influence of fabrication processes on the properties of materials and contaminations [109, 114, 115].

The glop-top and underfill materials are among the first materials whose electrical parameters are to be investigated at microwave frequencies as it is noticed that their presence change the electrical characteristics of the connections and circuitry of components [112]. Studies on the influences of the underfills on a flip chip assembly of a low noise amplifier showed a small detune caused by the underfill at a few GHz [32]. Further investigation revealed that the underfill increased the losses of the 0.6 mm CPW transmission lines with up to 1dB and detuned it by increasing the reflection losses with up to 3 dB at 40 GHz [33]. The Measurements up to 115 GHz of a 1.6 mm flip chip test coupon with lead-free interconnections showed that the insertion losses of the coupon with/without an underfill are the same 0.8dB/mm at 110GHz while the reflection losses are 6dB / (9 dB) at 110GHz [36]. The metal plane

together with the bump height contributed to the change of electrical parameters of the component [96].

The results from research on materials and high density interconnections are utilized in the development of the models of new chip in board assembly technologies. The connections of embedded components to PWBs are realized utilizing blind or buried vias and package materials are the ones of the buildup layers of PWBs. The lumped element model is determined for Bumpless Build-up Layer packaging (BBUL) technique, as its inductance is important for the PDN [20]. The model of CiB for MCM is realized with the help of distributed transmission lines up to 100 GHz [63].

2.3.2. Circuit models of interconnections

Circuit models together with circuit simulators represent a very powerful tool to determine the electrical performances of circuits and systems. The precision of the simulation results depend on the accuracy of models utilized and assumptions made in the calculation process. The models are selected considering the complexity of calculations, accuracy and bandwidth.

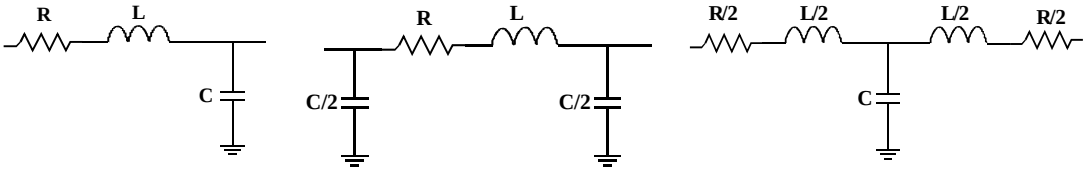


Fig. 2.7 Circuit cells utilized for cascaded networks.

The complexity of the model depends on the electrical length of the circuit, the intricacy of the signal path and the bandwidth. The bandwidth of a circuit model of an interconnection, measured in Hz, represent the highest sine wave frequency that is accurately predicted by the actual behavior of the structure it is representing. An interconnection is considered to be electrically short if its physical length is shorter than $\lambda/10$ of the highest frequency of the bandwidth [116, 117]. For electrically short connections, the values of voltages at the ends of the trace are assumed to change instantaneously and the travel time is neglected. In this case, the model of connections

is an element or a network. A circuit network is realized with the help of ideal R, L, and C components disposed on *L* (Fig. 2.6.a), π (Fig. 2.6.b), or *T* (Fig. 2.6.c) configuration according to the geometry of assemblies (Fig. 2.7). Electrically long circuits are modeled utilizing cascaded networks, distributed circuits, and transmission lines. A simple cell did not suit large signal simulations because the RLC parasitics are not concentrated in one spot but distributed along the trace. Cascaded networks are utilized to obtain models with large bandwidths [7, 13]. The large bandwidth models are realized by dividing the total values of RLC parameters into an *n*-sections cascaded network. The number of cascaded networks (*n*) is determined knowing the required bandwidth of the model (BW_{model}) and the estimated time delay (t_d) of the structure (2.13) [7]. The *n* is calculated taking into account that the BW_{model} had to be larger than the BW_{signal}. For digital applications the rise time and time delay are utilized to determine the BW_{model} (2.14) [7]. After the initial calculations, fine-tuning of models is required as the close form formulas failed to account for the delays introduced by the parasitics of the discontinuities. Usually, a higher number of cascaded networks are required for accurate modeling of interconnections. Another solution to develop the models of interconnections utilizes the predefined circuit models of the individual component of the assembly, e.g. the wire bond, lead, bump, vias and trace all bend into a distributed model that represents each impedance discontinuity.

$$n = 10 * BW_{model} * t_d \tag{2.13}$$

$$n > 3.5 \frac{t_d}{t_r} \tag{2.14}$$

2.3.3. Simulation methods

The numerical analyses are the preferred methods utilized to evaluate the performances of interconnections and determine their models [118 - 120]. The accuracy of all models depends on the errors from the modeling methodology, knowledge of the material properties, calculation errors, over-simplifications and assumptions. The choice of the simulation methodology depends on the complexity of the assemblies, the accuracy required and the performances of systems for which the models are developed.

The finite-element method (FEM), finite-difference method (FDM) and method of moments (MoM) are numerical techniques that utilize the Maxwell's equations to solve complex 3D problems in frequency or time domains [121]. Based on full wave electromagnetic analysis they are used for modeling and simulating the interconnections as they accurately predict the behavior of structures with complex field distributions. With their help can be determined the models of interconnections, the critical reflection sites and the effects of different geometries on the distribution of electromagnetic field and propagation modes, thus improving the performances of packages.

Electromagnetic modeling is a broad subject that is widely covered in the literature [120 - 123]. There are a high number of applications for numerical calculations of the electrical parameters of 2.5D and 3D electrical circuits. A review of the commercially available simulators is published by Swanson and here will be introduced some of the main players and their products [121]. Ansoft Corporation develops: Maxwell 2D, Maxwell 3D and High Frequency Structure Simulator (HFSS) software. HFSS application performs full wave calculation utilizing finite element method. It is suitable for small structures with radiation problems and it can predict the performances of complex structures and material spatial distribution for high frequency applications. The main disadvantage is the time and calculation power required to solve the problems. The obtained results must be further manipulated before utilizing them with a low cost commercial circuit simulator. The Maxwell software is intended to provide fast calculation and accurate circuit solution to be utilized in low cost simulators. Zeeland Software Inc. started with the IE3D, a full wave 3D solver that utilize the method of moment. This is suitable for planar electromagnetic simulation and optimization package for circuit and antenna applications. Fidelity is the second product that is a full wave 3D simulator that utilizes finite-difference time-domain (FDTD) method for calculation. It suits simulation package and RF applications. Agilent Technologies, develop as their main products the Advanced Design System (ADS), MoMentum (MoM) and Electromagnetic Design System. ADS is a electronic design software for high-frequency system and circuit design. It has, by default, integrated good link to other software and measurement instruments, and has integrated physical layout and art work translator. MoM, is a 2.5D planar simulator used for passive circuit analysis that

can cope with multi-layer structures and complex electromagnetic effects such as coupling and parasitics. It is easily linked with ADS and together they are a powerful set of tools where the number of steps between the EM simulations to time domain simulations, equivalent circuit model development and artwork are small. Sigrity Inc, has SPEED2000 special software based on the FDTD solver for modeling interactions in multi-layer chip packages and printed circuit boards in time domain.

Electromagnetic modeling approaches can be classified in two groups: differential equation based (DE) and integral equation based (IE) [122]. The finite-difference (FD) and finite element (FE) analysis belong to differential equation group as they utilize the direct discretization of the Maxwell's equations. The discretization is done to the entire volume of interest. In the case of FD, the Maxwell's equations are determined at each node of the grid while for FEM, a function is introduced that is minimized over the volume of interest by solving the Maxwell's equations. For the representation of the electromagnetic fields, local non-zero functions are employed. Using the Galerkin technique, the Helmholtz equations are transformed into weak integral form. To solve them, boundary conditions such as perfect magnetic conduction and electric conducting surface must be empowered. After this the discrete approximation of the problem is translated into matrix form. The matrix is sparse, making it appropriate for iterative solving techniques, which is one of the two advantages of the method. The second advantage is the modeling versatility, both in complexity of materials and their spatial variation. But, this represents the main disadvantage because the matrix becomes large and difficult to inverse as the calculations are done for each node of the mesh. Another disadvantage is the discretization where the curved surfaces and nonrectangular volumes are usually modeled as a staircase, increasing considerably the number of nodes to be computed.

Based on the FD method the FDTD was first is a popular time-domain method utilized to simulate 3D circuits [15, 123 - 125]. It utilize Cartezian grid that reduce significantly the matrix size. The space steps Δx, Δy, Δz, are chosen that the integral number suits the various dimensions of the model. One rule of thumb to reduce the truncation and grid dispersion errors is to utilize the step size of $\lambda/10$ of the highest frequency that matters in the simulation. Courant stability criterion is used to select a time step that insures numerical stability. The first step is to ensure that the iterative

solver converges. The convergence criterion can have different values that have to be set for each parameter calculated. For S-parameters is specified that the relative residual norm to be less than 10^{-5} to 10^{-6} as they are sensitive to the minima and maxima positions of the voltage standing wave pattern. The numerical convergence depends also on the electrical parameters under study. Dense meshing can be required as up to 30 cells per wave length. The solution for this is to use higher order basis functions that can complicate computations but provide faster convergence for both electric and magnetic fields. Comparison of the FEM and FDTD methods for packaging problems showed that the results are in good agreement [90, 126]. The MoM method will be presented in detail as it is utilized in this work to study the interconnection performances at microwave frequencies together with the advantages and disadvantages as compared to FEM and FDTD.

2.3.4. Method of Moments

The electromagnetic analysis utilizing Agilent – MoM is divided into two parts: the physical design and calculation. The physical design is the first step of the modeling and it focused on identification of the metal and dielectric materials in the structure. During this procedure, the layers with eventual mixed dielectric materials are identified and preliminary calculations performed to evaluate which assumptions introduced least errors. After the initial investigations and calculations the dielectric layers and their thickness are defined and the metallization patterns built. When the electromagnetic model is constructed, the amount of information available is usually limited. Typically, however, the electrical performances of dielectric at different frequencies are not well known. On the other hand, the geometry of structures is too full of details to be included in the model and simplifications have been adopted. The boundary conditions are set as free space or close boundary depending on the neighboring environment of the component. The last step of the physical design of the model is the placement of the ports where the energy is injected into the system.

The simulation part starts with the definition of the mesh. The size of the edge mesh is calculated to be between 2-5 % of the line width for good accuracy [127]. The number of mesh cells per wavelength is determined by considering the size of the structure and accuracy. Finally, the range of simulation frequencies is defined as well as the

calculation method. During the calculations, the metal patterns are meshed using general polygonal cells or elementary rectangles or triangles. Maxwell's equations are translated into integral equations for each node of the mesh where the Green's dyadic $dS\overline{\overline{G}}(r,r')$ of the layered medium acts as the integral kernel (2.15) (Fig. 2.8a). The $J(r)$ represents the unknown surface currents and the $E(r)$ the known excitation of the problem. The surface currents of the metallization structures are calculated utilizing rooftop basis functions defined over the cells in the mesh (2.16) (Fig. 2.8b). Next the Galerkin testing procedure is applied to impose the boundary conditions, resulting in a method of moments interaction or impedance matrix. The unknown surface currents are discretized to I_j by meshing the planar metallization patterns and applying an expansion in finite numbers of sub-sectional basis functions $B_1(r)$, $B_N(r)$ (2.16). In this network, the nodes correspond to the cells in the mesh. Each cell corresponds to a capacitor to the ground representing the electric self-coupling of the associated charge basis function. All nodes are connected with branches which carry the current flowing through the edges of the cells. Each branch has an inductor representing the magnetic self-coupling of the associated current basis function and a resistor representing the conductor loss due to the current basis function (2.17). The final results are presented as scattering parameters.

$$\iint dS\overline{\overline{G}}(r,r').J(r) = E(r) \tag{2.15}$$

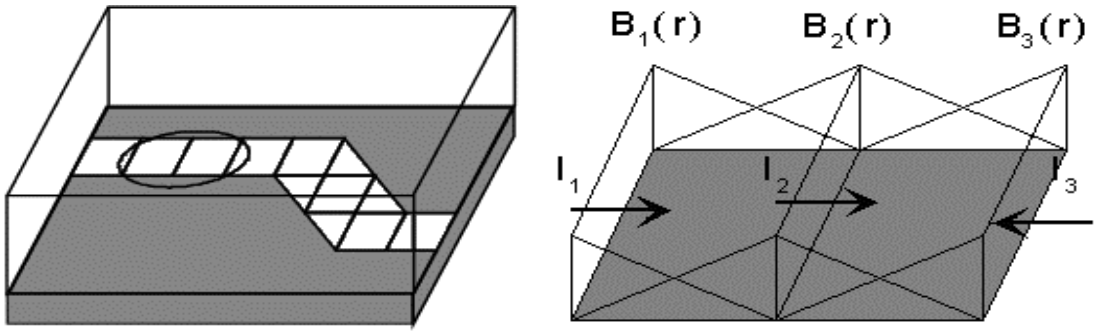
$$J(r) = \sum_{j=1}^{N} I_j B_j(r) \tag{2.16}$$

$$[Z] \bullet [I] = [V] \tag{2.17}$$

$$[Z] = [R] + j\omega[L(\omega)] + \frac{1}{j\omega C}[C(\omega)]^{-1} \tag{2.18}$$

From the calculation method it can be seen that, the accuracy of the Agilent Advanced Design System (ADS) – Momentum (MoM) is limited by the meshing process and material properties. High accuracy is achieved when dense mesh is used - yet it is negatively affected by an aggressive approach that can lead to heavy calculation and convergence problems [127]. In fact, the accuracy and the number of cells follow a Gauss type curve with a maximum at 30 cells/wavelength and size of the edge mesh 3

% of the conductor width [127]. Moreover, the calculated electrical losses are affected because the roughness of the conductors and the dispersion of dielectrics are not considered. The definition of the ports and their ground reference needed to be considered together with the signal return paths.



a. b.

Fig. 2.8 Schematic representation of meshing and calculations of Method of Moments.

The assignment of the ports plays an important role. When reference ports are utilized, the return currents are forced to close at a specific point. The errors from the calculation engine are the same for any integrals solver: these include such things as round-off errors or local and global truncation errors. The truncation error (discretization error) can be generated by the algorithm and by the mesh procedure. The numerical error has little impact on the results due to the calculation procedure. Momentum calculates Summerfield integrals in a numeric way to obtain the green's functions of an open multilayered medium. In a closed box medium, Green's functions are analytically known as a series expansion. For this no numerical evaluation is required but the discretization of the shapes is restricted to a uniform grid. The round-off error is related to layout details. Mesh resolution is directly related to the Layout Precision data base units (dbu) value. All gaps or other unresolved layout vertices will be resolved by the mesh generator if their distance is less than 2 dbu. By measuring the performances of a circuit and comparing the experimental results to the calculated ones, the models for research are improved. Moreover, the results from different simulations are compared with one another to study how sensitive the model is to the adjusted parameters.

The main differences between FD and FE methods and the MoM method rest on the method of numerical calculation and meshing. The FDM and FEM suits to small, non radiant circuits with inhomogeneous materials as the meshing is done over the volume and for good accuracy of the results some parts have to be very fine meshed up to □/20 of the highest frequency [122]. The MoM utilizes the surface integral technique, where only the boundary surfaces are meshed. This results in smaller but denser matrix to be solved. The 2.5D MoM simulator is appropriate for unbounded structures with radiation problems, having ideal metals and homogenous dielectric layers. The advantage of MoM technique over the FEM and FDM is the short time required to solve the problems. The MoM together with ADS form a very useful tool where the precision of EM solved can be utilized for time domain simulation, electrical circuit extraction and easily create the artwork. Comparison of MoM to FEM and FDM methods was carried out in several papers [125, 128 - 132]. The results proved that the MoM method suits interconnection modeling as the results from MoM, FEM, and equivalent circuit calculations and measurements were in good agreements up to 20 GHz in frequency domain and showed very good match in time domain [125, 132]. The comparison of FEM, FDM and MoM for simulation of antenna showed that the errors are minimal but MoM provides the shortest time of calculation with the least CPU loading [129]. De Moerloose in [131] presents the differences between the integral equation and differential equation based methods utilized for shielding calculations. It is emphasized that each method has to be carefully evaluated for each application.

2.3.5. Time domain methods

Time domain reflectometry or TDR is a measurement technique used to determine the characteristics of electric lines by observing the reflected waveforms. The technique relies on the transmission line theory. The analysis is performed in the time domain by stimulating the device under test with a short edge voltage step. The incident and reflected waves are monitored by an oscilloscope. This echo technique reveals the characteristic impedance of the line and shows both the position and the nature (resistive, capacitive, or inductive) of each discontinuity along the line and at the terminations. Moreover, it shows weather the losses are shunt or series losses. The propagation constant γ is utilized to define the current and the voltage at any distance

down the line and identify the location of mismatches. Knowing the voltage and current it is determined the local characteristic impedance of the line at any point. This method allows identification of the mismatches at the driver, receiver and on the line. The advantage of the technique is that the results are facile to determine and analyze.

The analysis of the line mismatches is done assuming that the line ends at the discontinuity point. The remaining part of the line is modeled as a impedance equal to the Z_0 of the line connected in series with the equivalent circuit of the discontinuity. The shape of the reflected wave is valuable because it reveals both the nature and the magnitude of the mismatch. The overshoot of the signal indicate the presence of an inductive load and the undershoot the presence of a capacitive load. Complex combination of the RLC parameters can be determined from the obtained waveform.

In this research the analysis is carried out utilizing both time and frequency domain calculations, as they are dual. The results obtained from the time and frequency domains contain the same information but there are differences in the ways the results are presented. To fine tune the system, precise information is needed on impedance discontinuities where the highest reflections occurs. This information can be obtained from the results from the time domain investigations as their output is impedance and reflections versus time (2.19) (2.20) [17]. Nevertheless, the scattering parameters also become important in the high-speed applications design process [133 - 137]. The resulting information obtained from the S-parameters without further manipulation is insertion loss, reflection loss, and resonance frequency. The time and frequency domains are dual. Analysis of the digital systems utilizing the S-parameters required that certain methodologies be adopted. Utilizing the inverse fast Fourier transformation (IFFT) from the scattering parameters, the reflection and transmission coefficients are determined (2.21), (2.22). The Agilent software had already implemented functions that calculate the time domain response form the S-parameters [127, 135].

$$\Gamma(t) = \frac{V_{refl}}{V_{inc}} = \frac{Z_{DUT}(t) - Z_{source}(t)}{Z_{DUT}(t) + Z_{source}(t)} \tag{2.19}$$

$$\tau(t) = \frac{V_{trans}}{V_{inc}} = \frac{2Z_{term}(t)}{Z_{DUT}(t) + Z_{term}(t)} \tag{2.20}$$

$$S_{11}(f) = 20\log_{10}[FFT(\rho(t))] \tag{2.21}$$

$$S_{21}(f) = 20\log_{10}[FFT(\tau(t))] \tag{2.22}$$

In the ADS program, the S-parameters are transformed to the time domain by applying the IFFT and the LaPlace transform along with normalization factors to calculate the TDR reflection coefficient (tdr_sp_gamma) (2.23) and impedance variation with time (tdr_sr_imped) (2.24) or older functions (ts together with zin). The input data for calculation is the S-parameter matrix (Sdataheet), delay, start time (Tstart), stop time (Tstop), window and number of points (num pts). The window specifies what procedure to be utilized in the calculation (None, Hamming 0.54, Hanning 0.50, Gaussian 0.75, Kaiser 7.865, etc). A delay can be introduced into the calculations ($E^{j\omega\tau}$ phasor) to shift the time of the simulated data. The ts function performs only the frequency to time transformation (2.25). Compared to the tdr sp_ functions, it offers the user more control over the calculation process. The number of calculated points, which normalizes a trace to a known amount of energy in the transform, can be controlled for all models settings (2*BW/num pts). It accounts for the number of first harmonics to be transformed (nptsspec) and the dimension to be transformed (dim). 1/jω is the LaPlace integral that convert an impulse response into a step response. The results from this transformation are utilized to analyze the impedance, reflections and eye diagrams. The impedance analysis (zin) (2.26) is performed considering TDR [0] as the first point in the TDR trace and presumably 50Ω. Any difference from zero is a constant of the integration caused by the 1/jω integration.

*Rez_gamma=**tdr_sp_gamma** (Sdatasheet, delay, Tstart, Tstop, dim, window).* (2.23)

*Rez_Z=**tdr_sp_impedance** (Sdatasheet, delay, ref imped, Tstart, Tstop, num pts, window)* (2.24)

*Rez_TDR=**ts** (Sdatasheet ($S_{i,i}$)*delay*(2*BW/ num pts) / (j2πf), Tstart, Tstop, dim, window, nptsspec).* (2.25)

*Rez_Z=**zin**(Rez_TDR – Rez_TDR[0], 50).* (2.26)

The other function implemented in ADS tools is the automatic circuit model development from the S-parameters. This is achieved by converting the S-parameters to y-matrix (s2spice) and interpolating it by a rational polynomial approximation (Spice Model Generator - Agilent), or vector fitting to the Spice model. The accuracy of these tools is good up to a few GHz after which fine-tuning is required.

2.3.6. Measurement methods

Experimental analysis is the ultimate test of the quality of the packages. From the experimental results the models of the interconnections are determined, the resonance of the package investigated, and the accuracy and bandwidth of the equivalent circuit model created utilizing the numerical tools are verified [138 - 141]. Due to cost and practical limitations this method is utilized in the last stage of package development. A JEDEC standard is elaborated to provide guidelines for extraction of the parasitic L and C of the assembly [72, 142 - 144]. All measurements are performed in time or frequency domains utilizing an impedance analyzer, an LC meter, a time domain reflectometery (TDR) analyzer, and a vector network analyzer (VNA). In the time domain, the device under test (DUT) is stimulated by a voltage step in the time domain analysis (TDR, TDT). In the frequency domain the DUT is characterized at each frequency relative to the amplitude and phase of the incident wave.

The results in TD are presented as local impedances or the reflection coefficients function of time. The rise time degradation, time delay and type and magnitude of discontinuity provide the knowledge on losses and reflections of signals. The change of the impedance of the trace is influenced by the size of discontinuity and the transition time of signals. The values of parasitic L and C of discontinuities are easily calculated utilizing the circuit theory. The measurements are less prone to design and measurement errors, less costly, easier to perform and the results are too facile to be analyzed. These measurement methods are usually utilized when the coupling between connections generates important crosstalk noise and multiple ports measurement is required. The limitations are introduced by the dynamic range of the oscilloscope (about –50 dB) and the limited rise time of the pulse that can overlook small discontinuities [145, 146].

The second possibility to analyze the assemblies is to utilize the frequency domain experimental measurement. The high frequency responses of the packages are estimated measuring the admittance (*y*), impedance (*z*), transmission (*t*) and scattering (*s*) parameters. The S-parameters are the most utilized because the measurement techniques provide accurate results at high frequency, the theory is well established, and the measurement equipment is freely available. The performance of DUTs is evaluated knowing that the amplitude and phase of each wave is affected differently by the material losses and the discontinuities of interconnections. The dynamic range of measurement devices can be 100 dB and the highest frequencies can be 110 GHz. The accuracy of the measurement results depends to a large degree on the calibration of the measurement set-up. The calibration process is a critical step in the frequency domain experimental measurements. It is utilized to eliminate the parasitic influences of cables and connectors on the measured results of the performances of the DUT. A considerable amount of research had been carried out to study and improve the calibration techniques [86, 145, 147]. The measured scattering parameters can be utilized as a "black box" matrix for RF simulations or a mathematical process to further convert them into Z, Y, H or ABCD matrixes or to determine the circuit model.

The quality of packages is an important issue for signal integrity. The packages are selected for each application considering the bandwidth of the connections and losses. The complete path within the package should not introduce more than –15 dB of return loss or –3 dB of insertion loss [58, 128, 148, 149].

3. Experimental procedures

In this chapter the design, materials, manufacturing and measurement processes, methods and procedures of the test boards are presented. The experimental work formed an important part of this research as some of the effects of materials and assembly techniques on signal integrity were closely examined for the first time. The influence of packaging materials and assembly techniques has been investigated experimentally utilizing three different systems. Each system was developed to perform precise electrical functions that enabled the achievement of accurate results while fabrication and testing errors were kept to a minimum. To begin with, test coupons were developed to study the influence of the oxide layers and the microstructure of solders on the signal integrity. Secondly, systems which utilized specially designed and fabricated WLCSP components and test boards were studied in order to determine the detuning and losses effects of three different underfills on the circuits and interconnections of the components. Study of the influence of the assembly techniques (IMB and SMT) on signal integrity were carried out with the help of a third test set-up. For this test, special components and test boards were designed and fabricated. The design process of all the systems was carried out by careful consideration of the electrical performance of the circuits, the manufacturing technologies and the measurement set-up. Transmission line and electromagnetic field theories were employed to calculate the characteristics of the boards and to provide analysis of the experimental results. The test boards were fabricated using both PWB and clean room processes and the assembly techniques utilized were IMB and SMT. The measurements were performed with a vector network analyzer and the connection to the test boards was realized with on wafer probes or test fixtures.

3.1 Development of the test boards for studies of the effect of oxide and microstructure on SI

The influences of oxide layers and microstructures of lead-free solder materials on insertion losses of high-speed signals up to 50 GHz were evaluated utilizing specially designed, manufactured and measured prototype boards. The insertion loss of several

hundred bumps was measured to a good degree of accuracy with the help of the newly developed investigation technique. For this, 4-cm-long microstrip transmission lines were manufactured out of the lead-free materials under investigation to simulate the effect series connected solder balls. The carrier substrates for all samples were manufactured from the same material. The same fabrication process was applied to all the test boards. Therefore, the dielectric loss of the substrate and the radiation loss were the same for all boards. The values of attenuation due to conductor loss induced by a particular oxide layer thickness and microstructure size were determined by measuring the total power loss of the test coupons, and comparing the results obtained with those from the reference test boards (3.1) [18]. In the case of oxide layer investigation, the measured losses of the highly oxidized solders (SnO and SnAgCuO) were compared to the ones of the natural oxides (Sn and SnAgCu). For the microstructure analysis, the comparison was carried out between the losses of the reference test boards that had the finest microstructures and the ones having different degrees of coarseness.

$$\alpha_T = \alpha_c + \alpha_d + \alpha_r \qquad (3.1)$$

Where α_T is attenuation due to total losses, α_c is attenuation due to conductor loss, α_d is attenuation due to dielectric dissipation loss, and α_r is attenuation due to radiation loss.

The test board consisted of two parts, the carrier substrate and the lead-free material under investigation (Fig. 3.1). The material for the carrier substrate, liquid crystal polymer (LCP), was selected because of the stability of its electrical parameters over a broad band of microwave frequencies; the dielectric constant (ε_r) was 3 and loss tangent ($tan\delta$) was 0.003 [113]. Furthermore, by using thin substrates of 125 μm, multiple mode wave propagation in the dielectric at high frequencies was avoided [150]. Thus, the radiation loss of the transmission line was kept to a minimum, and high frequency dielectric loss was decreased. The lead-free materials under investigation were pure tin (Sn) and a lead-free solder alloy Sn3.8Ag0.7Cu (abbreviated here as SnAgCu). The 100 μm thick sheets of the pure tin (Sn 99.999) were provided by Goodfellow Inc. UK. The SnAgCu material was provided by Multicore Solders Ltd., Henkel, in bars and was cold-rolled down to a thickness of 100 μm.

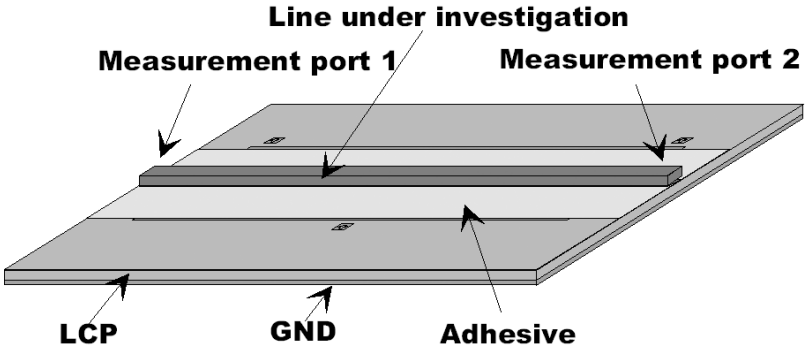


Fig. 3.1 Schematic presentation of the test board.

The lead-free materials were annealed before assembly to the carrier substrates. Thus, the substrate carrier had the same properties for both the highly oxidized samples and the natural oxide ones. The influence of the etching process that exposed the natural oxide material on the sidewalls of the trace was negligible. At high frequencies the electrical field of the microstrip line becomes concentrated below the line, and the current flows over the oxidized area as the electric field value from the sidewalls decreases while the frequency increases. The dimensions of the transmission lines were calculated to meet the 50 Ω characteristic impedances required by the measurement system utilizing the microstrip transmission line software from Agilent. Nevertheless, owing to manufacturing constraints associated with the narrow width of the required line, the thickness of the sheet of lead-free material, and the poor adhesion of the polymer to the metals, the dimensions of the line could not meet the 50 Ω requirements, and 40 Ω characteristic impedance microstrip lines, with a width of 450 μm, were fabricated instead.

Two procedures were applied to the treatment of the solder materials to investigate the oxide layers and microstructure influence on signal integrity. Firstly, to simulate the long-term thermal effects induced by hot running components, the Sn and SnAgCu materials were annealed at 200 ^{o}C for up to 30 days to create a thick oxide layer (SnO and SnAgCuO). Investigations on SnO_2 layers have shown that the material is an n-type semiconductor, which, oxidized below 170 $^{\circ}$ C appears to be amorphous. The oxidation rate is logarithmic at 30 $^{\circ}$ C and parabolic from 180 to 450 $^{\circ}$ C for thicknesses up to 700Å [28].

Secondly, the different microstructural features (grain size, colonies size, and intermetallic particles) in the solder interconnections can be influenced by different reflow parameters. Reflow parameters such as cooling rate, time above liquids and dissolution of metallization are the key factors that influence the formation of microstructures during soldering operations. The experiments and analyses conducted at the EPT laboratory showed that the alteration of the reflow profile is an effective way of influencing the degree of the coarseness of the microstructure. Likewise, the degree of coarseness of the microstructure is also changed by cold rolling and annealing. Cold rolling the SnAgCu plastically deforms its microstructure. During the annealing process the solder will recrystallize and the microstructure will become coarser. To create different degrees of coarsening, the samples were annealed at 200°C in atmospheric conditions for different time periods: t1-natural oxide, t2 = 10^3 sec, t3 = 10^4 sec, t4 = 10^5 sec t5 = 10^6 sec and t6 = $2.6*10^6$ sec. The material was placed into oven for annealing starting with the longest time. This was done to avoid the eventual fabrication inconsistencies, and for this reason all the test boards were fabricated at the same time.

The test boards were fabricated using a subtractive process. The detailed scheme of the process was presented in Fig. 3.2. First, the Cu foil on top of the substrate was patterned to create alignment points for the transmission line since it must make a 90^o angle with the measurement device. The fabrication was completed using a subtractive photolithographic process (Fig. 3.2a). To avoid any contamination from the cold rolling of the SnAgCu, a thin layer of material was removed mechanically with emery paper. First a rough cleaning was carried out with a paper of 1200 grit, and then polishing was done with a paper of 4000 grit. The final surface roughness of the material was about 2.5 μm, and the final thickness of the metal sheet was about 100 μm. The Sn sheets were not polished in a way similar to the SnAgCu because the manufacturer cleaned the samples before delivery. Nevertheless, the attempt to polish the Sn caused wrinkles to the samples as they were very soft – and this affected both the length of the line and the characteristic impedance. The pure Sn and SnAgCu strips with natural oxide and highly oxidized SnO and SnAgCuO were attached to the carrier substrate with an epoxy adhesive. Since the adhesive thickness had to be the same for all samples, so that the RF parameters would be the same for all test boards,

two strips of polyimide tape were applied to the edges of the substrate to supply a height reference for the applicator (Fig. 3.2b). The adhesive was spread over the area without tape (Fig. 3.2c). After the adhesive was applied, the metal strip under investigation was attached to the carrier substrate, and the assembly was passed through a laminator heated at 75 ºC, with the laminator being set to the highest pressure to eliminate any air bubbles trapped between the metal strips and the substrates (Fig. 3.2d). Finally, the line dimensions were adjusted to the required target with the use of the high-resolution lithography process available in the laboratory. A 30-μm-thick sacrificial layer of AZ 4500 from Clariant GmbH was spun, exposed, and developed (Fig. 3.2e). The patterned artwork was designed taking into account the under-etch previously determined for each material, which varied from 100 μm for Sn to 300 μm for SnAgCuO. Finally, the metal sheets were patterned and etched to the required width to meet the 40 Ω characteristic impedance (Fig. 3.2.f).

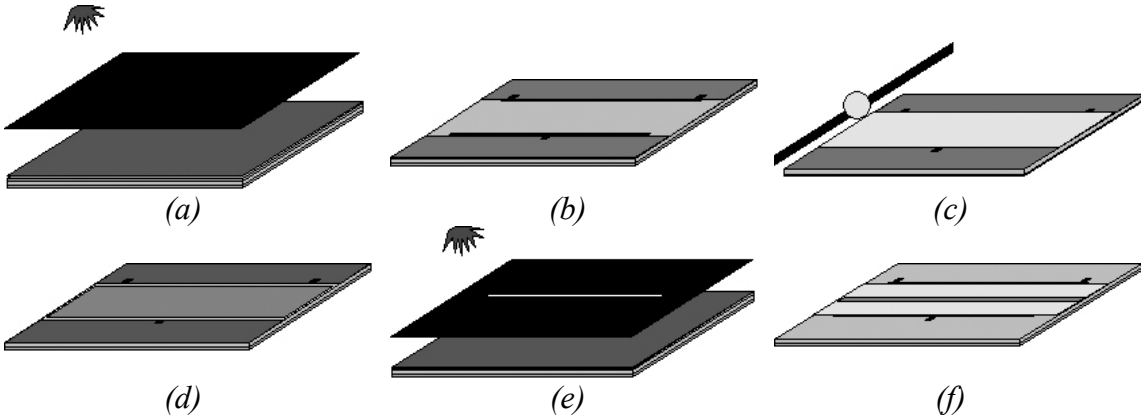


Fig. 3.2 Schematic presentation of the manufacturing process.

The quality of the test boards was evaluated with an optical microscope to ensure that there was no damage and that the dimensions matched with the design specifications. More information about the quality was collected from cross-sectional samples prepared from the measured boards (Fig. 3.3). Some anomalies were found, apparently due to the etching process, which was influenced by the oxide layer formation and the orientation of the Sn grains.

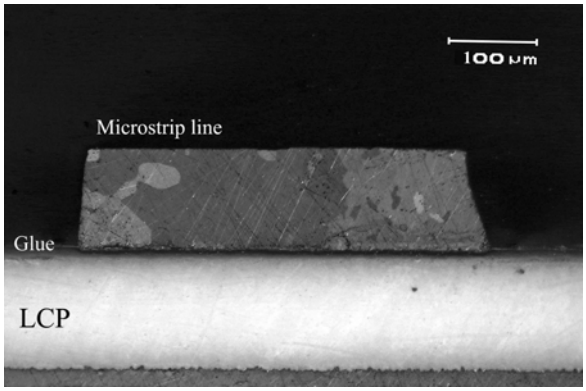


Fig. 3.3 Cross-section of a pure Sn test board.

3.2 Test setup for investigations of underfill influences on SI of WLCSP

The studies of the detuning and losses effects of underfills on WLCSP components and interconnections were carried out utilizing specially designed and fabricated components and test boards. The test assemblies were composed of 2 parts, the carrier substrates and the WLCSP components. The design of the test assemblies was executed by concurrent consideration of the microwave characteristics of the circuits, the experimental measurement set up and the fabrication possibilities. To minimize the high frequency losses and transmission line detuning, the carrier substrates for both the components and test boards were the high resistivity Si. The wave-guide employed in this research was the CPW transmission line as it had low dispersion over a large range of frequencies and was sensitive to changes in the properties of the dielectric material in its close proximity - as most of the electric field propagates through the air and medium present in the gap between the signal and ground planes. Being a single layer structure, it was easy to interconnect the components and measurement device and was less costly to manufacture. To avoid reflections and radiations induced by the changes in the propagation modes at the interconnections, the same transmission line type was utilized for both the carrier substrates and the WLCSP components. The lines were designed to have the characteristic impedance of 50 Ω. The calculated dimensions of the CPW line for a 600 µm thick Si substrate metalized with 0.5 µm thick Al were: line width –220 µm and space –125 µm.

The structures present on the carrier substrates were: the connection pads to the test fixture, the wave guides that connected the launch ports to the components, and the

interconnections area for the WLCSP components. The measurement pads were designed to fit the ground-signal-ground (GSG) type probing required by the Anritsu 3680 test fixture. They were situated at the edge of the boards, had the length and width of 500 μm, and were connected to the signal lines with 400 μm long tapered lines. The wave guides connecting the port and components were 5 mm long. To investigate the influence of the high-density circuitry routed under the components on signal integrity, two carrier substrates were designed (Fig. 3.4). The presence of high-density circuitry was simulated with the help of a metal plane which was placed under the component and connected to the ground layers of the components and test boards (Fig. 3.4a). The spacing between the ground planes and the signal lines and their pads was 125 μm. To simulate the low density circuitry and routing solutions utilizing the metal layers inside the substrates, the metal layer was removed up to the third row of bumps (Fig. 3.4b). All outer bumps were connected to the ground planes. The width of the test board was 8 mm larger than the width of the component to provide a technological area for the placement of underfills.

The components were designed according to WLCSP packaging fabrications rules [151]. The bumps had a diameter of 300 μm, a height of 200 μm and the smallest pitch of 500 μm. A compromise had to be adopted between the electrical parameters of the CPW lines and the underfilling process. The capillarity flow underfills required that the bumps be distributed as evenly as possible under the component. The presence of the metal structure of the bumps in such close proximity to the line, however, affected its electrical parameters because the electromagnetic field coupled to these structures. Nevertheless, the absence of the bumps in the center of the assemblies might allow air to be trapped under the component, resulting in an inaccurate underfilling. As a result, a space of 1.7 mm was assigned as a bump free zone in the middle of the component (Fig. 3.5). This provided a clearance of about 500 μm from the edge of the CPW to the closest row of bumps. Being 4 times larger than the gap between the line and ground plane it was considered adequate to avoid coupling.

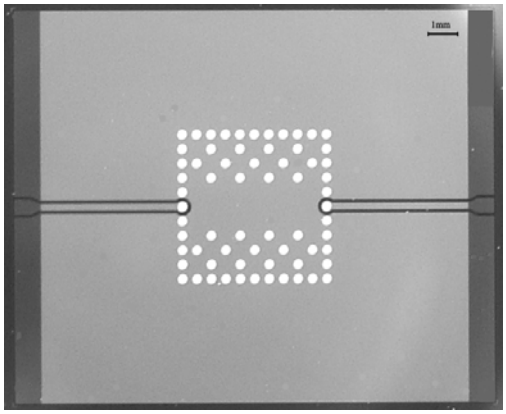


Fig. 3.4.a The test board with metal layer under WLCSP components.

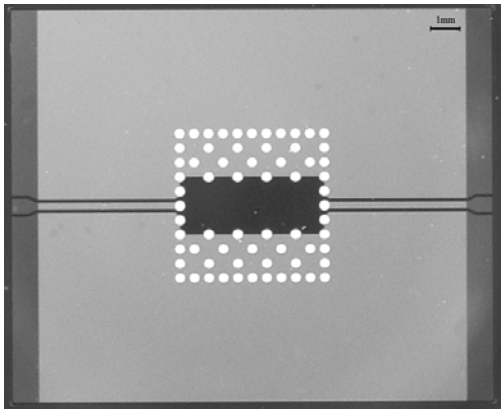


Fig. 3.4.b The test board without metal layer under WLCSP components.

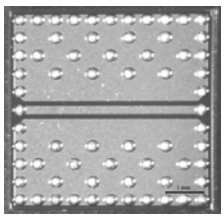


Fig. 3.5 The WLCSP test component.

Table 3.1 - The manufacturing parameters of the underfills.

	1093 A	FP 4532	1093	
Curing temperature	125	150	180	˚C
Curing time	30	5	60	min
Viscosity	11000	16000	93000	mPa.s
Filler	50	62		%
Filler size	9	6		µm
Substrate preheat	55	90		˚C

The underfill materials utilized in this study were two standard capillarity flow underfills and one corner no-flow underfill (Table 3.1). The corner underfill (3509) and one standard underfill (FP 4532) were provided by Henkel – Loctite while the low viscosity standard underfill for flip chip packaging was provided by Sunstar Engineering Inc. The fabrication parameters of the materials were different; the corner underfill was designed to cure during the reflow process, the FP 4532 was a fast curing material, while the 1093 A required a longer time.

The mounting of the WLCSP components on the carrier substrates and underfilling processes were carried out in the Electronics Production Technology laboratory. A carrier wafers jig that supported the Si wafers during the solder paste printing and reflow process was designed and fabricated. After paste printing on the wafers, the components were manually placed utilizing the flip chip-bonder, (FinePlacer, Finetech GmbH). The precision of the assembly was investigated during the bonding process utilizing the X-Ray inspection. After all the components were mounted on the wafers, they were placed on the reflow oven. The reflow profile was set to a high temperature of 250 ˚C for 30 sec to achieve good wetting and melting of the bumps. The final X-ray inspection proved that there were no misalignments. The assemblies were detached from the wafer and cleaned from the sawing residues with the help of ultrasound equipment (Fig. 3.6). The SEM investigation of the cross samples showed that the bumps became firmly attached to both the components and substrates (Fig 3.7).

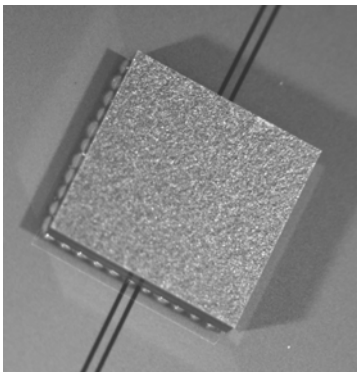


Fig. 3.6 Optical polarized micrograph of the WLCSP assembly.

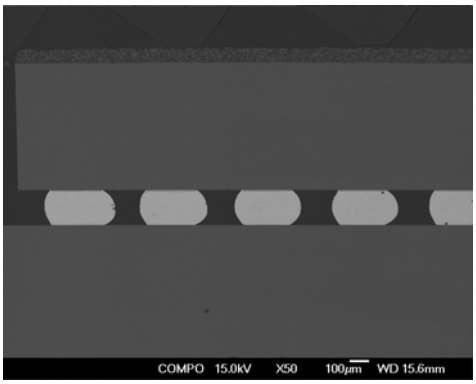


Fig. 3.7 SEM micrograph of the WLCSP assembly.

The deposition of the capillarity flow underfills was carried out with the help of the dispenser unit, Asymtek Axiom SMT, and the parameters of the process such as, needle speed, initial delay, back time and back run distance were first determined for each material (Table 3.2). The needle utilized was a 216P/.020x.25. The first results showed that the materials were flowing faster on the outer sides of the components. Thus, there was a risk that air could be trapped under the component or the material was not distributed uniformly over the entire surface of the assemblies. This could have affected the outcome of the study, as the area of interest was the middle of the assembly. The solution adopted was to deposit the material only on one side of the

component with a larger amount of material at the center rather than at the corners (Fig 3.8.b). Creating a higher pressure on the middle, the materials were forced to flow faster toward the center of the components. Furthermore the dispensing length was adjusted to be with 500 μm shorter than the length of the components to prevent the underfill reaching the outer row of bumps too rapidly. As a result, air was displaced before the underfills sealed the outer sides of components. The optical investigation of the cross samples showed that the underfill was uniformly distributed under the component with no air voids (Fig. 3.8.a, Fig. 3.8.b). A total of 20 samples were processed for each material, 10 test boards with metal under the component and 10 test boards without metal.

Table 3.2 Dispensing program for the underfills.

Underfill	1093 A	4532	3509	
Pre-move delay	350	0,4		sec
Dispense gap	0,8	0,9	0.2	mm
Speed mm/sec	16000	19000		mm/sec
Dwell	0,02	0,02	0,3	
Retract distance	5,08	5,08	5,08	mm
Backtrack gap	0,5	0,5		mm
Backtrack length	0,4	0,5		mm
Backtrack speed	50,8	50,8	50,8	mm/sec
Down speed	50,8	50,8	50,8	mm/sec
Down acceleration	7620	7620	7620	mm/sec^2
Retract speed	50,8	50,8	20,5	mm/sec
Retract acceleration	7620	7620	3500	mm/sec^2
Suck-back	0,1	0,15	0,2	sec

To study the effects of the no flow corner underfill on the signal integrity a compromise was adopted. The test set up did not have a wave guide connected to the corners of the components. Thus, the underfill material was deposited on the edge of the components, around the signal bumps. The deposition of the corner underfill required special attention as it was applied after the components were mounted. In

order to obtain similar results to the process when the material was placed before the component assembly, a special processing technique had to be employed [40, 152]. Being a no flow material, it had to be coerced to diffuse under the component. The needle was lowered to a distance of 200 μm from the substrates and drove at 20 μm to the edge of the component. A large amount of material was allowed to flow during the first sequence. On the second step, part of it was sucked back at the same time as the elevation of the needle (Table 3.2). The cross section investigations showed that the method was good and the material was present under the components and between the bumps (Fig. 3.8.c).

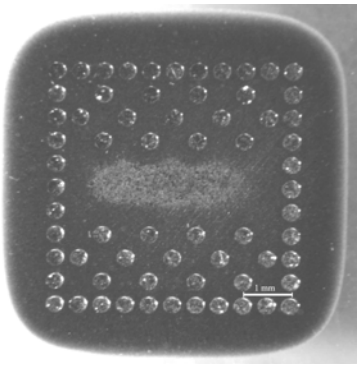


Fig. 3.8.a Cross-section of the WLCSP assembly with FP 4532 underfill.

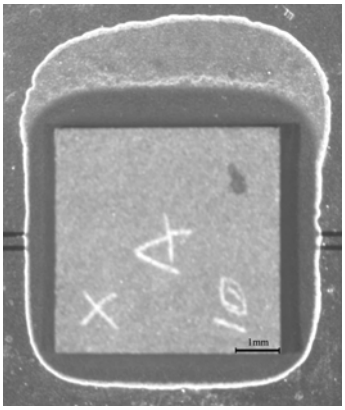


Fig. 3.8.b Top view of the WLCSP assembly with FP 4532 underfill.

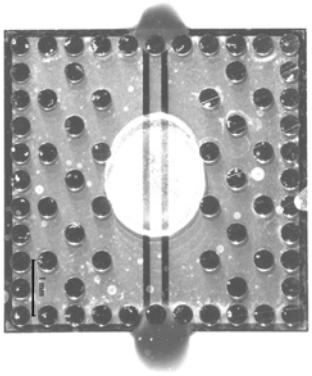
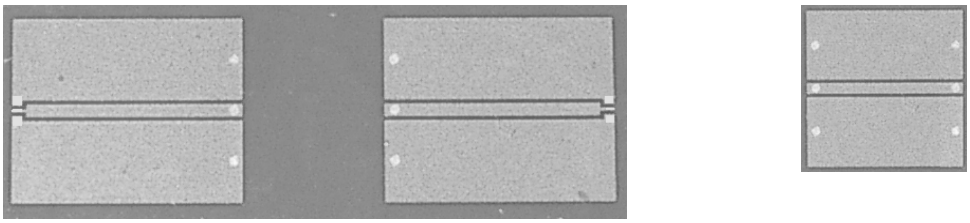


Fig. 3.8.c Cross-section of the WLCSP assembly with 3509 corner underfill.

3.3 Test setup for investigations of assembly process influences on SI

The third system was developed to evaluate the microwave electrical performances of the IMB assemblies and compare them to the ones of the FC. For this evaluation, two types of test boards were designed and manufactured utilizing the IMB and SMT techniques. The prototype boards consisted of two parts: carrier substrates (Fig. 3.9.a) and components (Fig. 3.9.b).



(a) (b)

Fig. 3.9 Top view of the FC carrier substrate (a) and component (b).

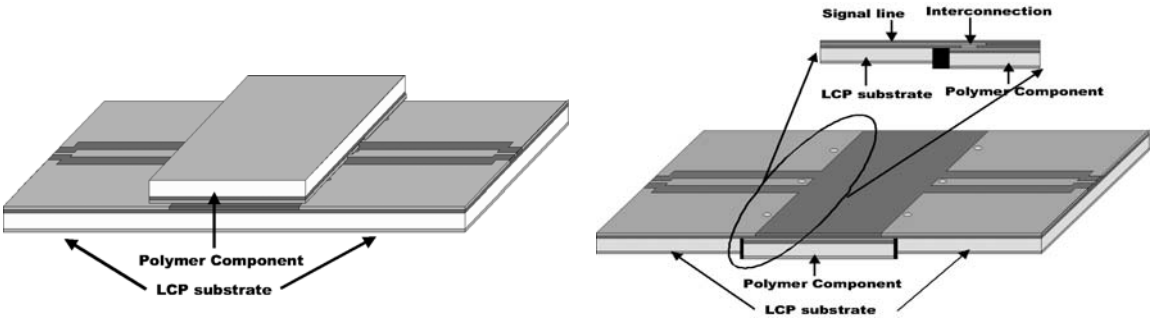
The design of the test board aimed to provide the same electrical properties for both IMB and FC test boards by creating similar power flow paths through the component and the carrier substrate even when connected to the measuring device. Considering the measurement setup, the thickness of the substrates and the geometries of the assemblies, the presence of a continuous ground plane on the bottom of the test board components was required. The measurement set-up utilized on-wafer GSG type probes, thus the signal and ground pads connections were required to be on the same plane. To be able to fit the 125 μm pitch probes the launch port had to be modified. The width of the line and the space to the ground planes were decreased down to 75 μm. For the reasons presented above, the FGCPW was selected as the transmission line for the study. Utilized as a wave guide for both the carrier substrates and the components, undesired wave reflections and radiation losses at the interconnections caused by the changes of the wave propagation modes from different transmission types were avoided. Furthermore, the electrical parameters of the assembled components with IMB and FC and their substrates were the same as the power flow paths and the materials were similar. The detuning of the mounted components was regarded as a result of the assembly technique utilized. With the help of this transmission line, the fabrication process was kept as simple as possible, minimizing the influence of manufacturing errors on the measured results.

The material of the carrier substrate, a 125 μm thick liquid crystal polymer (LCP) from W.L. Gore & Associates Inc., was selected considering the stability of its electric parameters over a broad band of microwave frequencies and its low thickness [109]. This ensured not only that the errors resulting from circuit parameter are stable with frequency and low dielectric losses were minimized but also the multiple-mode wave propagation into the substrate at high frequencies was prevented as the substrate

was thin. The component was a thin film LCP device containing a FGCPW transmission line connected to the substrate with the help of six lead-free interconnections, each 250 μm in diameter - Sn3Ag (wt-%) for the FC and Cu for the IMB. The assembly pitch was 1.1 mm, large enough to prevent parasitic coupling to the interconnections situated in close proximity to the ones under investigation. The components, having a length and width of 5 mm, replaced the silicon chips, preventing frequency dependent errors and high-frequency losses introduced by the silicon substrate. The use of this setup was also encouraged by the successful manufacturing results achieved when 50-μm-thick silicon ICs were embedded into IMB boards in an earlier study and by the possibility of embedding ICs made out of different materials into the substrate [48].

The first step of the fabrication process was the manufacturing of the carrier substrates of the FC assemblies and the components used for both the IMB and FC assemblies, which utilized a semi-additive process. The FGCPW metallization for the carrier substrates and components was fabricated using electroless copper seed metallization of 1 μm (Cuprothick 84 by Schlotter), and finalized by the electro deposition of Cu up to a thickness of 4 μm. Afterwards, a thin layer, 7 μm thick, of photo definable epoxy (Probelec XB 7081 by Vantico) was deposited on top of the substrate to define the interconnection areas.

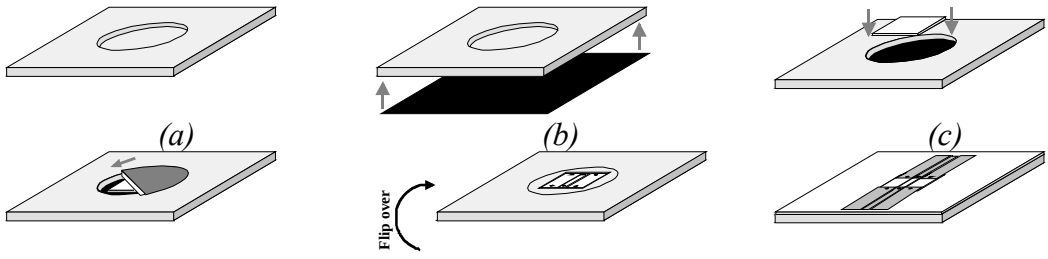
The second step was the finalization of the assemblies. The components for the FC assembly were prepared for the mounting process by bumping each of them with bumps 80 μm in height and 250 μm in diameter using the SnAg electroplating process. The chemical baths utilized for the formation of the bumps were Sn (Shiny Sn Mf) and Ag (Silver GLO 3K) from LeaRonal. Next, the components and the substrates for the FC were wafer-sawed from the carrier substrates. Prior to bonding, a lead-free solder paste was dispensed on the solder interconnection areas of the carrier substrate so as to ensure good interconnection quality. Finally, the FC components were assembled on to the substrate using the surface mount technique (SMT), with the help of a manual high-accuracy FC bonder (FinePlacer, Finetech GmbH) (Fig. 3.9a).



(a) *(b)*

Fig. 3.10 Schematic presentation of the FC (a) and IMB (b) assemblies.

The IMB test boards were assembled using a similar semi-additive process as for the FC and components. The components were embedded into the 1.7-cm-long and 5-cm-wide carrier substrate (Fig. 3.10.b). The main process steps in the IMB fabrication are presented schematically in Fig. 3.11. A hole was drilled through the substrates to create the place to seat the components (Fig. 3.11.a). Then the adhesive tape was attached to the bottom of the substrate (Fig. 3.11.b) and the components were bonded onto it (Fig. 3.11.c). After this, the components were encapsulated using the molding polymer (Nagase-Ciba R-1004) (Fig. 3.11.d), which was cured during the baking process. The adhesive tape was then removed and the module was flipped over (Fig. 3.11.e). Finally, the same semi-additive process that had been used to manufacture the FC carrier substrates and the components was used to fabricate the interconnections of the components to the substrates (Fig. 3.11.f).



(a) *(b)* *(c)*

(d) *(e)* *(f)*

Fig. 3.11 Schematic presentation of the IMB manufacturing process.

The optical and X-ray investigations showed that the assembly process was successful. The FC assembly revealed that there were solder residues scattered around the interconnection. The optical inspection of the embedding process of the components into the substrates utilizing the IMB process showed air trapped in the moulding epoxy. The figures are presented later in the chapter which deals with the results and discussions of this research.

3.4 Calibration and experimental measurements set-up

The calibration process was one of most critical parts of the experimental measurements in the frequency domain. Electrical measurements of the oxide layers, microstructure and underfills investigations were carried using the equipment in the Radio Laboratory. The two-port S-parameters measurement were conducted from 500 MHz up to 50 GHz with the help of HP8510C and HP8363C vector network analyzers (VNA) for 401 frequencies. The VNA connection to the test coupons was realized with the help of the universal text fixture (UTF) 3680 from Anristsu. The measurement system was calibrated using a TRL calibration technique performed with the help of the microstrip calibration kit 36804-10M from Anritsu. The insertion loss measurement was performed for 4 cm of line.

To validate the measurement and the calibration set-up, a reference test board utilizing a Cu transmission line was manufactured at the same time as the SnAgCu samples (Fig. 3.12). The Cu metal was chosen because the material properties were well documented on the manufacturer data sheet.

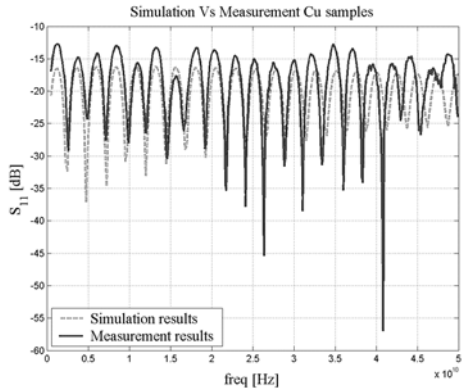


Fig.3.12.a Comparison of simulated and measured S11 of the Cu test board.

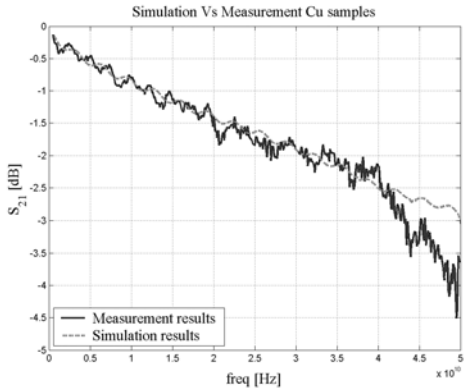


Fig. 3.12.b Comparison of simulated and measured S21 of the Cu test board.

The simulation of the reference board was performed with the help of 2.5D full-wave simulator ADS-Momentum from Agilent. The glue was simulated as a dielectric layer having the dielectric constant of 3 and the loss tangent of 0.03. Simulation and measurement results showed good correlation for frequencies up to 42 GHz. The measured and simulated refection and attenuation coefficients had the same resonance

frequencies and had similar values of amplitude up to 42 GHz (Fig. 3.12). For higher frequencies, however, the amplitudes and phase changed. This was caused by the electrical detuning at microwave frequencies and by the calibration set-up. At 40 GHz a different transmission line was used to calibrate the system, and from this frequency up to 50 GHz, different parameters were used. Thus, the measurement and calibration techniques utilized were validated. Considering the measurement and simulation large band, the results obtained were very good. To validate the calibrations on-site, this assembly was measured before each measurement and the results were compared to the ones from previous measurements and simulations.

4. Electrical modeling and calculations

An essential part of the development of electronics was the modeling process. Two calculation methods were employed in the analysis of performances of systems to determine the best geometries for highest performance: closed form calculation formulas and electromagnetic modeling and simulations. The closed form expressions were developed and standardized to model the performances of RF assemblies and transmission lines. They were simplified calculations based on Maxwell's equations, which provide accurate solutions if the initial conditions were met and the dispersion of the materials' properties with frequency had minor effects. The CAD tools resolved this inconvenience with the price of time and power consumption. The full wave electromagnetic field solvers were utilized to calculate the electrical losses and changes of electrical parameters of the circuits of complex assemblies. In the models, the electrical properties of the materials utilized, were assumed to be uniform, isotropic and homogeneous with no magnetic properties. In this chapter were introduced the closed form expressions utilized to determine the correction coefficient for the effects of oxide layers as well as the models for the studies of influence of underfills and assembly techniques on signal integrity.

4.1 Modeling of the effects of oxide layers on interconnections

To determine the correction coefficient that account for the presence of the oxide layers on the solder connections of hot running components, close form calculation expressions for microstrip lines were utilized. Utilizing the transmission line theory, the insertion losses were calculated and compared to the ones determined from the experimental results. The correction coefficient for the insertion losses introduced by a thick oxide layer present at the conductor surface was determined utilizing the curve-fitting algorithm. The assumptions made were that the dielectric losses were the same for all boards and all transmission lines had the same dimensions.

The calculated values of the resistive and dielectric attenuation coefficients of the test boards with SnAgCu were determined with the help of the closed-form expressions published by Gupta *et al* [150]. Conductor losses accounted for the resistivity of the metal, the skin effect, and the surface roughness (4.1). In the calculations, the characteristic impedance and the dielectric constant were frequency dependent, giving good accuracy over a large frequency range.

$$\alpha_c = 6.1*10^{-5}\left(1+\frac{h}{W}\left[1+\frac{1.25}{\pi}\ln\left(\frac{2h}{t}\right)\right]\right)\frac{R_s Z_0 \varepsilon_{re}(f)}{h}\left[\frac{W_e}{h}+\frac{0.667\frac{W_e}{h}}{\frac{W_e}{h}+1.444}\right]\left(\frac{dB}{unit}\right) \quad (4.1)$$

The formula was valid for the initial condition: $W / h > 1$, where $\varepsilon_{re}(f)$ was the effective dielectric constant frequency dependent, W the width of the line, h the height of the substrate, W_e the effective width of the line, t the thickness of the metal.

The surface resistivity (4.2) (R_s), was calculated taking into account the frequency effects and the calculated resistivity (ρ_c) of the SnAgCu. The calculated value of the resistivity of the alloy was similar to the one made of pure Sn and its concentration was over 95%.

$$R_s = \sqrt{\pi f \mu_0 \rho_c} \quad (4.2)$$

The RMS of the surface roughness height (Δ) was approximated to about 1.6 μm knowing the particle size and the roughness of the paper being 4000 grit. The final value of the attenuation coefficient of conductor loss (α_{cr}) was calculated (4.3) by taking into account also the roughness of the solder material [17]. The skin depth penetration coefficient δ_{sk} value (4.4) was included in the formula as it was the critical factor that contributed to increased losses due to roughness.

$$\alpha_{cr} = \alpha_c\left[1+\frac{2}{\pi}a\tan\left(1.4\left(\frac{\Delta}{\delta_s}\right)^2\right)\right](dB) \quad (4.3)$$

$$\delta_s = \sqrt{\frac{\rho_c}{\pi f \mu_0}} \quad (4.4)$$

The attenuation coefficient of the dielectric loss was calculated using (4.5). Where η was the wave impedance of the substrate calculated as frequencies depend and σ_d the

substrate conductivity (4.6). The loss tangent of the material utilized in the calculations was the one determined from experimental measurements [109, 113].

$$\alpha_d = 4.34\eta\sigma_d \frac{\varepsilon_{re}(f)-1}{(\varepsilon_r-1)\sqrt{\varepsilon_{re}(f)}}\left(\frac{dB}{unit}\right) \tag{4.5}$$

$$\sigma_d = 2\pi f\varepsilon_0\varepsilon_r \tan\delta \tag{4.6}$$

In the calculation, the radiation losses were not considered. Preliminary investigations showed that the small thickness of the substrate prevented the excitation of higher order modes and any coupling between the quasi-TEM modes specific to the microstrip line and the surface wave spurious modes (4.7). The plainness of structures and the fact that 2 port measurements were utilized did not trigger significant radiation losses.

$$f_c \cong \frac{300}{\sqrt{\varepsilon_r}(2W+0.8t)} \tag{4.7}$$

The literature survey indicated that the oxide of Sn performs as an n-type semiconductor. Therefore, further research on the detuning effects due to the change of the dielectric constant was investigated. The method utilized investigated the impedance variations of a two-port T-network with the frequency, knowing that the capacitive loading due to extra capacitance changes the impedance of the lines. The scattering parameters matrixes of the SnAgCu and SnAgCuO test samples were transformed into impedance matrixes (Z). Then the Z-parameters were transformed to a T-network for calculation of the input (Z_{11}) and transfer impedances (Z_{12}) (4.8) (Fig. 4.1) [17]. The transfer impedance provided a quantitative measure of the impact of oxide on the capacitive loading of the interconnections.

$$Z_{11}=Z_c((1+S_{11})(1-S_{22})+S_{12}S_{21})/((1-S_{11})(1-S_{22})-S_{12}S_{21});$$
$$Z_{12}=2Z_cS_{12}/((1-S_{11})(1-S_{22})-S_{12}S_{21}); \tag{4.8}$$
$$Z_{21}=2Z_cS_{21}/((1-S_{11})(1-S_{22})-S_{12}S_{21});$$
$$Z_{22}=Z_c((1-S_{11})(1+S_{22})+S_{12}S_{21})/((1-S_{11})(1-S_{22})-S_{12}S_{21});$$

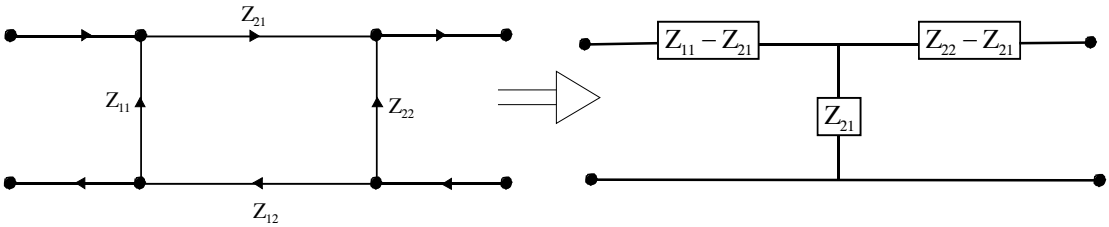


Fig. 4.1 Z parameter matrix transformation to a T-network.

The next step of our investigations was to determine the influence of the oxide layers on the signal integrity of the interconnections of the WLCSP assemblies. Utilizing the determined design rule, the changes in the values of conductor loss were calculated when the oxide layer was present for single ended and differential signal communications. The interconnections were considered as short transmission lines and their type was evaluated considering the distribution of the electromagnetic field. The evaluation of losses was performed considering that the bump surface was smooth. It was difficult to simulate one IC interconnection as the distribution of the electromagnetic field depended on the return path of the signal and the voltage levels of the neighboring connections. Due to this difficulty, more simplified assumptions were made.

The calculations for single ended signaling were performed taking into consideration that the bumps in close proximity to the interconnection under investigation were at a lower voltage level. The investigation was simplified by considering the neighboring bumps to be connected to the ground. Electromagnetic simulation of the WLCSP assembly showed that the electric field distribution resembled the one in a coaxial cable where the inner radius was the bump radius and the outer radius was equal to the pitch of the bumps (Fig. 4.2). The characteristic impedance and the conductor losses were calculated taking the diameter of the inner line to be equal to the diameter of the bump. The value of the gap between the bumps was assigned as the distance between the inner line and the outer shield (4.9). The conductor losses were calculated utilizing the conductivity of the SnAgCu to determine the surface resistivity of the line (4.10).

$$Z_{0-coax} = \frac{\eta}{2\pi}\ln\left(\frac{b}{a}\right)(\Omega) \tag{4.9}$$

$$\alpha_{c-coax} = \frac{R_s}{4\pi Z_{0-coax}}\left(\frac{1}{b}+\frac{1}{a}\right)\left(Np/m\right) \tag{4.10}$$

The electromagnetic simulations of the differential signaling showed that the electric field distribution resembled the one of the twin-wire transmission line. For the conductor loss calculation, the diameter of the wires was assigned as being equal to the diameter of the bumps. The distance between the wires was equal to the gap between the bumps (4.11). The resistivity of the SnAgCu material was considered for attenuations calculations (4.12) (Fig. 4.3).

$$Z_{0-tw} = \frac{\eta_0}{\pi\sqrt{\varepsilon_r}} \cosh^{-1}\left(\frac{D}{d}\right)(\Omega) \tag{4.11}$$

$$\alpha_{c-tw} = \frac{P}{2d} \frac{\sqrt{f\varepsilon/\sigma}}{\cosh^{-1}\left(D/d\right)}(Np/cm) \tag{4.12}$$

Where: $P = \dfrac{D/d}{\sqrt{(D/d)^2 - 1}}$ (4.13)

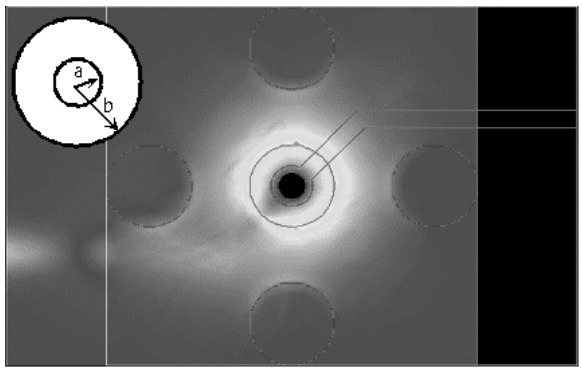


Fig. 4.2 Electric field distribution in an interconnection in the center of the package.

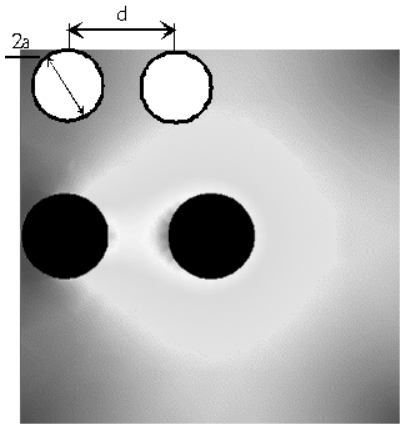


Fig. 4.3 Electric field distribution in an interconnection for differential signaling.

4.2 Modeling of the effects of underfills on the SI of assemblies

Electrical models of the test boards were built and simulated to get a better understanding on the effects of underfills on the detuning of the circuitry and on the packaging interconnections of WLCSP assemblies. Momentum 12 models were developed which utilized the 2.5D full wave simulator from the Agilent Advanced Design System. The simulations of the test boards without underfills were developed first. The electrical size of the board and the number of the interconnections were

considerably large for the frequency under study. Fine meshing was required for accurate calculations that overwhelmed the computing power. Results were achieved only for coarse mesh and only up to 3 GHz. At frequencies higher than 4 GHz, surface waves were generated and a denser mesh was required.

To analyze the effects of underfills in more detail, a smaller model, similar to the assembled WLCSP, had to be employed. The lengths of the feed lines on the carrier substrate were reduced to 500 μm. There were two advantages of utilizing short feed lines. Firstly, smaller calculation power was required; and secondly, the detuning effects on the feed lines generated by the 2.5D simulator for the models with underfills were eliminated. The visual inspection of the fabricated test boards showed that the underfills extended around the components for up to 1 mm. The simulated components resembled the middle part of the WLCSP assemblies. They were 2 mm long and 1.5 wide, having 12 interconnections (Fig. 4.4). The size of the bumps was 300 μm and the height was 200 μm. The components had two pitches, 500 μm at the input and output of the components and 1 mm along the signal propagation direction as the components were limited at the third row of the bumps aside the signal lines. These rows were included in the models because it was noticed, from the test board simulation, that part of the return current utilized them to close the electrical circuits. The bumps situated near the edges did not show an important current flow and were therefore not considered in the model.

The material of the carrier substrate of the components and test boards was the 600 μm thick Si having the dielectric constant of 10 and the loss tangent of 0.0002 [153]. The values of the dielectric constant and the loss tangent of the underfills were selected from the published literature considering the filler content [33, 112, 154, 155]. The electrical properties of the underfills utilized in the simulations were for the dielectric constant – 3.5 and for the loss tangent –0.002. The meshing was generated for the maximum frequency under study (20 GHz) having 30 cells per wavelength, the arc resolution was 15 degrees and the edge mesh of the conductors was 15 μm. The simulations were carried out up to 20 GHz where the upper limit of the calculation power was reached.

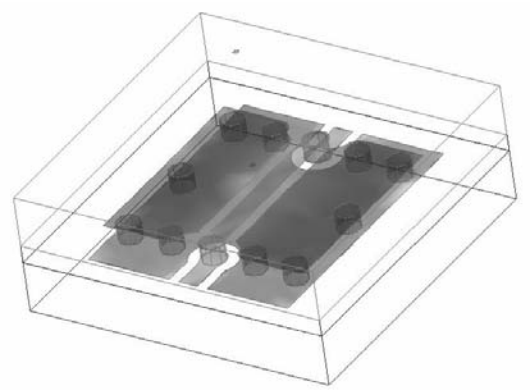


Fig. 4.4.a Schematic presentation of the CPW - WLCSP components with a metal layer model.

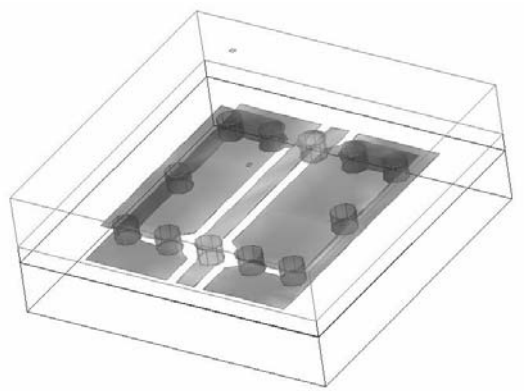


Fig. 4.4.b Schematic presentation of the CPW - WLCSP components without a metal layer model.

Eight models were developed to take into account the three variables of high-density circuitry, the transmission line type and the presence of underfill materials. The presence of the high pitch routing was simulated with the help of a metal plane present under the component which was connected to the ground interconnections of the component and of the substrate (Fig. 4.4.a). The lower density circuitry was simulated, by removing the metal plane up to the third row of bumps that were connected to the ground of the system (Fig. 4.4.b). The underfill presence was simulated for both situations. A detailed presentation of the CPW set-up was presented in Chapter 3 – the Experimental part of this research.

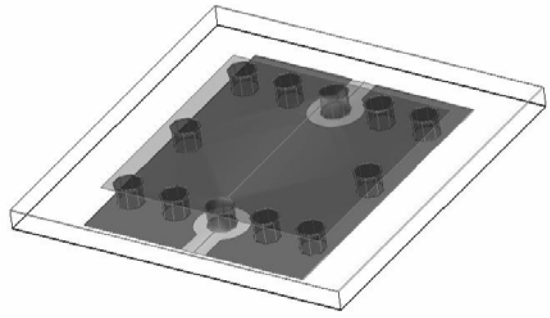


Fig. 4.5.a Schematic presentation of the Microstrip - WLCSP components with a metal layer model.

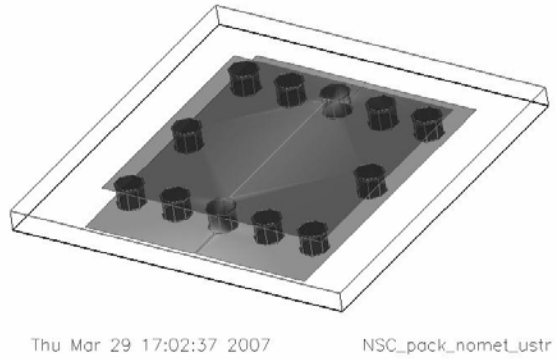


Fig. 4.5.b Schematic presentation of the Microstrip - WLCSP components without a metal layer model.

With the help of these models it was possible to study also the effects of the underfills when the transmission lines were of the microstrip line type. The models of the assemblies with the microstrip line were similar to those of the CPW lines except for the transmission line (Fig. 4.5). The distribution of the bumps and the dimensions of

the assemblies were the same. The differences were to be found in the ground distribution. Vias in pads were utilized to connect the ground layers of the components and carrier substrates to the bumps. The separation dielectric between the signal line and the ground plane was 8 μm thick Si_3N_4. The properties of the material showed a dielectric constant of -7 and a loss tangent of -0.002 [156, 157]. The calculated width of the microstrip line was 10 μm for a characteristic impedance of 50 Ω for this configuration.

The studies of high frequency effects of underfills on the WLCSP interconnections were carried out with the help of the CPW (Fig. 4.6) and microstrip (Fig. 4.7) transmission lines for frequencies up to 40 GHz. The models were created from those of the test boards where only the area around the signal interconnections was evaluated. The signal bump and the two adjacent bumps utilised by the return currents were taken into consideration in the models. The longitudinal dimension of the models was 1 mm and the width was 1.5 mm. These values were determined from the references to the technological requirements for the ICs mounting and the boundary conditions of the models. The length of the transmission lines on the substrates and components transmission was 500 μm.

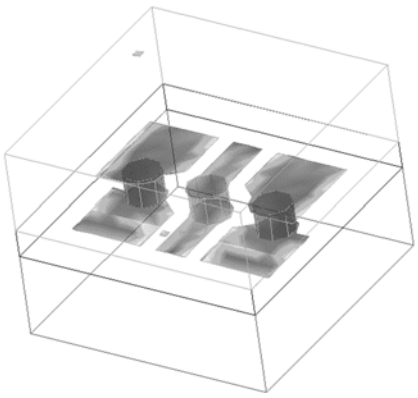


Fig. 4.6 Schematic presentation of the CPW - WLCSP interconnection model.

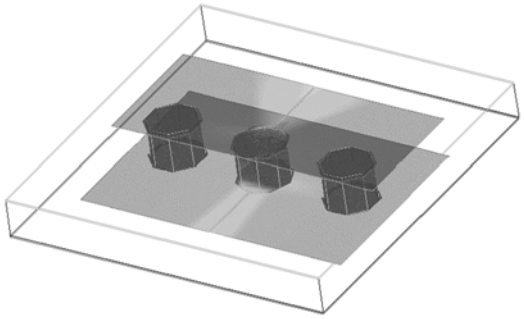
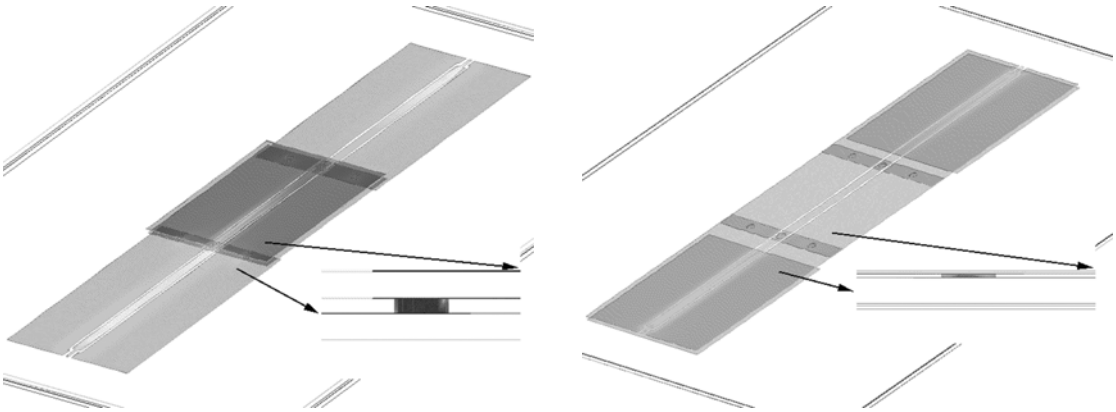


Fig.4.7 Schematic presentation of the Microstrip - WLCSP interconnection model.

4.3 Modeling of the IMB and FC assemblies

The investigations of the influences of assembly techniques on signal integrity were carried with the help of the SMT and IMB test boards. The models of the test boards were developed and simulated with the help of the Agilent – Momentum software.

The simulations of the IMB and FC test modules were carried out from 5 to 26 GHz. Due to the limitation of the 2.5D simulator, simplified models were employed concerning the materials distribution. As a result, the electrical parameters of small volumes of materials had to be reassigned for both the IMB and FC models. For the copper traces, the effective conductivity used was $\sigma=1.5*10^7$ S/m [158] as a 1μm thick electroless Cu was deposited as a seed layer. This value was utilized because the software program could not cope with multilayer metal deposition. Nevertheless, at high frequency, the skin effect together with the proximity effect forced most of the current to flow through the outer surface of the conductor where the high resistivity Cu was deposited, thus the metal losses were mainly induced by this layer.



(a) (b)

Fig. 4.8 Model presentation of the test boards for the FC (a) and IMB (b) assemblies.

The ADS program was utilized to calculate the electrical parameters of the boards, including the two fundamental propagation modes of electromagnetic waves present on the FGCPW, the CPW, the microstrip and the parallel plate. The parallel plate wave propagation consideration was a necessary measure as the ground planes of the CPW were designed to perform as having an infinite width [80, 159]. The calculations were performed using the linear interpolation with a frequency step of 0.1 GHz. The mesh was defined for the highest simulation frequency, with 30 cells per wavelength and edge meshing for the FGCPW structures and manually refined mesh at the interconnection area.

In the case of the IMB model, the dielectric losses were accurately calculated as the LCP accounted for about 90% of the volume of the media and its electrical parameters had less than a 5% variation [113]. The photo definable epoxy and the moulding epoxy accounted for the remaining 10% of the substrate material by volume, but the

data for their electrical properties provided by the manufacturer was available for only up to a 1 GHz frequency. The dielectric properties of the materials utilized in the simulations are presented below in Table 4.1.

Table 4.1 Dielectric parameters of the materials used in the simulations.

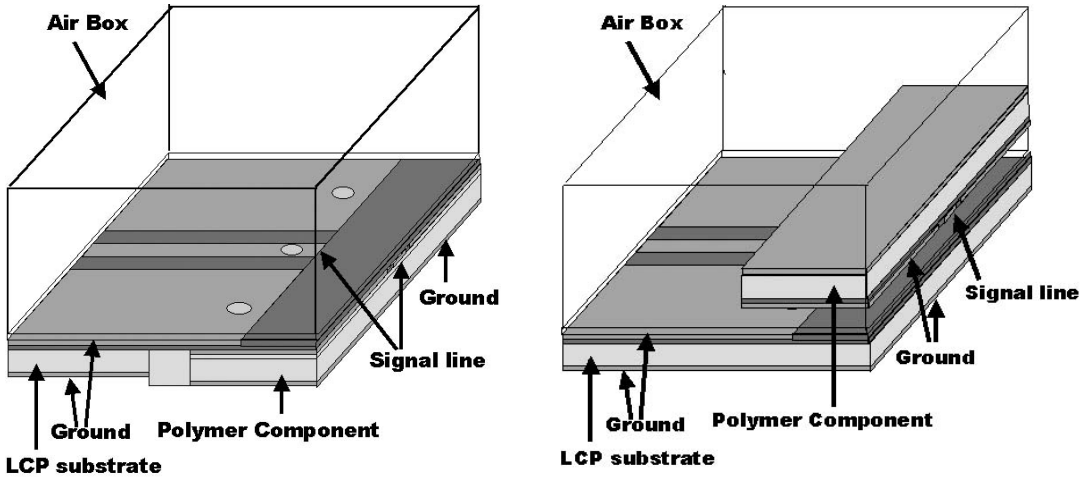
	Dielectric constant (ε_r)	Loss tangent (tan δ)
Liquid Crystal Polymer (LCP) at 18 GHz	3.0	0.003
Probelec – Vantico at 1 GHz	3.5	0.03

In order to achieve the smallest margin of error, the redistribution of the materials concerned only the molding epoxy and a 10-μm-thick layer of photo-definable epoxy present on the top of the component that was simulated as an LCP substrate. As a result, small differences may occur at very high frequencies between the calculated and measured results of the insertion and reflection losses. The impact of this simplification on the final results was calculated utilizing transmission line theory to be lower than 5%; as less than 3% of the total volume of the materials utilized for IMB assemblies was reassigned and the difference between the dielectric constants was only 0.5.

The ADS Momentum did not, however, take into account the roughness of the substrate. To demonstrate the effect of roughness on insertion losses, a new simplified model of the IMB module was built with the help of ADS - Schematics. Five FGCPW lines, having the width and space similar as the ones of the test boards, were connected in a series. The multiple line connection was done to replicate the reflections introduced by the discontinuities from the ports. Two situations were considered; firstly, where the substrate was perfectly smooth and the roughness assigned to be zero; and secondly, where the roughness was assigned to be 1.5 μm as it was for the test boards. The thickness and resistivity of the metal layer was considered similar to the ones utilized in the ADS-Mom IMB model. The substrate was of LCP material as the program did not allow multilayer substrate definitions for this transmission line.

Further studies focused on the investigation of the influences of the measurement pads on the results of the test boards. A new IMB model (IMB-pde) was built where the measurement ports were replaced with a 50 Ω-FGCPW line, identical to the one utilized as the transmission line. In this way the characteristic impedance mismatch between the ports and the transmission lines was eliminated.

The model of the FC test boards was built to satisfy the simulator requirements and adjustments were performed for the material distribution on the upper part of the test board model. In fact, the air presence accounted for only 75 μm (the same as the bump height) as no underfill was used for the assembly. The detuning error resulting from the presence of the dielectric material above the structure was investigated. For this, a model of the FGCPW was build having free space as the upper boundary. The comparison of the results of the FGCPW having air above and the one used in the FC model showed that the errors were less than 3% at 26 GHz. The shape of the bumps was modeled as being cylindrical. Thus, the parasitic capacitance of the interconnection was slightly reduced. The errors introduced by this simplification were low compared to the board size.



(a) *(b)*

Fig. 4.9 3D model (a) of the IMB and (b) of the FC interconnections.

The microwave performance of the interconnections of IMB and FC for FGCPW lines were simulated with the help of two new models. They were created from those test boards where only the area around the interconnections was evaluated (Fig. 4.9). The longitudinal dimension of the model was 2 mm. This value was determined with reference to the technological requirements for the ICs mounting and the boundary

conditions of the models. The feed lines were 1.5 mm long on the carrier substrate site and 1 mm long on the assembled component. Further investigations on the electrical performances of the IMB interconnection realized with FGCPW lines were carried out for four more values of the pitch between the bumps: 55 μm, 45 μm, 35 μm, 25 μm and 20 μm. Moreover, to study the effects of the gap in the bottom ground plane near the components, due to drilling, a free space boundary condition was assigned for the lower part model instead of the perfect conductive plane. This simulated the situation when the modules were mounted as daughter boards. Four more models were built to study the effects of pitch size on this assembly and the results compared with the ones of the close boundary models.

4.4 Modeling of the IMB interconnections

In order to learn more about the effects of the IMB assembly technique on signal integrity, diverse geometries of interconnections, routing, distributions of signal and power layers, as well as discontinuities in the current return path and stack-up possibilities were all modeled, simulated and studied. The calculations were performed with the help of the ADS-Momentum for frequencies up to 50 GHz.

The studies were carried out utilizing two types of transmission lines: microstrip line and stripline as they were widely utilized in assemblies and PWB design. The effects of geometries of interconnections and discontinuities in the signal paths were investigated by changing the diameters of vias, the dimensions and shapes of the pads, the return path of the current, the thickness of the dielectric layers and the power distribution planes. The diameters of the vias utilized in this study were 20 μm, 25 μm, 50 μm and 100 μm. Two shapes were employed for the pads: round and square. Their sizes were calculated according to the laser drilling requirements of PWB manufacturers. The rule states that the radius of the pads had to be with at least 60 μm larger than the radius of the vias for a good yield [5]. Nevertheless, smaller sizes of the pads were also considered in this study as SIA roadmaps estimate that the diameter of the pads will soon be only 40 μm larger than the ones of the vias [5]. The dimensions of the square type pads utilized were the smallest dimensions available of Si chips for WLCSP packaging, 100 μm and a pitch of 160 μm. The thickness of the

carrier substrate was 25 μm for all models (layer 1) (Fig. 4.10). The thickness of the build up dielectric layer deposited on the top (layer 2) of the components separating the signal layers was 25 μm, 50 μm and 100 μm. The width of the space between the PWB and the component was augmented from 100 μm to 500 μm up to 1mm.

The electrical properties of the carrier substrates for both test boards and components were the ones of the LCP material having the dielectric constant of -3 and the loss tangent of -0.002. When connections to Si components were simulated, the substrate between the microstrip line and ground layer was Si_3N_4 having the thickness of 10 μm. The properties of the material were a dielectric constant of –7 and a loss tangent of -0.002 [153]. The metal conductors were considered to be fabricated out of Cu, having the resistivity of $1.7*10^{-8}$ Ωm and the thickness of 5 μm for the lines and 3 μm for the vias.

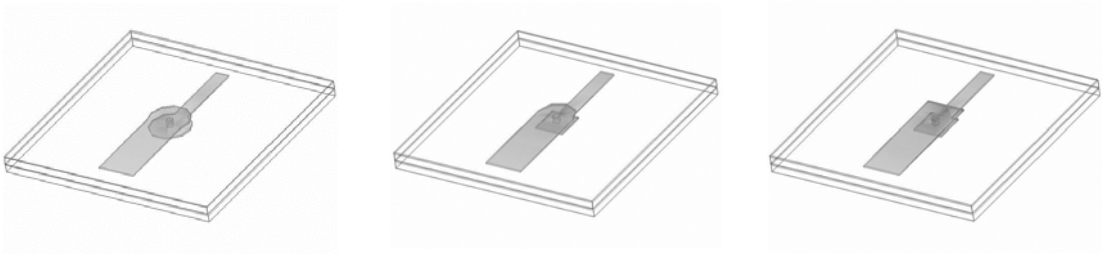
Accurate comparisons of the performance of different interconnections were achieved by keeping the length of the feed lines the same for all models, at a consistent length of 250 μm. The length was measured from the ports (edge) to the first discontinuity (pad or gap in the plane) for the PWBs and from the connection pads to the ports for the components. The distance from the outer edge of the pads to the edge of the carrier substrate (PWB or component) was 75 μm. The physical dimensions of the models varied in the width of the gaps present between the components and the boards, as well as the dimensions of the vias and their pads. For a facile identification of the interconnections, the following notation was utilized for the purpose of describing the connections: v50_t25_s100 referred to the structure as having the diameter of the via at 50 μm (v50), the thickness of the substrate at 25 μm (t25) and the width of the gap between the PWB and the component at 100 μm.

4.4.1. Microstrip line connection

4.10 Schematic of the microstrip interconnection.

In the first simulations the influences of the size of the vias, the shape of the pads and the thickness of the substrate - where microstrip lines were utilized as wave guides for

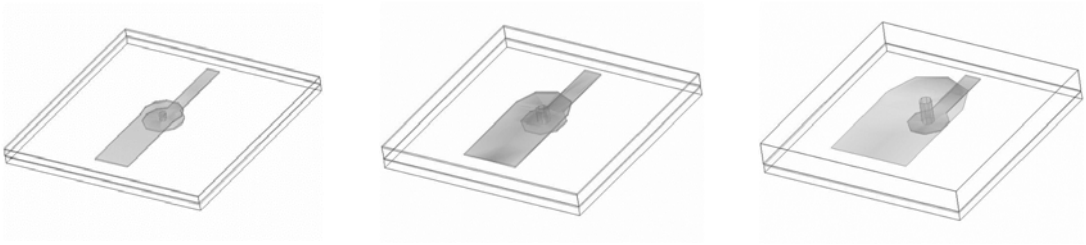
routing of both the PWBs and the components - were analyzed. These assemblies resembled the integration of RF modules with a small number of I/Os and a low pitch PWB. For the purpose of simplifying the analysis and achieving an accurate comparison between models, the current return path was considered to be ideal. The components considered were realized out of LCP and shared the same ground plane with the PWBs. This stack-up could be realized by metallizing the bottom of the carrier substrate with a Cu layer after the module had been assembled (Fig. 4.10).



a. Round – round. *b. Round – square.* *c. Square – square.*

Fig. 4.11 Microstrip models with different shapes of pads.

The variables considered in this study were as follows: the diameter of the vias –20 μm, 25 μm, 50 μm and 100 μm, the thickness of the substrate –25 μm, 50 μm and 100 μm, as well as the round and square pads. Three combinations of the shape of the pads of the PWB and the component were analyzed with the height of the vias being 25 μm: round PWB with round component (Fig 4.11.a); round PWB with square component (Fig 4.11.b); and square PWB with square component (Fig 4.11.c).



a. 25 μm *b. 50 μm* *c. 100 μm*

Fig. 4.12 Microstrip models with different substrate thicknesses.

The characteristic impedance of the feed lines was calculated to be 50 Ω. Thus, the width of the microstrip built on the PWB increased with the thickness of the substrates (Table 4.2) (Fig. 4.12). As a result, for thicker substrates the PWB lines did not require connection pads as their widths were larger than the diameter of the pads (Fig 4.12.b, Fig 4.12.c). The width of the feed line of the component did not require

changes, as its Z_0 was not affected by the increase of the thickness of the substrates over 25 μm.

Table 4.2 Values of the line widths function of substrate thicknesses.

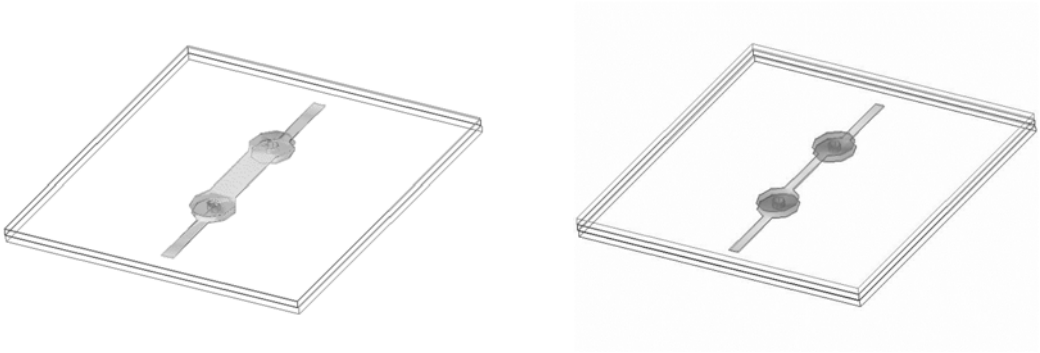
t (μm)	25	50	100
Width_PWB (μm)	130	200	340
Width_Comp. (μm)	50	50	50

4.4.2. Microstrip bridge connection

The cost of modules could be increased when the components were exposed to less fabrication steps. The circuitry on the PWBs was manufactured prior to the integration of the ICs into the substrate. After embedding the ICs, the signal layers of the PWB and the ICs were at about the same level. The connections of the components to the PWB were realized with bridge-like structures over the space required for the component assembly. For this an additional build up layer was employed (Fig. 4.13). The elements needed to realize these connections were two vias and one bridge line. The variables considered were: the width of the required mounting space (100 μm, 500 μmm and 1mm), the thickness of the dielectric substrate between the bridging line and the carrier substrate (25 μm, 50 μm and 100 μm), the line width of the interconnection line and the diameters of the vias (50 μm and 100 μm). The return path was considered ideal and the PWBs and ICs both shared the same ground layer.

Fig. 4.13 Schematic presentation of the bridge connections.

Two situations were analyzed concerning the width of the line of the bridge connection. First, the line was designed to maintain constant impedance, 50 Ω, of the interconnection (MI) over the gap (Fig. 4.14.a). Thus, the width of the bridge line was increased with the thickness of the substrates; the values were similar with the ones calculated in the previous study (Table 4.2). Second, the width of the bridge was 75 μm for all thickness of substrates to create high density interconnections (HDI) (Fig. 4.14.b). The following notations were utilized: v50_t25_g100_t when the bridging line had the width of 75 μm and v50_t25_g100 for the structure built with a matched impedance line.



a. Matched impedance (t-25 μm) *b. High density connection.*

Fig. 4.14 Models of the bridge connections.

4.4.3. Microstrip ground distribution and high dielectric constant materials

Fig. 4.15 Schematic presentation of the model for high dielectric materials analysis

To improve the performances of systems, high dielectric constant materials were integrated into the carrier substrates. In the microstrip configuration the high dielectric layer was assigned to be at to the bottom of the modules. Utilizing this stack-up it was possible to study the influence of the split in the ground plane of the PWB and the components. The GND layers of the PWBs and the components were separated due to the assembly process (Fig. 4.15). This study focused on two issues: firstly, the influence of the current return path; and secondly, the effects of high dielectric constant materials integrated into the substrate on the signal integrity of one net.

To investigate the influence of the return path on signal integrity, one initial condition was set to close the electrical circuits. The new metal layer on the bottom was assigned as the reference ground of the model and connection vias were designed to connect this layer to the GND layer of the component and the PWB. This solution might be adopted when bridge GND connections were avoided and the component had an available GND plane. The two variables considered were the assignment of the reference ports and the distribution of the vias that interconnected the ground planes.

The gap in the plane was 100 μm for all models and the diameter of the vias 50 μm. The stack-up was composed of 3 layers: two 25 μm thick layers of LCP and one 3 μm thick layer of high dielectric material.

The first model (gd_v50_t25_01) was the reference one. The PWB and the component shared the same ground layer without discontinuities. In the second model (gd_v50_t25_02), fifteen vias were utilized to connect the ground planes of the component and the PWB to the reference plane of the module. They were equally distributed under the signal line with a pitch of 100 μm. A simplification of this model was adopted in the third model (gd_v50_t25_03). Five vias were distributed under the signal line; two of them were placed close to the edge of PWB and component, one for the component and one for the PWB. Further simplifications were applied to the fourth model (gd_v50_t25_04) when only three connections were utilized (Fig. 4.16). Two were places close to the launch ports and one under the interconnection. The last model utilized two vias, situated at a distance of 500 μm from the ports and the lines (gd_v50_t25_05) (Fig. 4.17). The dimensions of the ground plane of the PWB were 250 x 500 μm and of the components were 420 x 500 μm.

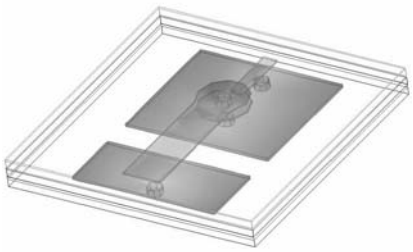


Fig. 4.16 gd_v25_t25_04.
Models of the return path connections.

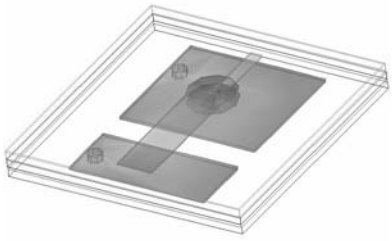


Fig. 4.17 gd_v25_t25_05.

After determining the optimal placements of return vias, advanced studies were employed to minimize the number of vias while improve the quality of signals. For this the EMI control theory was adopted and two issues were solved with only one design: a good current return path and EMI suppression of parasitic waves to and from the component. This was realized utilizing a row of vias placed on each side of the gap (Fig. 4.18). The pitch was calculated to be equal to λ/20 of the highest frequency [13, 49]. The size of the model was increased on the *y*-axis to 700 μm to accommodate a larger number of vias as smaller pitches were also studied. The model

(gd_p150) had twenty interconnections having a gap of 150 μm (150p). The number of interconnections was reduced to thirteen on the model gd_p150_p225. The vias were distributed as follows: ten at the edge of the PWB and component (five and five) and the rest under the component with a pitch of 225 μm, centered to the signal line. The number of connections was decreased further to ten (gd_p150_500_2) as the pitch vias under the component was increased to 500 μm. In this model no via was present in the vicinity of the port. Utilizing this pitch allowed two more models to be created. First with eleven connections, ten at the edges and one under the signal line on the component close to the port (gd_p150_p500_1). The second (gd_p150_p500) where the two ground connections were located at a distance of 250 μm from the signal line of the component near the edge of the model. Further cost reduction was studied when the pitch between the edge vias was increased to 225 μm. Two models were employer gd_p225 and gd_p225_1. The first had nine vias, six at the edges and three evenly distributed under the component. The second had six vias, two at the edges of the gap and four under the component.

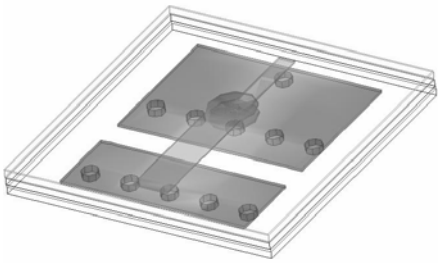


Fig. 4.18 gd_p150_p500_1.
Models of the return path connections.

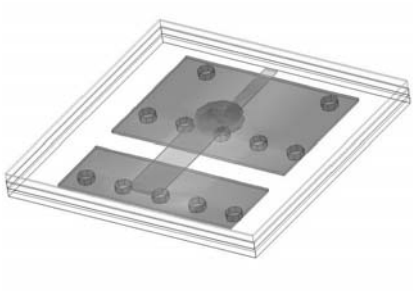


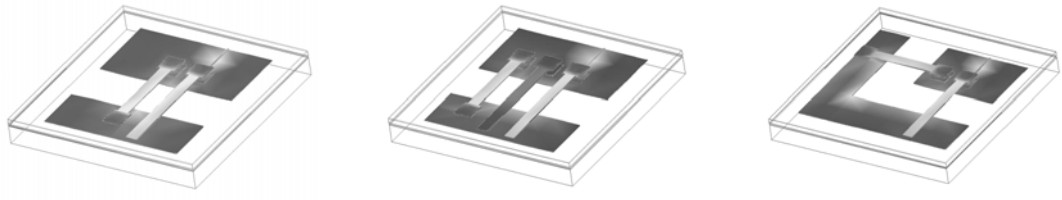
Fig. 4.19 gd_p150_p500.

The second part of the analysis focused upon the influence of high dielectric layers integrated into the substrates on signal integrity. The values of the dielectric constant of the separation layer between the ground planes were 3, 10 and 100. The gap between the PWBs and the components were 100 μm, 500 μm and 1mm. The models employed were the ones optimized from the analysis of the current return path (gd_p150_p500 and gd_p150p_p500_1). The dimensions of the ground planes were reduced with 500 μm to increase the resonance of the structure above 50 GHz. This was adopted as the size of modules were increased as 1mm gaps were modeled and were capacitive loaded by the presence of high dielectric materials.

4.4.4. Microstrip connection to the Si chip

Fig. 4.20 Schematic presentation of the microstrip connection of the Si components.

The connection of the Si components to the PWB required the analysis of two connections, the signal and its return path. The GND connection between the PWBs and ICs was realized with the help of a second bridge type connection similar to the signal one (Fig 4.20). The variables considered were the distribution of the return current path, the pitch of connections and the size of the gaps in the return paths. Three possible ground connections were studied. First, the signal and its current return path were considered adjacent, and three values of the pitch between the pads were analyzed 160 μm (p160), 250 μm (p250) and 500 μm (p500) (Fig. 4.21.a). Second, for the 160 μm pitch, two signals were considered to share the same return path (Fig. 4.21.b). The third scenario was when the signal and GND were situated on the corner of the component and were connected on different sides (Fig. 4.21.c). The width of the PWB feed lines and of the bridge connections was 60 μm and of the microstrip line from the component was 10 μm. The pads were square and had a size of 100 x 100 μm. The gaps between the PWB and the component were assigned to be 100 μm, 500 μm and 1 mm for the situation when the signal and its return current were adjacent.



(a). *(b).* *(c).*

Fig. 4.21 Models of the signal and ground connections of the Si components.

4.4.5. Stripline interconnections

The stripline interconnections resulted from the increased functionality of components where a large amount of I/Os had to be connected to the PWBs and PDN noise levels had to be low. To satisfy these requirements, multilayer boards were employed with a

complex distribution of the power and signal layers. To achieve less SSN noise levels the power network was built on top of the embedded components; transforming the interconnection transmission lines into striplines. The discontinuities in the signal had larger capacitive parasitics when compared to the microstrip line as strong coupling occurs between the pads and the neighboring reference planes.

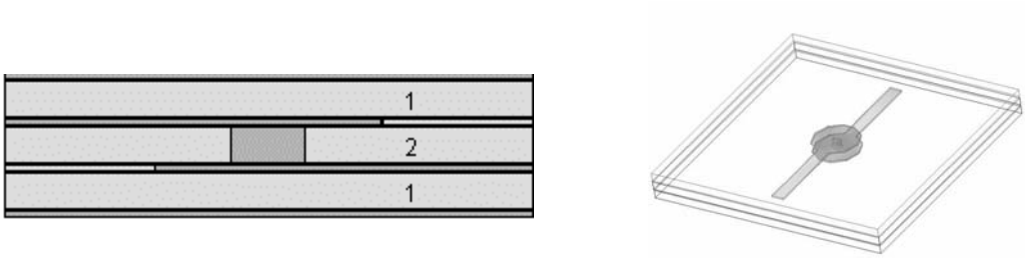


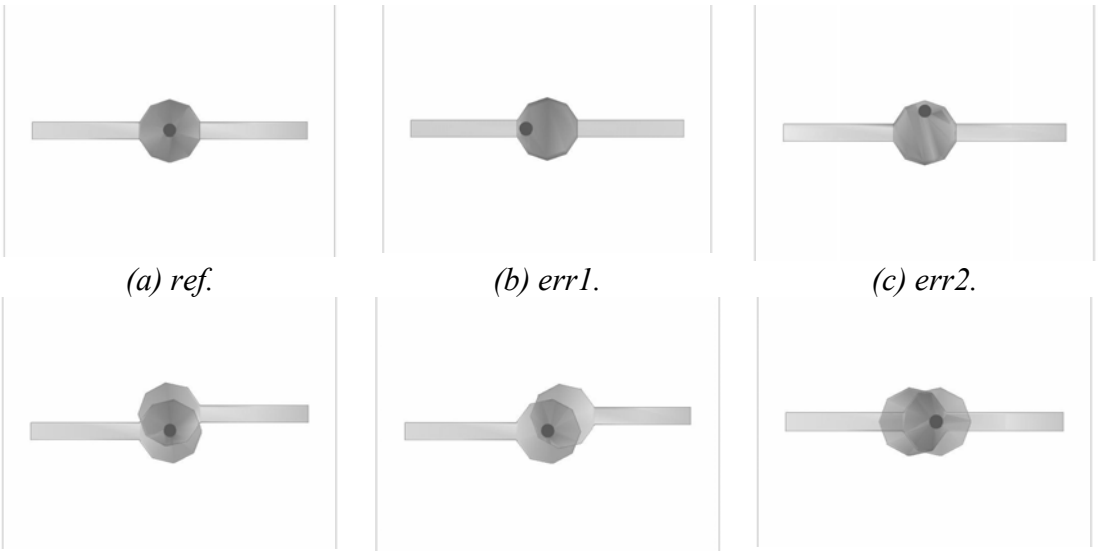
Fig. 4.22 Schematic presentation and model of the stripline connection.

The variables considered were the diameter of the vias (20 μm, 25 μm, 50 μm, and 100μm), the size and shape of the pads, and the thickness of the layer deposited on top of the component (layer 2 = 25 μm, 50 μm, and 100μm). The widths of the feed lines were calculated for each stack-up (Table 4.3). The width of the feed lines on the PWB and component were identical as the stack-up was symmetrical (Fig. 4.22).

Table 4.3 Calculated widths of the stripline feed lines.

t (μm)	25	50	100
w (μm)	40	45	60

The influence of manufacturing errors on the electrical characteristics of the interconnections was studied utilizing five models. The two variables were the misplacement of the vias resulting from laser drilling error, and the alignment of the upper layers. The laser drilling errors were simulated with the help of the first two models and the misalignments with the help of the last three models. In the first model (err1) a shift of 50 μm of the drilled via in the direction of the *x*-axis was considered (Fig. 4.23.a) while in the second (err2) the shift had the same value but was in the direction of the *y*-axis (Fig. 4.23.b). A shift of the upper layer of 50 μm on the *y*-axis was simulated in the third model (Fig. 4.23.c) and in the fourth model an additional error of 50 μm on the *x*-axis was considered (Fig. 4.23.d). The final model presented only an alignment error in the longitudinal direction (Fig. 4.23.e). This study was carried out utilizing v25_t25 and v25_t50 structures.



(a) ref. *(b) err1.* *(c) err2.*

(d) err3. *(e) err4.* *(f) err5.*

Fig. 4.23 The models utilized to investigate the assembly errors.

4.4.6. The RLC parameters

The RLC circuit models of stripline connections were determined utilizing the calculated scattering parameters of the models developed. Stripline transmission lines were utilized for this research because the impedance of the line did not vary significantly with the frequency. The feed lines were considered part of the connections because they couple to the pads and add discontinuities. Ladder type distributed RLC networks with *n*-sections were utilized to achieve the bandwidth of 50 GHz. The minimum number of the sections was calculated considering the electrical length of the transmission line having the length of the models (4.14) [17]. The calculated time delay for a 1 mm long stripline was 5.7 10^{-12} seconds, indicating that, more than three sections were required to achieve the bandwidth of 50 GHz. The models were tuned by comparing the results of the ADS and circuit simulations. A good agreement was achieved when 5 π segments were cascaded. The additional sections were required due to the presence of the discontinuities in the signal path.

$$n = 10 * BW * t_d \qquad (4.14)$$

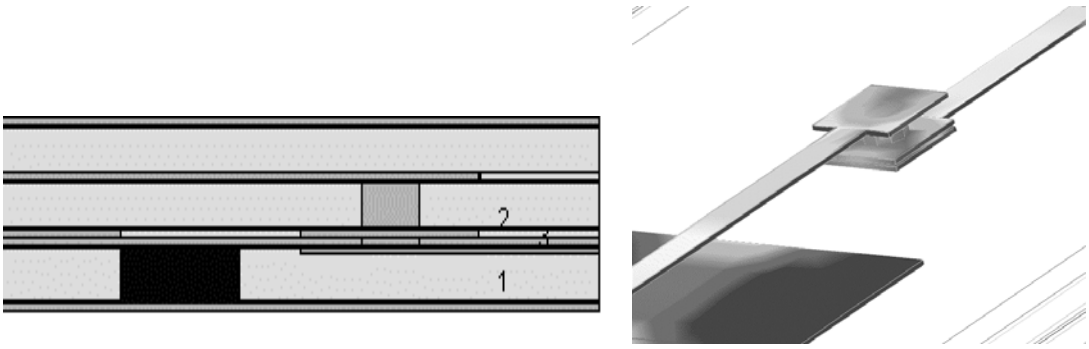
4.4.7. Stripline bridge connections

The design of the bridge connections utilizing striplines for signal integrity was facile because the substrate was symmetrical and good impedance control achieved. The

two variables of this research were the width of the split in the planes (100 μm, 500 μm and 1mm) and the thickness of the substrate between the signal layers (25 μm, 50 μm and 100 μm). The initial condition was that the return path of the module was ideal and the PWB and the components shared the same GND plane (Fig. 4.24). The widths of the bridging lines were designed to be equal to that of the feed lines. As the influence of the diameters of the vias on the performance of the interconnections was studied in earlier sections of this research, this part utilized only the structures with the diameter of 50 μm.

Fig. 4.24 Schematic presentation of the stripline bridge connection.

4.4.8. Stripline interconnection with high dielectric constant materials



(a) Schematic presentation. *(b) Interconnection model.*

Fig. 4.25 Stripline connection with the high dielectric constant material

The influence of the presence of a high dielectric constant material on top of the component on signal integrity was analyzed with the help of the striplines (Fig 4.25). Utilizing this set-up, power distribution noise levels were reduced as decoupling and filtering capacitors were fabricated in close proximity to the components and the impedance of the PDN was reduced. The variables of this research were the dielectric constant of the additional layer (3, 10 and 100), the widths of the gap between the PWB and the component (100 μm, 500 μm and 1mm). All the structures had the diameter of the vias of 50 μm and square-shaped pads. The reliability of the module was considered and a pad was added for the vias connection on the metal layer of the high dielectric constant layer. To avoid the changes of the parameters of the line due to high dielectric constant materials, the reference plane of the PWB signal was

modeled as the top metal layer of the new layer. The models had ideal current return paths and the widths of the striplines were calculated taking into consideration the additional layer.

4.4.9. Stripline connection to the Si chip

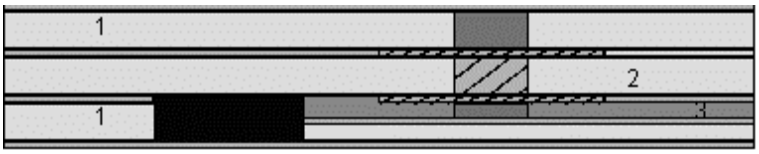
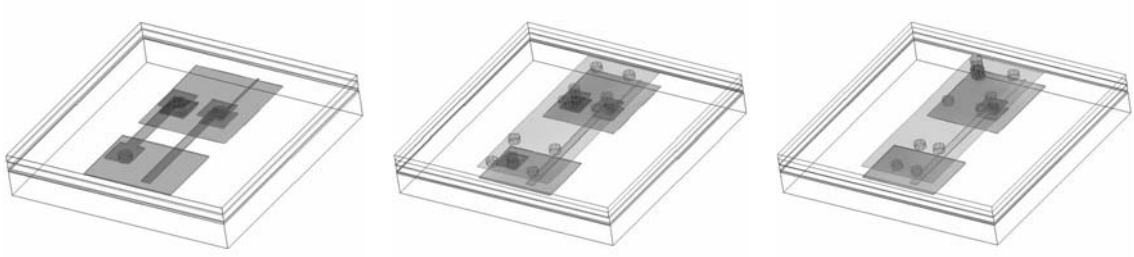


Fig. 4.26 Schematic presentation of the Si component connection.

The investigations of the interconnections of the Si components to the PWBs utilizing stripline transmission lines proved to be very challenging (Fig. 4.26). Due to the complex stack-up, there were many variables to be considered which affected the result of this research. The first challenge was the assignment of the ground reference ports to one of the reference layer. Preliminary calculations showed that the performances of the structures improved when the reference ground port was assigned to the plane where most of the return current flew. Two scenarios were set up for comparison: first of all, the ground reference was set on the lower reference plane of the PWB and the return current was forced to close utilizing a bridge connection (_b) (Fig. 4.27.a) and connections of the vias to the upper plane that was connected to the component (_u1) (Fig. 4.27.b). The second scenario utilized the upper plane as the ground reference for the chip (_u5) (Fig. 4.27.c).



(a). _b. *(b). _u1.* *(c). _u4.*

Fig. 4.27 Models of the Si component connection to the PWB.

The influence of the width of the assembly required gap (100 μm, 500 μm and 1 mm) was studied utilizing three models: _b, _u1, and _u2. The parameters of the models utilized in this study were as follows: the diameter of the vias –50 μm, the thickness

of all three substrates –25 μm and size of the square-shaped pads –100 μm. The size of the ground plane of the PWBs was 250 μm x 350 μm and the component was 250 μm x 380 μm. The top part of the model was assigned as a closed boundary and the upper ground layer was simulated as a solid plane connected to the closed boundary with the help of ten vias. Thus, it was possible to change the reference plane for port 1 from the lower plane to the upper one and be able to study the effects on the electrical parameters of the interconnections and return current paths.

The reference model had an ideal ground plane on the bottom. In the second model, the lower power plane of the PWB was assigned as ground references (v50_t25_s100_b). A bridge type connection was utilized to close the circuit providing a path for the return current. The pitch of the interconnection was 160 μm. To investigate the effects of the reference port assignment in the third model, the IC was connected to the upper plane (_u1) of the model while the ground reference port for port 1 was assigned to the lower power planes. In the fourth model the scenario simulated was one where the signal and ground connections were not adjacent to one another. In this case the connection to the GND of the IC was realized utilizing a via situated on the second row of bumps. The distance from the signal connection to the ground one was 200 μm in both the directions of the *x*-axis and the *y*-axis (_u4). For this simulation no reference ground ports were assigned, with the consequence that the return current was not forced to close in a specific point. The fifth and sixth models were similar to the third one (_u1) with regard to their geometries. In the fifth model the ground reference ports were removed so the return current could scatter on both ground planes (_u2). In the sixth, the ground reference of port 1 was assigned to the upper plane (_u3). The ground connection in the last model (_u5) was realized by connecting the bump adjacent to the signal one to the upper plane. The upper plane was assigned as the ground reference for port 1.

5. Results and discussions

In this chapter the influences of the assembly materials and of the WLCSP, FC and IMB fabrication techniques on signal integrity are presented and discussed. The studies were carried out utilizing the transmission line theory and close form formulas in time and frequency domains up to frequencies of 50 GHz. The increases in the return and insertion losses of assemblies were studied both experimentally and theoretically.

5.1 Influence of solder oxide layer on SI

The hot temperature of the running components creates optimal conditions for the growth of the oxide layers on the surface of the solder bumps. The oxidation rate is logarithmic at 30 °C and parabolic from 180 to 450 °C for thicknesses up to 700Å. Investigations of the SnO_2 layer have shown that the material in an n-type semiconductor that became oxidized under 170 °C appears to be an amorphous layer [27, 28]. The effect of thick oxide on the bump surface is similar to the effect of high resistivity metal layers, the high dielectric constant deposited on the outer surface of metals having been described earlier by Denlinger *et al,* Sobol and Burlacu *et al.* [25, 29, 160]. Furthermore, being a semiconductor layer, its presence affects also the dielectric constant of the transmission line by increasing its value and detunes the electrical circuit [31].

The electrical losses of the lead-free materials under investigation (Sn3.4Ag0.8Cu and pure Sn) were researched by measuring the scattering parameters of the test boards up to frequencies of 50 GHz. The experimental results obtained were manipulated mathematically with the help of the Matlab program to determine the insertion loss per unit length (5.1) [17].

$$S_{21} = 20\log_{10}\left(\sqrt{\left(S_{21-real}\right)^2 + \left(S_{21-img}\right)^2}\right) / 4(dB) \tag{5.1}$$

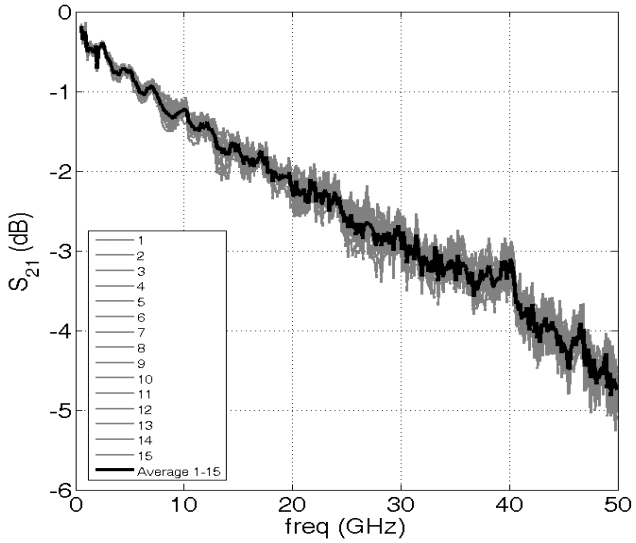


Fig. 5.1 Repeatability of the insertion loss SnAgCu test boards.

The ease with which the experimental results obtained from the electrical measurement of the test samples could be repeated was a key factor observed in this study. The analysis assumed that the dielectric radiation losses were the same for all test boards. Changes in the fabrication process would result in higher losses that could affect the accuracy of the studies. The results measured showed a low value of the dispersion for the fifteen lines under study. The standard deviation of the insertion losses of the transmission lines was calculated to be $q = 0.0587$ for an average value $g = -2.95$ dB at 30 GHz [161]. The results achieved were good considering the noise present in the measurement results and that the deviation was calculated for fifteen lines out of the twenty manufactured (Fig. 5.1). The loci of the Sn, SnO, SnAgCu and SnAgCuO transmission lines which best matched the average values were utilized for further analysis.

Comparison of the insertion losses of the SnO and Sn samples (Fig. 5.2) showed similar values for the losses up to 40 GHz and an increase of about 0.1 dB/cm for SnO at 50 GHz. The difference between the tin samples was about 6.5% at high frequencies. The difference was small because the Sn reference material had been stored at room temperature for a long time and the oxide layer was already considerably thick. In the case of the SnAgCuO, the increase in the insertion losses at high frequency was about 14 % relative to SnAgCu (Fig. 5.3). This larger difference could be the result of three possible factors: the thickness of the natural oxide, the

roughness of the surface or the oxidation mechanism. The SnAgCu samples were mechanically cleaned before annealing to ensure that the oxide layer present in the SnAgCu samples was thin and the surface was rough. The oxidation process was different for the alloy when compared to the pure metal. Therefore, it is likely that the electrical parameters may be different as well.

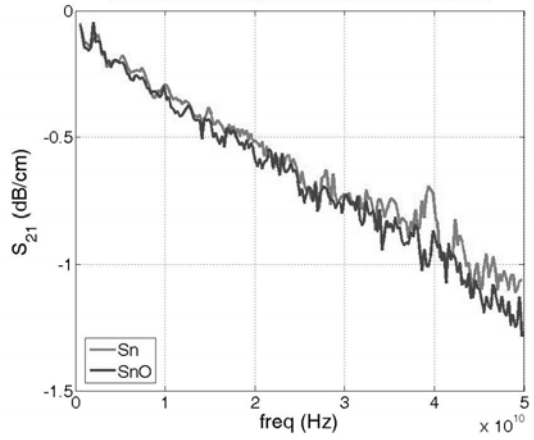


Fig. 5.2 Comparison of insertion losses for the Sn and SnO test boards.

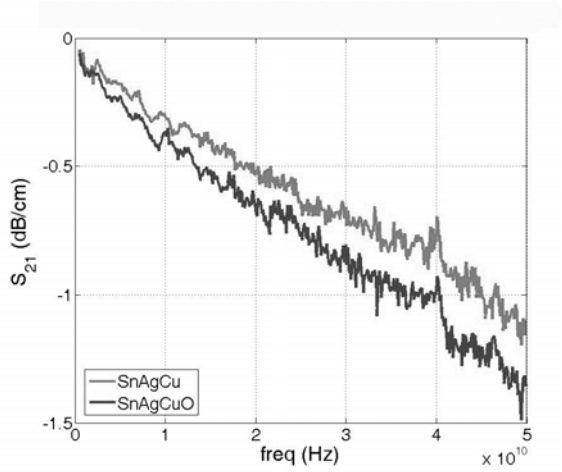


Fig. 5.3 Comparison of insertion losses for the SnAgCu and SnAgCuO test boards.

To determine the correction coefficient that account for the oxide layer presence, the values of the resistive and dielectric attenuation coefficients for the SnAgCu test boards were firstly calculated with the help of the closed-form expressions published by Gupta *et al*. [150]. The choice of these formulas was done after comparison with other calculation expressions presented by Pozar and Wadell [17, 79]. The main reasons for this choice were: the calculation technique of conductor loss that were based on the Wheeler's method and because the dielectric losses were calculated considering that the effective dielectric constant varies with frequency. The results represented a good approximation of the electrical performances of the circuit over a large bandwidth. These formulas were utilized in previous scientific papers to determine the conductor and dielectric loss up to 40 GHz. Kemppinen showed that the calculated results obtained with the close form formulas match the measured results [162]. A comparison between the measured and calculated total losses (α_T) of the 4 cm SnAgCu microstrip line is presented in Fig 5.4. The results show good agreement up to 40 GHz, where the difference was within 10%. The mismatch between the experimental and calculated results at frequencies above 40 GHz resulted from the calculation approximations, the fabrication process, and the calibration of the

measurement set-up. The TRL measurement calibration set-up was an important factor. From 40 GHz the electrical parameters of a shorter transmission line were used for the calibration set-up. This meant that the calculated S-parameters for the calibration at high frequencies were different to the ones utilized for frequencies up to 40 GHz [86]. The fabrication process affected the under etch of the lines that were not accounted for in the formula and affected the characteristic impedance and losses.

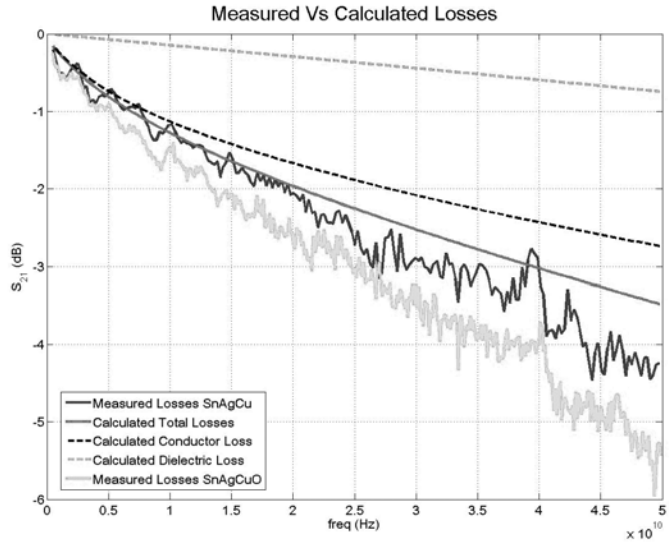


Fig. 5.4 Comparison of the measured and calculated losses for the SnAgCu sample.

The increase in insertion losses due to the oxide layer SnAgCuO was calculated by the curve fitting method with the help of the Matlab program. The dielectric losses were the same as in the case of the SnAgCu test boards. Comparison of the total losses for SnAgCu and SnAgCuO demonstrated that the total losses increase with the square root of the frequency. This corresponds to the evolution of the conductor loss with the frequency. A good match was found for SnAgCuO when the calculated conductor loss of the SnAgCu microstrip line was multiplied with a correction factor of 1.41. With this value factored into the equation, the calculated and measured results of highly oxidized samples showed similar values up to frequencies of 40 GHz. The results were in good agreement with the theory of multi-layer metal transmission line losses (Fig. 5.5). The oxide layer resembled the thin, high resistivity metal layers used for the fabrication of the adhesion layers in microwave circuits that are known to increase the conductor loss [25].

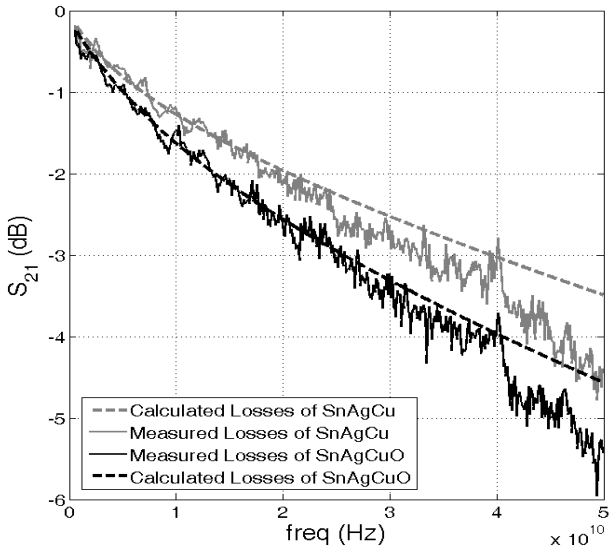


Fig. 5.5 Comparison of the measured and calculated total losses for the SnAgCu and SnAgCuO samples.

The literature survey showed that the oxide layer performs as an n-type semiconductor. For this reason, the effect of the change in the dielectric constant due to the presence of the oxide layer was investigated using the impedance of a two-port T-network (Fig. 5.6). The difference between the measured resonance frequencies of the transfer impedance of the SnAgCu and SnAgCuO samples was about 0.6 GHz at 20 GHz and 0.8 GHz at 40 GHz. By considering the transmission line as a series resonator, an increase of about 3% was calculated in the equivalent dielectric constant of the SnAgCuO line.

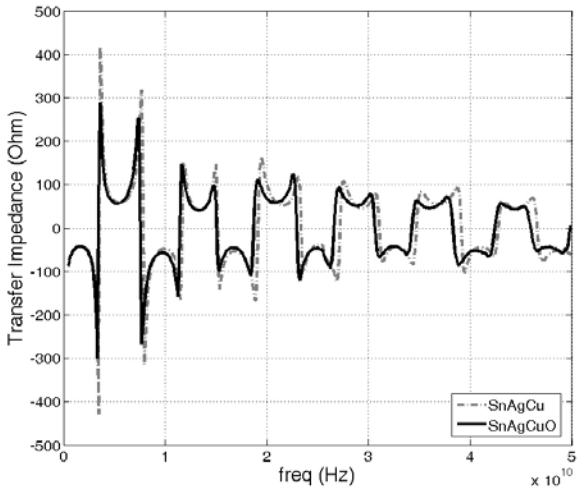


Fig. 5.6 Comparison of the resonance of the transfer impedance for SnAgCu and SnAgCuO.

Utilizing the determined correction coefficient for the conductor loss, it was possible to estimate the effect of the oxide layer on the WLCSP package having the bump diameter of 300 μm and the pitch of 500 μm. The interconnections perform as wave guides at high frequency, making it possible to determine their losses utilizing the transmission line theory. The changes in the values of the conductor loss when the oxide layer was present were calculated for both single ended and differential signal distribution. The losses were evaluated out by considering the bump surface to be smooth. Simulating one IC interconnection was difficult as the distribution of the electromagnetic field depends on the return path of the signal and the voltage levels of the neighboring connections. Assumptions were, therefore, simplified concerning the bump voltages and placements.

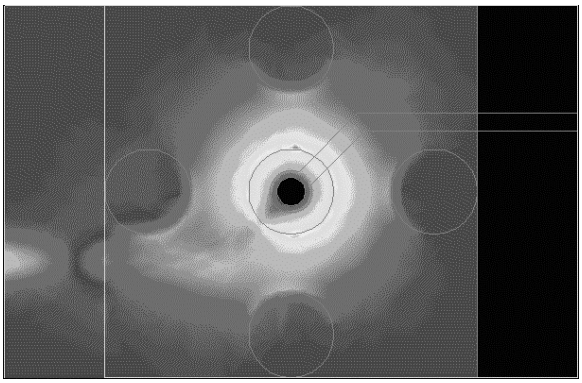


Fig. 5.7 Electric field distribution in an interconnection in the center of the package.

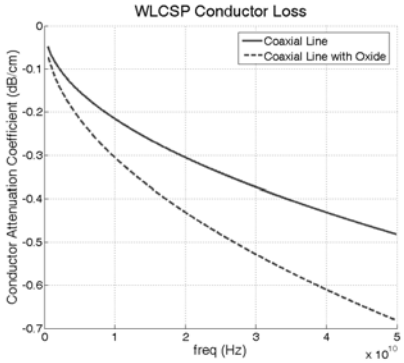


Fig. 5.8 Comparison of conductor losses of the coaxial line with and without oxide influence.

The calculations for single ended signaling were performed considering the bumps in close proximity to the interconnection under investigation were at a lower voltage level. They were simulated as being connected to ground. Simulation of the WLCSP assembly showed that the electric field distribution resembled the one in the coaxial cable where the inner radius was the bump radius and the outer radius was equal to the bump radius plus the gap between the bumps (Fig. 5.7). Applying the correction coefficient, the conductor loss increased from 41% to 0.68 dB/cm when compared to the natural oxide (Fig. 5.8).

The electromagnetic simulation results of the differential signaling showed that the electric field distribution resembled the one of the twin-wire transmission line. For the conductor loss calculation the wire diameter was assigned equal to the bump diameter,

the distance between the wires was equal to the gap between the bumps and the resistivity of the twin wire lines was equal to the one of SnAgCu (Fig. 5.9).

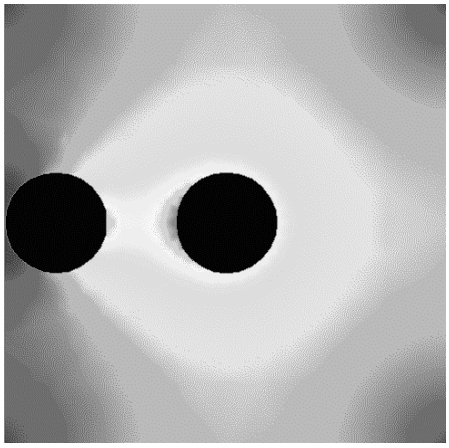


Fig. 5.9 Electric field distribution in an interconnection set up for differential signaling.

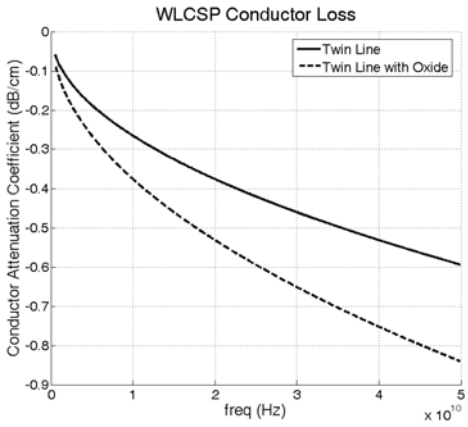


Fig. 5.10 Comparison of conductor losses of the twin-wire line with and without oxide influence.

The results showed that the presence of the oxide increased the conductor loss with 41% up to 0.85 dB/cm as compared to the natural oxide (Fig. 5.10). The value of the conductor loss was higher in the case of differential signaling in comparison with the single ended signaling. The reason for this is the current distribution on the surface of the bump resulting from the effects of close proximity. In the case of the coaxial line type, the current was almost equally distributed on the entire surface of the bump as the electrical field was evenly distributed around the inner conductor. For the twin line, however, the current density was higher where the lines were closer to one another as the electrical field has higher values at the points of the minimal distances between the lines.

Because this is the first time to measure the effect of solder oxide layers on conductor losses the results can be compared only with the work that focused on the effects of power losses on multi-layer conductors that have high resistivity materials as surface finish. The oxide layer resembled the thin, high resistivity metal layers used for the fabrication of the adhesion layers in microwave circuits that are known to increase the conductor loss up to 50 % [25, 29]. The results of this study are in good agreement with the literature as the determined correction coefficient was 1.41 that represents an increase of conductor loss with 40%.

5.2 Influence of microstructures on SI

The different microstructural features (grain size, size of colonies, and intermetallic particles) in the solder interconnections are influenced by different reflow parameters. Solidification, the cooling rate and the dissolution of metallizations were the key factors that influence the formation of microstructures during the soldering operation. The analyses and experiments showed that the alteration of the reflow profile is an effective way of influencing the microstructure [163]. Likewise, the degree of coarseness of the microstructure can be also changed by cold rolling and annealing.

To simulate the effects of different degrees of the coarseness of the solder bumps on the signal propagation, the SnAgCu material was cold rolled and then annealed for different lengths of time. By cold rolling the SnAgCu, its microstructure was plastically deformed so that it became very fine. During the annealing process the solder recrystallized and the microstructure became coarser. To create different degrees of coarseness, the samples were annealed at 200°C in atmospheric conditions for different time periods: t1-natural oxide, t2 = 10^3 seconds, t3 = 10^4 seconds, t4 = 10^5 seconds t5 = 10^6 seconds and t6 = $2.6*10^6$ seconds (Fig. 5.11). The material was placed into an oven for annealing starting with the longest time period. This was done in order to avoid the eventual fabrication inconsistencies, and all the test boards were fabricated at the same time.

The polarized optical micrographs of these cross-sectional views of the structures above show clearly that the size of the grains increased due to recrystallization and that the growth of the grain occurred as a result of longer annealing times. It was noticed that the most significant microstructure changes occurred in the first 10^3 seconds. The experimental results showed that the losses increased with the annealing time. This was as a result of pronounced oxide growth on the surface of the conductor (Fig. 5.12).

The insertion losses of the samples annealed for 10^3 seconds were similar to the ones of the natural oxide. Nevertheless, the microstructure was considerably different as the Sn grains were coarser after 10^3 seconds (Fig. 5.11). When annealing the samples for more than 10^4 seconds, the difference in insertion losses becomes small, being

about 0.3 dB. For these periods of time the microstructure of the samples became even coarser as the annealing time increased. For samples annealed for 10^5 seconds and 10^6 seconds, the insertion loss is almost the same for all the frequency range. The samples annealed for the longest time showed the increase of the resistive loss up to about 1 dB compared to that of the natural oxide for the 4 cm microstrip line. As the changes in the microstructure did not influence the electrical losses, it was considered that the losses were as a result of the oxide layer growth on the conductor surface.

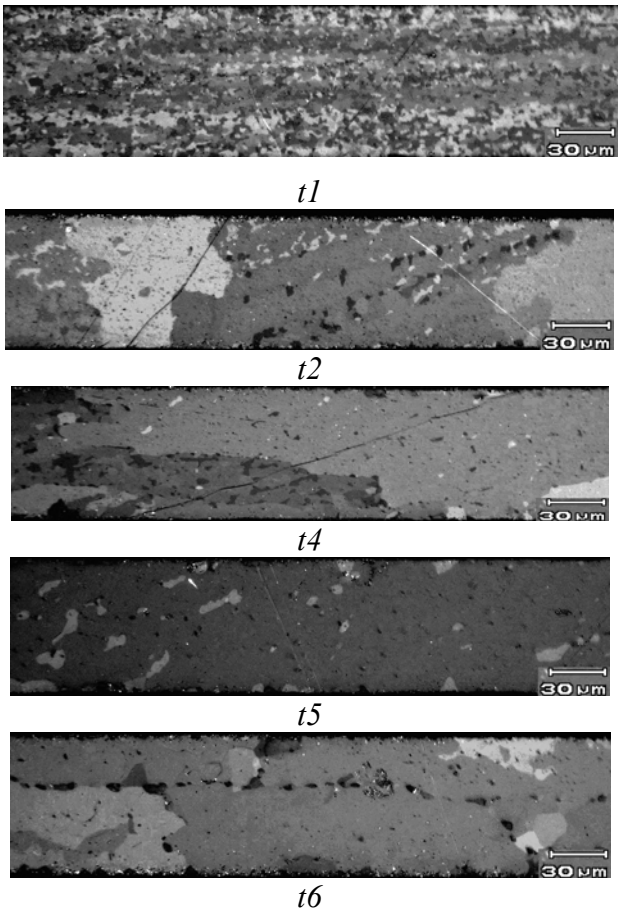


Fig. 5.11 Optical polarized micrograph showing the cross-sectional structure of the SnAgCuO after different annealing times.

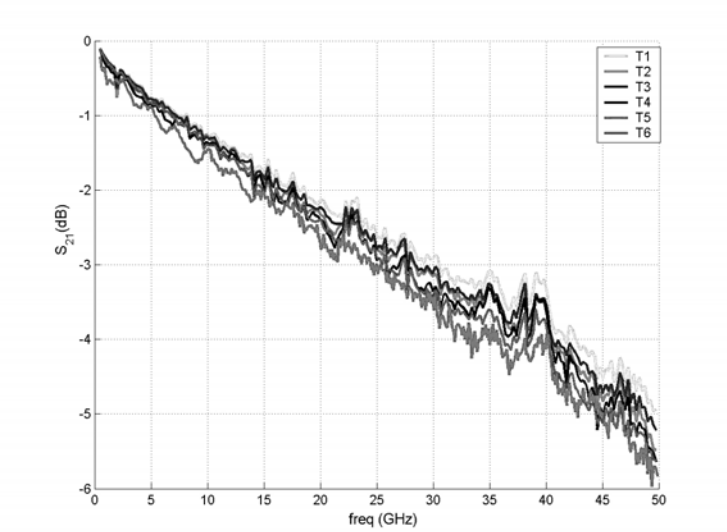
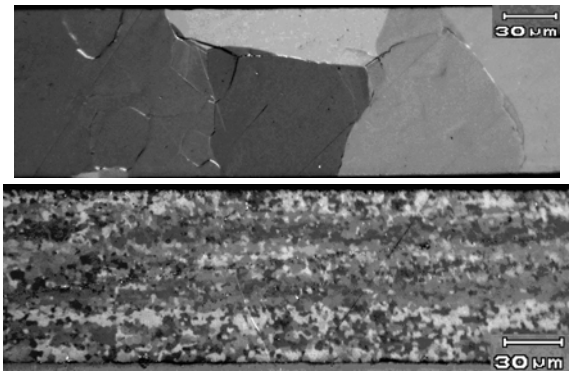


Fig. 5.12 Measured insertion loss parameter for the 4cm transmission line.



(a)

(b)

Fig. 5.13 Optical polarized micrograph of Sn (a) and SnAgCu (b) with natural oxide.

Further investigations of the microstructure effect on high frequency losses were carried out comparing the electrical losses of pure Sn and SnAgCu with natural oxide layers. The resulting measurements of the test boards showed similar values up to 50 GHz. The dimensions of the transmission lines were the same for all test boards and the only difference was the solder material. The micrograph of the cross section of the conductor materials taken with polarized light illustrates that the bulk microstructures of the Sn and SnAgCu are very different (Fig. 5.13). The microstructure in the pure Sn sample is coarse (Fig 5.13. (a)), whereas in the SnAgCu the microstructure is very much refined (Fig. 5.13 (b)).

In spite of these marked differences in the bulk microstructures, the losses in both Sn and SnAgCu were of about the same magnitude (Fig 5.14) and the influence of the solder bulk microstructure on the high-speed propagation signals was low. This is due to the fact that at high frequencies the signal travels on the surface region of the

conductor and it is the properties of the surface – not those of the bulk – that determine the losses.

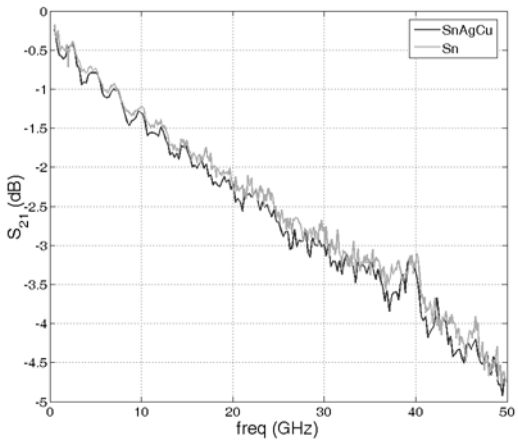


Fig. 5.14 Comparison of insertion losses of the Sn and SnAgCu samples with natural oxide and thick oxide layers.

The literature review unveiled that the effects of microstructure and intermetallics formation were studied at DC voltages and for thermal-mechanical reliability. The results of the DC investigations pointed out that the main cause of the increase up to 100 % of the resistivity of the solder joint is due to the formation of intermetallics and not due to the changes of the microstructure [164, 165]. The RF performances of solder materials were not investigated. The results presented in this work are in good agreement with the transmission line theory, which states that at high frequencies the conductor losses depend on the surface quality of the materials and not on the inner structure. This is due to the skin effect that at high frequencies repels the current toward the outer surface of the conductor making the conductor losses sensible to oxide presence and roughness of the surface [17, 30].

5.3 Influence of underfills and high density PWB routing on SI

The presence of underfill materials and metal structures in close proximity to the RF and high speed components changed the electrical properties of their circuits. For this research, two types of test boards were successfully manufactured and the effects of three different underfills on signal integrity were studied. One type of test board had a metal layer under the WLCSP component to simulate the high density routing under the PWBs. The second one did not have any metal present on the PWBS in the

vicinity of the signal line. Twenty test boards, ten of each type, without underfills were considered as the reference test modules. For a facile identification of the test boards and underfill materials, a 2-digit rule was applied in the legends of the loci. The first letter marked the presence of the metal layer under the component: X – no-metal, O – metal. The second letter marked the type of underfill: C – corner underfill, A – 1093A material and L – FP4532, O – air (reference).

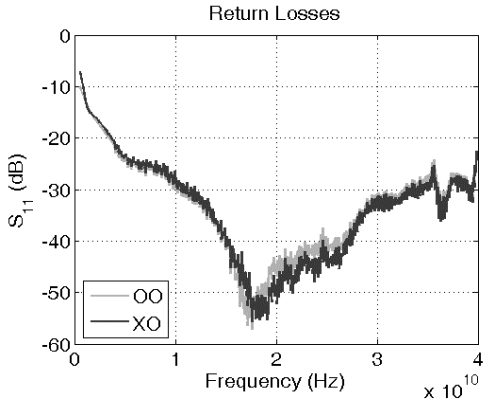


Fig. 5.15 Return losses of the reference test boards.

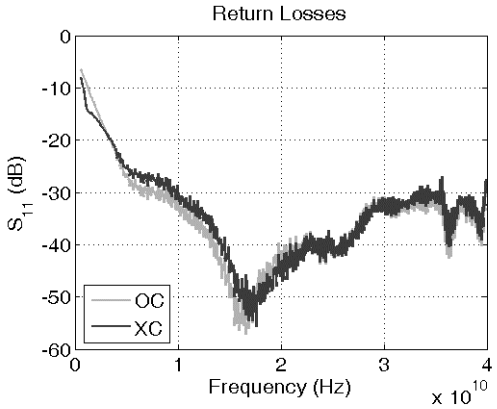


Fig. 5.16 Return losses of the test boards with corner underfills.

The resulting measurements for all the test boards showed high values in the reflection losses at low frequencies from 500 MHz up to 3 GHz. This was due to the non perfect compatibility between the measurement set-up and the test board. The test fixture had a cylindrical shaped pin for probing. The connection pads were made out of very smooth 0.5 μm thick Al. The formation of an oxide layer on top of Al and the impossibility of the cylinder to easily penetrate the layer caused conduction problems at low frequency. To improve the situation, the position of the probing pin was modified to increase the pressure on the pad. Another issue was the contamination of the Au plated pin with Al residues from the pads. To avoid measurement errors due to contact problems, the pin was cleaned after every 10 measured samples. The resonance present at frequencies above 37 GHz in the measured results was due to the calibration errors at the end of the interval.

Comparisons of the reference boards with (O) and without (X) high density circuitry showed that the presence of the metal plate under the component decreased the resonance frequency by 0.8 GHz from 18.5 GHz down to 17.7 GHz (Fig. 5.15) (Table 5.1). The metal structure below the component performed as an RF shield for the

CPW line. This resulted in the propagation modes of the waves being changed as the shielded CPWs supported both the CPW and the parallel plate modes, making them resemble the FGCPW lines [166, 167]. This affected the power loss since a new mode was generated at the input and suppressed at the output of the components. Similar results were obtained for the corner underfill. The difference between the resonant frequencies of the X and O samples was about 0.8 GHz. This indicated that the corner underfill did not influence the parameters of the CPW lines (Fig. 5.16). The effect of the metal plate on circuit detuning was smaller when capillarity flow underfills were utilized. For both materials the detuning errors were about 0.5 GHz (Fig. 5.17, Fig. 5.18). The high dielectric constant materials increased the capacitance of the line while at the same time reducing the electromagnetic field coupling to the metal plate. Stronger coupling occurred between the line and adjacent ground planes because the dimension of the gap was about half the value of the height of the bumps.

Table 5.1 The measured electrical properties of the test boards.

Underfill / Metal presence	Air	Corner (C)	Low viscosity (A)	High viscosity (L)
	f_r (GHz)	f_r (GHz)	f_r (GHz)	f_r (GHz)
Metal (O)	17.7	16.7	17.2	16.5
No Metal (X)	18.5	17.5	17.7	17

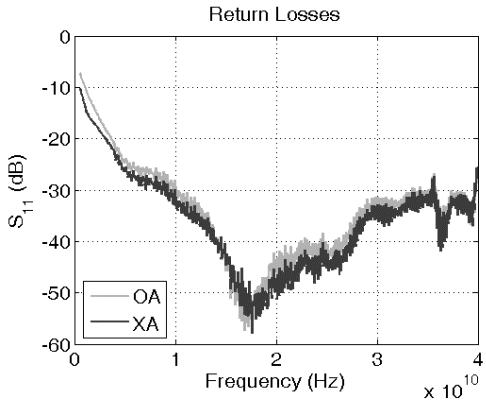


Fig. 5.17 Return losses of the test boards with 1093A underfill.

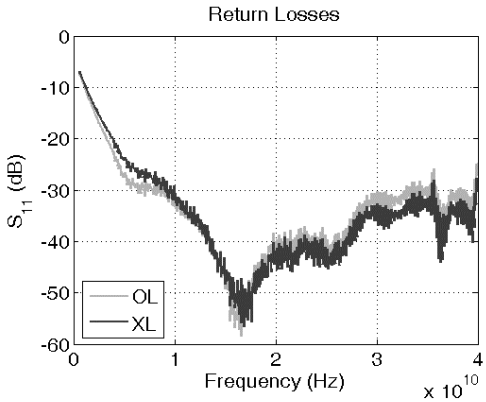


Fig. 5.18 Return losses of the test boards with FP 4532 underfill.

The comparison between the results of the test boards with corner underfill and of the reference assemblies showed that the presence of the underfill decreased the electrical performances (Table 5.1). The resonant frequencies of the X and O assemblies with corner underfill were about 1 GHz smaller compared to those of the reference boards.

Therefore, it was demonstrated that the underfill affected the electrical parameters of the interconnections but did not affect the electrical parameters of the CPW lines.

The measured results of the test boards with the standard capillarity flow underfills showed that the material properties had an important impact on the electrical properties of the assemblies. The 1093A showed lower changes compared to the FP4532 as it had had a lower viscosity and lower filler content. Comparisons of the results of the 1093A with those of the reference boards showed a decrease in the resonance frequency of 0.8 GHz for the X samples and 0.5 GHz for the O modules. The FP4532 material had the highest influence on the electrical performances of the WLCSP assemblies. It decreased the resonant frequency of the O samples with about 1.2 GHz while the X with by 1.5 GHz when compared to the reference test modules.

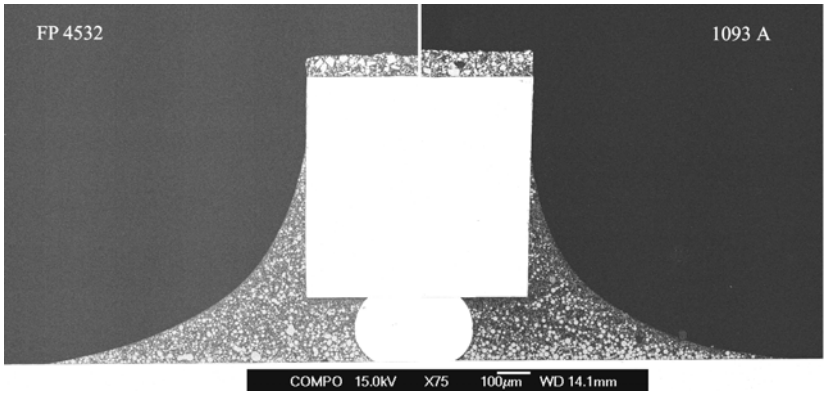


Fig. 5.19 SEM micrograph of the Silica particles distribution on FP 4532 and 1093A.

Comparison of the electrical performances of the 1093A and FP4532 showed that the resonant frequency of the test boards with FP4532 was lower by about 0.7 GHz. The shift was the same for both X and O assemblies. The reasons were to be found in the amount and size of filler particles present in the underfills as well as in the curing processes. The FP4532 had 12 % more filler than the 1093A and the mean size of the particles was 6 µm compared to the 9 µm of the 1093A. Having a smaller particle size and a short curing time, the fillers did not have time to settle (Fig. 5.19). A result was that a higher dielectric constant was present in the vicinity of the line as the silica particles were present in greater number and had a higher dielectric constant when compared to the epoxy [168]. The SEM micrograph showed that in the case of 1093A, the long curing time allowed the filler particles to settle. In this case a larger concentration of the filler particles was present at about 45 µm from the component.

The simulation of the modules was utilized to extend the research also to the microstrip transmission line and to be able to analyze in greater detail the effects of underfills on the electrical performance of WLCSP interconnections. The simulation results of the test boards showed detuning errors when the underfill and metal plane were present (Table 5.2). The larger dispersion of the resonant frequencies compared to the values measured was due to the fact that in the simulations the electrical parameters of low resistivity Si were utilized. This compromise was adopted because the calculation bandwidth was limited at 20 GHz and to achieve resonant frequencies in this interval, fast propagation waves were required. The calculation results for the CPW lines confirmed that the high-density circuitry on the PWB detuned the WLCSP packed components. By comparing the calculation results of the X and O test boards it was shown that the metal presence down shifted the resonance frequency of the reference modules by 2.7 GHz. The presence of the underfill decreased the shift to 2.5 GHz, as the scatter of the electromagnetic lines in air was larger (Fig. 5.20). Comparisons of the electrical characteristics of the modules with or without the underfill showed that the presence of the underfill shifted the resonance frequency of the X modules by 2 GHz while the O module by 1.8 GHz. The results demonstrated that the assembly with the underfill and metal on the PWB had the lowest resonant frequency, only 12.5 GHz.

Table 5.2 The simulation results of the test coupons.

	CPW – air	CPW – u	Microstrip – air	Microstrip – u
	f_r (GHz)	f_r (GHz)	f_r (GHz)	f_r (GHz)
Metal (O)	14.3	12.5	7.7	7.5
No Metal (X)	17	15	7.75	7.6

The analysis of the microstrip line configuration indicated that the structure had a small bandwidth being limited by the interconnection discontinuity (Fig. 5.21). The first resonance occurred at about 7.5 GHz for all the models. The results indicated that the metal presence did not influence considerably the electrical parameters of the transmission line. The relatively small difference of only 0.05 GHz noticed was a result of the parasitic coupling of the interconnection to the metal plane. It was not

due to the transmission line detuning. The results were inconsistent with electromagnetic theory, which states that most of the field of microstrip line propagates inside the substrate. Therefore, the fringing fields that coupled with the PWB metal were insignificant. When the underfill was present, however, the effective dielectric constant of the circuit changed noticeably (Table 5.2). The resonant frequency down shifted to 7.5 GHz being 0.2 GHz lower than that of the model with air. When the metal layer was not present, the change of the S-parameter of the interconnection was only 0.15 GHz.

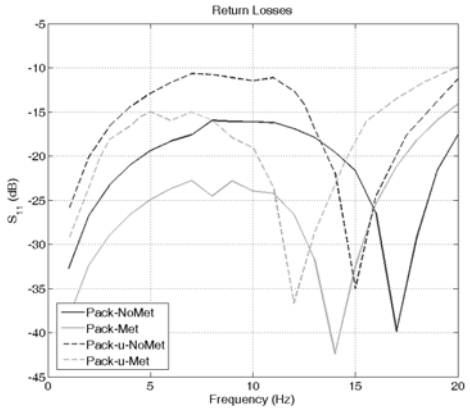


Fig. 5.20 Reflection scattering parameters S_{11} of the WLCSP-CPW simulated modules.

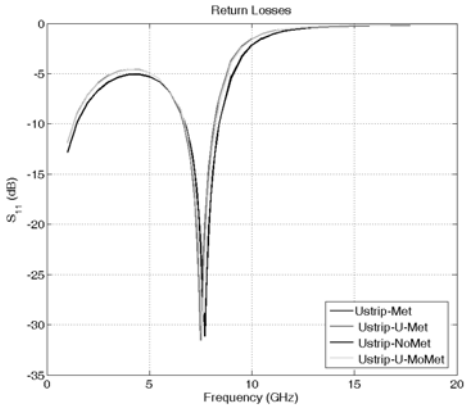


Fig 5.21 Reflection scattering parameters S_{11} of the WLCSP-microstrip simulated modules.

A thorough research of electrical performances of WLCSP interconnections with underfill was carried out in time and frequency domains up to 40 GHz. The results from the frequency domain calculations showed that the CPW lines had a much higher bandwidth, more than 40 GHz, compared to the microstrip lines (Fig. 5.22). For the microstrip connections, the presence of the underfill material between the bumps down shifted the resonance frequency from 38 GHz to 36 GHz. The time domain calculations confirmed that the underfill increased the capacitance of the interconnection (Fig. 5.23). The local characteristic impedance of the interconnection with air was 17.7 Ω. That decreased to 16.6 Ω when the underfill material was present resulting in a difference of about 5 %. For the CPW interconnections, however, no resonant frequency was present up to 40 GHz. The interconnections with air showed lower return losses compared to the underfilled structure. Considering the maximum of the curves of the return losses, a downshift of about 3 GHz was noticed when the underfill was present down to 34 GHz. The time domain calculations proved that the discontinuities of the CPW lines were small as the shift of the local impedance at the

interconnection was only 5 Ω from 50 Ω when the air was present. The increase of the capacitance of the interconnections when the underfill was present in the circuit resulted in a lower characteristic impedance of 41.5 Ω.

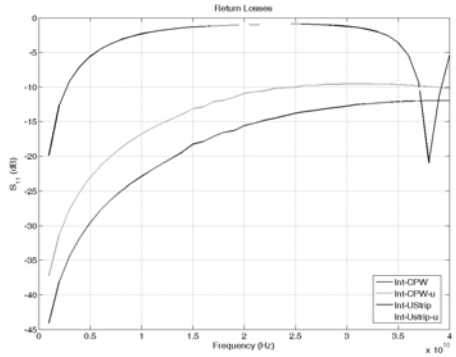


Fig. 5.22 Reflection scattering parameters S_1 of the WLCSP-CPW and WLCSP-microstrip interconnections.

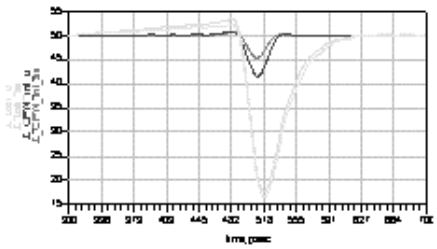


Fig. 5.23 Time domain characteristic impedance of the WLCSP-CPW and WLCSP-microstrip interconnections.

In the published literature it was not found a similar study that compared the electrical influences of different underfills. The published results focused on the comparison of the performances of component with and without underfills [35 - 37]. The measured results of this study are in good agreement with the published ones, which reported detuning effects of up to 10 % when the underfill was present under the component.

The measured result showed that the presence of the high density circuitry affect the CPW circuitry on the component by capacitive loading the line and reducing the resonant frequency with 0.8 GHz in the case of air and corner underfill and 0.5 GHz in the case of capillarity flow underfills. The results are in good agreement with the report of substrate influence on the electrical parameters of the lines [3, 169]. Sturdivant reported a decrease of the impedance of the CPW when the substrate was in close proximity. The differences between the published results and the ones determined in this work were due to the following facts: firstly the dimensions of the structures were dissimilar. The CPW line in this work had the dimension of the gap between signal and ground planes of 125 μm and air gap of about 200 μm as compared to the 35 μm and 100 μm. The result is a stronger coupling with the neighboring material in the case of the wider slot. Secondly, in this work the metal plane under the component acted as an RF shield strongly coupled to the line under investigation. The assumption of strong coupling with the metal part under the component was demonstrated when results of the measured air samples were

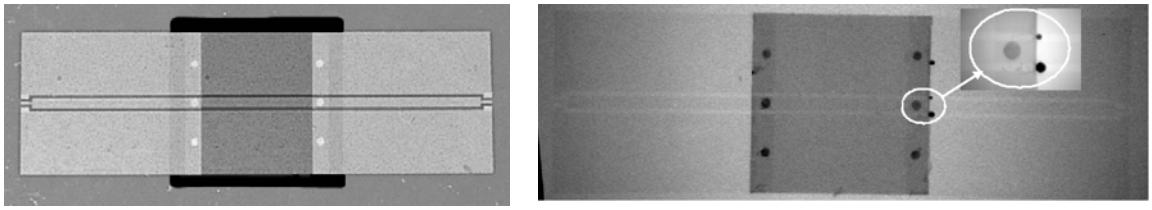
compared to the ones of the samples with underfills. The presence of the underfills changed the resonant frequency by decreasing the shift from 4.5 % to 2.9 %. Thus, forcing the fields to be confined in the neighboring of the line the coupling to the metal shield was decreased.

5.4. Influence of IMB and FC assembly techniques on SI

The effects of the IMB assembly on signal quality were investigated utilizing test coupons, which had been experimentally developed and tested, as well as electromagnetic simulations [170]. First of all, the electrical performance of two assembly techniques, the IMB and FC, were compared. Two types of test modules were fabricated and modeled to research the reflections and insertion losses of signals and resonance of assemblies. The fabrication of the IMB and the FC test samples was successful (Fig. 5.24). The optical and X-ray investigations showed a good control of the lines dimensions and a reliable embedding and interconnecting of the IMB and FC components into their carrier substrate. Comparison of the simulation with the results of the experiments obtained from the insertion and return losses of the IMB (Fig. 5.25) and FC (Fig. 5.28) assemblies showed good agreement. However, there were minor differences existing at high frequencies. The reasons for this were found in the manufacturing, measurement, and simulation processes.

The laboratory fabrication process influenced the geometries and material properties of the assemblies. Cross-sectional samples of the IMB assemblies revealed small air bubbles trapped in the moulding epoxy that has an affect on the dielectric constant. After the embedding of the components, the bottom of the modules were no longer flat due to the excess of the moulding epoxy. This influenced the thickness of the photo definable epoxy layers deposited on the non-perfectly flat and flexible substrates utilizing the spinning process. Changes in the properties of the substrates increased the return losses as the transmission lines were detuned in some regions. Moreover, for a good adherence of the conductor to the substrate, the polymer had to be chemically roughened up to around 1.5 μm. This manufacturing step was important for a good adhesion but increased the insertion losses of the modules [18]. The usage of the 1 μm thick electroless Cu as a seed layer increased further the resistive losses,

as its resistivity was four times greater than that of the electrodeposited Cu.



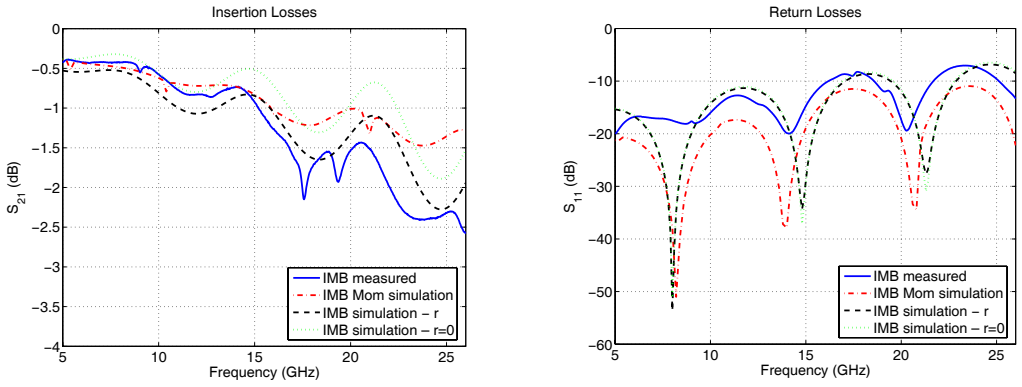
(a) *(b)*

Fig. 5.24 X-Ray image of (a) the IMB and (b) FC test assemblies.

The measurement setup introduced further inaccuracies into the resulting data. The microscopy inspection performed after the measurement process showed a slight difference in the probes' contact pressure. The main cause was the planarity of the samples. Moreover, a thin layer of oxide was noticed on the measurements pads. The factors mentioned above influenced the values of the reflection losses as parasitic capacitance was introduced by the high dielectric constant layer and the contact area was not similar for the ports due to the non planarity of the sample. The oxide layer also increased the insertion losses, as it was a high resistivity layer series connected to the circuit under study.

The high frequency differences between the ADS-Mom simulation and the results of the measurements are also to be found in the modelling and simulation processes. The return losses simulated and measured showed a good match for the resonant frequencies up to 20 GHz. This indicates that the equivalent dielectric constant of the model was similar to the one of the test board (Fig. 5.24 (b)). At 21 GHz a slight shift of 0.5 GHz was observed as the effective dielectric constant of the board increased with the frequency. The reason for this was found in the modelling of the IMB assembly. The 2.5D simulator required some simplifications to be applied to the distribution of the materials and their geometries. The software program, however, was unable to consider more than one material on the same layer. As a result, the add-on Probelec layer deposited on top of the embedded components and the moulding epoxy were assigned as LCP material. Therefore, the detuning errors and insertion losses at the component were decreased in the calculations as the LCP material had a smaller loss tangent and dielectric constant when compared to the Probelec and the epoxy. Moreover, the electrical parameters of the photo definable polymer utilized in the simulation were the ones provided by the manufacturer, which were measured at

1GHz. A 3 dB difference was observed between the measured and simulated reflection losses for the entire interval of study. Differences in the reflection losses were introduced also by the mismatch between the geometries of the model and the test boards. In the model, the edges were perfectly square and the spaces had constant values - even at the discontinuities - while the manufactured structure showed rounded edges and the discontinuities were not perfectly defined.



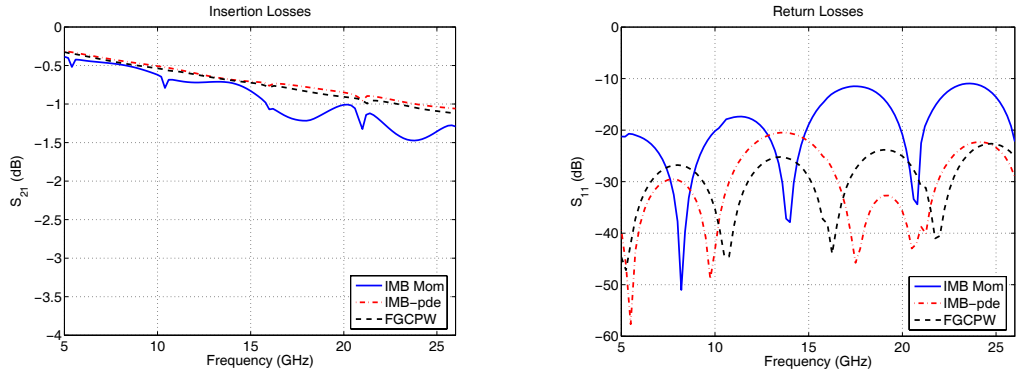
(a) *(b)*

Fig. 5.25 Comparison of the simulated and measured (a) insertion and (b) return losses for the IMB test board.

The values of the measured and calculated insertion losses were similar up to 15 GHz (Fig. 5.24 (a)). Above this frequency, however, the measured losses increased by up to -2.4 dB at 23 GHz, while the calculated ones reached -1.5 dB at the same frequency. The main cause of this mismatch was found to be in the calculation of the metal losses of the software that failed to consider the roughness of the substrates. To prove this, a simplified version of the IMB test board was modeled and simulated with ADS Schematics. The results pointed out that by increasing the roughness of the substrate up to 1.5 μm, the total losses of the test board increased by up to 1 dB (IMB-Simulation - r) (Fig. 5.25.a). The difference between the experimental and calculation data was about 0.1 dB. The largest mismatch was 0.3 dB at 21 GHz as the test assembly presented the effect of double resonance (Fig. 5.25). The frequency shift due to the mismatch of the effective dielectric constant of the model and test assembly was about 1 GHz. When the roughness of the substrate was assigned to be zero, the results were closer to those obtained with the ADS-Mom (IMB-Simulation - r = 0).

For a fuller understanding of the microwave characteristic of the IMB assembly, a

new model was built without the connection pads for measurement (IMB-pde). The electrical parameters calculated were compared to those of a FGCPW line that had similar parameters to the transmission line utilized for the IMB module.



(a) *(b)*

Fig. 5.26 Comparison of the simulated IMB models and the FGCPW line.

The insertion and return losses of the modeled test assemblies of the IMB (IMB Mom), IMB-pde, and FGCPW were compared (Fig. 5.26) and the influence of the measurement ports was determined by comparing the results of the IMB-pde and the IMB Mom (Fig. 5.26.a). The graphs showed that the ports introduced a maximum insertion loss of about 0.5 dB at frequencies of 17.5 GHz and 23 GHz. The insertion losses of the IMB-pde and the FGCPW models were similar as the structures and materials distribution were almost identical. The comparison of the loci of return losses of the IMB-Mom and IMB-pde showed a downshift in the resonant frequencies by about 2.5 GHz of the IMB-Mom (Fig. 5.26.b). The reasons for this were the parasitics and Z_0 mismatch due to the measurement ports that increased the return losses by about 15 dB. The behavior of the IMB-pde was similar to that of a dual resonator with resonant frequencies at 12 GHz. The comparison of the reflection losses of the IMB-pde and FGCPW models showed that the resonant frequencies of the IMB-pde were downshifted by about 1 GHz and the reflection losses larger by up to 5 dB at 12 GHz. The main causes of this were capacitance introduced by the interconnections, the double resonator behavior and the component detuning.

The time domain investigations of the IMB and IMB-pde models showed the impedance variations of the models were due to discontinuities. The value of the characteristic impedance of the structure after manufacturing was 48 Ω (Fig. 5.27). The Z_0 of the connection ports was 54 Ω being 15 % larger than the impedance of the

system. The IMB interconnections performed as LC circuits. The loop created by the return current was the cause for the increase of the local inductance. The overlapping metal pads increased the capacitance of the line.

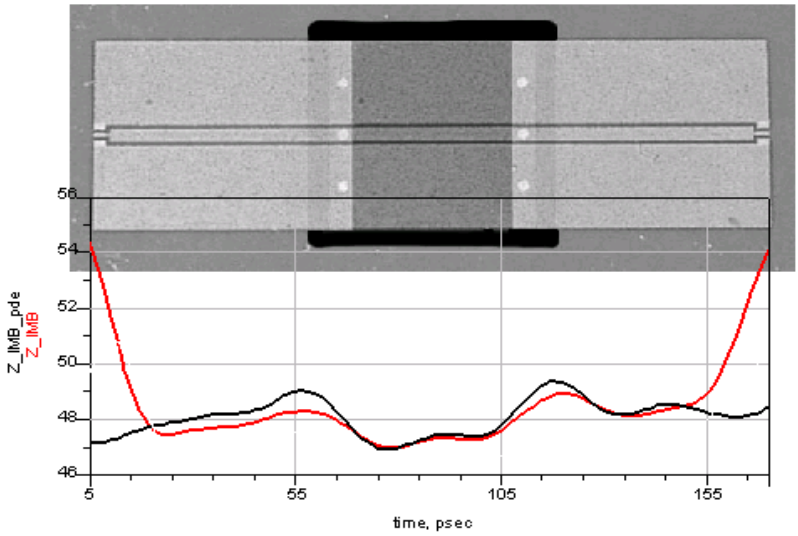
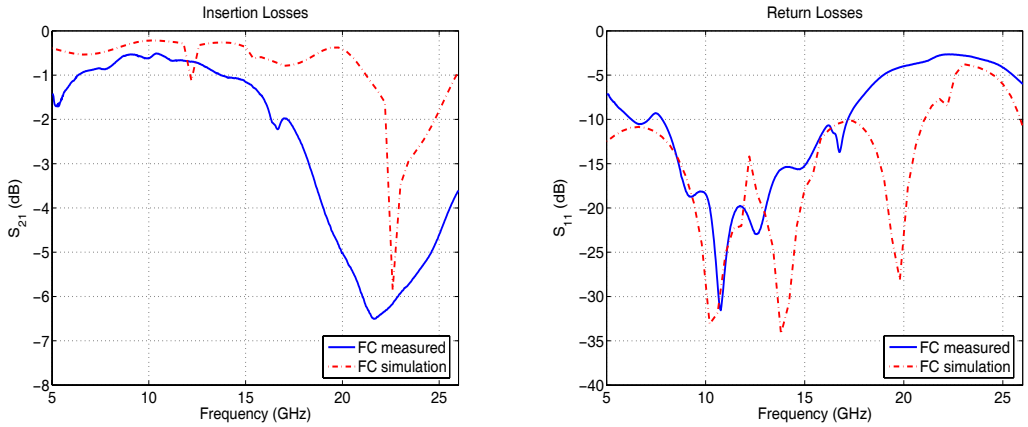


Fig. 5.27 Time domain results of the IMB-Mom module.

The measured and simulated return losses of the FC assemblies showed larger scattering at higher frequencies. In addition to the manufacturing issues discussed earlier, the X-ray analyses showed solder residues in the interconnection areas (Fig. 5.24.b). This, together with the differences in the diameters and heights of the bumps that were specific to the FC assembly process of the flexible components, caused further errors for the circuit at higher frequencies [80]. The misalignment of the component made possible the coupling of the unwanted modes to the normal CPW transmission ones, resulting in increased losses [158, 166]. As in the case of the IMB simulations, the differences between the measured and simulated results of the insertion losses at high frequency were due to the smooth substrate considered in the model. The simplifications adopted for the FC model, such as bump geometry, the absence of intermetallics, and air distribution on the upper side of the board, are additional reason for the differences to be seen between the results (Fig. 5.28).

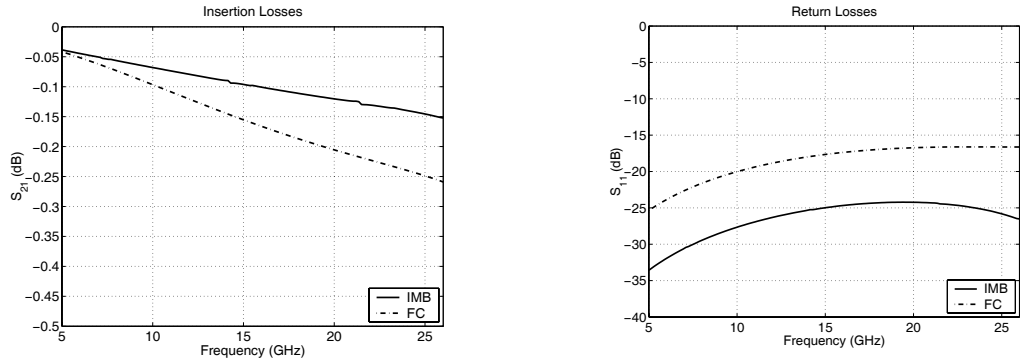
The simulated insertion losses of the IMB and FC test boards were similar up to 21 GHz. This meant that when the assemblies were built with the same components, the differences were caused mainly by the interconnection technique. Above 21 GHz, the insertion losses of the FC increased to 4.6 dB at 22.5 GHz as a result of test board resonance. The reflection losses of the FC assembly were about 5 dB higher than

those of the IMB. This can be explained by the fact that in the IMB case the signal mainly propagates in a microstrip-like mode and the presence of an embedded structure interacts minimally with the wave propagation. In the FC case, however, the interconnection introduces larger discontinuities and the assembly geometry changes the propagation wave paths media detuning the IC which increases the insertion losses.



(a) *(b)*

Fig. 5.28 Comparison of the simulated and measured (a) insertion and (b) return losses for the FC test board.

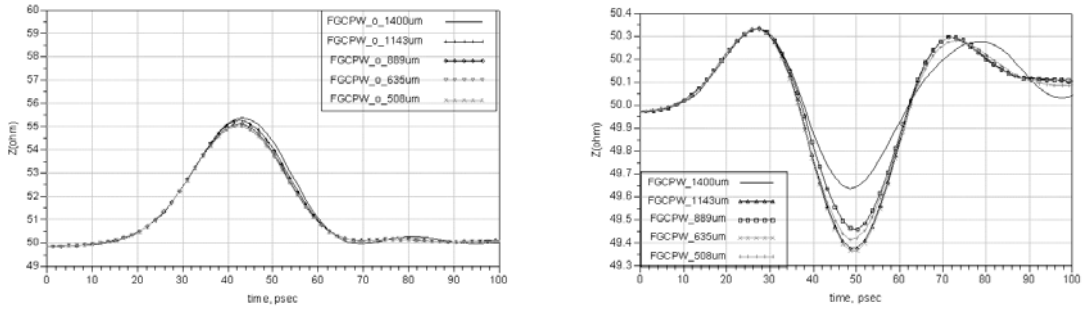


(a) *(b)*

Fig. 5.29 Comparison of the simulated (a) insertion and (b) return losses for the FC and IMB interconnections.

The simulated results of the interconnection area showed that the IMB interconnection performed better that the FC. At 26 GHz, the insertion losses of the IMB were lower, 0.15 dB, than those of the FC, 0.25 dB (Fig. 5.29.a). Furthermore, the maximum reflection coefficient of the IMB was 24.2 dB at 19.5 GHz, compared to only 16 dB at 22 GHz for the FC (Fig. 5.29.b). It was noticed that the resonant frequency of the IMB model was lower in comparison to the FC because the IMB acts like a long transmission line resonator, while the FC behaves like two independent resonators.

The interconnection height had a major influence on the performance of the assemblies. The bump heights of the FC were larger by about 10 times when compared to the IMB microvias. The increase in height led to an augmentation of the inductance, capacitance and radiation conductance of the assembly.



(a) *(b)*

Fig. 5.30 Time domain analysis of the FGCPW IMB interconnection with different pitches.

Time domain analysis was performed for several models of IMB derived from the model of interconnection (Fig. 5.30). The models all had different interconnection pitches and boundary conditions. The results showed that the boundary conditions had an important effect on the electrical characteristics of the interconnections. The absence of the conductive boundary forced the return currents to use only the side planes. As a result, the interconnections performed as inductive loads and the characteristic impedance increased by about 15 % up to 55 Ω (Fig. 5.30.a). By closing the boundary under the model, the variation of the local characteristic impedance was considerably decreased. The highest variation was only about 0.6 Ω. The interconnections performed as LCL loads and because they have small values, the discontinuities were facile to identify (Fig. 5.30.b). The gap between the PWB and the component created the first L discontinuity. The overlap of the pads of the assembly introduced the parasitic capacitance which decreased the local impedance. The last L was induced by the loop created by the return current. The pitch of the assembly also influenced the electric lengths of the interconnections. A delay of about 6 psec was noticed for the interconnections having the pitch of 1.4mm.

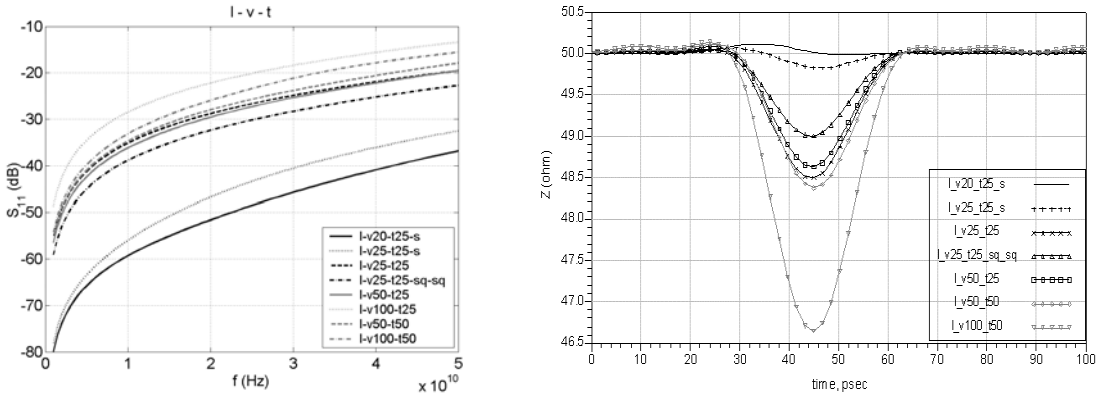
Good performances of the CiB techniques similar with the ones obtained in this work were reported in [47, 59, 62, 63]. The direct comparison of the results was not possible because the fabrication methods, the dimensions of the test set-ups and materials were different.

5.5. IMB assembly analysis

Analysis of the IMB interconnections was carried out in frequency and time domains for microstrip and stripline configuration. The research focused on the influence of the assembly discontinuities on the quality of signals in one net. The discontinuities addressed, specific to the IMB technology, were the following: the transmission line type utilized for the connections, the size and height of the vias, the dimensions and shape of connection pads of the vias, the current return paths and, finally, the influence of high dielectric constant materials. The bandwidth limitations of the interconnections were analyzed taking into consideration as limiting factors the resonant frequency and the –15 dB reflection loss threshold.

5.5.1. Microstrip interconnection

Microstrip interconnections were the first to be analyzed because thorough knowledge acquired from this study was utilized to design and characterize the other interconnection solutions. The variables considered in this analysis were the ones specific to the vias: the dimensions and height of vias and the size and shape of the connection pads. The dimensions of the pads were the main cause of signal distortion. The area of pads, the coupling area between the lower pads and the ground planes, as well as the differences between the widths of the feed lines and the size of pads all influenced the capacitance of the connection. The thickness of the substrate (height of vias) was the second parameter that affected the RLC of vias.



(a) Frequency domain. *(b) Time domain.*

Fig. 5.31 Frequency and time domain simulation results for the IMB microstrip interconnections.

The simulation results for the 25 µm thick substrate showed that the interconnections built utilizing small vias and pads had the best electrical performances. The v20_t25_s and v25_t25_s showed the lowest return losses of about 80 dB at 1 GHz (Table 5.3). The 5 µm difference between the sizes of interconnections counted at frequencies above 10 GHz where the return losses of v20_t25_s were smaller by about 6 dB (Fig. 5.31.a). The discontinuities of the Z_0 on the signal path were very slight - only about 0.2 Ω (Fig. 5.31.b). The augment of the dimensions of the pads to satisfy the requirements of the laser drilling process resulted in an increase of the return losses by about 20 dB. The connections having the diameters of the vias of 25 µm and 50 µm performed well as the variation of the Z_0 was small, about 1.5 Ω.

Table 5.3 Electrical properties of the microstrip line connections.

v (µm) \ t (µm)	25			50			100		
	1 GHz	50 GHz	Z	1 GHz	50 GHz	Z	1 GHz	50 GHz	Z
v20_s	80	37	50.1						
v25_s	78	32.5	49.8						
v25_sq	60	22	49.2						
v25_sq_sq	59	21.5	49						
v25	56	20	48.5	62	22	47.5			
v50	55	19	48.4	55	18	48.4	54	16	48
v100	48	12	46.8	48	13	46.6	46.5	11	46

Comparison of the performances of the v25_t25 with v25_t25_sq and v25_t25_sq_sq showed that the connections having square pads had less return losses because they had a smaller interconnection area. The v100_t25 showed the highest return losses of about 48 dB at 1GHz, the largest variation of the Z_0, 3.2 Ω, and the bandwidth was limited at about 43 GHz by the 15 dB limit.

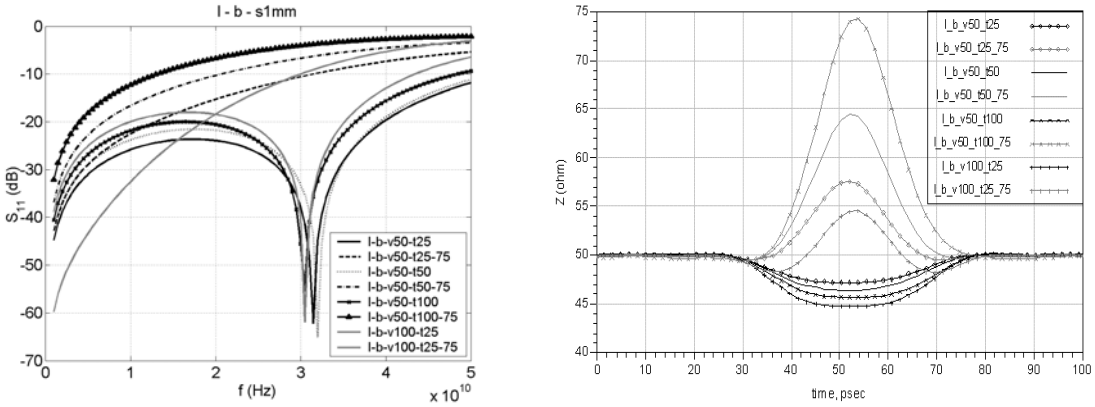
Table 5.4 The width of the feed lines for microstrip connections.

Height	25 µm	50 µm	100 µm
Cond 1	130	200	340
Cond 2	50	50	50

The increase in the thickness of the layer 2 to 50 μm and then to 100 μm did not change considerably the electrical parameters of the interconnections when compared to the t25 ones (Fig. 4.10). It was expected that the increase of the thickness would most likely result in decreasing capacitance of the connections. This, however, did not occur because the size of the upper conductor was increased by the thickness of the substrate to maintain 50 Ω impedance of the PWB feed line (Table 5.4). As presented in the modeling chapter, the width of the conductor was larger than the diameter of the pads. The effect of large pads was noticed for the v25_t50 as its parameters improved when compared to the v25_t25. Its Z_0 was smaller with 1 Ω. The electrical performance of v100_t50 and v_100_t100 were not on a par with the ones from the connections with small vias and thin substrates. Their high frequency performances were limited by the 15 dB level at about 35 GHz. This analysis showed that the microstrip interconnections perform well at microwave frequencies if the area of the pads and the diameter of the vias were small and the substrates were thin.

5.5.2. Microstrip bridge interconnection

The bridge interconnections realized with the help of an additional build up layer represented a cost effective alternative for the IMB fabrication. The research focused on the analysis of the influence of design for match impedance (MI) and for high density (HD). The other variables considered were the thickness of layer 2, the diameter of the vias and their pads as well as the dimensions of the assembly drill diameter. The results showed that, at low frequencies, the characteristics of the MI connections did not depend on the length of the interconnections (Fig. 5.32.a). Their parameters were mainly affected by the diameters of the vias, the size of the pads and the thickness of layer 2. However, the electrical performances of the HD bridge connections were influenced by all the variables.



(a) Frequency domain. *(b) Time domain.*

Fig. 5.32 Frequency and time domain calculation of the bridge connections.

The MI connections had the lowest return losses when the diameter of the vias was 50 μm and the thickness of the layer 2 was 25 μm – only 45 dB at 1 GHz (Table 5.4). The return losses increased with the thickness of the substrates to 43 dB for the 50 μm respectively up to 41 dB for t = 100 μm. The b_v50_t25_s100 and b_v50_t25_s500 were the only interconnections that had bandwidths larger than 50 GHz. The high frequency performances of the other MI were limited by the 15 dB level and resonant frequencies as the connections were electrically long and had large capacitive discontinuities. The increased thickness of layer 2 to 50 μm and 100 μm resulted in a decrease in the bandwidth of the assemblies because the width of the bridge line was augmented together with the thickness of the substrate. This was proven by the impedance analysis which showed that the variation of the Z_0 with t was about 1 Ω. The calculation results showed that the high frequency performance of the connections bridging the 100 μm space were limited by the 15 dB level, at 30.5 GHz for the 50 μm thick substrates and at 25 GHz for the 100 μm ones due to the increase in capacitance of the structure. The high frequency performances of the 500 μm and 1mm long interconnections were limited by their resonance frequencies as the structures were electrically long. The resonant frequency of the 1 mm long structures was about 30 GHz for all the substrates and the local impedance variation was about 1 Ω. Analysis of the influence of the dimensions of the space between PWB and component, the dimensions of vias and their pads, and the thickness of the substrate showed that for small gaps and large vias, the capacitive loading of the line had a larger impact on the electrical characteristics of the bridge connections. For longer connections, the change of capacitance did not have significant impact.

Table 5.5 Electrical parameters of the matched impedance (MI) microstrip bridge connections.

v / t (μm) (μm)		50			100		
	gap	100μm	500μm	1mm	100μm	500μm	1mm
25	1 (GHz)	44	45	45	38.3	38.5	38.8
	50 (GHz)	15	32	12	10	22	6.5
	f_r (GHz)			31.5		46	30.5
	15dB (GHz)			45	15.5	18	38
	Z (Ω)	45	46	47.2	41.5	42.8	44.8
50	1 (GHz)	43	43	43	37.5	37.5	37.5
	50 (GHz)	14	31	11	10.5	18	6
	f_r (GHz)		47	32		44.5	30.5
	15dB (GHz)	30.5		44	14	16	38
	Z (Ω)	44.5	45.5	46.5	41	42	44
100	1 (GHz)	41.2	41	40.5	36	36	36
	50 (GHz)	16	18	9.5	13	11.5	5
	f_r (GHz)		42.5	30		40.5	29
	15dB (GHz)	25		40	12	13	35
	Z (Ω)	44	45	46	40	42	44

The simulation results for the structures having the diameter of the vias at 100 μm confirmed the theory that large connections were not suited to microwave applications (Table 5.5). The low frequency return losses were about 6 dB larger than those of v50 and all the interconnections had bandwidths smaller than 50 GHz. The Z_0 of connections decreased to about 40 Ω. The increased capacitance influenced the electrical characteristics of the bridge connections over a 500 μm gap as their bandwidth decreased at about 15 GHz, where the S_{11} loci reached the 15 dB level. Nevertheless, the performances of the 1 mm long structures were not considerably affected by the size of the circuit.

The simulation results of the HD interconnection showed that careful analysis was required when these connections were utilized (Table 5.6). The results obtained from the analysis of the HD bridge interconnections presented a large scattering. Of all the connections having diameters of the vias at 50 μm, only two had bandwidths larger than 50 GHz, the b_v50_t25_s100 and b_v50_t50_s100, as they performed as capacitive loads. The rest performed as inductive loads and the 15 dB level limited their high frequency performance. The low frequency return losses were influenced

by the balance between the inductance of the "bridge" line and the capacitance of the pads. The connections with the Z_0 of about 52 Ω showed the lowest return losses at low frequencies (Fig. 5.32.b). A clear pattern was noticed in the electrical performances of the interconnections, with similar results to be seen for the flowing pairs: b_v50_t100_s100 and b_v50_t25_s500, b_v50_t50_s500 and b_v50_t25_s1mm and b_v50_t100_s500 and b_v50_t50_s1mm. This demonstrated that any bridge interconnection had the same parameters if one of them had half the length and double the thickness of layer 2 when compared to the first one. Nevertheless, the increase in the thickness of the substrate and the length of the lines resulted in poor electrical performance of the interconnections. The worst performance results were obtained with b_v50_t100_s1mm that had the Z_0 of 74 Ω: this caused reflections of about 12 % in the signal.

Table 5.6 Electrical parameters of the high density bridge connections.

t (μm) \ v (μm)		50			100		
	gap	100 μm	500 μm	1 mm	100 μm	500 μm	1 mm
25	1 (GHz)	49	60	43	40.5	46	60
	50 (GHz)	25	10	5	16	7	3
	f_r (GHz)					27	
	15 dB		39	21	21	39	23
	Z (Ω)	47.5	51.8	57.5	43.1	48	55
50	1 (GHz)	50	45.5	37	41.5	53	42
	50 (GHz)	19	5.5	3.5	30	4	2
	f_r (GHz)				47.5	11	
	15 dB		24	12		29	15
	Z (Ω)	48.5	56	64.5	44.5	52	61
100	1 (GHz)	57.5	38.5	32	44.5	47	35
	50 (GHz)	10	3	2	9.5	3	2
	f_r (GHz)				33		
	15 dB	38	14	7.5	44	20	9.5
	Z (Ω)	52	62	74	47	58	70

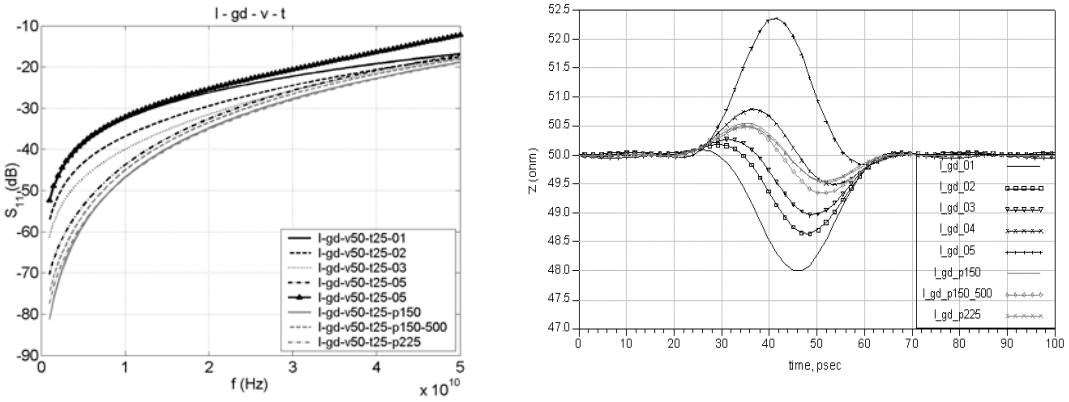
The electrical performances of the interconnections with the diameter of the vias of 100 μm had a lower performance compared to the structures with v50. The large scattering of the results made it difficult to determine any rule. The effect of large pads was evident as all the 100 μm long connections and the b_v50_t25_s500

performed as capacitance loads. The variation of the local characteristic impedance was very large, ranging from 40 Ω up to 70 Ω.

Therefore, the electrical performance of the match impedance design out performed the ones of the high density connections when large gaps had to be bridged for any thickness of the substrate. The disadvantage of the MI was the width of the line for thick substrates that used the important PWB area. The narrow line designs are well suited to the short gaps and small diameters of the vias and pads, but they come at the expense that the analysis had to be carried out for each individual structure.

5.5.3. Microstrip ground distribution and high dielectric constant materials

The influences of high dielectric materials embedded into the PWB on the signal integrity of the interconnections were studied together with the return path of the signal. To maintain the microstrip configuration, the high dielectric material layer was considered to be located under the IMB module. Utilizing this stack-up, the effects of the gaps in the ground planes were studied.



(a) Frequency domain. *(b) Time domain.*

Fig. 5.33 Frequency and time domain results of the distribution of the current return path.

The calculation results showed that the return path had an important influence on the signal integrity (Fig. 5.33.a). The reference model performed as a capacitive load as there were no gaps in the reference plane. Splitting the ground layers caused the characteristics of the connections to change to series LC type circuits (Fig. 5.33.b). The augment of the inductance of the assembly had two causes: the increased

thickness of the substrates and the size of the current return loops. The best results were achieved when the current return vias were situated under the signal lines, close to the edges of the gap on both sides (components and PWB) and close to the ports, which minimized the return currents loops (gd_02, gd_03 and gd_04) (Table 5.7). Moreover, the use of a small pitch ground connection did not improve the signal integrity (gd_02). The return currents utilized more vias to close the circuits - especially at lower frequencies – and that increased the parasitics of the assemblies. Furthermore, the electrical parameters deteriorated considerably when the return current vias were positioned at 500 μm away from the interconnection. The inductance of the loop created by the return currents reduced the bandwidth of the interconnection to 42 GHz and increased the return losses up to 52 dB (Table 5.7). In conclusion, utilizing a large number of ground connections did not improve the SI. Careful placement, however, was required to reduce the current loops of the return currents.

Table 5.7 Electrical characteristics of the ground distribution vias.

	1	50	15 dB	Z(Ω)	
Connection	GHz	GHz	GHz	max	min
gd_01	52	17			48
gd_02	58	18		50.2	46.8
gd_03	60	18		50.3	49
gd_04	70	19		50.8	49.5
gd_05	52	11	42	52.4	49.8

The results from the analysis of the ground distribution showed an improvement in the electrical characteristics of the interconnections when the ground connections were situated very close to the edge of the components and PWBs and when the vias were positioned very close to the ports. Consequently, a new design was investigated. This employed two pitches for the ground connection vias. First of all, a small pitch was utilized at the boundary between the PWBs and the components that had a double role. They reduced the EMI to and from the components and reduced the loop of the return currents around the gap. Secondly, the pitch for the ground distribution to the components was larger and aimed to create a good grid of the ground network.

The pitch of the guard connections was determined utilizing the λ/20 rule used to reduce the radiated emissions of the modules. The simulation results indicated that when the guarding and ground distribution pitches were the same 150 μm and 225 μm, the assemblies showed good electrical performance. This suggests similar electrical performance. Augmenting the pitch of the ground distribution vias to 225 μm and 500 μm caused the electrical performances of the assemblies to be influenced by L and C parasitics (Table 5.8). It was noted that the results were influenced by the position of the vias with regard to the signal lines and ports. When no return path via was considered in the model except the guard ones, the interconnection performed as an L load (gd_p150_p500) as the return current closed utilizing the closed boundary of the model. Placing the return via at about 225 μm away from the signal, the low frequency losses improved and the high frequency performances were similar to the ideal situation where the vias were situated close to the driver and receiver (ports).

The influences of high dielectric constant materials were studied utilizing two of the models previously developed: gd_p150_p500 and gd_p150_p500_1. The calculation results showed that the differences between them were small for values of the dielectric constant larger than 10 (Fig. 5.34). For the purpose of simplification, the results presented here were for the gd_p150_p500 models (Table 5.9). The low frequency losses were smaller than 52 dB for all connections. The assemblies having the gaps of 100 μm, performed as capacitive loads for all the materials. With increases in the width of the gaps, the loops of the current return augmented, increasing the values of parasitic inductance. As a result, the connections performed as LC loads.

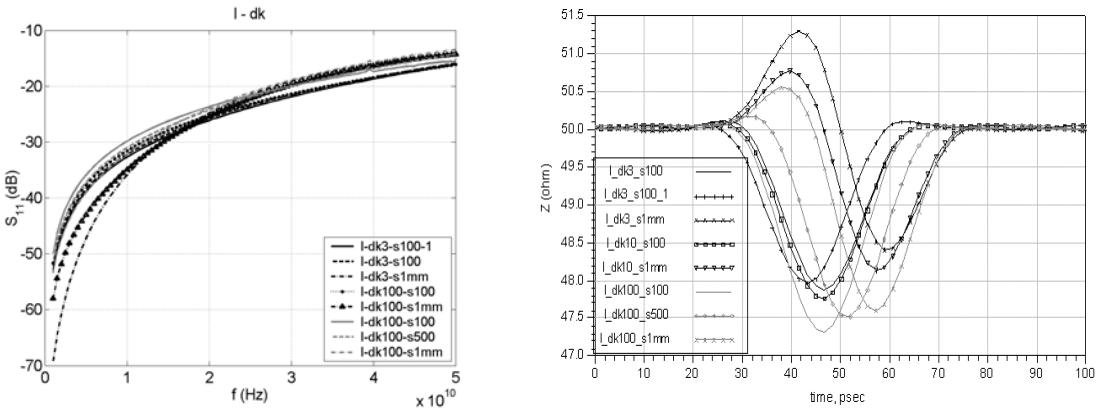
Table 5.8 Electrical characteristics of the 2 pitch ground distribution vias for the EMI.

	1	50	15 dB	$Z_0(\Omega)$	
	GHz	GHz	(GHz)	max	min
gd_p150	80	20		50.5	49.5
gd_p150_p225	68	21		50.6	49.75
gd_p150_p500	59	22		50.8	
gd_p150_p500_1	67	18		50.45	49.1
gd_p150_p500_2	74	19		50.5	49.35
gd_p225	80	20		50.5	49.55
gd_p225_1	80	20		50.5	49.55

Table 5.9 Electrical characteristics of the IMB interconnections with high ε_r materials.

	1	50	15 dB	Z_0 (Ω)	
	GHz	GHz	(GHz)	max	min
dk3_s100	52	17			48
dk3_s500	59	16		50.5	48.5
dk3_s1mm	70	15		51.3	48.5
dk10_s100	52	16			47.5
dk10_s500	54	15		50.3	48
dk10_s1mm	58	14	45	50.8	48.2
dk100_s100	50	15			47.3
dk100_s500	52	14	48	50.2	47.5
dk100_s1mm	53	13	45	50.6	47.7

The dk3_s1mm had the highest inductance that increased the local impedance to 51.3 Ω. Better results were obtained for the dk10_s1mm and dk100_s1mm as the high ε_r, helped to diminish the variation of local impedances as the capacitance of the line increased. The time domain analysis therefore supports the transmission line theory showing that the capacitance of the interconnections increased with the dielectric constant of the additional material. The local impedances of the dk100 interconnections were smaller by about 0.5 Ω when compared to the dk10, and by about 1 Ω when compared to the dk3. With the increase of the dielectric constant, the differences between the electrical parameters of the 500 μm and 1mm long interconnections became smaller. Nevertheless, the presence of high ε_r materials on long circuits decreased the high frequency performances as the electrical length of the circuit was larger. The bandwidths of the dk10_s1mm, dk100_s500 and dk100_s1mm were limited to about 45 GHz by the 15 dB level.



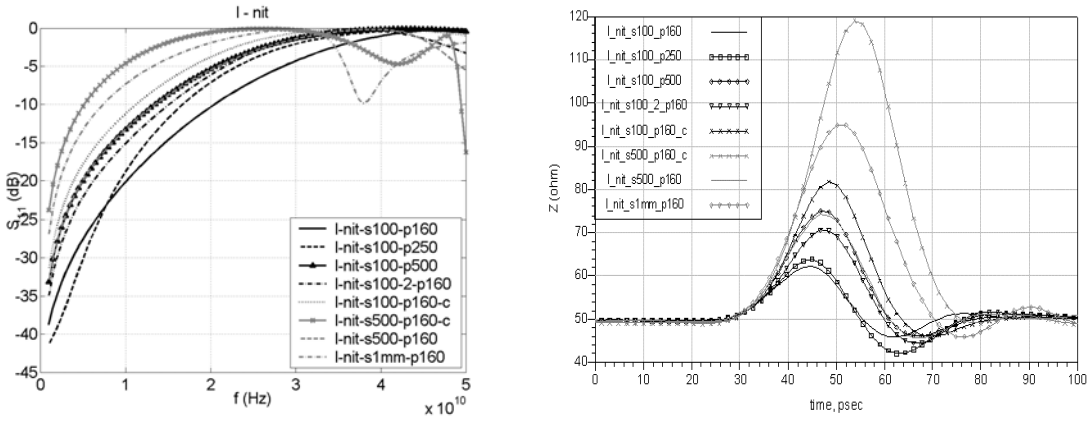
(a) Frequency domain. *(b) Time domain.*

Fig. 5.34 Frequency and time domain analysis of the IMB interconnections with high ε_r materials.

The use of higher dielectric materials inside the carrier boards affected the signal integrity. This research showed that the width of the gaps had a minor influence on the electrical parameters of the interconnections when high dielectric materials were present. Increases in the value of the dielectric constant resulted in an increase of the electrical length that limited the bandwidth of long interconnections. The time domain analysis showed that the structures performed like LC loads having variations of up to 2.5 Ω.

5.5.4. Microstrip connection to the Si chip

The interconnections to the Si components required special consideration as the reference planes of the PWBs and the components were interconnected utilizing two bridge type connections. The substrate between the line and reference plane on the component was 10 μm thick Si_3N_4. Therefore, additional capacitance was added to the connection as a result of the large step between the microstrip line and the pad on the Si components. The variables of the analysis were: the pitch of the pads, the width of the gap and the routing solutions for the current return path.



(a) Frequency domain. *(b) Time domain.*

Fig. 5.35 Frequency and time domain results of the IMB connections to Si components.

The simulation results showed that the pitch of the pads had an important effect on the electrical properties of the interconnections (Fig. 5.35.a). It influenced the size of the signal loop over the split in reference plane that affected the inductance of the connections. The connections pads also performed as capacitive loads and the interconnections begin to act like LC type discontinuities. The effects of the pads'

pitch on the electrical performance of the connections were analyzed for an assembly space of 100 μm. The interconnections having the pitch of 160 μm showed the best performance (Table 5.10). The increase of the pitch by 90 μm from 160 μm to 250 μm resulted in a decrease of the bandwidth of the interconnection with frequencies from 2 GHz to 13 GHz. In fact, these interconnections showed the smallest parasitic inductance, as the maximum of the Z_0 was about 65 Ω. The performance of connections decreased when the pitch increased to 500 μm, as the impedance increased up to 75 Ω, and the bandwidth decreased to 8.5 GHz. When one return path was assigned to two signal connections (g100_2_p160) the electrical performance of the line situated further away from the return path was poor as it had high inductance (Fig. 4.21.b). In fact, it performed as an interconnection having the pitch of 320 μm. Moreover, when the ground connection was realized utilizing the corner bump of the component and connected to the other side (Fig. 4.21.c), the electrical parameters decreased further. The extra travel distance of the current considerably increased the inductance making it the worst performer for this gap size.

The impact of the width of the gap on the electrical parameters showed that the increase of the length of the lines resulted in increased inductance of the circuits. As a result, the bandwidths of the interconnections decreased down to 4 GHz for the gap of 1 mm from 15 GHz for the 100 μm gap. The impedance loci showed that s100_p500 had similar electrical characteristics as the s500_p160 as the areas of the return currents were similar (Fig. 5.35.b). It also indicated that the path of the current return increased the length of the circuit, decreasing the bandwidth and generated impedance discontinuity.

Table 5.10 Electrical characteristics of the IMB connections to the Si components.

	1	50	15dB	f_r	Z_0	
	GHz	GHz	GHz	(GHz)	(Ω)	
g100_p160	39	0.3	15	47.5	62	46
g100_p250	37	0.3	13	46	65	47
g100_p500	33	0.5	8.5	43	75	47
g100_2_p160	35	3.3	10	37	70	44
g100_p160_c	31	0.9	6.7	38	82	46.5
g500_p160_c	24	11	3	26 & 42	120	
g500_p160	35	5.5	8.7	39	75	45
g1mm_p160	31	2	4	32 & 38	95	45

5.5.5. Stripline interconnections

High density, high functionality modules require a complex routing and more build up signal layers. The presence of reference planes on top of signal layers converts the microstrip into stripline connections. The influence of the size and shape of the pads were studied with the help of the v25_t25 vias. The simulation results showed that all the connections performed as capacitive loads. The small structures v20_t25_s and v25_t25_s had the best electrical performances having a bandwidth larger than 50 GHz and the variation of the Z_0 was smaller that 1 Ω (Table 5.11). With the increase in the size of the pads, the capacitance of the interconnections increased. The influence of the size of the pads was more significant than in the case of the microstrip. The coupling to the upper metal layer increased the capacitance of the pads. As a result, the high frequency performances of the interconnections were limited by the 15 dB level at frequencies lower than 50 GHz. When square pads were utilized, the capacitance from the discontinuity between the feed lines and pads increased the capacitance even further (Table 5.10), showing the largest reflection loss and smallest bandwidth. The situation improved when the dimensions of the square pads were reduced. This solution was helpful but still they were outperformed by the structures with round pads.

Table 5.11 Electrical performances of the IMB stripline connections.

t (μm) / v (μm)	25			
	1	50	15 dB	Z
	GHz	GHz	GHz	(Ω)
v20_t25_s	84	31		50
v25_t25_s	59	25		49
v25_t25	44.5	11.5	35	45.8
v25_t25_sq_s	45	12	33.3	45.5
v25_t25_sq	42.5	9.5	24.2	44.2
v25_t25_sq_sq_s	43.5	11	28.1	44.8
v25_t25_sq_sq	41	8.5	20.7	43.1

Table 5.12 Electrical parameters of the stripline connections with thick substrates.

v (μm) / t (μm)		25	50	100
25	1 GHz	44.5	42	37
	50 GHz	11.5	9	5.5
	15 dB (GHz)	35	22.5	13
	Z_0 (Ω)	45.8	43.8	40
50	1 GHz	49.5	43.5	38
	50 GHz	17.5	12.2	7.2
	15 dB (GHz)		29.3	14.5
	Z_0 (Ω)	47.5	45	41
100	1 GHz		41	53
	50 GHz		26	18
	f_r (GHz)		49.5	35
	Z_0 (Ω)		49	44

The increase of the substrate thickness to 50 μm improved the electrical parameters of the interconnections as the capacitance between the pads halved as compared to the 25 μm thick substrate (Table 5.12). The analysis of the structures with the diameter of the vias being 50 μm and the thickness of layer 2 being 25 μm and 50 μm, showed that the increase of the substrate thickness increased the high frequency performances. The v25_t50 interconnection had a bandwidth larger than 50 GHz and a variation in the impedance of 2.5 Ω. When the thickness of the substrate was augmented to 100 μm, the electrical dimensions became large and the structures performed as LC loads with the bandwidths of the circuits limited by the resonance frequency. Compared to the thinner substrate, the overall electrical parameters were better as the bandwidth of the v50_t100 assembly was 49.5 GHz and of the v100_t100 which was 35 GHz.

Table 5.13 Electrical parameters of the stripline connections with manufacturing errors.

t (μm) / type	25				50		
	1 GHz	50 GHz	15 dB GHz	Z (Ω)	1 GHz	50 GHz	Z (Ω)
ref	44.5	11.5	35	45.8	49.5	17.3	47.3
err1	45.1	12.1	33.2	45.6	47.7	17.3	46.8
err2	44.6	11.5	31.1	45.35	46.8	15.8	46.45
err3	43.8	11	28.5	45	46.9	16	46.5
err4	43.8	11	28.6	45	47.2	16.3	46.6
err5	44.1	11	29.1	45.05	46.6	15.5	46.35

The investigation of the influence of fabrication errors on signal quality of one net was carried out with the help of the interconnections with the diameters of the vias being 25 μm. The results showed that the manufacturing errors did not have an important impact on electrical performance (Table 5.13). The largest differences were about 1 Ω for the characteristic impedance and about 1 dB between the return losses at 1 GHz. The 50 μm drill error of in the direction of the *x*-axis improved return losses at a low frequency by 0.6 dB (err1) when compared to the reference connection. This was due to the fact that the current did not disperse through the entire lower pad. The shift of the vias in the direction of the *y*-axis decreased the bandwidth of the connections by 4 GHz as the current loop was larger. The misalignment of the pads had the largest influence on the bandwidth of the models. The shift of the upper pads (err3, err4 and err5) resulted in a decrease of the capacitance between the pads. In fact, the decrease in the capacitance value due to misalignment was small compared to that between the pads and the reference layers. For the substrate with a thickness of 50 μm the results were similar to the results obtained with the 25 μm thick substrate. In conclusion, it can be stated that the drilling errors had less influence on signal quality than misalignment of the signal layers errors.

5.5.6. The RLC parameters

The RLC circuit models of the stripline interconnections were determined with the help of the Spice model generator and fine tuned to match the results obtained with the electromagnetic simulator. The results showed that by utilizing the 5-section ladder models, the bandwidth of the connections was larger than 50 GHz. The structures built utilizing the 25 μm thick substrate had the values of the resistance at about 70 mΩ, the inductance at about 0.18 nH, and the capacitance ranged from 75 fF to 167 fF (Table 5.14). The resistance of the assemblies decreased with the increase in the diameters of the vias as the DC current had a larger path to flow. Nevertheless, the losses induced by the DC resistance were very small, and by increasing their values by up to 20 %, no major changer were noticed in the simulated S-parameters. The small structures showed the least inductance that increased with the size of the pads. The capacitance of the structures with vias with diameters of 100 μm was more than double compared to the v20_t25_s.

The comparison of the RLC parameters of the interconnections with square and round pads showed that the variations of the resistance and inductance were small. The values of the resistance ranged between 80.9 mΩ for the structure with a round pad up to 81.1 for the structure having a square and a round pad. The interconnections having both pads round had the largest inductance 185 pH while the structure having two small square pads had the smallest L of 179 pH. The smallest capacitance was about 116.5 fF for the round pads as the surface and the discontinuity between the feed line and discontinuity was small and increased up to 138.4 fF for the structure having two large square pads.

Table 5.14 The RLC parameters of the stripline connections.

Structure		R	L	C
		(Ω)	(nH)	(pF)
sl_v20_t25_s		0.079231	0.18196	0.07562
sl_v25_t25_s		0.075943	0.176501	0.081195
sl_v25_t25		0.080971	0.185114	0.116543
sl_v50_t25		0.073128	0.183875	0.129606
sl_v100_t25		0.063727	0.184356	0.167368
sl_v25_t25		0.080971	0.185114	0.116543
sl_v25_t25_err1		0.075537	0.18742	0.116431
sl_v25_t25_err2		0.080218	0.192177	0.116425
sl_v25_t25_err3		0.080563	0.186442	0.119588
sl_v25_t25_err4		0.081311	0.181851	0.117498
sl_v25_t25_err5		0.075762	0.175621	0.11403
sl_v25_t25		0.080971	0.185114	0.116543
sl_v25_t25_sq_s		0.081146	0.182355	0.118082
sl_v25_t25_sq_sq_s		0.081006	0.179394	0.120219
sl_v25_t25_sq		0.081174	0.183293	0.127642
sl_v25_t25_sq_sq		0.080991	0.180893	0.138451
sl_v50_t25		0.073128	0.183875	0.129606
sl_v50_t50		0.076744	0.216781	0.133676
sl_v50_t100		0.093255	0.299059	0.139976
sl_v_t25_line		0.03	0.075337	0.031192

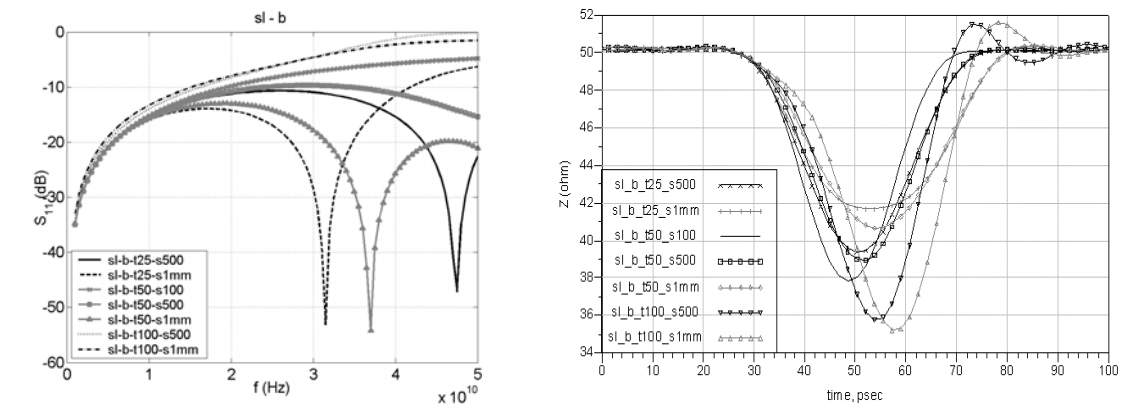
The effects of manufacturing errors resulting from misplaced drilling points on the RLC parameters of the interconnections were decreases in the resistance and increases in the inductance. The misalignment of the upper layer resulted in increased

capacitance. This was, however, larger when the error was in the direction of the *y*-axis, and smaller when the error was in the direction of the *x*-axis as the overlapping area was reduced. Nevertheless, the inductance of these interconnections was smaller compared to the one of the reference structure.

The effects of the substrate thickness on the RLC parameters were investigated with the help of the structures having the vias with diameters of 50 μm for the 25 μm, 50 μm and 100 μm thick substrates. The v50_t25 had the smallest RLC parameters while the largest were to be found for the 100 μm thick substrate. The increase in the resistance with the thickness of the substrate was about 27 % as the length of the interconnection increased by 4 times. The inductance increase was about 63 % and the capacitance only 8 % as the capacitance largely resulted from the coupling of the pads to the reference planes and from the discontinuities. The RLC parameters of the 250 μm long feed line were calculated: R –0.03 Ω, L –75 pH and C –31.1 fF. The differences between these values and the ones of the interconnections resulted from the parasitics of the pads.

The RLC study made possible to compare the IMB results with the published results. The determined RLC parameters for the IMB for stripline were in good agreement with the results published by [171 - 174] for microvias, blind and buried vias connections as the values of inductance were in the range of 0.1 – 0.4 nH and of the capacitance in the range of 0.1 – 0.2 pF. Differences were introduced by the different test set-ups. In the case of [171] there were no pads utilized, the dielectric constant of the materials was larger and sizes different. This resulted in smaller values of the capacitance as compared to the ones obtained here. The buried vias studied by [172] and [173] interconnected two signals were separated by thick dielectric layer and had larger dimensions of the pads. Nevertheless, the ratio between the area of the pads and the thickness of the separation dielectric layer were close to the ones present in this work. Maeda *et al*. confirmed the results presented in this research that most of the interconnections performed as capacitive loads by analyzing the time domain results as it was stated in this work [174].

5.5.7. Stripline bridge connections



(a) Frequency domain. *(b) Time domain.*

Fig. 5.36 Frequency and time domain simulation results of the IMB stripline connections.

The advantages of the bridge type interconnections utilizing the stripline configuration were the facile control of the impedance and the small width of the line. As a result of the good Z_0 control, all the connections showed similar return losses at low frequencies of about 35 dB (Table 5.15). The higher frequency performances were limited for all the structures by the 15 dB level even though the 500 μm and 1 mm long structures had resonant frequencies at frequencies lower than 50 GHz (Fig. 5.36). The bandwidth of the assemblies was influenced by the thickness of the substrates. For the 25 μm and 50 μm thick substrates the bandwidths were about 10.5 GHz. The increase in the thickness to 100 μm decreased the bandwidth to about 8.5 GHz.

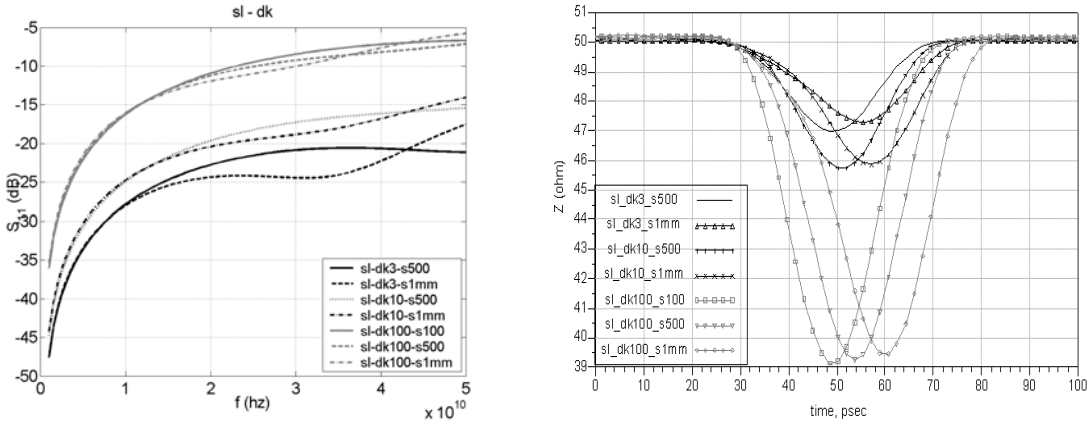
Table 5.15 Electrical performances of the stripline bridge connections.

gap / t (μm)		100 μm	500 μm	1 mm
25	1 GHz	35	35	35
	50 GHz	6.5	22	6
	f_r (GHz)		47	31.5
	15 dB (GHz)	10.5	10.5	11
	Z (Ω)	38	39	42
50	1 GHz	35	35	35
	50 GHz	5	15	21
	15 dB (GHz)	10.4	10.5	11
	Z (Ω)	38	39.5	43
100	1 GHz	34	34	33
	50 GHz	1	1	2
	15 dB (GHz)	9.2	8.8	8
	Z (Ω)	36.5 / 51	36 / 51.7	35.3 / 51.8

The results obtained were similar to the ones obtained for the microstrip bridge connections with a match impedance design; the size of the gaps did not affect the electrical performances. The combination of long circuits and thin substrates resulted in the resonance of the circuits at frequencies below 50 GHz. The time domain analysis showed that the effects of the capacitance of the pads was reduced for the longer structures which improved the characteristic impedance by about 4 Ω, increasing it up to 43 Ω as compared to the short lines.

5.5.8. Stripline with higher dielectric constant materials

With the help of the stripline configurations the effects of the presence of high dielectric layers present on top of the components on signal integrity were investigated. The results indicated that the electrical performances of the interconnections changed with the value of the dielectric constant of the additional layer. Nevertheless, no major differences, only about 1 dB, were noticed between the return losses of the interconnections having the same stack-up but different lengths as the width of the gap was increased up to 1mm.



(a) Frequency domain. *(b) Time domain.*

Fig. 5.37 Frequency and time domain results of the IMB stripline connections with high ε_r.

The increase of the dielectric constant, of the additional layer, from 3 to 100 resulted in a decrease in low frequency return losses from 47.5 dB to 35.5 dB (Fig. 5.37.a). The bandwidths of the assemblies decreased from over 50 GHz in the case of dk3 to 12 GHz in the case of dk100 (Table 5.16). The main reasons were the change of

electrical characteristics of the components and the increase of the capacitance of the pads due to the presence of the higher dielectric constant material. The time domain analysis showed that all the interconnections performed as capacitive loads and the electrical length of connections increased with the ε_r of the substrate (Fig. 5.37.b).

Table 5.16 Electrical performances of the stripline connections with high ε_r materials.

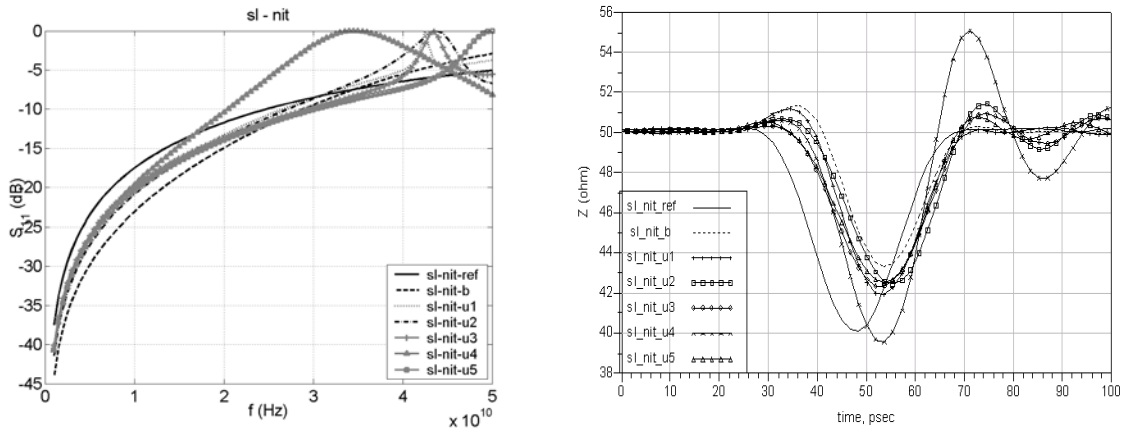
	1	50	15 dB	Z
	GHz	GHz	GHz	(Ω)
dk3_s100	48	16		46.8
dk3_s500	47.5	21		47
dk3_s1mm	47	17.5		47.5
dk10_s100	45	13.5	36	45.8
dk10_s500	44.5	15.5		45.8
dk10_s1mm	44	14	46	46
dk100_s100	36	6.5	12	39.2
dk100_s500	35.5	7	12	39.2
dk100_s1mm	35	6	12	39.4

The following pairs had similar delays introduced: dk10_s1mm and dk100_s500 and dk3_1mm, the dk10_s500 and dk100_s100. For the dk3 structures, the Z_0 of connections was around 47 Ω. When the value of the dielectric constant was increased to 10 and then to 100, the Z_0 decreased to about 46 Ω and 39.2 Ω respectively. The differences between the characteristic impedances were at maximum 0.2 Ω for the assemblies having the ε_r larger than 10 for different lengths. The reason for this was the electrical length of the circuit that was changed when high dielectric materials were added into the stack-up.

5.5.9. Stripline connection to the Si chip

The studies of the IMB stripline connections of the Si components were carried out considering different ground connection possibilities and three dimensions of the gap between the PWBs and the components. The studies were carried out utilizing the v50_t25_s100 interconnection model. When the ground was distributed to the component from the lower plane of the PWB with the help of the bridge connection, the interconnection showed the smallest return loss, 44 dB and the highest bandwidth,

20 GHz (_b) (Fig. 5.38.a). This occurred as a result of balanced LC parameters, L of the bridge line and C of the connections pads (Fig. 5.38.b). By utilizing the upper reference layer to connect the component to the ground of the model, the return losses were about 40 dB at 1 GHz and the bandwidth was about 17 GHz (Table 5.17). The changes in the assignment of the reference plane for the PWB port did not have an impact on the low frequency return losses. Moreover, the bandwidth of the connections did not changed significantly when the reference port was moved from the lower layer (u1) to the upper one (u3). When no reference port was assigned to the PCB port (u2) the bandwidth of the structure improved by about 0.8 GHz as the return current did not crowd to flow through the vias toward one plane but it dispersed on both reference layers. The location of the ground connection with regard to the signal line proved to be important. When the ground bump was positioned at 200 μm away from the signal connection, inside the component, the bandwidth decreased to 14.6 GHz and the circuit start resonating at 34.5 GHz (u4). The best performing interconnection was found to be when the ground was situated on the upper layer and the return path connection was adjacent with the signal line (u5). The size of the ground planes utilized affected the high frequency performances. The resonant frequencies present at about 43 GHz were mainly induced by the sizes of the reference planes.



(a) Frequency domain. *(b) Time domain.*

Fig. 5.38 Frequency and time domain results of the IMB stripline connection to the Si components – ground distribution.

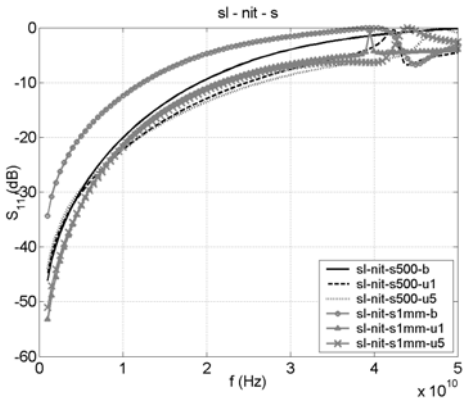
The time domain analysis showed that the interconnections performed as LCL type loads (Fig. 5.38.b). The inductance of the current path to the nearby bump increased the local impedance up to about 51 Ω in the first and the last parts of the circuits. The

transition over the gap was present as a capacitive load that decreased the Z_0 down to about 42 Ω (Table 5.17). The highest variation of the characteristic impedance was observed for the u4 model that also showed the longest flight time due to the longer current circuit. In the first phase, the current loop increased the impedance up to 55 Ω then it was decreased down to 39.8 Ω as the interconnection was affected by the component presence. The reference interconnection performed as capacitive load.

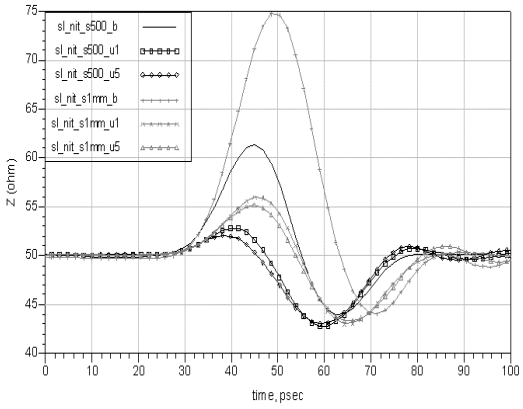
Table 5.17 Electrical results of the IMB stripline connection to the Si components – ground distribution.

	1GHz	50 GHz	15 dB	f_r	Z_0 Max	Z_0 Min
	(dB)	(dB)	(GHz)	(GHz)	(Ω)	(Ω)
ref	37.5	5	13.4			40
b	44	3	20		51.5	43.4
u1	41.5	3.9	17	42.6	51.2	42
u2	41.5	6.5	17.8	44	51.5	42.5
u3	40.5	5.5	17.2	43.5	51	42.4
u4	41	8	14.6	34.5	55	39.8
u5	40	0	18		50.8	42.6

The study of the influence of the gap width (100 μm, 500 μm and 1mm) on the signal integrity was performed with the help of three of the models previously analyzed: _b, _u1, and _u5. The results showed that, for small gaps of about 100 μm, the best solutions proved to be the bridging connections as they had the largest bandwidth; which was about 2 GHz compared to the other solutions (Table 5.18). For wider gaps, this solution was not any longer acceptable as it resulted in high return losses and the smallest bandwidth. For large gaps the best solution proved to be the delivery of the ground from the upper plane (_u5). The time domain results confirmed the results and provided a better understanding of the performances of the interconnections (Fig. 5.39 (b)). With increases in the width of the gap, the bridge connection had the highest variation of impedance that increased from 51.5 Ω to 61 Ω and then to 75 Ω for the 100 μm, 500 μm and 1mm thicknesses. The comparison of the results of the models _u1 and _u5 showed that the changes of the impedances were similar, but smaller for the one where the reference ground was the upper layer for the PCB port (_u5).



(a) Frequency domain.



(b) Time domain.

Fig. 5.39 Frequency and time domain results of the IMB stripline connection to the Si components – different gap widths.

Table 5.18 Electrical results of the IMB stripline connection to the Si components – different gap widths.

	1GHz	50 GHz	15 dB	f_r	Z Max	Z Min
	(dB)	(dB)	(GHz)	(GHz)	(Ω)	(Ω)
v50_t25_s100_b	44	3	20		51.5	43.4
v50_t25_s100_u1	41	4	17	42.5	51.2	42
v50_t25_s100_u5	40	0	18		50.8	42.6
v50_t25_s500_b	46	0	14		61	44
v50_t25_s500_u1	45	4.5	17	43	53	42.8
v50_t25_s500_u5	44	2	18	48	52	43
v50_t25_s1mm_b	34	3.5	8		75	44.2
v50_t25_s1mm_u1	53	4	15	39	56	43
v50_t25_s1mm_u5	52	9	16	39	55	43.5

5.6 Summary of results

The influences of the assembly materials (solder and underfills) and of the assembly techniques (WLCSP, FC and IMB) on signal integrity are presented. The studies were carried out utilizing three fields of expertise electronic design and material science and manufacturing. This work focused on both experimental and theoretical simulation approaches. The research was carried out utilizing the transmission line theory and close form formulas in time and frequency domains up to frequencies of 50 GHz and rise times of 20 psec [175]. In this subchapter, the main findings of this work are collected and the main findings and the design rules are highlighted.

The effect of the microstructure and oxide layers of Sn and SnAgCu solder interconnections on signal integrity were analyzed for the first time at microwave frequencies. In the case of oxide layer investigation, the measured losses of the SnO and SnAgCuO microstrip lines were compared to those of Sn and SnAgCu. At high frequencies, the skin effect forced the current to flow into the n-type semiconductor material (SnO), which increased the conductor losses by up to 40% and detuned the line by about 3 %. A design rule was developed to account for these losses utilizing the close form formulas. Utilizing the curve-fitting algorithm, a correction coefficient of 1.41 for conductor losses was determined to match perfectly the curve of SnAgCuO up to 40 GHz. The impact on technology is important as the high order harmonics of the signals are attenuated and the phase changed due to the high frequency losses and changes of the electrical parameters. This led to SI problems with high frequency signals.

The microstructure analysis was carried out by comparing the losses of the reference test boards that had the finest microstructures with the ones having different degrees of coarseness. The effect of the microstructure was analyzed by measuring the total power loss and comparing the degree of coarseness of the microstructure after different annealing times. The insertion losses of the samples annealed for 10^3 seconds were similar to the ones of the natural oxide, but the microstructure was considerably different. The samples that were annealed for the longest time showed an increase of the resistive loss of up to about 1 dB. Further verification of the results was carried out by comparing the total power loss of SnAgCu with fine microstructure to the one of Sn with coarse microstructure. The results showed that the power loss was similar. It can be concluded that the microstructure does not affect the power losses of the high frequency signals. The changes in the microstructure did not influence the electrical losses at high frequencies; the losses were a result of the oxide layer growth on the conductor surface during annealing.

The effects of the presence of three underfills and high density circuitry routed on PWB under WLCSP components on signal integrity were studied. Three underfill materials having different curing times, concentration of filler sizes and different sizes of filler particles were studied. These materials were the corner underfill, the low

viscosity underfill and the high viscosity underfill. The results were compared to those of the test boards where air was present between the component and test board. Two types of test boards were employed to replicate the effects of high density routing under the WLCSP component. The simulations were employed to analyze in detail the effect of underfills on the detuning of the circuitry on the component and of the interconnections. Two types of transmission lines, CPW and microstrip line were simulated to determine their sensitivity to the presence of underfills and metal plane when utilized for design of circuits for WLCSP assembled components.

The comparison of effects of three different underfills on the signals integrity showed that the rheology and curing parameters have an important impact on electrical characteristics of the circuit. The smallest changes in resonant frequency, about 4%, were noticed when the low viscosity material was utilized. The SEM micrograph showed that the material was nonhomogenous in z-direction and a small amount of filler particles were in close proximity to the component. The corner underfill had the second largest impact in this study, about 5.7 %. Not being a capillarity flow underfill, it strongly detuned the interconnections and the area around them. The highest impact on electrical circuit detuning was introduced by the underfill with short curing time, small size of filler particles and high concentration of filler particles, about 8.8 %. The SEM investigation showed that the high dielectric constant filler particles were homogenous and distributed in z-direction, augmenting the effective ε_r of the circuit. The simulation results of the component models with CPW lines were in good agreement with the measured results, showing changes of about 12 % of the value of resonant frequency when the underfill was present under the component. The results obtained for the microstrip line showed a dispersion of about 2.6 %. This was explained by the field propagation in the case of microstrip lines.

It can be concluded that the rheology and the curing parameters of underfill materials affect the electrical parameters of components and interconnections. The presence of a high density circuitry under the component detuned the component with by about 5 %, as it performs as an RF shield. The degree of change depends on the type and parameters of the transmission line and presence of underfills. In the case of the CPW, it is significant that the size of the slot is much smaller that the air gap, thus the fields

do not couple to the metal on the substrate below. The microstrip line circuitry was not affected by the metal presence.

The effects of new assembly techniques on signal quality were investigated with the help of the FC and IMB techniques. Special test coupons were fabricated and tested at microwave frequencies. The results of the comparison of the electrical performances of IMB and FC indicated that both assembly techniques suit microwave applications very well. The IMB technique proved to have small insertion and return losses as the disturbances of the electric field at the connection were minimized. In the case of the CPW line, it was demonstrated that the presence of the ground plane was important as the interconnections performed as an inductive load, increasing the value of local impedance by up to 10 %, due to the large return current loop.

Based on the good correlation between experimental and calculation results, the IMB analysis were extended with microstrip and stripline connections. Four interconnection possibilities were analyzed for each type of transmission line and part of the stack-ups was changed to consider the integration of the high dielectric materials and study their influence on performances of IMB connections. The circuit models with bandwidths of up 50 GHz were determined for stripline connections. The analysis was carried out in both frequency and time domains. Comparison of the performances of microstrip and stripline connections showed that the performance of the first better suited fast applications with higher bandwidth. Furthermore, it was shown that, the smaller the pads, the better the electrical performances that can be achieved, and that the round shape best suits the stripline connections. But, the bandwidth of stripline connections decreased with about 10 GHz every time the thickness of the substrate doubled its value. Investigation of the fabrication errors pointed to the fact that they can reduce the bandwidth of interconnection by up to 7 GHz by reducing the Z_0 with 1 Ω. The study of the bridge interconnections emphasized the need for a good control of the impedance of the connections. The long bridges utilizing the controlled impedance solution proved to outperform the high density solution. In the case of the stripline, the length of the bridge and thickness of dielectric layers had no significant impact on the bandwidth of connections because the impedance of the bridge line was controlled with the help of the upper ground layer. The analysis of the return currents in the microstrip line demonstrated that the

control of the path is important. Depending on the return current path, the interconnections performed as L, C or LC loads. The performances of the connections proved to be sensitive to the presence of high ε_r materials in the PWB. When the ε_r was up to 10 and the width of the separation gap was less than 1 mm, the structures performed as capacitive loads. The 1 mm long interconnection performed as LC loads. In the case of stripline connections, all the connections acted as capacitive loads. The highest detuning was encountered for ε_r 100, as the high dielectric material was present on top of the component. Interconnections to the Si components had the smallest bandwidth compared to other situations studied in this thesis. The absence of GND solid ground planes forced the return current to create large loops. The largest impact was noticed for the microstrip connections, where all connections performed as L loads. The reduction of the distance between signal and return current bump showed little impact compared to that of the size of the gap between component and PWB. In the case of striplines, the effect of planning the ground layer was also studied. When the return ground was assigned as the upper layer, the current loop was small, thus the long connections performed better than the bridge-type solution.

The studies of the assembly technologies showed that the IMB assembly performs very well at microwave frequencies. The simulated results showed very good agreement with the measured results and the results published in the literature. There are six design rules to be highlighted. Firstly, the shape and size of the pads of interconnections influence the electrical performances. Secondly, the control impedance of the lines must be utilized for the high frequency applications and the IMB interconnections showed they have this flexibility. Thirdly, the type of transmission line must be chosen according to the applications; striplines are electrically longer with smaller bandwidth but offer a very good control of the impedance of the line. The control of the impedance of a microstrip line is not so easy, but can be achieved. Fourthly, the return path is very important and must be very carefully considered, together with the ground reference in the case of striplines. Fifthly, due to current return paths, the presence of high ε_r materials in the assembly must be taken into account when analyzing the assemblies. Lastly, it is recommended that the interconnection to Si components be made utilizing the stripline and that the reference ground should be the one built-up on top of the component.

6. Summary of the thesis

In this thesis the influences of assembly materials and fabrication techniques on the signal integrity of high-speed, high density electronics has been studied experimentally and theoretically utilizing the transmission line theory and employing specially designed and fabricated test modules.

The fundamentals of signal integrity and transmission line theory are presented in Chapter 2. The emphasis was placed on the design and modeling of packages as they were no longer transparent to high frequency signals. The driving forces for the development of new assembly materials and technologies were presented together with the solutions. The availability of data concerning the influence of assembly materials and fabrication techniques on high-speed applications in the literature was limited. Good knowledge, however, was achieved from the research conducted on assemblies for microwave applications. To bridge the gap between the circuit simulation methods utilized in digital design and complex electromagnetic field calculation methods, the analysis of the electronic assemblies was carried out with the help of the transmission line theory. The transmission line theory was introduced and emphasis was placed on the signal losses and distortions due to design and fabrication processes. The modeling and measurement methods for the study of electrical performances of electronic packages were introduced.

In the Chapter 3, the design and fabrication processes of the test modules utilized to analyze the effects of oxide layers present on the surface of the bumps of hot running components, the microstructure of solders, underfills, and IMB and FC assembly techniques, on signal integrity were introduced. The experimental work was an important part of this thesis because the measurement results were utilized as references for electromagnetic simulations and theoretical calculations. The study of the effects of oxide layers and microstructure on high frequency signal integrity was carried out for the first time. A new test method was developed and specially designed and fabricated modules developed. Special WLCSP components and test boards were designed and fabricated to measure the impact of three different underfills on signal

integrity. In order to research the influences of the IMB and FC assemblies on microwave signals, two types of test boards were manufactured and assembled. Based on these results the analysis of the IMB assembly technique was extended to microstrip and stripline connections. In the last part of the chapter, the calibration methods of the vector network analyzer were presented.

In the Chapter 4 were presented the close form formulas for microstrip transmission lines utilized to determine the design rule for losses of solder connections when oxide layers were present. The design rule was developed by scientifically analyzing and calculating the conductor and dielectric losses of the microstrip line and applying curve fitting algorithm to determine the correction coefficient. The 2.5D full wave electromagnetic simulator, ADS-Mom, was employed to model the test boards utilized to measure the effects of underfill materials, and IMB and FC assembly techniques on signal quality. With its help, the analysis of the underfills effects was extended to WLCSP assemblies with microstrip lines. Thorough modeling of the IMB assemblies with two types of transmission lines, stack-ups that included high dielectric constant materials, and four connection solutions were carried out to determine the effects of discontinuities in one net, return path and ground distribution.

In the Chapter 5 the results and discussions were presented. The influence of the microstructure and oxide layers on high-speed signal propagation was studied by annealing the SnAgCu samples for different times. By utilizing the experimental, modeling and calculation information obtained from test coupons, it was demonstrated that the presence of the oxide layers on the surface of solder bumps increased the conductor losses by up to 40 % at 50 GHz. A design rule was determined that accounted for this losses. Utilizing this correction coefficient the attenuation of signals for single ended and differential signaling of WLCSP connections showed an increase of losses by about 46 % at 50 GHz. As a result, the harmonics of the signals were attenuated and their phases were shifted. As the Sn oxides performed as n-type semiconductor, the affected characteristic impedance of the connections was decreased by about 3 %, thus augmenting the reflection losses. The research showed that the degree of the coarseness of the microstructure did not have a significant effect on high frequency signal propagation losses. At high

frequencies, the current flow at the surface of the conductor was influenced by the quality of the surface.

The analysis of effects of underfills and high density PWB routing under the WLCSP components on signal integrity showed that both parameters detune the circuitry present on both the components and the interconnections of the assembly. The signal quality was affected as the reflection losses were increased due to a mismatch of the characteristic impedances; the resonant frequency of the assembly was decreased by about 11 %. The presence of the metal structure accounted for about 6 % of the changes. The capillarity flow underfill with a small filler size, a high viscosity and a short curing time had the highest impact on circuit detuning, decreasing the resonant frequency of the test structure by about 10 %. The capillarity flow material with a large filler size and a long curing time had the lowest impact as the underfill settled during the curing process leaving the low dielectric constant epoxy in the neighboring area of the circuit. The simulation results proved that the underfills and high density routing on the PWB, detuned the interconnections but did not affect the microstrip line circuitry designed on the WLCSP components.

The research into the effects of fabrication techniques on signal integrity was carried out with the help of the flip chip and the IMB. The results proved that the IMB technique is well suited to high-speed and microwave applications as it introduced small discontinuities in the signal path, the waves were propagated through the low loss materials, and had an optimized path. Thorough modeling and analysis were carried out in time and frequency domains to determine the influence of transmission line, connection discontinuities, the current return path and ground assignments on the electrical characteristics of the IMB interconnections. Results showed that the microstrip connections were best suited to fast applications as they had the largest bandwidth and smallest return losses. With the stripline connections, a facile control of the impedance of interconnections was achieved and good power and ground distribution to the Si components. The design of the current return path for the Si connections had a major effect on signal integrity.

In this thesis it was demonstrated that the assembly materials (solder connections and underfills) and fabrication (IMB, FC, WLCSP) techniques affect the signal integrity

of electronic systems by attenuation and distortion due to material losses and their dispersion with frequency and fabrication processes. Signal integrity is also affected as a result of detuning and reflection losses introduced by the assembly techniques and the design of the packages. Transmission line theory, and analysis in time and frequency domains proved to be a very powerful method to study and model the losses and reflections of high-speed signals on high-density interconnections.

References

[1] R.R. Tummala and J. Laskar, "Gigabit wireless: System-on-a-package technology," *IEEE Transactions on Component and Packaging Technology*, **92**, 2, (2004), pp. 376 – 387.

[2] R.R. Tummala, V. Sundaram, F. Liu, G. White, S. Hattacharya, R.M. Pulugurtha, M. Swaminathan, S. Dalmia, J. Laskar, N.M. Jokerst, and S. Y. Chow, "High- density packaging in 2010 and beyond," *The Proceedings of the 4th International Symposium on Electronic Materials and Packaging*, Kaohsiung, Taiwan, December 4–6 2003, IEEE, (2003), pp. 30-36.

[3] K. Boustedt, "GHz flip chip-an overview," *The* P*roceedings of the 48th IEEE Electronic Components and Technology Conference*, Seattle, Washington, May 25-28 1998, IEEE/CPMT, (1998), pp. 297-302.

[4] C.S. Chang, A. Oscilowski, and R.C. Bracken, "Future challenges in electronics packaging," *IEEE Circuit and Devices Magazine*, **14**, 2, (1998), pp. 45 – 54.

[5] International Technology Roadmap for Semiconductor, "Assembly and Packaging," (2005), 50 p.

[6] G.E. Moore, "Cramming more components onto integrated circuits," *The Proceedings of the IEEE*, **86**, 1, (1998), pp. 82 – 85.

[7] E. Bogatin, *Signal integrity – simplified*, 1st ed., New-York, 2003, Prentice Hall PTR, 608 p.

[8] W.J Dally and J.W. Poulton, *Digital system engineering,* 1st ed., Cambridge, UK, 1998, Cambridge University Press, 693 p.

[9] E. Bogatin, "Signal integrity and HDI substrates," *Circuitree Magazine,* **1**, (1999), pp. 22 – 35

[10] Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of the Use of Certain Hazardous Substances in Electronic and Electronic Equipment (*RoHS*), 27 Jan, 2003.

[11] H.W. Johnson, *High speed signal propagation: Advanced black magic*, 1st ed., New-York, 2003, Prentice Hall PTR, 766 p.

[12] H.W. Johnson and M. Graham, *High-speed digital design: A handbook of black magic*, 1st ed., New York, 1993, Prentice Hall PTR, 447 p.

[13] D. Brooks, *Signal integrity issues and printed circuit board design*, 1st ed., New York, 2003, Prentice Hall PTR, 432 p.

[14] D. Staiculescu, A. Sutono, and J. Laskar, "Wideband scalable electrical model for microwave/millimeter wave flip chip interconnects," *IEEE Transactions on Advanced Packaging*, **24**, 3, (2001), pp. 255–259.

[15] H.H.M. Ghouz and E.-B. El-Sharawy, "An accurate equivalent circuit model of flip chip and via interconnects," *IEEE Transactions on Microwave Theory and Techniques*, **44**, 12, (1996), pp. 2543 – 2554.

[16] S. Sasaki, R. Konno, H. Tomimuro, and T. Ohsaki, "3-D electromagnetic field analysis of interconnections in copper-polyimide multichip modules," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, **14**, 4, (1991), pp. 755-760.

[17] D.M. Pozar, *Microwave engineering*, 2nd ed., New-York, 1998, John Wiley and Sons Inc., 736 p.

[18] T.C. Edwards, *Foundations for microstrip design*, 1st ed., New-York, 1981, John Wiley and Sons Ltd., 280 p.

[19] A. Deutsch, "Electrical characteristics of interconnections for high-performance systems," *The Proceedings of the IEEE*, **86**, 2, (1998), pp. 315 – 357.

[20] H. Braunisch, S.N. Towle, R.D. Emery, H. Chuan, and G.J. Vandentop, "Electrical performance of bumpless build-up layer packaging," *The Proceedings of 52nd Conference on Electronic Components and Technology*, San Diego, CA, USA, 28-31 May 2002, IEEE/CPMT, (2002), pp. 353 – 358.

[21] J. Choi, S.-H. Min, J.-H. Kim, M. Swaminathan, W. Beyene, and X. Yuan, "Modeling and analysis of power distribution networks for Gigabit applications," *IEEE Transactions on Mobile Computing*, **2**, 4, (2003), pp. 299 – 313.

[22] A. Chandrasekhar, S. Brebels, S. Stoukatch, E. Beyne, W. De Raedt, and B. Nauwelaers, "The influence of packaging materials on RF performance," *Microelectronics Reliability*, **43,** (2003), pp. 351-357.

[23] R.A. Pucel, D.J. Massé, and C.P. Hartwig, "Losses in microstrip," *IEEE Transactions on Microwave Theory and Techniques*, **16**, 6, (1968), pp. 342-350.

[24] H. Sobol, “A review of the technological and electromagnetic limitations of hybrid circuits for microwave applications,” *IEEE Transactions on Parts, Hybrids, and Packaging*, **8**, 2, (1972), pp. 59 – 66.

[25] E.J. Denlinger, “Losses of microstrip lines,” *IEEE Transactions on Microwave Theory and Techniques*, **28**, 6, (1980), pp. 513-522.

[26] R.A. Konetzki, “Oxidation kinetics of Pb-Sn alloys,” *Journal of Material Research Society*, **4**, 6, (1989), pp. 1421-1425.

[27] P. Kofstadt, *Nonstoichiometry, Diffusion and electrical conductivity in binary metal oxides*, 1st ed., New-York, 1972, John Wiley and Sons Ltd, 355 p.

[28] O. Kubaschewski and B.E. Hopkins, *Oxidation of metals and alloys*, 1st ed., London, 1967, Butterworth and Co., 259 p.

[29] H. Sobol, “Applications of integrated circuit technology to microwave frequencies,” *The Proceedings of IEEE*, **59**, 8, (1971), pp. 1200-1211.

[30] D. Staiculescu, J. Laskar, J. Mendelsohn, E. Sweetman, D. Rudy, and I. Artaki, “Ni-Au surface finish effects on RF performance,” *The Proceedings of IEEE MTT-S International Microwave Symposium Digest*, Anaheim, CA, USA, IEEE/MTT-S, **4**, (1999), pp. 1909 – 1912.

[31] H.J. Finlay, R.H. Jansen, J.A. Jenkins, and I.G. Eddison, “Accurate characterization and modeling of transmission lines for GaAs MMICs,” *IEEE Transactions on Microwave Theory and Techniques*, **36**, 6, (1988), pp. 961 – 967.

[32] A.F.J. Baggerman, J.F.J.M. Caers, J.J. Wondergem, and A.G. Wagemans, “Low-cost flip-chip on board,” *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, **19**, 4, (1996), pp. 736 – 746.

[33] Z. Feng, W. Zhang, B. Su, K.C. Gupta, and Y.C. Lee, “RF and mechanical characterization of flip chip interconnects in CPW circuits with underfill,” *IEEE Transactions on Microwave Theory and Techniques*, **46**, 12, (1998), pp. 2269 – 2275.

[34] C. Brosseau, “Generalized effective medium theory and dielectric relaxation in particle-filled polymeric resins,” *Journal of Applied Physics*, **91**, 5, (2001), pp. 3197 – 3204.

[35] H. Kusamitsu, Y. Morishita, K. Maruhasi, M. Ito, and K. Ohata, ” The flip-chip bump interconnection for millimeter-wave GaAs MMIC,” *IEEE Transactions on Electronics Packaging Manufacturing,* **22**, 1, (1999), pp. 23 – 28.

[36] K. Onodera, T. Ishii, S. Aoyama, S. Sugitani, and M. Tokumitsu, ”Novel flip-chip bonding technology for W-band interconnections using alternate lead-free solder bumps,” *IEEE Microwave and Wireless Components Letters*, **12**, 10, (2002), pp. 372 – 374.

[37] J. Zhao and Q.-L. Chen, “A new methodology for simultaneous switching noise simulation,” *The Proceedings of IEEE Conference on Electrical Performance of Electronic Packaging*, Scottsdale, AZ, USA, October 23-25 2000, IEEE/CPMT, (2000), pp.155 – 158.

[38] G.R. Traut, “Clad laminates of PTFE composites for microwave antennas,” *Microwave journal*, **23**, (1980), pp. 47 – 54.

[39] J.H.C. van Heuven and T.H.A.M. Vlek, “Anisotropy in alumina substrates for microstrip circuits,” *IEEE Microwave Transactions on Microwave Theory and Techniques*, **20**, 11, (1972), pp. 775 – 777.

[40] B.J. Toleno and J. Schneider, “Processing and reliability of corner bonded CSPs,” *The Proceedings of 28th International Electronics Manufacturing Technology Symposium*, San Jose, CA, USA, July 16-18 2003, IEEE/CPMT/SEMI, (2003), pp. 299 – 304.

[41] M. Mantysalo and E.O. Ristolainen, “Modeling and analyzing vertical interconnections,” *IEEE Transactions on Advanced Packaging*, **29**, 2, (2006), pp. 335 – 342.

[42] K. Yoshida, T. Shirasaki, S. Matsuzono, and C. Makihara, “50 GHz broadband SMT package for microwave applications,” *The Proceedings of 51st Electronic Components and Technology Conference*, Orlando, FL, USA, May 29 – June 01 2001, IEEE/CPMT, (2001), pp. 744 – 749.

[43] W.-Y. Yip, J.-M. Jong, and V.K. Tripathi, “Electrical characterization of multi-layer BGA packages for high-speed, high switching activity applications,” *IEEE 5th Topical Meeting Electrical Performance of Electronic Packaging*, Napa, CA, USA, October 28-30 1996, IEEE, (1996), pp.114 – 116.

[44] H. Liang, J. Laskar, M. Hyslop, and R. Panicker, “Development of a 36 GHz millimeter-wave BGA package,” *The Proceedings of IEEE MTT-S International Microwave Symposium*, Boston, MA, USA, June 11-16 2000, IEEE/MTT-S, **1**, (2000), pp. 65 – 68.

[45] A. Kujala, R. Tuominen, and J.K. Kivilahti, “Solderless Interconnection and packaging technique for embedded active components,” *The Proceedings of 49th*

Electronic Components and Technology Conference, San Diego, CA, USA, June 1-4 1999, IEEE/CPMT, (1999), pp. 155 – 159.

[46] R. Tuominen and J.K. Kivilahti ”A novel IMB technology for integrating active and passive components,” *The Proceedings of 4th International Conference on Adhesive Joining and Coating Technology*, Espoo, Finland, June 18-21 2000, Helsinki University of Technology, (2000), pp. 269 – 273.

[47] P. Palm, R. Tuominen, and A. Kivikero, “Integrated module board (IMB), an advanced manufacturing technology for embeding active components inside organic substrate,” *The Proceedings of 53rd Electronic Components and Technology Conference*, Las Vegas, NV, USA, June 2-4 2004, IEEE/CPMT, (2004), pp. 1227 – 1231.

[48] T.F Waris, R. Saha, and J.K. Kivilahti, "Manufacturing and reliability of flexible integrated module boards,” *The Proceedings of 2nd International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics,* Zalaegerszeg, Hungary, June 23-26 2002, Budapest University/IEEE, (2002), pp. 73 – 78.

[49] M.I. Montrose, “Overview on design techniques for printed circuit board layout used in high technology products,” *The Proceedings of Symposium on Electromagnetic Compatibility*, Cherry Hill, NJ, USA, August 12-16 1991, IEEE, (1991), pp. 61 – 66.

[50] A. Deutsch, G.V. Kopcsay, P.W. Coteus, C.W. Surovic, P. Dahlenz, D.L. Heckmann, and D.W. Duan, “Bandwidth prediction for high-performance interconnections,” *The Proceedings of 50th Electronic Components and Technology Conference*, Las Vegas, NV, USA, May 21-24 2000, IEEE/CPMT, (2000), pp. 256 – 266.

[51] L. Ritchey, *Right the first time, a practical handbook on high speed PCB and system design*, CA, USA, 2003, Speeding Edge, 288 p.

[52] S. Gong, H. Hentzell, S.-T.Persson, H. Hesselborn, , B. Lofstedt, and M. Hansen, “Packaging impact on switching noise in high-speed digital systems,” *The Proceedings of IEEE Circuits, Devices and Systems,* **145**, 6, (1998), pp. 446 – 452.

[53] J.P. Schoellkopf, “Impact of interconnect performances on circuit design,” *The Proceedings of IEEE 1998 International Interconnect Technology Conference*, San Francisco, CA, USA, June 1-3 1998, IEEE, (1998), pp. 53 – 55.

[54] W. Minchuan, A. Langari, and H. Hashemi, "Advanced packaging for GHz switching applications," *The Proceedings of 52nd Conference on Electronic Components and Technology*, San Diego, CA, USA, May 28-31 2002, IEEE/CPMT, (2002), pp. 634 – 640.

[55] H. Liang, H.L. Barnes, J. Laskar, and D. Estreich, "Application of digital PGA technology to K-band microcircuit and microwave subsystem packages," *IEEE Transactions on Microwave Theory and Techniques*, **48**, 12, (2000), pp. 2644 – 2651.

[56] S. Ahn, J.-W. Lee, J. Kim, W. Ryu, Y.-S. Kim, and C.K. Yoon, "High-frequency electrical performance of a new high-density multiple line grid array (MLGA) package," *The Proceedings of 50th Electronic Components and Technology Conference*, Las Vegas, NV, USA May 21-24 2000, IEEE/CPMT, (2000), pp. 497 – 501.

[57] R.R. Tummala, M. Swaminathan, M.M. Tentzeris, J. Laskar, C. Gee-Kung, S. Sitaraman, D. Keezer, D. Guidotti, H. Zhaoran, L. Kyutae, W. Lixi, S.K. Bhattacharya, V. Sundaram, L. Fuhan, and P.M. Raj, "The SOP for miniaturized, mixed-signal computing, communication, and consumer systems of the next decade," *IEEE Transactions on Advanced Packaging*, **27**, 2, (2004), pp. 250 – 267.

[58] H. Jantunen, T. Kangasvieri, J. Vahakangas, and S. Leppavuori, "Design aspects of microwave components with LTCC technique," *Journal of the European Ceramic Society,* **23**, (2003), pp. 2541 – 2548.

[59] T.M. Schaefer, J.J. Kacines, and B.A. Randall, "A chip-first multichip module implementation of passive and active test coupons utilizing Texas Instruments' high density Interconnect technology," *IEEE Transactions on Components, Packaging and manufacturing Technology*, **19,** 2, (1996), pp. 402 – 416.

[60] T. Mangold, P. Gulde, and G. Neumann, "A multichip module integration technology on silicon substrate for high-frequency applications," *Digest of Papers Topical Meeting on Silicon Monolithic Integrated Circuits in RF System Papers,* Ann Arbor, MI, USA, September 17–18 1998, IEEE/MTT, (1998), pp. 181 – 184.

[61] V. Sundaram, F. Liu, S. Dalmia, G.E. White, and R.R. Tummala, "Process integration for low-cost system on a package (SOP) substrate," *The Proceedings*

of 51st Electronic Components and Technology Conference, Orlando, FL, USA, May 29 – June 01 2001, IEEE/CPMT, (2001), pp. 535 – 540.

[62] A. Ostmann, A. Neumann, J. Auersperg, C. Ghahremani, G. Sommer, R. Aschenbrenner, and H. Reichl, "Integration of passive and active components into build-up layers," *The Proceedings of 4th Electronics Packaging Technology Conference*, Singapore, Malaysia, December 10-12 2002, IEEE/EPTC, (2002), pp. 223 – 228.

[63] T. Mangold, J. Wolf, M. Topper, H. Reichl, and P.A Russer, " A multichip module integration technology for high-speed analog and digital applications," *The Proceedings of URSI International Symposium on Signals, Systems, and Electronics,* Pisa, Italy, September 29 - October 2 1998, URSI, (1998), pp. 91 – 96.

[64] V. Sundaram, F. Liu, S. Dalmia, J. Hobbs, E. Matoglu, M. Davis, T. Nonaka, J. Laskar, M. Swaminathan, G.E White, and R.R. Tummala, "Digital and RF integration in system-on-a-package (SOP),"*The Proceedings of 52nd Conference on Electronic Components and Technology*, San Diego, CA, USA, 28-31 May 2002, IEEE/CPMT, (2002), pp. 646 – 650.

[65] T.A. Midford, J.J. Wooldridge, and R.L. Sturdivant, "The evolution of packages for monolithic microwave and millimetre-wave circuits," *IEEE Transactions on Antennas and Propagation*, **43**, 9, (1995), pp. 983 – 991.

[66] A.S. Sedra and K.C. Smith, *Microelectronics circuits*, 4th ed. Oxford, UK, 1997, Oxford University Press, 1360 p.

[67] P.E. Fornberg, M. Kanda, C. Lasek, M. Piket-May, and S.H. Hall, "The impact of a nonideal return path on differential signal integrity," *IEEE Transactions on Electromagnetic Compatibility,* **44**, 1, (2002), pp. 11 – 15.

[68] B. Archambeault, "Proper design of intentional splits in the ground reference plane of PC boards to minimize emissions on I/O wires and cables," *The Proceedings of IEEE International Symposium on Electromagnetic Compatibility*, **2**, (1998), pp. 768 – 773.

[69] Q. Chen and J. Zhao, "Via and return path discontinuity impact on high speed digital signal quality," *The Proceedings of IEEE Conference on Electrical Performance of Electronic Packaging*, Scottsdale, AZ, USA, October 23-25 2000, IEEE/CPMT, (2000), pp. 215 – 218.

[70] E. Bogatin and G. Garat, “What you lose from a lossy line,” *EDN – Electronics Design, Strategy*, 2, (2004), pp. 49 – 56.

[71] C. Sungjun, C. Jinseong, S. Dalmia, W. Kim, and M. Swaminathan, “Capturing via effects in simultaneous switching noise simulation,” *The Proceedings of IEEE International Symposium on Electromagnetic Compatibility*, Montreal, Canada, March 13-15 2001, **2**, IEEE, (2001), pp. 1221 – 1226.

[72] W. Shi, J. Fang and M. Yin, “Inductance measurement of lead-frame packages,” *The Proceedings of IEEE 7th topical Meeting on Electrical Performance of Electronic Packaging,* October 26-28 1998, West Point, NY, USA, IEEE, (1998), pp. 50 – 53.

[73] S. Chitwood and Z. Ji, “IR drop in high-speed IC packages and PCBs,” New York, 2005, *Printed Circuit Design and Manufacture*, **4**, 2005, pp. 16 – 18.

[74] P. Heydari and M. Pedram, “Ground bounce in digital VLSI circuits,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **11**, 2, (2003), pp. 180 – 193.

[75] N. Pham, M. Cases, D. de Araujo, and E. Matoglu, “Design methodology for multiple domain power distribution systems,” *The Proceedings of 54th Electronic Components and Technology Conference*, Las Vegas, NV, USA, June 1-4 2004, IEEE/CPMT, **1**, (2004), pp. 542 – 549.

[76] J. Kane and J. Fang, “On-chip power integrity including package effects,” *SOC central*, 3, (2005), pp. 42 – 45.

[77] V. Pandit, J. Rymkiewicz, R. Davis, and R. Raughuram, “Using signal integrity analysis to achieve EMC,” New York, 2004, *Printed Circuit Design and Manufacture*, (2004), pp. 22 – 27.

[78] M.P.R. Panicker, “Microwave and millimeter wave ball grid array (BGA) packages,” *The Proceedings of IEEE 7th topical Meeting on Electrical Performance of Electronic Packaging,* West Point, NY, USA, October 26-28 1998, IEEE, (1998), pp. 233 – 236.

[79] B.C. Wadell, *Transmission line design handbook*, Boston, 1991, Artech House Publishers, 500 p.

[80] H.H.M. Ghouz and E.-B. El-Sharawy, “Finite-difference time-domain analysis of flip-chip interconnects with staggered bumps,” *IEEE Transactions on Microwave Theory and Techniques*, **44**, 6, (1996), pp. 960 – 963.

[81] J. Laskar, N. Jokerst, M. Brooke, M. Harris, C. Chun, A. Pham, H. Liang, D. Staiculescu, and S. Sutono, **"**Review of RF packaging research at Georgia Tech's PRC," *The Proceedings of 4th International Symposium on Advanced Packaging Materials*, Braselton, GA, USA, March 15-18 1998, IEEE / Advanced Packaging, (1998), pp. 139 – 150.

[82] D. Staiculescu, J. Laskar, and M. Tentzeris, "Flip chip design rule development for multiple signal and ground bump configurations," *Proceeding of Microwave Conference, Asia-Pacific,* Sydney, Australia, December 3-6 1998, IEEE/MTT-S, (1998), pp. 136 – 139.

[83] E. Hammerstad and O. Jensen, "Accurate models for microstrip computer-aided design," *1980 MTT-S International Microwave Symposium Digest*, **80**, 1, (1980), pp. 407 – 409.

[84] H.A. Wheeler, "Transmission-line properties of a strip on a dielectric sheet on a plane," *IEEE Transactions on Microwave Theory and Techniques*, **25**, 8, (1977), pp. 631 – 647.

[85] J. McGrath, "Chip/package co-design," *IEEE Advanced Packaging*, **5**, (2001), pp. 47 – 53.

[86] I. Hamadi and K. Newman, "Mixed signal design and test education for high quality packaging development," *The Proceedings of 52nd Conference on Electronic Components and Technology*, San Diego, CA, USA, May 28-31 2002, IEEE/CPMT, (2002), pp. 1524 – 1527.

[87] T. Luk and M. Hosseini, "Characterization of electrical packages via simulation and measurement," *The Proceedings of the Tenth Biennial University/Government/Industry Microelectronics Symposium*, Research Triangle Park, NC, USA, May 18-19 1993, IEEE, (1993), pp.162 – 165.

[88] T. Mangold and P. Russer, "Modeling of multichip module interconnections by the TLM method and system identification," *The Proceedings of 27th European Microwave Conference and Exhibition*, Jerusalem, Israel, September 8-12 1997, IEEE/MTT-S, (1997), pp. 538 – 543.

[89] B. Young, "Package model synthesis," *Proceeding of 12th IEEE Topical Meeting on Electrical Performance of Electronic Packaging*, Princeton, NJ, USA, October 27-29, IEEE, (2003), pp. 173 – 176.

[90] J.-G. Yook, N. I. Dib, E. Yasan, and L.P.B. Katehi, "A study of hermetic transitions for microwave packages," *IEEE Transactions on Microwave Theory and Techniques*, **3**, (1995), pp. 1579 – 1582,

[91] R.H.G. Cuny, "SPICE and IBIS modeling kits the basis for signal integrity analyses," *The Proceedings of IEEE International Symposium on Electromagnetic Compatibility*, Santa Clara, CA, USA, August 19-23 1996, IEEE, (1996), pp. 204 – 208.

[92] S.B. Bulumulla, M.F. Caggiano, D.J. Lischner, and R.K. Wolf, "A comparison of large I/O flip chip and wire bonded packages," *The Proceedings of 51st Electronic Components and Technology Conference*, Orlando, FL, USA, May 29 – June 01 2001, IEEE/CPMT, (2001), pp.1122 – 1126.

[93] G. Baumann, H. Richter, A. Baumgartner, D. Ferling, R. Heilig, D. Hollmann, H. Muller, H. Nechansky, and M. Schlechtweg, "51 GHz front-end with flip chip and wire bond interconnections from GaAs MMICs to a planar patch antenna," *The Proceedings of IEEE MTT-S International Microwave Symposium*, Orlando, FL, USA, May 16-20 1995, IEEE/MTT-S, **3**, (1995), pp. 1639 – 1642.

[94] T. Krems, W. Haydl, H. Massler, and J. Rudiger, "Millimeter-wave performance of chip interconnections using wire bonding and flip chip," *The Proceedings of IEEE MTT-S International Microwave Symposium,* San Francisco, CA, USA, June 17-21 1996, IEEE/MTT-S, **1**, (1996), pp. 247 - 250.

[95] S.J. Pan, R. Kapoor, A.Y.S. Sun, C.K. Wang, and H.G. Low, "A comparison of electrical performance between a wire bonded and a flip chip CSP package," *The Proceedings of IEEE/CPMT/SEMI 28th International Electronics Manufacturing Technology Symposium 2003*, San Jose, CA, USA, July 16-18 2003, IEEE, (2003), pp. 125 – 130.

[96] W. Heinrich, A. Jentzsch, and G. Baumann, "Millimeter-wave characteristics of flip-chip interconnects for multichip modules," *IEEE Transactions on Microwave Theory and Techniques*, **46**, 12, (1998), pp. 2264 – 2268.

[97] H.H.M. Ghouz and E.-B. El-Sharawy, "An accurate equivalent circuit model of flip chip interconnects," *The Proceedings of IEEE MTT-S International Microwave Symposium*, San Francisco, CA, USA, June 17-21 1996, IEEE/MTT-S, **3**, (1996), pp.1827 – 1830.

[98] R. Vahldieck and H. Jin, "S-parameter analysis of flip-chip transitions**,"** *The Proceedings of Electrical Performance of Electronic Packaging*, Portland, OR, USA, October 2-4 1995, IEEE, (1995), pp. 175 – 177.

[99] D. Staiculescu, H. Liang, J. Laskar, and J. Mather, "Full wave analysis and development of circuit models for flip chip interconnects," *The Proceedings of IEEE 7th topical Meeting on Electrical Performance of Electronic Packaging,* West Point, NY, USA, October 26-28 1998, IEEE, (1998), pp. 241 – 244.

[100] Y.L. Wong, L. Pattison, and D. Linton, "Flip chip interconnect analysis at millimetre wave frequencies," *The Proceedings of High frequency Postgraduate Student Colloquium*, September 12-14 1999, Leeds, UK, IEEE, (1999), pp. 82 – 87.

[101] N.-H. Huynh, W. Heinrich, K. Hirche, W. Scholz, M. Warth, and W. Ehrlinger, "Optimized flip-chip interconnect for 38 GHz thin-film microstrip multichip modules," *The Proceedings of IEEE MTT-S International Microwave Symposium*, Boston, MA, USA, June 6-11 2000, IEEE/MTT-S, **1**, (2000), pp. 69 – 72.

[102] M.-J. Yim, W. Ryu, Y.-D. Jeon, J. Lee, S. Ahn, J. Kim, and K.-W. Paik, "Microwave model of anisotropic conductive film flip-chip interconnections for high frequency applications," *IEEE Transactions on Components and Packaging Technologies*, **22**, 4, (1999), pp. 575 – 581.

[103] S. Ahn, W. Ryu, M.-J. Yim, J. Lee, Y.-D. Jeon, W. Kim, K.-W. Paik, and J. Kim, "Over 10 GHz equivalent circuit model of ACF flip-chip interconnect using Ni-filled ball and Au-coated polymer balls," *The Proceedings of 24th IEEE/CPMT Electronics Manufacturing Technology Symposium,* Austin, TX, USA, October 18-19 1999, IEEE/CPMT, (1999), pp. 421 – 425.

[104] J. Heyen, J. Schroeder, and A.F. Jacob, "Low-cost flip-chip alternatives for millimeter wave applications," *The Proceedings of IEEE MTT-S International Microwave Symposium*, Seattle, WA, USA, June 2-7 2002, IEEE/MTT-S, **3**, (2002), pp. 2205 – 2208.

[105] F. Alimenti, U. Goebel, and R. Sorrentino, "Quasi static analysis of microstrip bondwire interconnects," *The Proceedings of IEEE MTT-S International Microwave Symposium*, Orlando, FL, USA, May 16-20 1995, IEEE/MTT-S, **2**, (1995), pp. 679 – 682.

[106] A. Chandrasekhar, S. Stoukatch, S. Brebels, J. Balachandran, E. Beyne, W. De Raedt, B. Nauwelaers, and A. Poddar, "Characterization, modelling and design of bond-wire interconnects for chip-package co-design," *The Proceedings of 33rd European Microwave Conference*, Munich, Germany, October 7-9 2003, IEEE, **1**, (2003), pp. 301 – 304.

[107] R.H. Caverly, "Characteristic impedance of integrate circuit bond wires," *IEEE Transactions on Microwave Theory and Techniques*, **34**, 9, (1986), pp. 982 – 984.

[108] IPC-2141A, "Design Guide for High-Speed Controlled Impedance Circuit Boards," Association Connecting Electronics Industries, 2004, 53 p.

[109] D.C. Thompson, O. Tantot, H. Jallageas, G.E. Ponchak, M.M. Tentzeris, and J. Papapolymerou, "Characterization of liquid crystal polymer (LCP) material and transmission lines on LCP substrates from 30 to 110 GHz," *IEEE Transactions on Microwave Theory and Techniques*, **52**, 4, (2004), pp. 1343 – 1352.

[110] X. Wu, D. Cullen, G. Brist, and O. Ramahi, "Surface finish effects on high-speed signal degradation," *IEEE Transactions on Advanced Packaging,* **31**, 1, (2008), pp. 182 – 189.

[111] S. Dalmia, J.M. Hobbs, V. Sundaram, M. Swaminathan, G.E. White, R.R. Tummala, and S. Ogitani, "Characterization of thin film organic materials at high frequency," *The Proceedings of Electrical Performance of Electronic Packaging*, Cambridge, MA, USA, October 29-31 2001, IEEE/CPMT, (2001), pp. 133 – 136.

[112] R. Sturdivant, C. Quan, and J. Wooldridge, "Investigation of MMIC flip chips with sealants for improved reliability without hermeticity," *The Proceedings of IEEE MTT-S International Microwave Symposium Digest*, San Francisco, CA, USA, June 17-21 1996, IEEE MTT, **1**, (1996), pp. 239 – 242.

[113] G. Zou, H. Grönqvist, J.P. Starski, and J. Liu, "Characterization of liquid crystal polymer for high frequency system-in-a-package applications," *IEEE Transactions on Advanced Packaging,* **25**, 4, (2002), pp. 503 – 508.

[114] W.-Y. Yin and X.T. Dong, "Wide-band characterization of average power Handling Capabilities of Some Microstrip Interconnects on Polyimide and polyimide/GaAs substrates," *IEEE Transactions on Advanced Packaging,* **28**, 2, (2005), pp. 328 – 336.

[115] D.A. Rudy, J.P. Mendelsohn, and P.J. Muniz, "Measurement of RF dielectric properties with series resonant microstrip elements," *Microwave Journal*, (1998), pp. 22 – 41.

[116] J. C. Rautio, "Synthesis of lumped models from N-port scattering parameter data," *IEEE Transactions on Microwave Theory and Techniques,* **42**, 3, (1994), pp. 535 – 537.

[117] F. Ktata, U. Arz, and H. Grabinski, "Electrical characterization of S/390 MCM packages from s-parameter measurements below 3 GHz," *The Proceedings of Electrical Performance of Engineering Packaging*, San Diego, CA, USA, October 25–27 1999, IEEE, (1999), pp. 75 – 78.

[118] C.-C. Huang, "Signal integrity modeling and simulation tools," *The Proceedings of DesignCon 2004*, Santa Clara, CA, USA, February 2-5, IEC, (2004), pp. 10 – 44.

[119] C. Chun, A. Pham, J. Laskar, and B. Hutchison, "Development of microwave package models utilizing on-wafer characterization techniques," *IEEE Transactions on Microwave Theory and Techniques*, **45**, 10, (1997), pp. 1948 – 1954.

[120] E. McGibney and J. Barrett, "An overview of electrical characterization techniques and theory for IC packages and interconnects," *IEEE Transactions on Advanced Packaging*, **29**, 1, (2006), pp. 131 – 139.

[121] D.G. Swanson Jr. and W.J.R. Hoefer, *Microwave circuit modeling using electromagnetic field simulatio*n*,* Norwell, MA, USA, 2003, Artech House Publishers, 474 p.

[122] A.E. Ruehli and A.C. Cangellaris, "Progress in the methodologies for the electrical modeling of interconnects and electronic packages," *The Proceedings of IEEE*, **89**, 5, (2001), pp. 740 – 771.

[123] R. Sorrentino, *Numerical methods for passive microwave and millimeter wave structures,* 1st ed., Piscataway, NJ, USA, 1989, *IEEE Press*, 496 p.

[124] K. Kunz and R. Luebber, *The finite difference time domain method for electromagnetics*, 1st ed., USA, 1993, *CRC-Press*, 464 p.

[125] H. Shi, W. T. Beyene, S. Khalili, and C. Yuan, "Study of electrical performance of flip-chip package via designs for gigahertz applications," *The Proceedings of 15th Topical Meeting on Electrical Performance of Electronic*

Packaging, AZ, USA, October 23-25 2006, IEEE MTT, IEEECPMT, (2006), pp. 261 – 264.

[126] A.C. Polycarpou, P.A. Tirkas, and C.A. Balanis, "The finite-element method for modeling circuits and interconnects for electronic packaging," *IEEE Transactions on Microwave Theory and Techniques,* **45**, 10, (1997), pp. 1868 – 1874.

[127] Agilent Technologies, *ADS - Momentum*, 1st ed, New-York, 2000, Agilent Press, 275 p.

[128] K. Fujimoto, K. Kawashima, M. Nishitsuji, K. Nobori, H. Nagata, and O. Ishikawa, "0.4-8 GHz broadband MMICs in novel RF chip size package for optical video distribution system," *IEEE Symposium Radio Frequency Integrated Circuits,* Boston, USA, June 11-13 2000, IEEE RFIC, (2000), pp. 161–164.

[129] M.S. Sharawi and D.N. Aloi, "Design of a linearly polarized rectangular patch antenna using MoM, FDTD and FEM," *IEEE Antennas and Propagation International Symposium,* Hawaii, USA, June 3-5 2007, IEEE APIS, (2007), pp. 3916 – 3919.

[130] D.M. Pozar, S. Duffy, and N. Herscovici, "A comparison of commercial software packages for microstrip antenna analysis," *IEEE Antennas and Propagation Society International Symposium*, Utah, USA, July 16-21 2000, **1**, (2000), pp. 152 – 155.

[131] J. De Moerloose, S. Criel, R. De Smedt, E. Laermans, F. Olyslager, and D. De Zutter, "Comparison of FDTD and MoM for shielding effectiveness modelling of test enclosures," *IEEE International Symposium on Electromagnetic Compatibility,* Austin, TX, USA, 18-22 Aug 1997, IEEE, (1997), pp. 596 – 601.

[132] E. Laermans, J. De Geest, D. De Zutter, F. Olyslager, S. Sercu, and D. Morlion, "Modeling complex via hole structures," *IEEE Transactions on Advanced Packaging*, **25**, 2, (2002), pp. 206 – 214.

[133] J. Loyer, "S-parameters and digital circuit design," *EDN – Electronics Design Strategy News Magazine*, (2005), pp. 17 – 22.

[134] Y. Tu and B. Caldwell, "High-frequency termination and the SCSI bus," *Printed Circuit Design*, **3**, (2002), pp. 58 – 65.

[135] Agilent Technologies Inc., *Limitations and accuracies of time and frequency domain analysis of physical layer devices*, 1st ed., USA, 2005, Agilent, 52 p.

[136] C.-C. Huang, "Using S parameters for signal integrity analysis," *Printed Circuit Journal*, **5**, (2003), pp. 15 -22.

[137] J. Meyer, "Modeling signal integrity in electro-optical systems," *Light wave Journal*, **12**, (2002), pp. 31 - 38.

[138] C.-C. Huang, B. Chia, A. Sarfaraz, and M.J. Fox, "Extraction of accurate package models from VNA measurements," *The Proceedings of IEEE/CPMT 26th International Electronics Manufacturing Technology Symposium,* Santa Clara, CA, USA, October 2-3 2000, IEEE/CPMT, (2000), pp. 55 – 59.

[139] J.A. Andrews and S. Kabir, "Package model extraction from multi-port S-parameters," *The Proceedings of Electrical Performance of Electronic Packaging*, Cambridge, MA, USA, October 29-31 2001, IEEE/CPMT, (2001), pp. 309 – 312.

[140] I. Kelander, A.N. Arslan, L. Hyvonen, and S. Kangasmaa, "Modeling of 3D packages using EM simulators," *The Proceedings of 8th IEEE Workshop on Signal Propagation on Interconnects*, Heidelberg, Germany, May 9-12 2004, IEEE/CPMT, (2004), pp. 183 – 186.

[141] A. Chandrasekhar, E. Beyne, W. De Raedt, and B. Nauwelaers, "Distributed circuit models for near-CSP interconnects," *The Proceedings of 11th Topical Meeting on Electrical Performance of Electronic Packaging*, Monterey, CA, USA, October 21-23 2002, IEEE/CPMT, (2002), pp. 63 – 66.

[142] D.A. Smolyansky, and S.D. Corey, "Computing self and mutual capacitance and inductance using even and odd TDR measurements," *The Proceedings of 11th Topical Meeting on Electrical Performance of Electronic Packaging*, Monterey, CA, USA, October 21-23 2002, IEEE/CPMT, (2002), pp. 117 – 122.

[143] D.F. Williams, "High frequency limitations of the JEDEC 123 guideline," *The Proceedings of IEEE 7th topical Meeting on Electrical Performance of Electronic Packaging,* October 26-28 1998, West Point, NY, USA, IEEE, (1998), pp. 54 – 57.

[144] EIA/JEP 123, "Guideline for measurement of electronic package inductance and capacitance model parameters," EIA/JEDEC Electronic Industries Association, 1995, 25 p.

[145] X. Yu, "Frequency versus time domain simulation of non uniform TDR system," *The Proceedings of 35th European Microwave Conference*, Paris, France, October 4-6 2005, **2**, EUMic, (2005), pp. 135 – 139.

[146] M.-S. Zhang, Y.-S. Li, L.-P. Li, and C. Jia, "Modeling and analyzing high-speed and high-density connectors by using multisegment multiple transmission lines model," *IEEE Transactions on Advanced Packaging*, **3**, 1, (2008), pp. 203 – 210.

[147] L.C. Hammond and L.K. Virga, "Network analyzer calibration methods for high-density packaging characterization and validation of simulation models," *The Proceedings of 50th Electronic Components and Technology Conference*, Las Vegas, NV, USA, May 21-24 2000, IEEE/CPMT, (2000), pp. 519 – 525.

[148] E. Bogatin, "Insertion loss and return loss," *Printed Circuit Design and Manufacture*, **21**, (2004), pp. 48 – 50.

[149] R.D. McBride, S.G. Rosser, and R.P. Nowak, "Modeling and simulation of 12.5 Gb/s on a HyperBGA/package," *The Proceedings of 28th International Electronics Manufacturing Technology Symposium*, San Jose, CA, USA, July 16-18 2003, IEEE/CPMT/SEMI, (2003), pp. 143 – 147.

[150] R. Garg, I. Bahl, P. Bhartia, and K.C. Gupta, *Microstrip lines and slotlines*, 2nd ed., Boston, 1996, Artech House Publishers, 535 p.

[151] AN-1112, *Micro-SMD wafers level chip scale package*, National Semiconductor Corporation, 2005, 12 p.

[152] G. Tian, Y. Liu, R.W. Johnson, P. Lall, M. Palmer, M.N. Islam, and L. Crane "Corner bonding of CSPs: processing and reliability," *IEEE Transactions on Electronics Packaging Manufacturing*, **28**, 3, (2005), pp. 231 – 240.

[153] D.R. Lide, *CRC Handbook of chemistry and physics*, 74th ed., USA, 1993-1994, CRC Press Inc., 2624 p.

[154] M.G. Todd and F.G. Shi, "Molecular basis of the interphase dielectric properties of microelectronic and optoelectronic packaging materials," *IEEE Transactions on Components and Packaging Technologies*, **26**, 3, (2003), pp. 667 – 672.

[155] J. Lau, C. Chang, and R. Chen, "Effects of underfill encapsulants on the mechanical and electrical performance of a functional flip chip device," *The Proceedings of 1st IEEE International Symposium on Polymeric Electronics Packaging*, Norrkoping, Sweden, October 26-30 1997, IEEE/CPMT, (1997), pp. 265 – 272.

[156] V. Veerlan, S. Houweling, K. van der Werf, H.D. Goldbach, and R.E.I. Schropp, "Silicon nitride as dielectric medium deposited at ultra high deposition

rate (>7 nm/s) using hot-wire chemical vapor deposition," *Japanese Journal of Applied Physics,* **46**, 3B, (2007), pp. 1290 – 1294.

[157] D. Vargheese and G. J. Mohan Rao, "Electrical properties of silicon nitride films prepared by electron cyclotron resonance assisted sputter deposition," *American Vacuum Society Technology*, **19**, (2001), pp. 2122 – 2126.

[158] W.L. Goh and K.T. Tan, "The use of electroless copper seed in electrochemical deposited copper interconnect," *Thin Solid Films,* **462–463**, (2004), pp. 275–278.

[159] M. Riaziat, R. Majidi-Ahy, and I.J. Feng, "Propagation modes and dispersion characteristics of coplanar waveguides," *IEEE Transactions on Microwave Theory and Techniques*, **38**, 3, (1990), pp. 245 – 251.

[160] D. Burlacu, L.Nguyen, and J.K. Kivlahti, "Effects of the solder oxide layer on high frequency signal propagation in Pb-free interconnections," *IEEE Transactions on Advanced Packaging*, (2008), in print.

[161] M.G. Bulmer, *Principles of statistics*, 1st ed., New York, 1979, *Dover Press*, 252 p.

[162] E. Kemppinen, "Effective permittivity and attenuation coefficient of microstrip transmission line determined by 1-port and 2-port measuring methods," *Measurement Science and Technology*, **11**, (2000), pp. 38–44.

[163] P. Viswanadham and P. Singh, "Failure modes and mechanisms in electronic packaging," 1st ed., New York, 1998, Springer Technology & Industrial Arts, 608 p.

[164] S.K. Kang, W.K. Choi, M.J. Yim, and D.Y Shih, "Studies of the mechanical and electrical properties of lead-free solder joints," *Journal of Electronics Materials*, **31**, 11, 2002, pp. 1292 – 1928.

[165] K. Zeng, V. Vuorinen, and J. K. Kivilahti, "Interfacial phase formation in Sn-Ag-Cu solder joints with Ni/Au coated boards," *IEEE Transaction on Component, Packaging and Manyfacturing Technology,* **25**, 3, (2002), pp. 162-167.

[166] R.W. Jackson, "Mode conversion at discontinuities in finite-width conductor-backed coplanar waveguide," *IEEE Transactions on Microwave Theory and Techniques*, **37**, 10, (1989), pp. 1582 – 1589.

[167] Y. Liu and T. Itoh, "Leakage phenomena in multilayered conductor-backed coplanar waveguides," *IEEE Microwave and Guided Wave Letters*, **3**, 11, (1993), pp. 426 – 427.

[168] K. Darbha, J.H. Okura, and A. Dasgupta, "Impact of underfill filler particles on reliability of flip-chip interconnects," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, **21**, 2, (1998), pp. 275 – 280.

[169] R. Sturdivant, "Reducing the effects of the mounting substrate on the performance of GaAs MMIC flip chips," *IEEE Transactions on Microwave Theory and Techniques,* **3**, 5, (1995), pp. 1591–1595.

[170] D. Burlacu, T. Waris, and J.K. Kivilahti, "A comparison between the integrated active component and flip chip assemblies," *IEEE Transactions on Advanced Packaging*, (2008), in print.

[171] H.H.M. Ghouz and E.-B. El-Sharawy, "An accurate equivalent circuit model of flip chip and via interconnects," *IEEE Transactions on Microwave Theory and Techniques*, **44**, 12, (1996), pp. 2543 – 2554.

[172] I.N. Ndip, W. John, and H. Reichl, "RF/microwave modeling and comparison of buried, blind and through-hole vias," *The Proceedings of 6th Electronics Packaging Technology Conference,* Singapore, December 8-10 2004, IEEE EPTC, (2004), pp. 643 – 648.

[173] T. Swirbel, A. Naujoks, and M. Watkins, "Electrical design and simulation of high density printed circuit boards," *IEEE Transactions on Advanced Packaging*, **22**, 3, (1999), pp. 416 – 423.

[174] S. Maeda, T. Kashiwa, and I. Fukai, "Full wave analysis of propagation characteristics of a through hole using the finite-difference time-domain method," *IEEE Transactions on Microwave Theory and Techniques*, **3**, 6, (1991), pp. 1003 – 1006.

[175] B. Young, *Digital signal integrity: modeling and simulation with interconnects and packages*, 1st ed., NJ, USA, 2000, Prentice Hall PTR, 551 p.