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Fabrication of silicon based through-wafer interconnects for advanced chip scale packaging

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Abstract

This paper presents a fabrication method to achieve through-wafer interconnects (TWIs) by etching, filling and grinding in sequence. Based on this method, advanced chip scale packaging (CSP) is performed. Compared to flip-chip technology, silicon based sensors or actuators, especially large scale detector arrays, can be assembled into a system with the sensing surface upwards, and electrical signals can then be extracted from the back side of the chip without sacrificing the front sensing surface by using TWIs. In addition, it also makes 3-D chip stacking possible. Generally speaking, less than 1.5 pF capacitance and 240 Ω resistance are measured from the fabricated wafer. In order to better integrate the TWIs into different sensor systems, the ability to vary the capacitance of the TWIs is discussed based on a metal-oxide-semiconductor (MOS) model. From leakage current simulation results, possible defects during the processing of TWIs are addressed and detected by introducing different failure mechanisms of the insulation of the TWIs. As a result, the fabrication of TWIs and their related CSP procedure have proved that it is a promising technology for a range of sensor applications.

Keywords: Through-wafer interconnects (TWIs); Chip scale packaging (CSP); Metal-oxide-semiconductor (MOS); Failure mechanism

1. Introduction

Due to miniaturization and the need for edgeless packaging, advanced packaging technologies are needed to increase the number of devices, not only micro electromechanical system (MEMS) devices but also, for example, planar processed sensor arrays. The main purpose of through-wafer interconnects (TWIs) is to access signals from the back side of the device. By this method, less space is needed for interconnects on the front, active side of the chip. Also, devices can be assembled together in two dimensions without the packaging gap that is normally required by wire bonding technology. Combined with area grid array contact pads on the back side of the chip, a packaging solution demonstrates that it will satisfy the demands of modern devices.

The fabrication of TWIs includes bulk micromachining, doping, isolating, filling, grinding and chemical mechanical polishing (CMP). Different combinations of these technologies will yield different TWIs structures, which can be utilized for various applications. Anisotropic wet etching, deep reactive ion etching (DRIE)/inductively coupled plasma etching (ICP), laser micromachining [1,2], photo-assisted electrochemical etching (PAECE) are usually used to achieve high aspect ratio structures in silicon substrates. From these four methods, both anisotropic wet etching and DRIE/ICP are compatible with semiconductor processing. However, anisotropic wet etching is greatly affected by the silicon crystalline orientation, and high aspect ratio structures with vertical walls are not possible in (1 0 0) orientation silicon wafers. In order to be compatible with semiconductor processing, high aspect ratio anisotropic etching structures in silicon are commonly realized by using the patented Bosch process in DRIE/ICP [3]. To fulfill the interconnection, the use of silicon nitride as the insulation layer and electroplated metal as fillings in TWIs have been reported extensively, and the com-

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bination has been proved to be well integrated with microwave devices, RFIC devices and pMOS devices [4–6]. But from the integration point of view, it is much easier to treat the fabrication of TWIs as the front-end portion for the industrial production, and the contaminations from the processing of the TWIs will also have much less impact on the device processing. So, with the merits of high temperature compatibility and fairly low resistivity, thermal oxide and doped polycrystalline silicon are more suitable for the insulation and filling materials. The problem associated with doped polycrystalline silicon by diffusion is that it takes so many cycles to deposit, dope and anneal the thin layer of polycrystalline silicon. On the other hand, boron doped polycrystalline silicon by diffusion could result in the formation of non-conductive borosilicate glass [7]. To avoid this, in situ boron doped polycrystalline silicon is now utilized to achieve more uniform doping and reasonable resistivity [8]. Through-wafer etching is used sometimes [9] in TWIs processing, but it is difficult to control the etching depth variation, which means that vias are through in the center area but may not be through in the edge area of the wafer. Besides, etching stop techniques are usually employed in the through-wafer etching processes and usually these cause a notching effect on the exit of the via. To better control the processing, blind etching is adopted in this paper, together with grinding and polishing. In the industrial assembly, the solder bumping method is a low cost print-detach-reflow process for CSP where Sn/Pb or Sn/Ag is normally used as the solder material, and the under bump metallization (UBM) must be used to prevent diffusion of harmful alloys into the silicon substrate and increase the attachment of different metal layers. The advantage of soldering joints in CSP is that devices are not subjected to any harmful assembling forces, and positioning of the assembly is self-aligning. Both pads and bumps on the devices can be easily re-arranged in advance.

The fabrication of a test chip with an array of TWIs and contact pads is described in this paper. The assembly work is demonstrated by mounting the test chip onto an intermediate, chip sized, low temperature co-fired ceramic (LTCC) carrier, and further assembling onto an organic substrate which represents the system board of a possible future application.

Finally, electrical parameters measured from the processed wafers and demonstrated modules are reported. As one of the most important features, the control of capacitance of TWIs is discussed based on the simulation of a metal-oxide-semiconductor (MOS) model. During the simulation, the silicon substrate doping type, doping concentration and the conductive filling materials are treated as the variables. In addition, leakage current simulations are used to detect the processing defects by introducing different failure mechanisms on the insulation sidewall of the TWIs. Based on the potential failure, some processing improvements are suggested.

2. Design and fabrication

A test chip with an array of 16×16 TWIs was designed for assembly demonstration and electrical parameter measurements. The pitch of the TWIs array was 1 mm in both directions. The size of each TWI was Ø 50 μm, and the depth, also the wafer

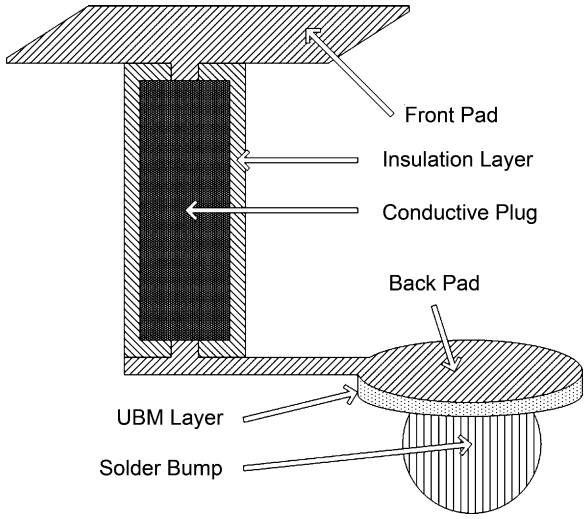


Fig. 1. Test structure design.

and device thickness, was 300 μm. In order to evaluate the TWI and relative CSP assembly, two pads were connected to each TWI. On the front side, a rectangular pad of 200 μm × 400 μm was designed for probing, and it was placed directly above the TWI. On the back side, a Ø 500 μm pad was designed for subsequent UBM and bumping, and the pad was re-arranged for easier packaging. The structure of an individual TWI after bumping can be seen in Fig. 1, where the isolation layer is silicon dioxide, the conductive plug is in situ boron doped polycrystalline silicon, the pads and wire are made of aluminum, and a thin layer between the back side pad and solder ball is the UBM layer. The size of the solder bump is estimated to be Ø 400 μm with 200 μm height. A few ohmic contact pads were also designed with the same size for contacting the silicon substrate.

During the fabrication, N type low resistivity silicon was used as the wafer substrate. The starting thickness of the wafer was 625 μm. The fabrication processing flow can be seen in

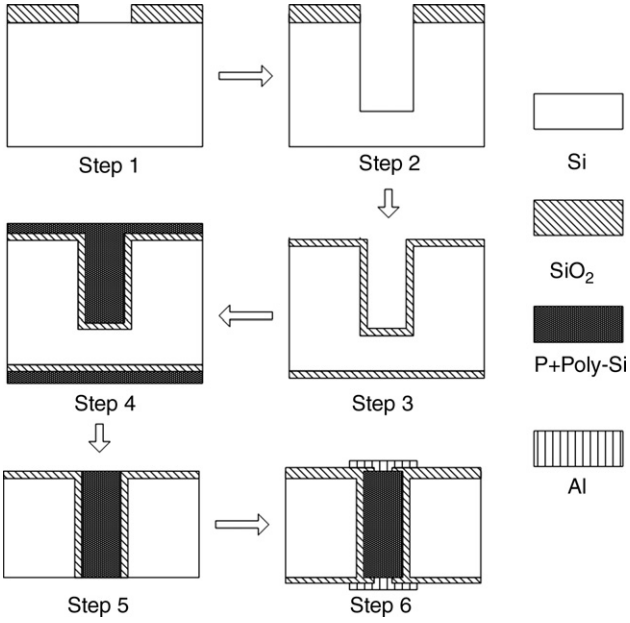


Fig. 2. Processing flow of TWIs' fabrication.

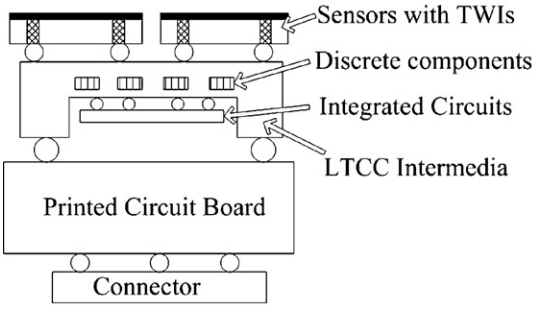
Fig. 2. The first processing step is field oxide growth to protect any potential working layer of the devices and then the low temperature oxide (LTO) is deposited to serve as a hard mask for the ICP etching. After mask patterning, the second step is the cavity etching by an STS ICP etcher using the Bosch method. The third step is thermal oxidation, so that the whole wafer surface, including the sidewalls of the etched cavities, is insulated by silicon dioxide. After insulation, the fourth step is the in situ boron doped polycrystalline silicon deposition which seals the openings of the blind cavities. Several deposition steps were used with a film thickness of 3 μm in each case. Because of the high internal stress that is built up in the polycrystalline silicon, a proper annealing procedure is necessary in the subsequent processing. The fifth step completes the TWIs. The silicon substrate is ground down to 300 μm from the back side, which makes the polycrystalline silicon plugs penetrate the whole substrate. In addition, grinding and CMP are needed as well for the front surface to remove the layer of polycrystalline silicon on top of the silicon dioxide. In the sixth step, thermal oxide is grown again. Contacts are opened on both sides of the polycrystalline silicon plugs. Aluminum is sputtered and patterned on both sides as contact pads.

For the purpose of the solder bumping, the UBM layer was processed on top of aluminum pads on the back side. The UBM layer consists of a thin sputtered seed layer and a 3 μm Ni/Au layer, which was electroplated and patterned by a lift-off technique. After dicing out the test chip from the wafer substrate, 63Sn/37Pb solder paste was printed on to the UBM pads through the apertures of a stainless steel stencil. The aperture size and stencil thickness were adjusted to attain a high bumping quality. After reflow, an area grid array of bumps was created on the back side of the chip for further assembly (Fig. 2).

3. Assembly and testing setup

A LTCC intermediate substrate and a FR-4 PCB were designed for the assembly demonstration. From considerations of the potential integration and the coefficient of thermal expansion, a test chip with a size of 2 cm × 2 cm was first attached to the LTCC intermediate substrate, which was then assembled to the PCB as a sub-module. The idea of the assembly demonstration is to show a possible solution for a highly integrated subsystem, including sensors, discrete components, interface circuits and integrated circuits. The left hand side of Fig. 3 shows a subsystem diagram of such a solution. The right hand side of Fig. 3 shows the microscopic side view of the assembled subsystem. Two sub-modules were assembled side by side on the same PCB. The gap between two sub-modules was within 50 μm. In each sub-module: the top layer of the sandwich structure is a dummy silicon chip with TWIs representing the sensor chip, the second layer is the LTCC substrate in which discrete components and integrated circuits can be embedded, the bottom layer is the PCB which has a BGA connector on its back side to provide and extract signals. There is one solder bump between each layer to make a signal path for each TWI inside the module. For large die sensor applications, as in this demonstration, underfill material is commonly used to improve the stability of the assembly. Instead of the 63Sn/37Pb solder paste, it is possible to change the bumping materials in different applications, for instance Ag/Cu, to fit the rules of hazardous substrates (RoHS) in the European Union.

In order to test the properties of the TWIs, the module was mounted onto a test bench within a probe station, having a matching counterpart for the connector of the module. An HP parameter analyzer 4156A was used for *I–V* measurement, and



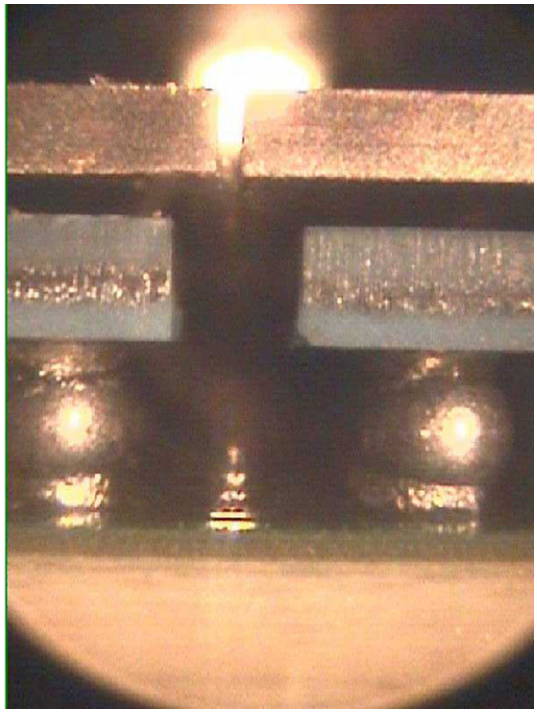


Fig. 3. Integrated subsystem diagram and demonstrated chip assembly module.

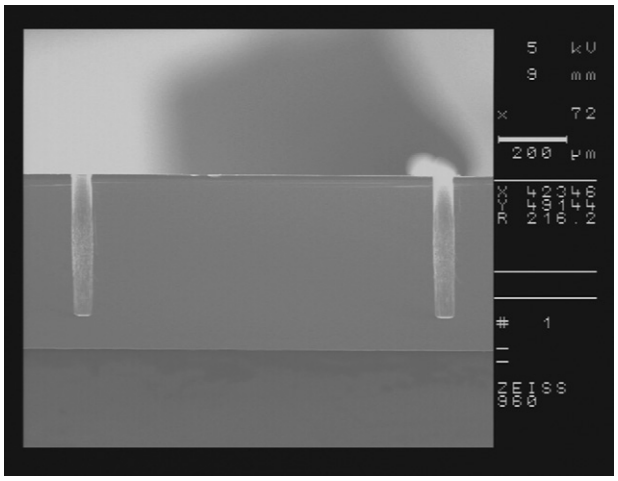


Fig. 4. ICP etching result, the etching depth is pre-set to 420 μm to guarantee that after ICP etching every cavity will reach the target depth.

a Keithley 590 CV meter was used for capacitance measurement between TWI and silicon substrate.

4. Results and discussion

4.1. Fabrication results

Fig. 4 shows a representative cross section of an ICP etched cavity. An etching speed of 3 μm/min was achieved. The etching rate is mainly limited by the ICP equipment itself. For a state-of-the-art ICP etcher, the etching rate can reach over 10 μm/min at the same feature size and density. For the in situ doped polycrystalline silicon deposition, a deposition rate of 40 nm/min was achieved in this demonstration. Fig. 5 shows the horizontal cross section of the TWI after polycrystalline silicon filling and back side grinding. The in situ doped polycrystalline silicon deposition is very conformal and sealed the cavity completely. The processing sequence of etching, filling and grinding has many advantages compared to the alternative processing sequence, which is etching, grinding and filling mentioned in [10]. No grinding particles can be trapped inside the TWIs. This improves the quality of isolating and filling.

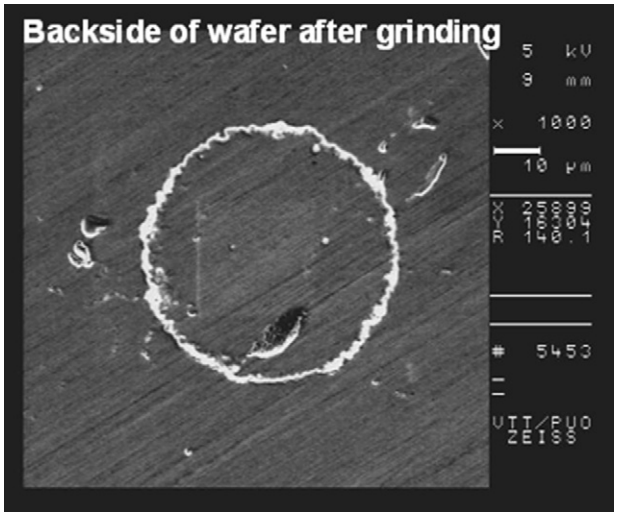


Fig. 5. Horizontal cross section of TWI after polycrystalline silicon filling.

4.2. Capacitance measurement and analysis

In order to measure the capacitance between TWI and silicon substrate more accurately, the testing was conducted at wafer level. A small testing pad was designed directly on each end of the TWI in a separate test structure. The pad size was 100 μm × 100 μm square on both sides. The capacitance, including the TWI and two contact pads, was measured from this structure. The measurement result is shown in Fig. 6 using the "+" mark line at 100 kHz frequency, while the "o" mark line is the theoretical value obtained using the capacitance analysis below with the proper assumptions and constants. The top of the curve shows the oxide capacitance, which is about 1.29 pF. The bottom of the curve shows the minimum capacitance. The shift of the curve at the bottom from theoretical value to real data is mainly because of the charges inside the oxide insulator and trapped along the interface. The shift of the curve indicates that positive charges were introduced during the processing.

The structure of the TWI is heavily doped polycrystalline silicon on a thick thermal oxide insulator combined with a silicon substrate. This structure is exactly the same as the MOS structure. So, the total capacitance of the TWI is a series combination of oxide capacitance and semiconductor depletion layer capacitance. Since the oxide capacitance is mostly defined by insulator thickness, the total capacitance can be affected greatly by depletion layer thickness in the silicon substrate. Assuming 5.05 eV is the work function ($q\phi$) for P+ doped polycrystalline silicon, 4.05 eV is the work function ($q\phi$) for N+ doped polycrystalline silicon, 4.05 eV is the electron affinity ($q\chi$) of silicon substrate, 1.12 eV is the band gap of silicon (E_g), ϕ_b is the potential difference between the Fermi level and the intrinsic Fermi level in bulk silicon. In strong inversion situations the depletion layer thickness becomes constant where the surface potential is equal to twice ϕ_b, and in accumulation situations the depletion layer thickness is zero [11]. In formula (1) and (2), the depletion width, W_{dep}, is given in terms of doping concentration and

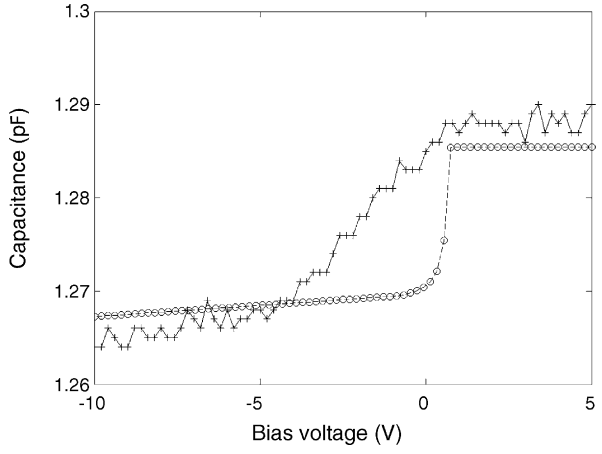


Fig. 6. Capacitance of the TWI with different bias voltages at 100 kHz frequency.

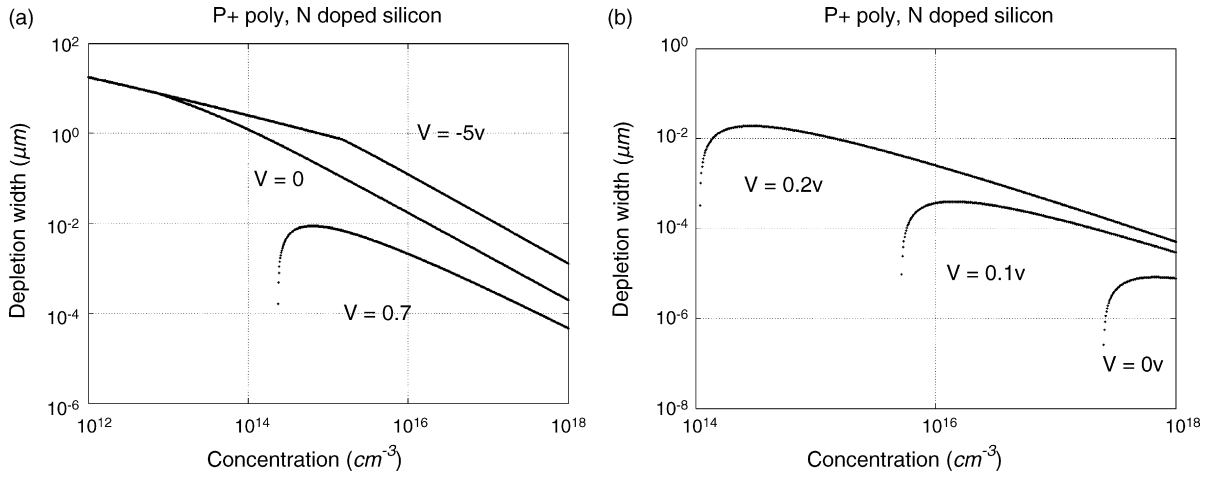


Fig. 7. (a) P+ doped polycrystalline silicon as conductive filling, depletion layer in N type silicon substrate. (b) P+ doped polycrystalline silicon as conductive filling, depletion layer in P type silicon substrate.

bias voltage, where N_a is the P type doping concentration in the silicon substrate, N_d is the N type doping concentration in the silicon substrate, ε_s is the permittivity of silicon, ε_{ox} is the permittivity of silicon dioxide, d is the thickness of the silicon dioxide layer on the side wall of the TWI. The thickness of the depletion layer is shown in Fig. 7a, b and Fig. 8a, b under different bias voltages as a function of the impurity concentration in the silicon substrate. Formula (3) shows the impacts of the depletion layer thickness on the minimum capacitance, which uses a cylindrical capacitor model for the TWI and a parallel capacitor model for contact pads, where d_1 is the thickness of the silicon dioxide layer under the contact pads, A is the contact pad area, L is the wafer thickness, R is the radius of the TWI.

$$\phi - V = \left(\chi + \frac{E_g}{2q}\right) + \phi_b - \left(\frac{qN_aW_{dep}d}{\varepsilon_{ox}}\right) - \left(\frac{qN_aW_{dep}^2}{2\varepsilon_s}\right) \quad (1)$$

$$\phi - V = \left(\chi + \frac{E_g}{2q}\right) - \phi_b + \left(\frac{qN_dW_{dep}d}{\varepsilon_{ox}}\right) + \left(\frac{qN_dW_{dep}^2}{2\varepsilon_s}\right) \quad (2)$$

$$C_{min} = \frac{\varepsilon_{ox}L}{\ln(1+d/R)+\varepsilon_{ox}\ \ln(1+W_{dep}/(R+d))/\varepsilon_s\ \ln(1+(d/R))} + \frac{\varepsilon_{ox}A}{d_1} \quad (3)$$

It turns out that different types of dopants must be used for polycrystalline silicon and for the silicon substrate respectively to reach maximum depletion width and minimum the capacitance. The lower the dopant concentration in the silicon substrate, the larger the depletion region could be, especially in small bias voltage applications.

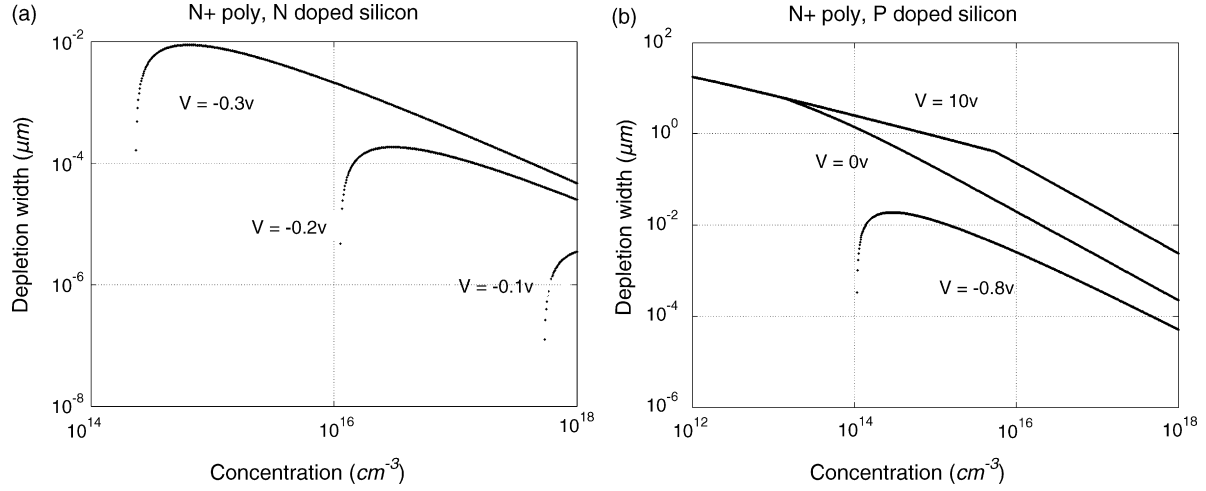


Fig. 8. (a) N+ doped polycrystalline silicon as conductive filling, depletion layer in N type silicon substrate. (b) N+ doped polycrystalline silicon as conductive filling, depletion layer in P type silicon substrate.

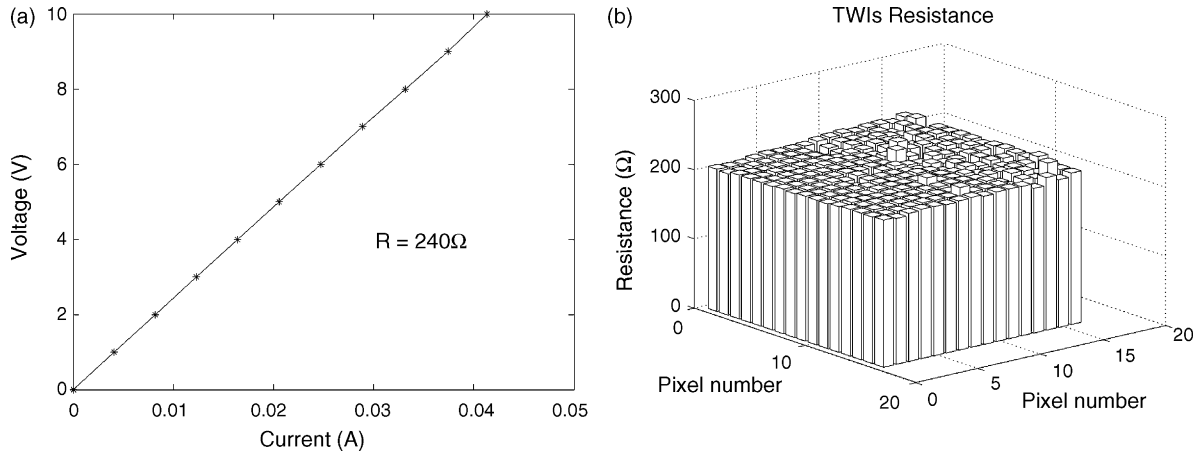


Fig. 9. (a) Individual TWI *I–V* curve characteristic. (b) Resistance distribution of TWIs array.

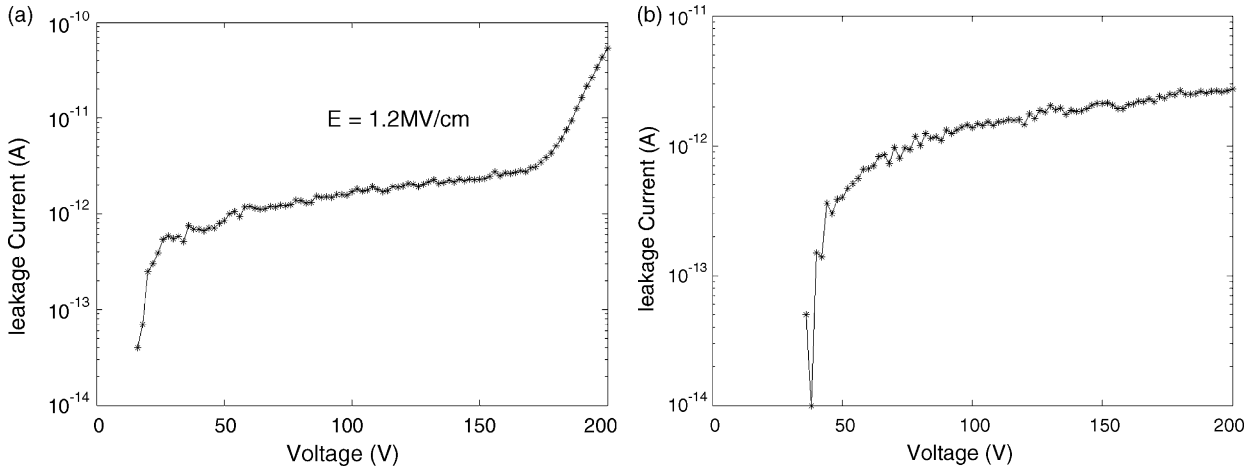


Fig. 10. (a) Leakage current from polycrystalline silicon plug to silicon substrate. (b) Leakage current between two adjacent TWIs.

4.3. Resistance measurement and analysis

Fig. 9a shows the *I–V* characteristic of an individual TWI. Resistances of TWIs in a 16 × 16 array are shown in Fig. 9b. An average resistance of 240 Ω is achieved, and the resistance variation is very small. The contact resistance of the polycrystalline silicon plug and the metal pad is around 30 Ω for each. This easily fulfils the requirements of the special application targeted by this demonstration.

By inserting geometric and resistance values into formula (4), the resistivity of in situ boron doped polycrystalline silicon in the interconnection is calculated as 0.118 Ω cm. In the formula, ρ is the resistivity of in situ boron doped polycrystalline silicon, L is the final length of the TWI, and A_1 is the cross section area of the TWI.

$$R = \frac{\rho L}{A_1} \tag{4}$$

In practice, the resistivity of in situ boron doped polycrystalline silicon is mostly affected by the annealing temperature and time [12]. Further research needs to be done to reduce the resistance for a wider range of applications.

4.4. Leakage current measurement and analysis

The voltage ramp test is commonly used for the detection of oxide breakdown. In this paper, the breakdown voltage was measured between a polycrystalline silicon plug and the silicon substrate. The result is shown in Fig. 10a, which shows that the breakdown is likely to happen at around 200 V. The corre-

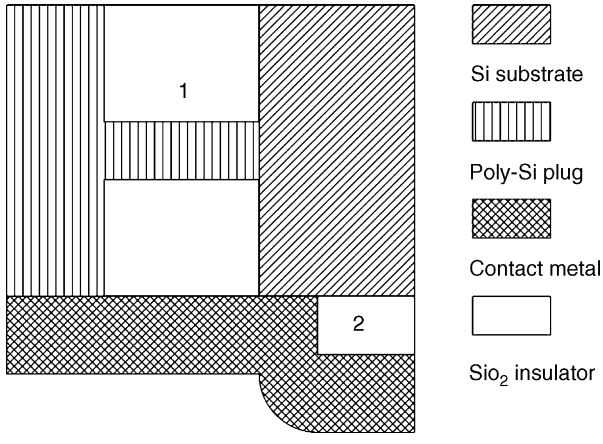


Fig. 11. Possible defect mechanisms on the sidewall of TWI.

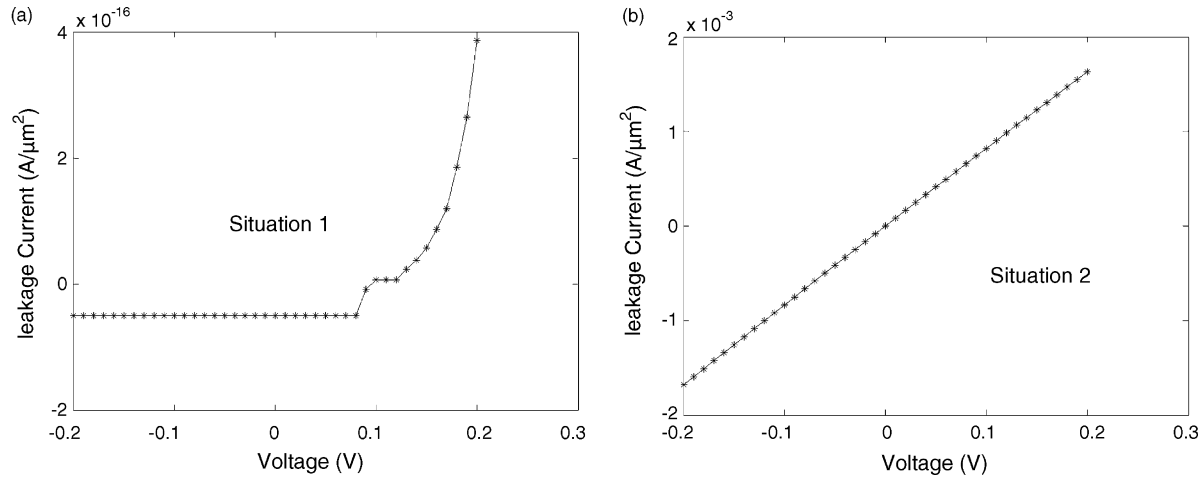


Fig. 12. (a) *I–V* simulation of defect situation 1. (b) *I–V* simulation of defect situation 2.

sponding electric field may be calculated to be about 1.2 MV/cm. Another measurement was done to assess the leakage current between two adjacent TWIs at a distance of 500 μm, and the result is shown in Fig. 10b. This indicates that there is no breakdown between two adjacent TWIs up to 200 V, which is the test limit of the equipment.

In many applications it is not possible to apply a high voltage to detect the potential leakage from the TWI itself, especially after integrating the TWI with working devices. In this paper, different structures are introduced to simulate processing defects in a TWI. Fig. 11 illustrates two situations. Situation 1 indicates that there is a pinhole on the sidewall: the leakage current could flow through directly between the polycrystalline silicon plug and the silicon substrate. Obviously a PN junction model can be used in this simulation. Situation 2 indicates that the defect is at the end of the sidewall: the leakage current could flow through by the contact metal, therefore a Schottky junction model is suitable.

Fig. 12a and b show the results for both situations based on the processing materials in this paper. It can be seen that the leakage currents behave very differently over the range of bias voltages. There is very large leakage current for situation 2 at both positive and negative bias voltage, but the leakage current is fairly small for situation 1, especially under reverse bias voltage. Situation 1, which usually happens during the ICP etching process, is called “break through” or “silicon grass”, and the subsequent oxidation is not as effective as it should be. In order to improve the quality of the TWI, a higher oxidation temperature and a longer oxidation time should be considered. Situation 2 usually happens if the contact opening for the TWI is overlapped onto the silicon substrate area, which can be due to either a big critical dimension loss on the bottom side of a blind via during the ICP etching or to back side misalignment during the backside lithography. This can be improved by better processing control. More discussions on the source of leakage current are reported in [13], which mainly concentrates on the effects of the ICP etching quality and insulator thickness. In practice, situation 1 can be made relatively unimportant to the function of the devices by choosing proper materials and working conditions, although on the other hand it may cause long-term stability problems. Situation 2 is a fatal defect in any sensor systems.

5. Conclusions

In this paper, the processing of through-wafer interconnects by an etching-filling-grinding approach has been proved to be a promising fabrication method. An advanced CSP has been demonstrated successfully by integrating TWIs with cost efficient solder bumps. Electrical parameters of TWIs have been measured at both the module level and the wafer level. The measurement data show that the TWIs have achieved a very low parasitic capacitance with a fairly high conductivity, and have a high breakdown voltage with very small leakage current. Based on the capacitance analysis, different doping types of polycrystalline plugs and silicon substrate can be chosen to be fit for different device designs. Processing improvement was also discussed according to the introduced failure mechanisms. Future efforts will aim to further improve the conductivity of the TWI in order to widen the application range.

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Biography

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