S. V. Lotkhov, A. Kemppinen, S. Kafanov, J. P. Pekola, and A. B. Zorin. 2009. Pumping properties of the hybrid single-electron transistor in dissipative environment. Applied Physics Letters, volume 95, number 11, 112507.

Pumping properties of the hybrid single-electron transistor in dissipative environment

S. V. Lotkhov,[1,a)] A. Kemppinen,[2] S. Kafanov,[3] J. P. Pekola,[3] and A. B. Zorin[1]
[1]*Physikalisch-Technische Bundesanstalt, Bundesallee 100, 38116 Braunschweig, Germany*
[2]*Centre for Metrology and Accreditation (MIKES), P.O. Box 9, 02151 Espoo, Finland*
[3]*Low Temperature Laboratory, Helsinki University of Technology, P.O. Box 3500, 02015 TKK, Finland*

(Received 20 May 2009; accepted 21 August 2009; published online 17 September 2009)

Pumping characteristics were studied of a hybrid normal-metal/superconductor single-electron transistor embedded in high-Ohmic environment. Two 3 μm long microstrip resistors of CrO_x with a sum resistance $R \approx 80$ kΩ were placed adjacent to the transistor. Substantial improvement of pumping and a reduction of the subgap leakage were observed in the low-megahertz range. At higher frequencies (0.1–1 GHz), pumping performance deteriorated compared to reference devices without resistors by the slowdown of tunneling and by electronic heating. © *2009 American Institute of Physics*. [doi:10.1063/1.3227839]

One of the paramount applications of metallic single-electron tunneling (SET) devices has been the generation and detection of very low quantized currents, $I \sim 1$ pA, for the purposes of charge metrology (see, e.g., Ref. 1). An important role is played by the fundamental trade-off between accuracy and high pumping rates, the former requiring opaque and the latter transparent tunnel barriers. Sophisticated algorithms are required for the operation of the multijunction and multigate SET pumps at a high level of accuracy. High-frequency pumping (for example, at $f \sim 1$ GHz and $I=ef \sim 160$ pA) or driving several pumps in parallel in order to produce nanoampere currents, is theoretically possible,[2] but technologically challenging.

Recently, single-gate pumping was demonstrated for very simple SET structures consisting of two ultrasmall $Al/AlO_x/Cu$ superconductor-insulator-normal metal (SIN) contacts, arranged either as NISIN (Ref. 3) or SINIS (Ref. 4) transistors. The pumping mechanism reproduces qualitatively the hold-and-pass strategy for the four-junction SET turnstile.[5] The mechanism is based on the charge hysteresis arising due to the gap Δ in the energy spectrum of the superconductor of the SIN junctions.

The pumping accuracy was analyzed in detail in Refs. 3 and 6. In particular, it was shown that for the SINIS type device with a high charging energy, $E_C \equiv e^2/2C_\Sigma > \Delta$ (C_Σ is the total capacitance of the transistor island), the lowest-order quantum leakage mechanism, the so-called Cooper-pair-electron (CPE) cotunneling, involves a coherent tunneling of three particles. This is an advantage of the hybrid device compared to, for example, a three-junction normal-state pump that is subject to two-electron cotunneling.[7] For realistic SINIS transistors with $E_C/\Delta \geq 2$ and a rectangular gate drive, the metrological accuracy of 10^{-8} is predicted for currents ~ 10 pA.[6,8] The simplicity of the device opens the possibility of on-chip integration toward higher currents.

In this letter, we address an important modification of the hybrid devices by including dissipative environment, realized as high-Ohmic on-chip microresistors. Our interest is motivated on the one hand by successful experiments on cotunneling suppression in the normal-state SET circuits.[9] On the qualitative level, similar improvements of the fundamental accuracy are expected for the hybrid devices as well. On the other hand, the electron pumping in hybrid devices often suffers from subgap leakage that is too strong to be explained by CPE cotunneling[3,4,8] and is possibly caused by structural nonidealities of the sample. This extra leakage has been described phenomenologically with a model suggested for the effect of Cooper-pair breaking.[10] Here we show that for hybrid devices, even the lowest-order model predicts an improvement in accuracy due to the implementation of the resistors. The resistors are therefore expected to suppress a broad spectrum of unwanted processes of different perturbation orders. High-order tunneling usually produces only a small contribution to the net current. Therefore we demonstrate the efficiency of the resistors by measuring the appreciable subgap onset current arising from processes of all orders.

For our experiment, we fabricated hybrid devices of four different types, with (R-SINIS and R-NISIN) and without (SINIS and NISIN) chromium resistors. We used a trilayer PMMA (polymethyl methacrylate)/Ge/copolymer mask and the shadow evaporation technique[11] for the structure of CrO_x (11 nm of Cr for the resistors, evaporated in O_2), Al (18 nm, oxidized after evaporation), and, finally, 15 nm of Cr as a counter electrode. One of the R-SINIS devices is shown in Fig. 1. The basic results of this work are demonstrated using samples fabricated in the same cycle, transistors SINIS–1,2 and R-SINIS–1, and a reference single junction SIN–1 with the following parameters (respectively): total asymptotic resistances $R_N = 140$, 195, 355, and 95 kΩ and charging ener-

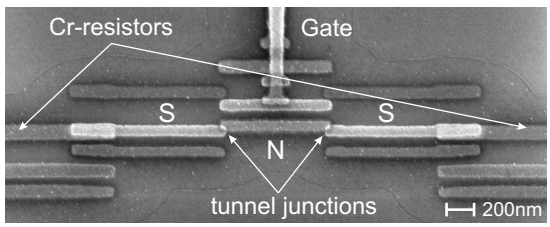

FIG. 1. Scanning electron micrograph of an R-SINIS device, fabricated through the triple-replica deposition of CrO_x, Al, and Cr (from top to bottom).

[a)]Electronic mail: sergey.lotkhov@ptb.de.

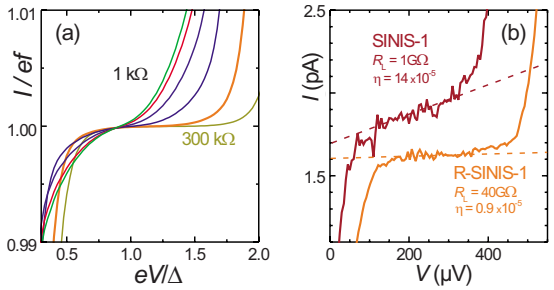

FIG. 2. (Color online) (a) Pumping plateaus calculated for different resistances $R=1,3,10,30,100,300$ kΩ and fixed $R_N=200$ kΩ, $E_C=\Delta=220$ μeV, $T=100$ mK, $f=10$ MHz, $C_gV_{g0}=0.5e$, and $C_gV_A=0.6e$, where C_g is a gate capacitance, and the open-state dc-leakage $I=5\cdot10^{-5}\times(R_N)^{-1}V$. (b) The plateaus measured under the same conditions as in (a). The plateau of the SINIS–1 device is shifted by +0.3 pA for clarity. The dashed lines show the minimum tilt along the plateau.

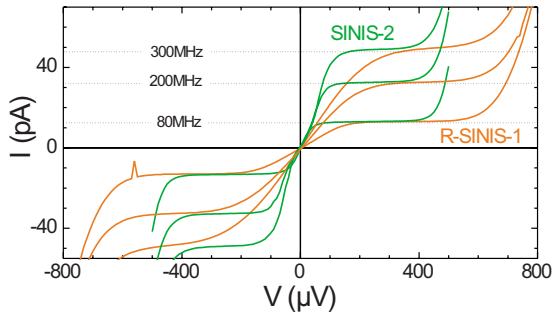

FIG. 3. (Color online) Pumping at higher frequencies. The gate sweep was optimized as in Fig. 2.

gies of the transistors $E_C=110$, 140, and ~200 μeV. The latter estimate is based on scaling the E_C of the bare transistors with the tunneling resistance ratios. The resistance of the Cr lines was $R=80$ kΩ ± 10% with a small nonlinearity observed as a zero-bias conductance dip (<50% at $T<100$ mK). The effective impedance seen by one of the identical junctions through the capacitance of the second one is $R/4$. With our choice of impedance, $R/4<R_Q\equiv h/e^2\approx25.8$ kΩ, the reduction of the single-particle tunneling rates (and, thus, that of the pumping frequency) is still moderate.[12]

We modeled the SET rates in R-SINIS devices with the $P(E)$ function formalism (see, e.g., Ref. 12), where P can be interpreted as the probability of the exchange of energy E between the SINIS transistor and its electromagnetic environment. The leakage was phenomenologically modeled by smearing the BCS (Bardeen–Cooper–Schrieffer) density of states by introducing an appropriate lifetime of quasiparticles,[10] resulting in a linear dc subgap current, $I=5\times10^{-5}\times(R_N)^{-1}V$, for the unblocked devices without resistors. For low $R=1$ kΩ, which corresponds to the resistance of the Cr island itself, the simulated leakage is almost linear and close to that of the bare transistor. However, for $R=100$ kΩ, the simulated subgap leakage is clearly nonlinear and it is suppressed by almost an order of magnitude at $eV=\Delta$.

Figure 2(a) shows the pumping plateaus at 10 MHz, calculated for the broad range of impedances R. We found that the high-Ohmic environment extends the plateau and shifts its inflection point toward higher voltages. The minimum of the slope is found at the voltages $eV/\Delta\approx0.9$ and 1.15 for $R=1$ kΩ and $R=100$ kΩ, respectively. Interestingly, the minimum of the slope appears to be at the current $I=ef$, which might help to locate the optimum operating point in practice. The lowest slope is expected for $R=100$ kΩ, about 17 times lower than for the case $R=1$ kΩ.

The experimental plateaus for the SINIS and R-SINIS devices are compared in Fig. 2(b), demonstrating the effect of the high-Ohmic environment on the quantized current plateau at a low frequency. The figure of merit can be expressed by means of the leakage parameter $\eta=R_N/R_L$, where R_L is the lowest slope along the current plateau. Adding the resistor resulted in considerable leakage suppression, corresponding to $\eta^{(\mathrm{R-SINIS})}/\eta^{(\mathrm{SINIS})}\approx16$, which is consistent with the prediction of the model, although an exact quantitative consistence of leakage magnitudes between theory and experiments would require a better understanding of leakage processes in Cr junctions, see below. Furthermore, the plateau of the R-SINIS sample extends to much higher voltages than has been observed for a bare hybrid turnstile.[3,4,8]

At higher frequencies, a noticeable slowdown of tunneling shows up for the R-SINIS devices, as compared to the devices without resistors. In the pumping I-V curves, Fig. 3, the rise to the plateau requires higher voltage, and the current versus gate-amplitude curve (not shown) demonstrates considerable backtunneling effects.[8] At the frequencies above 100 MHz, the plateau starts to deteriorate. According to our simulations, pumping in this frequency range is subject to intensive electron heating in the island. In the bare SINIS devices, pumping plateaus were observed up to the high-frequency roll-off, $f\sim1$ GHz, of our gate line.

For a more detailed insight into the subgap processes, we studied dc envelopes, Fig. 4, of both SINIS and R-SINIS devices in a wide range of R_N and E_C. The high-Ohmic environment is found to dramatically suppress the leakage while the slope of the leakage current is comparable to the tilt of the pumping plateau. In our simulations, Fig. 2(a), we apply a phenomenological leakage slope (the thin solid line in Fig. 4), which was close to the averaged envelope and provided us with a correct prediction. However, the detailed mechanism is probably more complex and includes processes beyond the lowest-order model. The dashed line in Fig. 4 shows the expectation for the bare transistor SINIS–2,

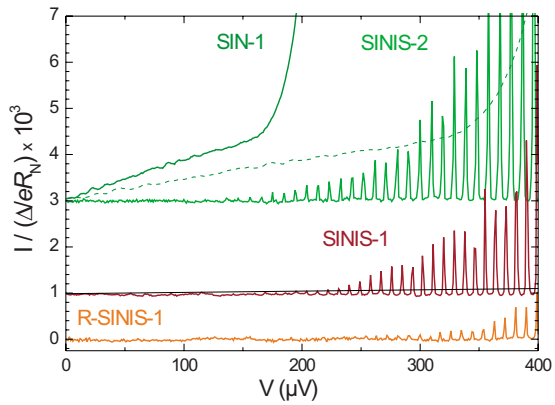

FIG. 4. (Color online) Normalized dc I-V characteristics. The I-V envelopes of the transistors were measured, while simultaneously sweeping the bias and the gate voltages, the latter over many oscillation periods. The dashed line shows the predicted curve for SINIS–2 in the gate-open state based on scaling the single-junction curve. The thin solid line indicates the slope corresponding to the density of subgap states phenomenologically used in the calculations of Fig. 2(a).

in the gate-open state, plotted by appropriate scaling of the *I-V* curve of the representative junction SIN–1, designed to be a half of the SINIS layout. The scaling approach is physically relevant, if we assume that the subgap current appears due to unblocked but still correlated SET transport through the subgap (e.g., "poisoning") states in the superconductor.

In contrast to the expected linear low-bias slope, the experimental envelopes show a clear voltage threshold, followed by a steep increase of the subgap current. One plausible interpretation for the peaks is Andreev reflection (AR), which may be stronger here than in other realizations[3,4,8] because of a lower barrier quality of $Al/AlO_x/Cr$ junctions. At low charging energies, $E_C<\Delta$, AR cycles can be launched in the following way. First, a nonequilibrium quasiparticle (often generated in the superconducting leads by external noise or single photons due to imperfect filtering or shielding) tunnels from a lead to the island and gets trapped there due to the charge hysteresis induced by Δ. Let us assume, e.g., that the gate charge C_gV_g/e is close to 0 and the island is trapped to the charge state 1. Now, AR cycles can contribute to the current by tunneling events between the charge states ± 1. The exact trapping mechanisms can vary between different experiments, see, e.g., Ref. 13 and the citations therein. Experimenting with several devices, we observed a large spread of leakage thresholds which may be related to the trapping-induced AR. The effective suppression of the leakage peaks by the resistors indicates thus their efficiency against higher-order processes. Together with the requirement $E_C>\Delta$,[6] a radical improvement can be expected.

To conclude, we demonstrate the effect of high-Ohmic environment on the hybrid turnstile. In the lower megahertz range, an order of magnitude improvement of the current plateaus was demonstrated theoretically and observed in experiment. Further analysis of the effect of the high-Ohmic environment on high-order processes is necessary for developing the hybrid turnstile toward metrological applications. Also, the effect of cooling or heating of the island[14] should be studied in more detail for further understanding of the device frequency limitations.

Fruitful discussions with M. Möttönen, O.-P. Saira, M. Meschke, and V. Bubanja are gratefully acknowledged. A.K. thanks Väisälä foundation for financial support. The work was partially supported by Technology Industries of Finland Centennial Foundation, the Academy of Finland, and by the European Union through the project SCOPE (Grant No. 218783).

[1] M. W. Keller, A. L. Eichenberger, J. M. Martinis, and N. M. Zimmerman, Science **285**, 1706 (1999); H. Scherer, S. V. Lotkhov, G.-D. Willenberg, and B. Camarota, IEEE Trans. Instrum. Meas. **58**, 997 (2009).
[2] H. D. Jensen and J. M. Martinis, Phys. Rev. B **46**, 13407 (1992).
[3] J. P. Pekola, J. J. Vartiainen, M. Möttönen, O.-P. Saira, M. Meschke, and D. V. Averin, Nat. Phys. **4**, 120 (2008).
[4] A. Kemppinen, M. Meschke, M. Möttönen, D. V. Averin, and J. P. Pekola, Eur. Phys. J. Spec. Top. **172**, 311 (2009).
[5] L. J. Geerligs, V. F. Anderegg, P. A. M. Holweg, J. E. Mooij, H. Pothier, D. Esteve, C. Urbina, and M. H. Devoret, Phys. Rev. Lett. **64**, 2691 (1990).
[6] D. V. Averin and J. P. Pekola, Phys. Rev. Lett. **101**, 066801 (2008).
[7] H. Pothier, P. Lafarge, C. Urbina, D. Esteve, and M. H. Devoret, Europhys. Lett. **17**, 249 (1992).
[8] A. Kemppinen, S. Kafanov, Yu. A. Pashkin, J. S. Tsai, D. V. Averin, and J. P. Pekola, Appl. Phys. Lett. **94**, 172108 (2009).
[9] A. B. Zorin, S. V. Lotkhov, H. Zangerle, and J. Niemeyer J. Appl. Phys. **88**, 2665 (2000); S. V. Lotkhov, S. A. Bogoslovsky, A. B. Zorin, and J. Niemeyer, Appl. Phys. Lett. **78**, 946 (2001).
[10] R. C. Dynes, J. P. Garno, G. B. Hertel, and T. P. Orlando, Phys. Rev. Lett. **53**, 2437 (1984).
[11] G. J. Dolan, Appl. Phys. Lett. **31**, 337 (1977); J. Niemeyer, PTB-Mitt. **84**, 251 (1974).
[12] G. L. Ingold and Yu. V. Nazarov, in *Single Charge Tunneling*, edited by H. Grabert and M. H. Devoret (Plenum, New York, 1992), Chap. 2.
[13] J. M. Hergenrother, J. G. Lu, M. T. Tuominen, D. C. Ralph, and M. Tinkham, Phys. Rev. B **51**, 9407 (1995).
[14] J. P. Pekola, F. Giazotto, and O.-P. Saira, Phys. Rev. Lett. **98**, 037201 (2007); S. Kafanov, A. Kemppinen, Yu. A. Pashkin, M. Meschke, J. S. Tsai, and J. P. Pekola, arXiv:0906.0597v1.