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TUNNEL JUNCTION THERMOMETRY AND THERMALISATION OF ELECTRONS

Doctoral Dissertation

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Aalto University
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Abstract

In this work, normal metal and superconducting tunnel junctions have been studied. In particular applications in low temperature electronic thermometry are investigated. The double oxidation method for achieving high resistance junctions is described and shown to produce high quality devices. A new in- vention, the single junction thermometer (SJT), is described, and proof of the concept experiments demonstrating the functionality of the device are described. A key feature of the SJT is a well controlled electromagnetic environment sur- rounding a single junction. It is shown that embedding a single junction within arrays of other junctions is a superior way for controlling the environment as compared to previously proposed methods. Improved thermalisation of electrons is shown to be beneficial for the per- formance of superconducting RSFQ (Rapid Single Flux Quantum) devices. The so called grey zone of the most basic of these devices, the balanced comparator, is investigated. Improved performance based on metallic cooling fins has been achieved. In the same spirit improved thermalisation of the Coulomb blockade thermometers extends their operation towards lower temperatures. A method employing thick metallic islands was developed and tested to this end.

Keywords Thermometry, CBT, SJT, Tunnel Junctions

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Preface

The work for this thesis was started in November 2005 when I moved to Pico group in Otaniemi. I thank my thesis instructor, Prof. Jukka Pekola, for bringing this work to a fruitful end. Over these years Prof. Pekola has garnered my respect for his work as a physicist and his drive and enthusiasm for science has been an inspiration. I would like to thank Mikko Paalanen, the director of Low Temperature Laboratory, for giving me the opportunity to work in that highly respected research environment. My supervisor, Prof. Matti Kaivola is living proof that professionalism is enhanced by kindness. Former and present members of Pico group have all contributed but Dr. Alexander Savin and Dr. Matthias Mescke stand out in their tangible influence on this thesis. I thank you all. I thank Juha Hassel, Leif Grönberg, Panu Helistö, Anna Kidiyarova-Shevchenko, Eeva Isosaari, and Martti Heinonen for rewarding collaboration. David Gunnarson, Rob Blaauwgeers, Pieter Vorselman, Andrey Timofeev, Rob de Graaf, Pauli Virtanen, Anssi Salmela, Sarah Macleod and Lorenz Lechner deserve thanks for helping me to preserve some sanity by contributing to my social support system. Everyones contribution has been appreciated and those not mentioned here can rest assured that they are not forgotten. I also thank Ingrid, Jörgen and Stina for their unconditional support. I finally thank Siri Edna Nelson for providing hope during my hours of darkness.

Espoo, March 2010

Tommy Holmqvist

List of publications

This Thesis consists of an overview and the following publications:

I A.M. Savin, J.P. Pekola, T. Holmqvist, J. Hassel, L. Grönberg, P. Helistö and A. Kidiyarova-Shevchenko, *High-resolution superconducting single flux quantum comparator for sub-Kelvin temperatures*, Applied Physics Letters **89**, 133505 (2006).

II T. Holmqvist, M. Meschke and J.P. Pekola, *Double oxidation scheme for tunnel junction fabrication*, Journal of Vacuum Science and Technology B **26**, 28 (2008).

III E. Isosaari, T. Holmqvist, M. Meschke, M. Heinonen and J.P. Pekola *Thermometry by micro and nanodevices*, The European Physical Journal Special Topics **172**, 323-332 (2009).

IV J.P. Pekola, T. Holmqvist and M. Meschke, *Primary tunnel junction thermometry*, Physical Review Letters **101**, 206801 (2008).

V T. Holmqvist, J.P. Pekola and M. Meschke, *Influence of environment on tunneling thermometry*, Journal of Low Temperature Physics **154**, 172 (2009).

Author's Contribution

The author has had an active role in all the phases of the research reported in this Thesis. In publication **I** he participated in the measurement, analysis and interpretation of the data. The author made all the samples for publications **II**, **IV** and **V** and the sample presented in publication **III**. He performed the measurements for publications **II**, **V** and part of them for publication **IV**. The author has written publications **II** and **V** and part of **IV** and participated in the preparation of the manuscripts for publications **I** and **III**.

Contents

Acronyms

CBT	Coulomb Blockade Thermometer
EBL	Electron Beam Lithography
ITS-90	International Temperature Scale of 1990
JJ	Josephson Junction
NIS	Normal metal - Insulator - Superconductor
NT	Noise Thermometer
PMMA	Polymethylmethacrylate
SIS	Superconductor - Insulator - Superconductor
SNT	Shot Noise Thermometer
PLTS-2000	Provisional Low Temperature Scale of 2000
RCSJ	Resistively and Capacitively Shunted Junction
RSFQ	Rapid Single Flux Quantum
SET	Single Electron Transistor
SJT	Single Junction Thermometer

Chapter 1

Introduction

Much of the physical sciences either concerns the determination of the constants of Nature or utilizes them to extract information on the surrounding world. The International System of seven units (SI) is an agreed upon system from which all other units are derived. The former ones rely upon a set of fundamental constants [1]. Temperature and its measurement are among the phenomena that have driven the development of science. The landmarks of it are noted as some of the highlights in the history of physics. Due to the fundamental importance of temperature, this is true not only in physics, but also in everyday life. The concept of warmth and coldness has, most likely, been around as long as human being has existed on the earth. The history of thermometry and temperature standards can be traced back to the second century A.D when Galen proposed a neutral temperature standard made up of equal amounts of ice and boiling water [2]. Around 1650 A.D. the gas thermometers were invented and in 1742 Celsius suggested a centigrade scale based on the freezing point and the boiling point of water. In the mid nineteenth century the advance of thermodynamics brought the idea of an absolute temperature scale, the kelvin scale, that has its zero defined where there is complete absence of thermal energy. This scale was modified in 1954 when the temperature of the triple point of water was defined to be 273.16 K. Thirteen years later the celsius temperature scale, t(°C) was redefined as t(°C)= T(K) − 273.15 K with T(K) as temperature on the absolute Kelvin scale [3]. The gradual development of thermodynamics brought a theoretical underpinning to the previous notions of temperature [4].

The concept of temperature is, on the macroscopic scale, based on the direction of heat flow between two bodies. If there is no heat flow the two bodies are at the same temperature, otherwise the heat flows from the hot to the cold one. In the microscopic scale the concept of temperature is based on the motion of bodies, e.g. molecules in an ideal gas. In this example, the temperature is directly given

by the average speed of the molecules. In the case of a solid body, temperature is related to vibrations of the molecules around their equilibrium position in the lattice. In metals, where much of the heat is transported by free moving electrons, the temperature is related to the kinetic energy of the electrons. The temperature of the electron gas and the temperature related to lattice vibrations may not be equal in the system.

The present official temperature scale is ITS-90 [5]. While representing a significant step forward from previous temperature scales, e.g. ITS-68, it does not, however, cover the range below 0.65 K. The ITS-90 uses material dependent fixed points and resistance measurements of platinum as interpolating thermometers between these fixed points down to 13.8 K. To supplement ITS-90, an additional temperature scale has been agreed upon. The Provisional Low Temperature Scale of 2000 (PLTS-2000) is meant to provide a temperature scale in the deep mK range (0.9 mK to 1 K) where, e.g. ^{3}He-^{4}He dilution refrigerators operate [6]. The PLTS-2000 is, however, an agreement between different measurement laboratories and is not fully satisfactory because of poor accuracy in the deep mK region.

Thermometers can be divided into primary and secondary ones. A primary thermometer needs no calibration but gives the temperature from direct measurement, whereas a secondary thermometer needs to be calibrated against another thermometer on at least one point. There are a number of thermometers based on solid state tunnel junctions. Among the more common ones are the Normal metal - Insulator - Superconductor (NIS) thermometer [7], the Shot Noise Thermometer (SNT) [8] and the Coulomb Blockade Thermometer (CBT) [9]. The two last ones are primary thermometers. The NIS thermometer is primary in principle but it requires exact knowledge of the superconducting gap, a parameter that can vary from sample to sample and has temperature dependence as well. One kelvin is today still defined as 1/273.16 of the triple point of water [3]. However, this can depend on isotopic composition of water, material of the container, etc. For this reason it is desirable to redefine the kelvin based on something not depending on a material specific property. It has been proposed to define the Boltzmann constant k_B and use this new definition to redefine the kelvin in turn [10]. The first step to redefine the kelvin is a sufficiently accurate determination of k_B. Several primary thermometers with sufficient accuracy for this purpose already exist [10]. Determining the Boltzmann constant will most conveniently be done at the triple point of water. Pinning the value of k_B will fix the scale of low temperature thermometers that utilise the Boltzmann constant for extracting the temperature from measurements.

A thermometer shows the temperature of itself, that may, or may not be the

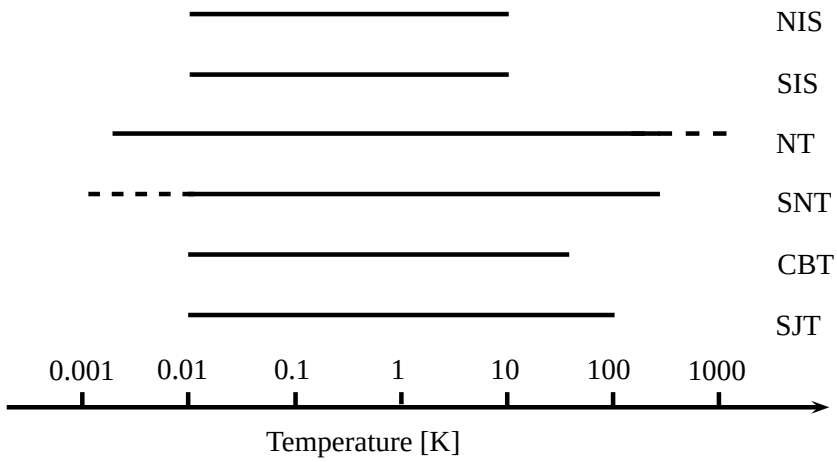

Figure 1.1: Some examples of thermometers based on tunnel junction technology. Normal metal-Insulator-Superconductor thermometer (NIS) [7, 11] and Superconductor-Insulator- Superconductor (SIS) [11] thermometer are considered to be secondary thermometers, i.e. they need to be calibrated before use. Noise Thermometer (NT) and Shot Noise Thermometer (SNT) [8, 12] extract temperature from noise properties of a resistor (NT) or a tunnel junction (SNT). CBT and SJT are discussed extensively in the text.

temperature of the object measured. In order for the thermometer to show the temperature of the object , the latter must be in thermal equilibrium with the thermometer. Thermometry below 1 K poses some challenges specific to this temperature range, for instance, in the case of electronic thermometers in metals, decoupling of the electron and lattice systems. Another issue, in the case of gas thermometers, is that gases do not behave as an ideal gas at low temperatures.

In the 1920's the quantum mechanical description of particles was developed [13, 14]. A consequence of the theory is that particles can traverse regions that are classically energetically forbidden. In the advent of this new paradigm in physics, such quantum mechanical tunneling was used for explaining ionisation of hydrogen [15], alpha decay in nuclear reactions [16] and electron emission from cold cathodes [17]. A theoretical desciption of a tunnel junction consisting of two metallic leads separated by a thin insulating layer, as shown in Fig. 1.2, that forms the potential barrier for electrons, came in 1930 [18]. This is the type of tunnel junction of interest in this thesis. The barrier thickness can be controlled during the fabrication process, e.g. by varying the oxidation conditions, but the barrier height (in terms of energy) is determined by the choice of the materials. Classically, in a simple model, this type of a tunnel junction is seen as a parallel plate capacitor with capacitance C. The change of energy due to a tunneling

process, where an electron goes from one to the other side of the barrier is given by the charging energy

$$E_c = \frac{e^2}{2C}. \tag{1.1}$$

Here e is the electron charge. An electron tunneling through the insulating layer will then increase the electrostatic energy by E_c. Hence E_c is called the charging energy which is the barrier that the electron to pass through the tunnel junction must overcome. In a voltage biased tunnel junction this means that for small voltages $< e/2C$, the conductance through the junction will be zero when $k_B T \ll E_c$. As the voltage is increased the barrier is overcome and electrons start to pass through the junction. One feature of the tunnel junction is that at a very high biasing voltage the current behaves essentially ohmicly with linear current - voltage (I-V) dependence. At small voltages there is no current flowing through the junction, creating the non-linear behaviour. However, it is very hard to observe this phenomenon in a single tunnel junction as will be discussed later. In reality tunneling is a quantum mechanical phenomenon beyond the simple model above for charging effects in a capacitor. Tunneling is described by the hamiltonian [19]

$$\mathcal{H}_T = \sum_{kq\sigma} T_{kq} c^\dagger_{q\sigma} c_{k\sigma} + H.c. \tag{1.2}$$

were $T_{kq} c^\dagger_{q\sigma} c_{k\sigma}$ denotes the annihilation of an electron with wave vector $\vec{k}$ and spin σ in the left electrode and the creation of an electron with wave vector $\vec{q}$ and spin σ in the right electrode, i.e., it describes the transfer of an electron from the left electrode to the right one. T_{kq} is the tunneling matrix. The hermitian conjugate, $H.c.$, denotes the process of an electron being annihilated on the right side and created on the left, i.e., tunneling in the opposite direction.
The tunneling picture leads to an ohmic expression for the current for a junction with fully normal conductors and in the absence of single-electron charging effects as a function of the applied voltage as [20]

$$I(V,T) = V/R_T, \tag{1.3}$$

where R_T is the tunneling resistance. Yet, in practice tunneling through the junction depends on the environment surrounding the junction: the electron exchanges energy with the electromagnetic environment, leading to nonlinear $I - V$ dependence.

Tunnel junctions find many applications, for instance in the low temperature technology. Under room temperature conditions magnetic tunnel junctions (MTJ) form between ferromagnetic leads. As a consequence the electrons will be spin polarized so that the current consists of two partial currents with either spin-up or spin-down electrons [21]. Practical applications of magnetic tunnel junctions

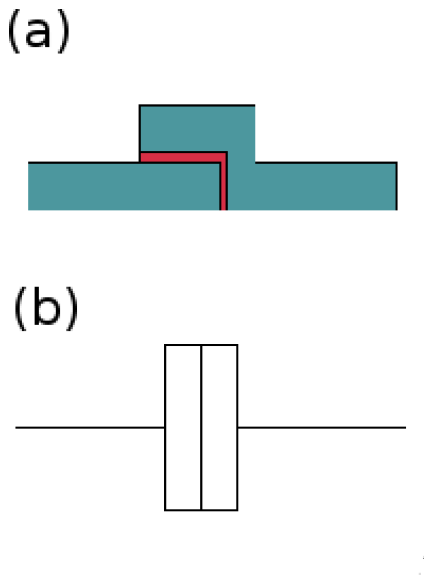

Figure 1.2: Representations of a planar tunnel junction. (a) Schematic of a junction. Blue denotes the metal layers and red refers to the dielectric layer forming the barrier of the tunnel junction. (b) A commonly used symbol of a small normal metal tunnel junction with charging energy (capacitance).

are today found in the read heads of hard disc drives [21, 22] and Magnetoresistive Random Access Memories (MRAMs) [21, 23]. The drive for increasing the speed of electronic components in semiconductor technology has forced the research community to look for other sources of digital electronics. One approach is to use Rapid Single Flux Quantum (RSFQ) logic based on superconducting Josephson junctions [24]. Instead of relying on transistors, as in traditional semiconductor technology, the RSFQ circuit is based on properties of superconducting junctions. As one particular application, RSFQ technology has been proposed to control quantum bit (qubit) operations.

The development of semiconductor electronics has driven the development of microfabrication techniques, aiming at making ever smaller components and utilising more exotic materials. While the fabrication of metallic structures, superconducting and normal, has its own intricacies, the methods are largery derived from what has become standard procedures in the semiconductor community. At the heart of these methods are those for drawing patterns onto a surface, lithography. Optical lithography at different levels of sophistication is employed to reproduce a pattern on a mask onto the surface by exposing a radiation sensitive resist with light with the photomask placed between the resist and the illumi-

nation source. Thus one transfers the pattern, initially on the mask, onto the photoresist. Photoresists are usually classified as either negative or positive, the difference being that the negative resist experiences a decreased solubility in the developer after exposure while for positive resists the solubility in the developer increases after exposure. One important figure of quality is resolution of the finished pattern that also depends on, e.g., the developer. For light the resolution is the smallest distance W between two Airy disks, the central maxima of the diffraction patterns of light from two apertures. The peaks can be resolved for $W \geq K\lambda/NA$. Here λ is the wavelength and NA is the numerical aperture. K is a constant that varies between 0.3 for surface image on top of the resist, 0.5 for multilayer resists, 0.75 for single layer resists and 1.1 for resists on reflective surfaces such as aluminum [25]. One obvious way to improve resolution is to decrease the wavelength of the incident radiation. The practical limit for this approach is the lack of optical components for refraction of X-rays. Instead, the use of electrons for both imaging and patterning offers improved resolution due to reduced de Broglie wave length, and optics in the form of magnetic lenses. Since 1970's electron beam lithography (EBL) has been a standard method for making high resolution patterns with a linewidth smaller than 100 nm on a surface by employing focused beams of electrons to expose a resist layer. Due to the higher resolution available with EBL, mask fabrication for optical lithography is manufactured primarily by defining the pattern on the mask with an electron beam. The disadvantage of any focused beam exposure scheme is that it is serial, i.e. it exposes the pattern in a sequence, whereas optical lithography exposes the whole wafer at the same time. Due to this parallelisation the time saving using optical lithography makes it often worthwhile to accept the lower resolution. The inherent flexibility in direct writing methods, where no mask is needed, can make EBL an attractive option in a research setting where only a small number of devices is made and parallelisation is not an issue.

In terms of resolution, novel parallel lithographic methods exist that retain the advantages of EBL, but have yet to become standard methods for manufacturing consumer goods. The prime examples are the various methods for imprinting and embossing a pattern on a stamp onto a resist covered surface [26, 27].

The standard method for fabricating tunnel junctions is by means of lift-off, i.e. after patterning and development the metal layers are deposited on top of both remaining resist and the areas where the resist has been removed. After the metal deposition the resist is removed, 'lifting off' the metal on top of the resist but leaving the metal where the resist was removed during development. Thus it leaves a metal pattern where before there was a pattern in the resist. For thin layers, lift-off is a standard procedure that is well established, but thick metal layers are more challenging because of the need for thicker resist layers than the metal layer itself. Thick metal layers are interesting for improving thermalisation between electron and lattice systems as will be described in the following sections.

The electron penetration depth for 15 kV electrons in resist is of the order of 5 μm setting a limit for how thick resist layers can be used for lift-off.
One possibility for achieving thick layers is to use overlay exposures [28] to stepwise build up several layers. This of course requires that the metal surfaces are completely clean. Thus a cleaning step inside the vacuum chamber is necessary immediately before metal deposition in order to avoid residues of resist, formation of oxides or a surface layer of water. The need for absolutely clean surfaces is not only for avoiding boundaries that impair heat flow but to achieve adhesion between the layers. Another approach is to use a mechanical mask but this will suffer from the same problems if care is not taken to deposit all layers in a single vacuum cycle.
Deposition of thin metal layers onto a surface is commonly done by heating a metal source in a vacuum chamber until the metal starts to evaporate. This can be achieved either by heating a crucible filled with the metal with an electric current or by focusing an electron beam on the crucible. Sputtering is also a common method for depositing metals but this technique is less suitable for lift-off since deposition is more isotropic than in thermal evaporation. Electroplating is used for thicker layers of > 1 μm thickness. It requires a conducting seed layer on the sample. The electrolyte is sensitive to contaminations and it should contain an additive in order to produce good quality surfaces.

The double angle shadow mask evaporation technique for fabrication of tunnel junctions was developed by Dolan [29] and Niemeyer [30] independently more than 30 years ago. As shown in Fig. 1.3 the method utilizes two layers of positive resist, where the bottom layer has higher sensitivity to radiation than the top one. The bottom layer will therefore, after development, have larger lateral openings to the substrate than the top layer. Two metal electrodes deposited at an angle relative to each other can thus be made to overlap if the bottom resist layer is completely removed in the area between the electrode pattern on the top layer. It is still the preferred technique for fabrication of tunnel junctions. Other techniques involving etching have also been used but the simplicity and the fact that very clean surfaces can be formed in the Dolan-Niemeyer technique, has ensured its survival.

The two main topics of this thesis are:

1. To improve a particular thermometer for low temperatures based on tunnel junctions, the CBT.

2. To develop a new type of a tunnel junction thermometer, the SJT.

Increasing the range downwards to 10 mK of an electronic thermometer would entail thermalization of the electronic system with the phonon system of the

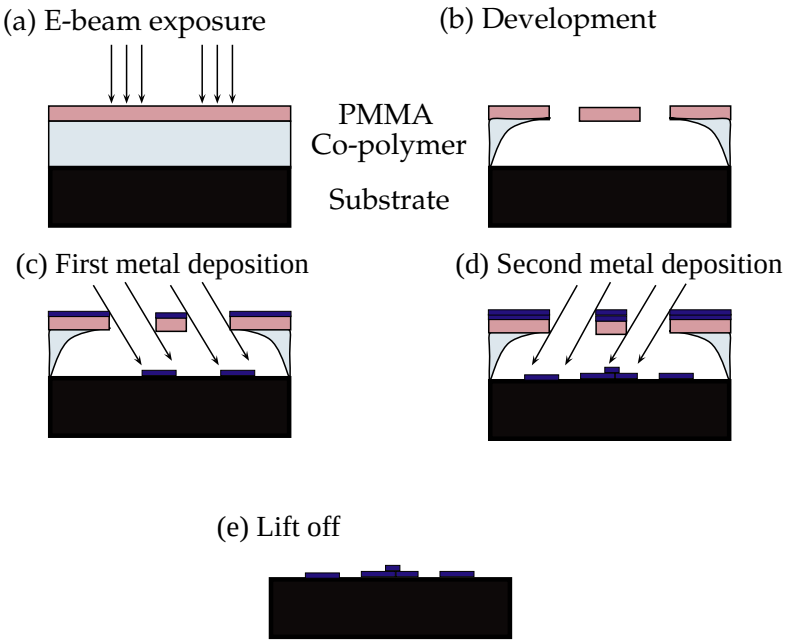

Figure 1.3: Schematic of the lift off process used for fabrication of tunnel junctions. (a) Exposure of photoresist with electron beam. (b) Development of the exposed photoresist. (c) Deposition of the first metal layer and subsequent oxidation. (d) Deposition of the second metal layer. (e) Removal of the resist and the metal deposited on top of the resist.

circuit. During practical measurements both self heating and noise will contribute to the heat load on the thermometer. Therefore care needs to be taken to filter the measurement lines and to control heat input and thermalisation. In the course of working with the CBTs at low temperatures, novel approaches for improving the measurement accuracy of the CBT were explored. In practice one CBT can not cater for all the temperature ranges. At low temperatures the junction area should be larger than for CBTs meant for higher temperatures. On the other hand, junction transparency has to be controlled for each temperature range. The parameters of the tunnel junctions employed for thermometry will have to be tailored for different temperature ranges using novel approaches developed in this thesis. The SJT was invented during the course of this thesis work. It is shown to be a primary thermometer with some appealing characteristics. There is no spread of junction parameters influencing the accuracy of the thermometer and the thermometer can be tailored so that the measurement is protected from the influence of the noise in the environment.

Chapter 2

Normal Metal Tunnel Junctions

2.1 General Properties

Three models for tunneling through a junction will be discussed here. One of them, the Simmons model focuses on the properties of the dielectric barrier of the tunnel junction to extract expressions for the $I-V$ behaviour of a single junction with finite barrier height and thickness. In the early 1960's a series of papers was published by Simmons presenting a model for tunneling between two electrodes [31, 32]. This became one of the standard models for describing tunnel junctions. A more formal approach to previous theoretical empirical investigations of the $I-V$ behaviour [33] was presented by Simmons based on earlier theoretical work [34]. The second model is the theory of sequential tunneling mainly developed in the mid-1980's [35]. The so-called orthodox theory was initially developed to account for the zero bias behaviour observed in granular metals [36–38]. The third model, the so called $P(E)$ theory describes the tunneling event in a circuit environment [20]. The $P(E)$ correlation theory has emerged as the standard model for tunneling of electrons through small tunnel junctions. It describes the process involving energy exchange between the tunneling electron and its electromagnetic environment.

2.1.1 Simmons model

The effect of an insulating layer in the junction is to form the barrier for tunneling. Classically an electron would have to possess kinetic energy in excess of the barrier height in order to pass above it to the opposite side of the junction. Quantum mechanically the charge tunnels through. Consider a rectangular barrier of height

ϕ_0 and width s. The application of a voltage V across the barrier will skew it into a trapezoidal shape, mathematically described as

$$\phi(x) = \phi_0 - \frac{eV}{s}x \tag{2.1}$$

where x is the position inside the barrier. The conductance of a tunnel junction is of the form [33]

$$G = \frac{dI}{dV} = G_0\left(1 + 3\gamma V^2\right). \tag{2.2}$$

G_0 and γ are determined as fitting parameters from measurements and the latter is related to the parameters as

$$\gamma = \sqrt{\frac{4\hbar^2}{e^2 m}\frac{\phi_0}{s^2}} \tag{2.3}$$

where m is the effective mass of an electron. Equations (2.2) and (2.3) can be used to determine the barrier parameters. G_0 depends on temperature.

In any real junction image forces experienced by the electron will distort the barrier so that the barrier height is reduced and the effective thickness is smaller than the real thickness. A charged particle in the vicinity of a metallic surface will polarize the surface, i.e., attract opposite charges to the surface. Due to this polarisation the particle will experience a force in the direction towards the surface. The resulting image potential is given by

$$V_i = \left(-\frac{e^2}{4\pi\epsilon}\right)\left[\frac{1}{2x} + \sum_{n=1}^{\infty}\left(\frac{ns}{\left[(ns)^2 - x^2\right]} - \frac{1}{ns}\right)\right] \tag{2.4}$$

where $\epsilon = \epsilon_r\epsilon_0$, here ϵ_r is the relative permittivity of the material and ϵ_0 is the vacuum permittivity. A common approximation for the image potential is given by [31]

$$V_i = -\frac{1.15\lambda s^2}{x(s-x)} \tag{2.5}$$

where

$$\lambda = \frac{e^2\ln(2)}{8\pi\epsilon s}. \tag{2.6}$$

Taking into account the approximate expression for the image potential, the total potential across the junction is expressed by

$$\phi(x) \approx \phi_0 - eV\frac{x}{s} - 1.15\lambda\frac{s^2}{x(s-x)}. \tag{2.7}$$

Since the image force depends on the dielectric constant of the insulating material in the barrier, inclusion of it has consequences for engineering of the junction

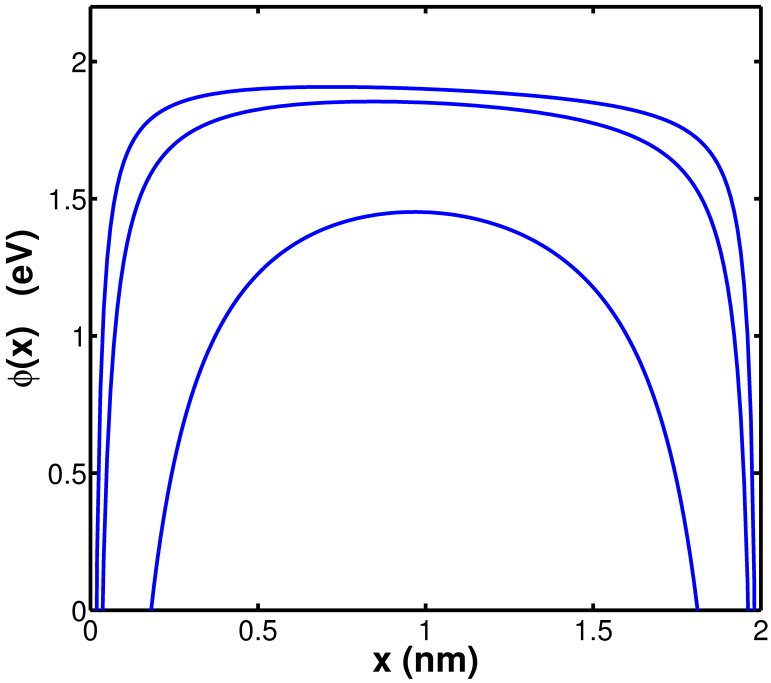

Figure 2.1: The potential barrier of Eq. (2.4) for $\varepsilon = 1$, 5 and 10 from bottom to top. The typical values for aluminum oxide barrier $\phi_0 = 2$ eV, thickness $s = 2$ nm and an applied voltage of $V = 0.1$ V across the junction were used here for all the curves.

parameters since a higher dielectric constant of the barrier material results in a higher barrier according to Eqs. (2.6) and (2.7). This is shown in Fig. 2.1 for a junction with $\phi_0 = 2$ eV that is biased at $V = 0.1$ V. The inclusion of image forces also smears the barrier, an effect that gets more visible the lower the dielectric constant of the insulating material gets. The computation resources available today have made the approximation (2.5) largely irrelevant for most purposes, but a simple analytical expression is still useful for grasping the concepts. Results from paper **II** were analyzed partly based on Simmons model. The model was useful in understanding the bias and temperature dependent conductance in the measurements.

2.1.2 Sequential tunneling

In the mid 1980's a detailed theory for correlated tunneling was developed [35, 39–41]. It was shortly after supported by experimental evidence [42]. The theory presumes that the tunnel junction has a resistance R that is sufficiently large $R \gg R_Q = \frac{\pi\hbar}{2e^2} \approx 6.4$ kΩ. Here the value for R_Q is from [35] instead of the more conventional value of $R_Q = h/e^2 \approx 25.8$ kΩ [20]. The value for R_Q indicates the order of magnitude and should not be taken as an absolute threshold for the junction resistance to apply the results to be presented. The order of magnitude of the tunneling rate Γ can be estimated as $\Gamma = V/eR$. As a consequence, the time between tunneling events τ can be estimated as $\tau = \frac{1}{\Gamma} = \frac{eR}{V}$. Due to the uncertainty principle the tunneling event can not be determined more accurately in time than $\hbar/eV$, this is referred to as the tunneling time, i.e. the time it takes for one electron to pass from one side of the junction to the opposite. While not the only definition of tunneling time [43] it is the most relevant for the purpose here. The condition that the resistance is much larger than R_Q thus means that the events are separate in time, i.e. the electrons tunnel one by one. For Coulomb blockade to be easily observed in experiments, the above criterion for junction resistance must be complemented by two further criteria. First, the charging energy of the junction must be higher than the thermal energy of the electrons, i.e. $E_c > k_BT$, otherwise the electrons will be thermally excited above the electrostatic barrier. Second, the applied bias with electrostatic energy eV should not exceed the charging energy. The charging energy is a measure of the repulsive electrostatic force affecting the electrons. If it is higher than the electrostatic force due to the bias voltage, the tunnel current decreases due to the repulsion. This is the so called blockade region. The change of electrostatic energy in the tunnel junction due to a single tunneling event is $W = Q^2/2C - (Q - e)^2/2C$ (see Fig. 2.2 (c)). Tunneling inside the blockade region, $-e/2C < V < e/2C$ is strongly suppressed as long as $k_BT \ll E_c$, but it is still possible.

The single electron transistor (SET) had attracted interest already before the first experimental realisation of this device [42]. To understand the SET, see Fig. 2.2 we consider a conducting island with a tunnel junction of capacitance C_1, C_2 on each side, respectively, forming source and drain. The island is capacitively connected to a gate that is used for controlling the charge number on the island. The capacitance of the island to the gate is C_g and thus the total capacitance of the island is $C_\Sigma = C_1 + C_2 + C_g$. The difference in free energy before and after a tunneling event is

$$-\Delta F_i = \frac{e}{2}[(\phi_2 + \phi_2') - (\phi_1 + \phi_1')] \tag{2.8}$$

for every event i, where ϕ_1 is the potential of the electrode from which the electron tunnels and ϕ_2 is that of the electrode where the electron ends up after the event.

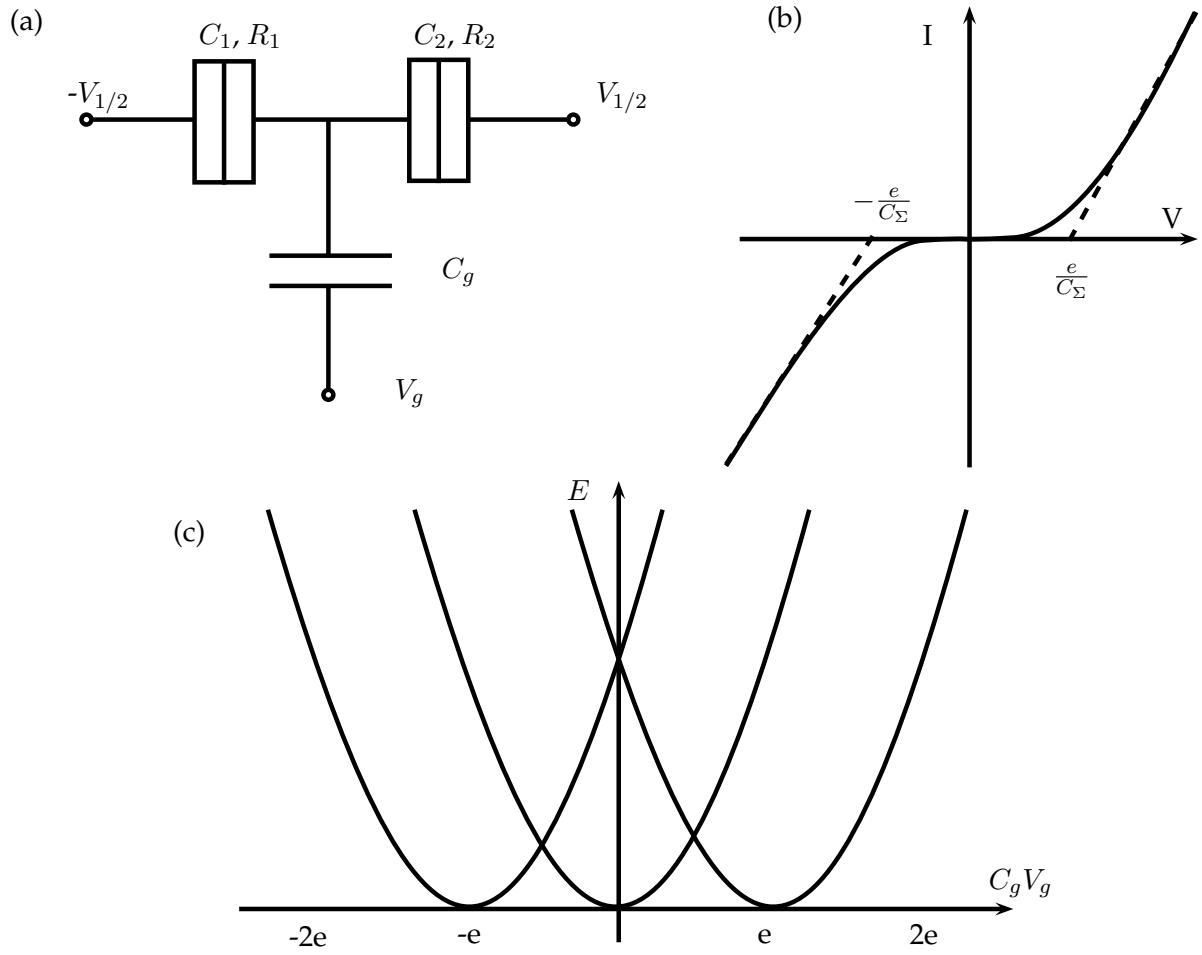

Figure 2.2: (a) Schematic of a single electron transistor (SET). (b) Typical $I-V$ curve of an SET. C_Σ is the total capacitance of the system. (c) Energy diagram of a SET. At the degeneracy points, i.e. at $C_gV_g/e = n+1/2$, with n as an integer, the two adjacent charge states have the same energy and tunneling becomes possible.

(Un)primed potentials in Eq. (2.8) are those (before) after the tunneling event has occured.

The tunneling rate is given by

$$\Gamma_i^{\pm} = \frac{1}{e^2 R_T} \frac{\Delta F_i^{\pm}}{1 - \exp(-\Delta F_i^{\pm}/k_B T)}. \tag{2.9}$$

where Γ_i^+ is the tunneling rate in the forward direction and Γ_i^- in the backward direction through junction i, similarly for the energies $\Delta F_i^{\pm}$. The tunneling current passing through the junction i is given by

$$I_i = e \sum_{n=-\infty}^{\infty} \sigma(n) \left(\Gamma_i^+(n) - \Gamma_i^-(n) \right) \tag{2.10}$$

where $\sigma(n)$ is the probability of finding n extra electrons on the island. The latter quantity can be determined either from monte-carlo simulations or by solving the master equation for charge probabilities. Under steady state conditions the master equation reads

$$\sigma(n)[\Gamma_1^+(n) + \Gamma_2^+(n)] = \sigma(n+1)[\Gamma_1^-(n+1) + \Gamma_2^-(n+1)]. \tag{2.11}$$

2.1.3 Environment

Consider an array of tunnel junctions as in Fig. 2.3, biased at voltage V and embedded in an environment of impedance $Z_e(\omega)$ at temperature T. The standard picture for tunneling is based on determining the exchange of energy between the junction and the surrounding environment [20]. Along the theoretical treatment detailed in [20], within the environment, the tunneling rate in the forward (+) and backward (-) direction through junction i at temperature T is given by

$$\Gamma_i^{\pm} = \frac{1}{e^2 R_{T,i}} \int \gamma(E) P(\Delta F_i^{\pm} - E) dE \tag{2.12}$$

where $\gamma(E)$ is the golden rule tunneling rate for no energy exchange of Eq. (2.9) with $\Delta F_i^{\pm} = E$. The change of electrostatic energy due to the tunneling event, can be divided into two terms as $\Delta F_i^{\pm} = eV_i + \Delta E_i^{ch,\pm}$, where $\Delta E_i^{ch,\pm}$ is the change of internal energy in junction i associated with charging of the capacitors, and V_i is the voltage across the junction. The probability density for the electron to exchange energy with the electromagnetic environment is described by

$$P(E) = \frac{1}{2\pi\hbar} \int_{-\infty}^{\infty} e^{J(t) + \frac{i}{\hbar} E t} dt, \tag{2.13}$$

where $J(t)$ is the phase-phase correlation function. For a purely resistive environment with $Z_e(\omega) = R$, surrounding a chain consisting of N identical junctions

with capacitance C, the phase-phase correlation function, $J(t)$ is given by

$$J(t) = \pi \frac{R_{eq}}{R_Q} \left(\cot(B)(1 - e^{-|\tau|}) - \frac{|\tau|}{B} - 2 \sum_{k=1}^{\infty} \frac{1 - e^{-k\pi|\tau|/B}}{k\pi(1 - (k\pi/B)^2)} - i \ \mathrm{sign}(\tau)(1 - e^{-|\tau|}) \right) \tag{2.14}$$

with $\tau = t/(R_{eq}C_{eq})$, $B = \hbar/(2k_BTR_{eq}C_{eq})$, $R_{eq} = R/N^2$ and $C_{eq} = NC$.

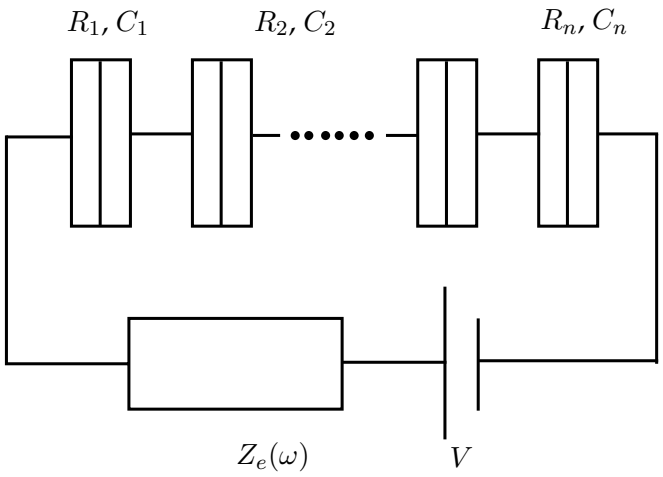

Figure 2.3: Circuit for modelling the environment surrounding an array of n tunnel junctions with capacitances C_i and resistances R_i. The frequency dependent impedance of the environment is denoted by $Z_e(\omega)$.

Very qualitatively, the spatial extent to which the environment of the junction is of importance can be estimated by the horizon model [44, 45]. It is based on an estimation of the uncertainty time τ for the electron to pass from one side of the tunnel junction to the other as outlined in [46],

$$\tau = \frac{\hbar}{max(eV, k_BT)}. \tag{2.15}$$

A length scale is introduced as $\ell \sim c\tau$ where c is the propagation speed of the electromagnetic signal in the media. An estimate of the length influencing the tunneling rates is then given at low voltage by

$$\ell \sim \frac{ce^2R_T}{k_BT} \sim \frac{hc}{k_BT} \tag{2.16}$$

where the last step applies for $R_T \sim h/e^2$. One important consequence of the abovementioned estimate of the horizon is that the intentionally engineered electromagnetic environment, for instance the next junction in an array, must be

positioned closer to the junction the higher the temperature is, in order to have no significant uncontrolled effect from the intervening leads on the tunneling properties of the junction.

2.2 Junctions as thermometers

Arrays of normal metal - insulator - normal metal tunnel junctions exhibit a conductance drop at zero bias due to Coulomb blockade. In 1994 it was shown that this is a useful property for primary thermometry under the condition $E_C \lesssim k_B T$ [9]. The operation of the CBT is closely related to the SET. In practical measurements a CBT usually consists of a large number of junctions.

The full analytical result for the conductance of an N-junction array, not necessarily a uniform one, in the limit $E_c \ll k_B T$, is given by [47]

$$\frac{G}{G_T} = 1 - 2\sum_{i=1}^{N} \frac{R_{T,i}}{R_\Sigma} \frac{\Delta_i}{k_B T} g\left(\frac{R_{T,i}}{R_\Sigma} \frac{eV}{k_B T}\right) \tag{2.17}$$

where $G_T = 1/R_\Sigma$ is the assymptotic conductance for $V \to \pm\infty$, $R_\Sigma \equiv \sum_{i=1}^{N} R_{T,i}$ is the total tunnel resistance of the full array with junction resistances $R_{T,i}$, Δ_i is the inverse capacitance matrix of the array, and

$$g(x) = \frac{e^x[e^x(x-2)+x+2]}{(e^x-1)^3}. \tag{2.18}$$

Assuming a fully symmetric array with equal resistances and capacitances for all junctions, Eq. (2.17) can be simplified to [47]

$$\frac{G}{G_T} \simeq 1 - u_N g(v_N) \tag{2.19}$$

where $u_N \equiv [(N-1)/N](e^2/Ck_BT)$ and $v_N \equiv eV/Nk_BT$. Equation (2.19) against bias voltage respresents a nearly bell shaped curve, see Fig. 2.4, with a full width at half minimum that depends on temperature and the number of junctions as

$$V_{1/2} = \frac{\alpha N k_B T}{e}, \tag{2.20}$$

where α =5.439... is an irrational constant. This relation says that the junction array can be used for primary thermometry as the temperature is extracted from the measurement of a single parameter, voltage $V_{1/2}$, that depends only on fundamental constants and temperature. The conductance drop at zero bias is

$$\frac{\Delta G}{G_T} \simeq \frac{1}{6} u_N. \tag{2.21}$$

This expression can also be used for thermometry but as it depends on the capacitance of the junctions as well, it serves as a secondary thermometer in this case. The conductance drop (2.21) is nevertheless used in thermometry, with calibration via $V_{1/2}$, because of the faster read-out. The parameters of a typical conductance curve are illustrated in Fig. 2.4.

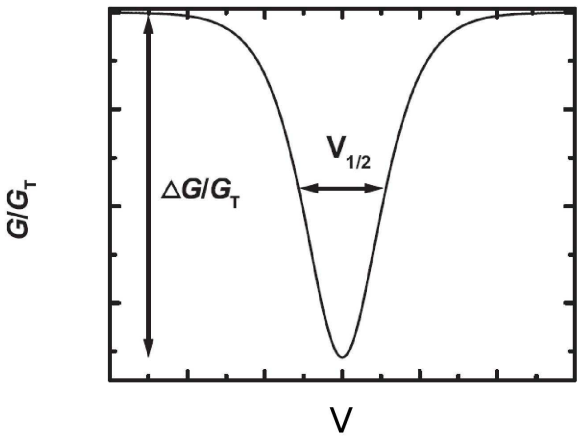

Figure 2.4: A typical conductance curve of a junction array used as a CBT thermometer. The curve is normalized against the asymptotic conductance G_T. The half-width $V_{1/2}$ is used for extracting a primary measurement of temperature. The depth of the conductance dip $\Delta G/G_T$ is used for a secondary temperature measurement once the capacitance is known (from the half-width measurement at one temperature).

In practice, a remotely voltage biased junction is surrounded by a dissipative environment with the impedance of $\sim \sqrt{\mu/\varepsilon} \sim 100\ \Omega$, where μ is the permeability and ε the permittivity of the medium, corresponding to $Z_e(\omega) = \sqrt{\mu/\ \varepsilon}$ in Fig. 2.3 for $N = 1$. Instead of embedding the junction in a resistive environment as has been previously proposed, embedding the junction in an environment consisting of other tunnel junctions has advantages. Most obviously from the fabrication point of view, making a resistor of several tens of MΩ at a distance of a few μm is not a trivial feat with most materials available in microfabrication. In practical CBT mesurements an array of tunnel junctions ($N > 20$) is employed in order to suppress errors due to the electromagnetic environment. Figure 2.5 (b) shows the errors of temperature determined from the half-width as a function of

the number of junctions in the array, for four different environment resistances. The free space impedance is $R_0 = \sqrt{\mu_0/\varepsilon_0} = 377\ \Omega$. For a circuit on top of a bulk silicon substrate the corresponding high frequency impedance $\sqrt{\mu/\varepsilon}$ is a few times lower, making the values for 100 Ω environment resistance most relevant for analyzing our experiments. The error in temperature in an array of junctions is suppressed approximately quadratically with the number of junctions in the surrounding arrays (see **IV**). Figure. 2.5 (b) shows that the error of the temperature measurement decreases indeed rapidly as a function of the number of junctions in the array.

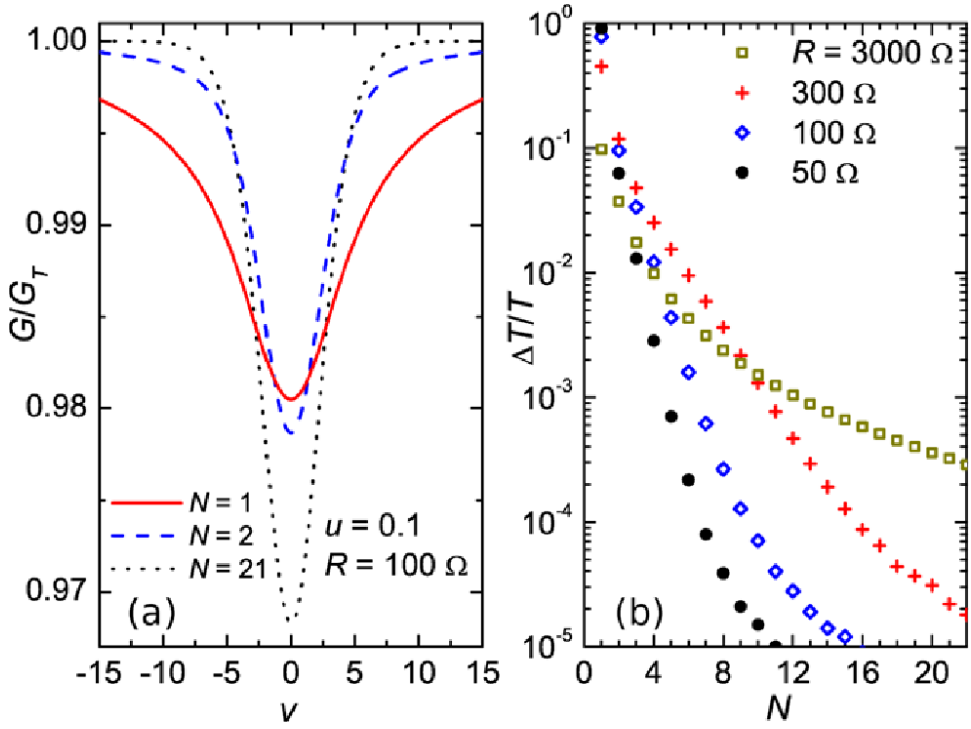

Figure 2.5: Calculated influence on the conductance peak of the number of junctions in an array of tunnel junctions, see Fig. 2.3 with $Z_e = R$. (a) Conductance curves for one, two and 21 junctions in series in an environment with impedance of 100 Ω. The voltage bias is scaled as $v = (eV)/(k_BT)$ where V is the measured voltage across one junction. We assume u =0.1, where $u = (e^2/2C)/(k_BT)$. (b) The calculated error of temperature measurement, defined as deviation from $T = (V_{1/2}e)/(5.439Nk_B)$, as a function of number of junctions in the array. Results for four different environment resistances are shown.

Unfortunately, an array of junctions introduces another type of an error from fabrication uncertainty. A variation in junction resistances within the array will

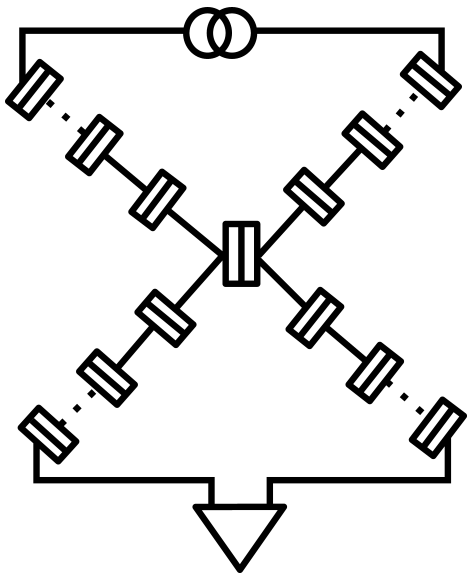

Figure 2.6: Schematic illustration of the Single Junction Thermometer (SJT). A single junction embedded within arrays of tunnel junctions is measured in a four probe configuration.

lead to an error in temperature, see Eq. (2.17). The problem is accentuated for small junctions since a small variation in absolute size will still constitute a large fraction of the junction area, and hence in junction resistance. In large area junctions with small charging energy used for low temperature applications, the problem is not severe.
By embedding a single junction in arrays of tunnel junctions, as shown in Fig. 2.6 the same effect of protection from environmental noise is achieved without having the disadvantage of a long array. A single tunnel junction embedded in four arrays of junctions in such a four probe configuration as in Fig. 2.6 presents a new primary thermometer, see publication **IV**. The analysis of this Single Junction Thermometer (SJT) follows the same ideas as that for the CBT. Under similar conditions as before for a CBT, the conductance of a single junction between two islands (denoted L and R) is given by

$$\frac{G(V)}{G_T} = 1 - \frac{\delta}{k_B T} g\left(\frac{eV}{k_B T}\right), \tag{2.22}$$

where $\delta = e^2[(\mathbf{C}^{-1})_{LL} + (\mathbf{C}^{-1})_{RR} - 2(\mathbf{C}^{-1})_{LR}]$, $\mathbf{C}$ is the capacitance matrix of the junction array and V is the bias voltage across this central tunnel junction. According to Eq. (2.22) a single junction can be used for exact thermometry

provided that V can be measured accurately.

2.2.1 Thermal transport

Energy transport between the lattice system and the electron system in a metallic island is given by [11, 48]

$$\dot{Q} = \Omega\Sigma \left(T_e^5 - T_{ph}^5\right). \tag{2.23}$$

Here Ω denotes the volume of the lead, Σ is a material constant, T_e is the electron temperature and T_{ph} is the phonon temperature. Typical values for Σ are $0.2{\cdot}10^9$ W/m^{3}K^5 for Al and $2{\cdot}10^9$ W/m^{3}K^5 for copper [11]. From Eq. (2.23) it can be seen that an obvious way to improve thermalization by increasing the heat flow between the electron system and the underlying lattice is to increase the volume of the conductors. This approach is limited by present standard fabrication technology where increase of volume can only be realized by increasing the area and thereby increasing parasitic capacitances. The standard lift-off technique is limited by the resist scheme as will be discussed later. One option is to attach a cooling fin of sufficient volume and low thermal resistance to the metal. Indeed this technique has been tried before on, e.g., shunt resistors of a DC SQUID [48]. In this approach the electrical current does not pass through the cooling fin which improves the frequency characteristics of the device. The fact that the electronic thermal conductivity is finite limits the effective size of the cooling fin so that the heat flow from the electron system to the lattice will only be significant close to the heat source. It is reasonable to introduce the requirement that the electron thermal resistance in the cooling fin is smaller than the electron-phonon resistance. The electron-phonon conductance at temperature T, common for electrons and phonons in this case, can be deduced from Eq. (2.23) by differentiating with respect to T_e yielding a conductance κ_{e-p} as

$$\kappa_{e-p} = 5\Sigma\Omega T^4. \tag{2.24}$$

In the one dimensional case, the electron heat conductance is given by

$$\kappa_e = \frac{k_e S}{x}, \tag{2.25}$$

where k_e is the electronic thermal conductivity, S is the cross sectional area of the cooling fin and x denotes the length of the conductor. Wiedemann-Franz law states that

$$\frac{k_e}{\sigma} = LT \tag{2.26}$$

where L is the Lorenz number and σ is the electrical conductivity. Equations (2.25) and (2.26) now yield

$$\kappa_e = \frac{\sigma LST}{x}. \tag{2.27}$$

Together with the requirement $\kappa_{e-p} \leq \kappa_e$, Eqs. (2.24) and (2.27) lead us to the condition that the cooling fin should have a length

$$x \lesssim \frac{L}{5\rho\Sigma t T^3} \tag{2.28}$$

in order to be efficient. Here $\rho = 1/\sigma$ is the resistivity and t denotes the thickness of the cooling fin. This model does not take into consideration the geometrical shape of the cooling fin. A more general model is obtained by assuming a uniform semi-infinite film connected in one end to a point-like heat source at constant temperature. The equation for the heat flux in the cooling fin can then, assuming cylindrical symmetry, be written in a dimensionless form by introducing the following definitions $u \equiv \left(\frac{T_e(r)}{T_0}\right)^2$, $\xi \equiv \frac{r}{r_s}$ and $r_s \equiv \sqrt{\frac{L}{2\rho\Sigma T_0^3}}$ [11]. Together with energy conservation, the expression for radial flux from the hot spot then reads

$$\frac{d^2u}{d\xi^2} + \frac{1}{\xi}\frac{du}{d\xi} = u^{\frac{5}{2}} - 1. \tag{2.29}$$

The length r_s is the scale over which the temperature relaxes towards the bath temperature T_0.
One important contribution to non-equilibrium is self heating of the device. The power of self heating of the thermometer biased at voltage V is given by $\dot{Q} = V^2/R$, where R is the resistance. High resistance is in this case desirable in order to reduce the heat load. The upper limit for R is given by the practical considerations in terms of noise matching of high impedance devices to the room temperature preamplifier, or by the dimensional constraints of the device and the measurement setup.

Electronic thermometers such as CBT and SJT measure electron temperature in the device connected to the metallic reservoirs. These reservoirs are in turn connected to the surrounding bath (see Fig. 2.7). In order for the thermometer to yield accurate measurements of temperature of the bath all the interfaces between these separate bodies must have sufficiently small thermal resistances. The electron system in equilibrium is described by the Fermi distribution

$$f_{eq}(E, T_e, \mu) = \frac{1}{\exp[(E-\mu)/k_B T_e] + 1} \tag{2.30}$$

where μ is the chemical potential. In equilibrium, i.e., in the case of fast electron phonon relaxation this is also the lattice temperature. This is the useful regime if one wants to probe the lattice temperature. In quasi equilibrium the electron - electron relaxation is still fast so that the electrons obey the Fermi distribution but the electron - phonon relaxation is slow. This means that the lattice temperature may differ from the electron temperature, both still being well defined

quantities. A common situation in the deep mK region is the rapid de-coupling of the electron system from the lattice with decreasing temperature. Finally, if the electrons in the probed device do not follow the Fermi distribution then the device is not an electronic thermometer.

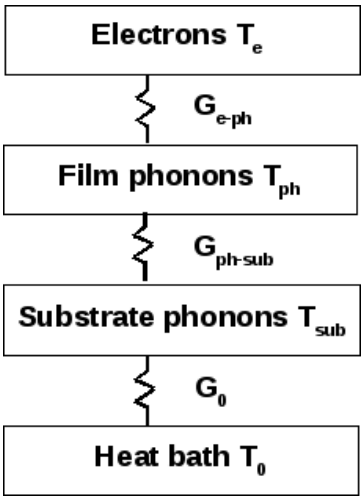

Figure 2.7: Thermal model for an electronic thermometer. In order for the electron temperature T_e in the thin metal film of the device to be in equilibrium with the phonon temperature T_{ph} of the film, the thermal resistance G_{e-p} should be small enough to allow energy transport between the two systems. The same is true for the phonons in the metal film and the phonons in the silicon substrate. G_{ph-sub} denotes Kapitza or thermal boundary resistance between film phonons and substrate phonons. At low temperature the heat conduction in silicon is usually good enough. A critical point is the thermal boundary between the substrate and the sample holder that is taken as the bath temperature in this model. This is motivated by the fact that the contact area between substrate and sample holder is usually very large, giving a low thermal resistance. A poor thermal contact will lead to a higher substrate phonon temperature and subsequently to a higher electron temperature in the device than the phonon temperature of the bath and the thermometer will therefore show temperature different from that of the bath.

2.3 Rapid Single Flux Quantum electronics

There is an interest in developing digital electronics based on superconducting Josephson junctions. In a superconductor, electrons form Cooper pairs of two

electrons and they move without resistance. When the leads of a tunnel junction are superconducting electrons will tunnel through the barrier as Cooper pairs instead of one by one. Two superconductors connected with a thin insulating barrier through which electrons and Cooper pairs can tunnel, forms a so called Josephson junction (JJ) [49]. In contrast to the normal metal junctions, the dynamic properties of a Josephson junction are governed by two basic formulas, the so-called Josephson relations

$$V(t) = \frac{\hbar}{2e}\frac{\partial \varphi}{\partial t} \tag{2.31}$$

for the voltage and

$$I(t) = I_c \sin \varphi(t) \tag{2.32}$$

for current. Here φ denotes the phase difference of the superconducting order parameter between the two superconductors [19]. I_c is the critical current, i.e., the largest supercurrent that the junction can support.

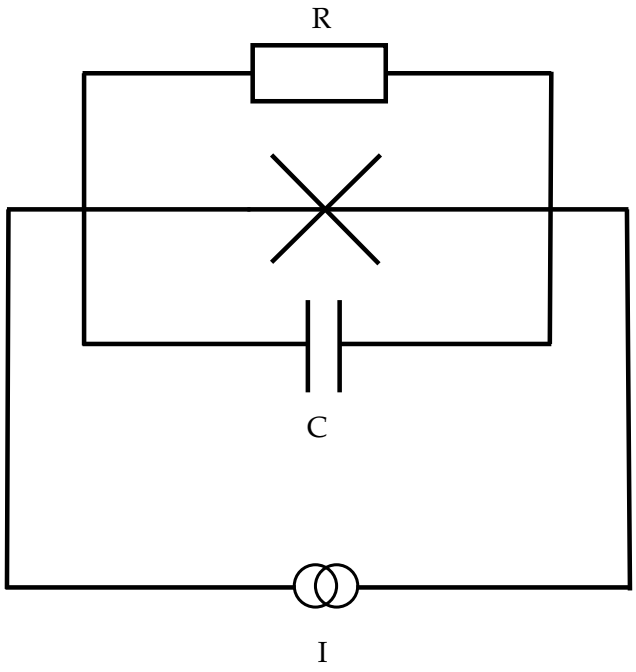

Figure 2.8: The RCSJ model. An ideal Josephson junction is connected in parallel with a capacitance C and a resistance R to a current source with current I.

Within the Resistively and Capacitively Shunted Junction (RCSJ) model, the Josephson junction is modeled as a pure JJ connected in parallel with a resistor

(R) and a capacitor (C), see Fig. 2.8. The time dependence for such a circuit is given by [19]

$$\frac{\partial^2\varphi}{\partial\tau^2} + \frac{1}{Q}\frac{\partial\varphi}{\partial\tau} + \sin\varphi = \frac{I}{I_{C0}} \tag{2.33}$$

where $\tau = \omega_p t$ is a dimensionless time variable, $\omega_p = \sqrt{2eI_{C0}/\hbar C}$ is the plasma frequency of the junction and $Q = \omega_p RC$ is the quality factor of the junction. If $Q > 1$, the junction is said to be underdamped and if $Q < 1$ the junction is overdamped. In an overdamped junction the IV-characteristic is non-hysteretic, i.e., with increasing current the voltage will increase continuously. An underdamped junction exhibits hysteretic IV characteristics where the voltage upon increasing the current will abruptly jump from zero to $V \sim 2\Delta_{BCS}/e$. Here, Δ_{BCS} is the superconducting gap. On decreasing the current the voltage retraps to the zero value at a lower value of current.

One group of Josephson junction devices is based on Rapid Single Flux Quantum (RSFQ) technology. When an overdamped Josephson junction shunted with a resistor is biased with a DC current $I_B < I_C$, a small current pulse will then drive the total current above I_C and cause a phase shift of 2π (Josephson phase slip). Such a phase shift will cause a voltage pulse. The magnetic flux quantum $\Phi_0 = h/(2e)$ is the SFQ pulse [24]. The connection between the voltage and magnetic terminology is motivated by the Faraday's induction law that states that the electromotive force, ε, is equal to the time derivative of the magnetic flux, Φ, in a circuit, i.e.,

$$\varepsilon = \frac{d\Phi}{dt}.$$

The main sources of heat generation in superconducting circuits originate due to dissipation in the shunt and bias resistors (see Fig. 2.9). Obviously the electron temperature of the dissipative elements determines the fluctuation induced errors in the circuits and is responsible for the noise generated by the circuits. Therefore cooling of the bath should decrease the electron temperature in order to lower the noise of the devices. The weak electron - phonon interaction makes it difficult to lower the electron temperature by means of the surrounding bath. It is also an issue that the total power dissipated by standard Josephson junction based logic exceeds available cooling power of most dilution refrigerators.

Recent advances in quantum engineering ask for improved control electronics for the new type of devices. In practice the quantum bit (qubit) must be integrated with control and readout. The most important requirements for such electronics are low power dissipation, high operation speed, low bit error rate, small back-action and thermal compatibility, i.e., the control electronics should not disturb the temperature of the qubit. A candidate for realising the control electronics for qubits is Rapid Single Flux Quantum (RSFQ) technology. The basic component for this purpose is the balanced comparator. In principle a whole array

of circuit elements for binary operations is possible [24]. There are proposals to place RSFQ control electronics on the same chip as the qubit. This simplifies coupling between the qubit and the control electronics and reduces noise, but it also places stringent requirements on the power dissipation. Traditionally SFQ circuits have been developed for temperatures of 4.2 K or above. A new design based on standard technology has been developed by us together with VTT Technical Research Center of Finland and Chalmers University of Technology in Sweden to solve these basic shortcomings.

2.3.1 The Balanced Comparator

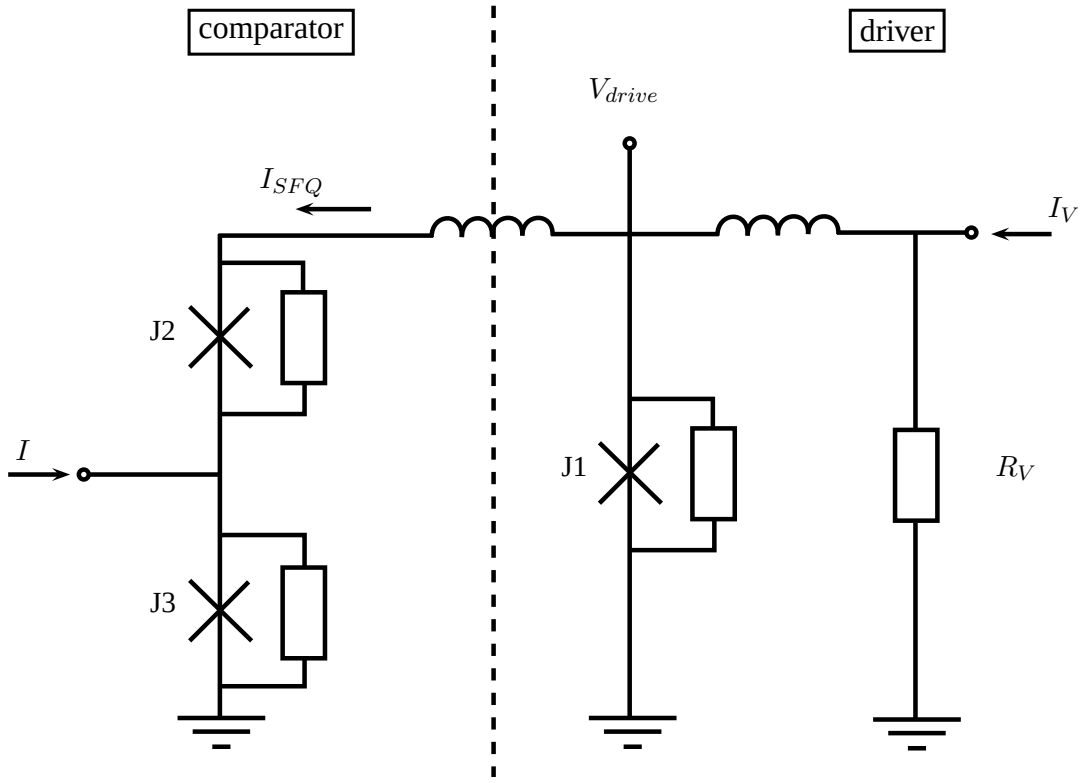

Figure 2.9: Sketch of the balanced comparator. J2 and J3 are mutually similar Josephson junctions. The driver generates SFQ pulses with a shunted Josephson junction, J1. The voltage over J1, that determines the frequency of the SFQ pulses is $V_{drive} = I_V R_V$. If I is positive, as shown here, I_{SFQ} enters the comparator and is added to I in the node between J2 and J3. Together both contributions to the current through J3 will induce switching in this junction.

The basic device in RSFQ technology is the comparator. It is a device for determining the sign of a current. A resistively shunted comparator is outlined in Fig. 2.9. If junctions J2 and J3 have values for critical currents that are close to each other, the comparator is said to be balanced [50]. The device is composed of a driver circuit and the comparator itself. The driver generates SFQ pulses that are propagated into the comparator, see Fig. 2.9. If the total current in one of the junctions exceeds the critical current, I_c, of the junction, the phase is switched by 2π and voltage develops. In the case of a balanced comparator the two nominally identical Josephson junctions have equal probability of switching. The device detects the sign of the current I in the leftmost terminal in Fig. 2.9. The driver circuit generates SFQ pulses at the Josephson frequency that brings the current over I_c. In other words, if $I > 0$ is satisfied, the Josephson junction J3 will experience a phase jump of 2π. If, on the other hand, $I < 0$ then J2 will switch. The switching of either J2 or J3 can be measured and thus the comparator can detect the sign of I.

The driver circuit consists of a resistively shunted Josephson junction. Using the notation in Fig. 2.9, the frequency ν of the SFQ pulses is expressed as

$$\nu = \frac{2eI_V R_V}{h}. \tag{2.34}$$

This assumes that the bias current has a negligible influence on the driving circuit. The reason for utilising a Josephson junction for generating the SFQ pulses is that the driver can be placed on the same chip as the comparator and, frequency is easy to control by means of I_V. The main drawback is that the shape of the pulses is hard to control.

2.3.2 Bit Error Rate and Greyzone

One of the most promising aspects of the RSFQ technology is the possibility for extremely low Bit Error Rate (BER) for this type of devices. The BER for RSFQ logic has been estimated to be as low as $\sim 1 \cdot 10^{-50}$ errors per bit [51] and experiments have indicated that this is not an unrealistic estimate [52]. A measure for the uncertainty of switching in the case of a comparator is characterized by the so called grey zone ΔI. It is most commonly defined as [53, 54]

$$\Delta I \equiv \left| \frac{dp}{dI} \right|^{-1}_{p=1/2} \tag{2.35}$$

where p is the switching probability. The grey zone depends on different factors such as temperature and frequency. The general behavior of the grey zone depends on the temperature at which the comparator is operated. The low temperature region is defined by $k_B T \ll \hbar\omega_c$, where $\omega_c = \frac{2eI_c R_s}{\hbar}$, is the characteristic

frequency of the overdamped Josephson junction and R_s is the shunt resistance. Here the grey zone is mainly determined by quantum fluctuations and it is temperature independent. The grey zone in the quantum limit is given by [54]

$$\Delta I \approx \sqrt{\frac{8e^2 I_c V_c}{\hbar}} \tag{2.36}$$

where $V_c = I_c R_s$. At higher temperatures, where thermal fluctuations become dominant, the greyzone is proportional to $\sqrt{T}$ [54]

$$\Delta I \approx 2\pi\sqrt{4\pi I_c I_T} \tag{2.37}$$

where $I_T = 2\pi k_B T/\Phi_0$. The crossover temperature between these two regimes is given by comparing Eq. (2.36) and Eq. (2.37) [54] and the result is

$$T_0 \simeq \frac{eV_c}{\pi k_B}. \tag{2.38}$$

As an example, for junctions fabricated with standard Nb trilayer of HYPRES 100 A/cm^2 technology [55], we have I_{c0} =6 μA and $R_s = 7.9\ \Omega$ [56]. The crossover temperature for these junctions is $T_0 \simeq 175$ mK, i.e. in the range of standard dilution refrigerator experiments. The most obvious way to decrease the grey zone is to operate the comparator at a low temperature down to T_0. When the temperature is reduced below T_0 the grey zone no longer depends on the temperature. It implies a twofold motivation for developing fabrication technologies with a lower critical current of the Josephson junctions. First, a smaller I_c will reduce the crossover temperature and thereby makes it possible to reduce ΔI by operating the comparator at a lower temperature. Moreover, the grey zone behaves as $\sim \sqrt{I_c}$ in the thermal regime. Samples based on HYPRES design rules have been developed by VTT to meet these new challenges. Characterisation of samples made with this new technology can be found in paper **I**. The switching probability p is descibed by the Gaussian cumulative distribution function (GCDF)

$$p\left(x\right) = \frac{1}{2}\left[1 + \mathrm{erf}\left(\frac{x}{\sqrt{2}}\right)\right], \tag{2.39}$$

$\mathrm{erf}(x) = \frac{2}{\sqrt{\pi}}\int_0^x e^{-t^2} dt$. The greyzone is related to the gaussian variance σ as $\Delta I_x = \sqrt{2\pi\sigma}$ [57]. In practice, the derivative of $p(x)$, i.e., the Gaussian distribution, is conveniently measured using lock-in techniques.

2.3.3 Power dissipation

One reason for investigating superconductor electronics as a candidate for integration with qubits is the low power dissipation of these devices. When integrating

qubits with control electronics there is a possibility that the control electronics will affect the proper operation of the qubit through back-action noise. Every switching event dissipates some energy in the shunting resistors of the RSFQ circuit and, as is shown in the next section, the ability to thermalise the resistor to the surrounding bath is of importance for the functionality of the device. If $\nu \ll \frac{1}{\tau_{e-p}}$, where ν is the RSFQ pulse repetition rate and electron-phonon relaxation time is given by [58]

$$\tau_{e-p} = \frac{\gamma_e T^3}{3\Sigma}, \tag{2.40}$$

the resistor will equilibriate with the bath temperature before the next RSFQ pulse arrives and there will be no significant overheating of the shunt resistor (see Fig. 2.10). As a numerical example consider a Josephson junction with a critical current $I_c = 10\ \mu$A. The energy dissipated by a single SFQ pulse is given by

$$Q_{SFQ} \approx I_c \Phi_0 \approx 2 \cdot 10^{-20}\ \text{J}. \tag{2.41}$$

The heat capacity of the electron gas C_e depends linearily on the electron temperature as $C_e = \gamma_e T_e$ [58–60]. Assuming a volume of the resistor $\Omega = 4 \cdot 10^{-18}$ m^3 and $\gamma_e = 70\ \text{m}^{-3}\text{K}^{-2}$ and electron temperature close to the bath temperature (~ 30 mK), we can estimate the temperature increase due to one SFQ pulse as

$$\Delta T_e = \frac{Q_{SFQ}}{C_e \Omega} = \frac{Q_{SFQ}}{\gamma_e T_e \Omega} \approx 3\ \text{mK}\ . \tag{2.42}$$

This temperature increase is about 10 % of the bath temperature. Now , if the period of the SFQ pulses is indeed larger than the electron-phonon relaxation time, τ_{e-p}, the average electron temperature of the device will stay close to the bath temperature with occasional peaks due to heating from the SFQ pulses, see Fig. 2.10(a). If, on the other hand, $\nu \gg \frac{1}{\tau_{e-p}}$, the average electron temperature will be higher than the bath temperature and it is determined by the average power dissipated in the resistor, see Fig. 2.10(b). When the device is operating at low temperature the overheating can be reduced by improving the energy flow between the (hot) electron system and the (cold) phonon system in the metal. This is in line with the recommendations of section 2.2.1, done by increasing the volume of the leads. Based on these considerations the new design for RSFQ electronics was developed and experimentally tested.

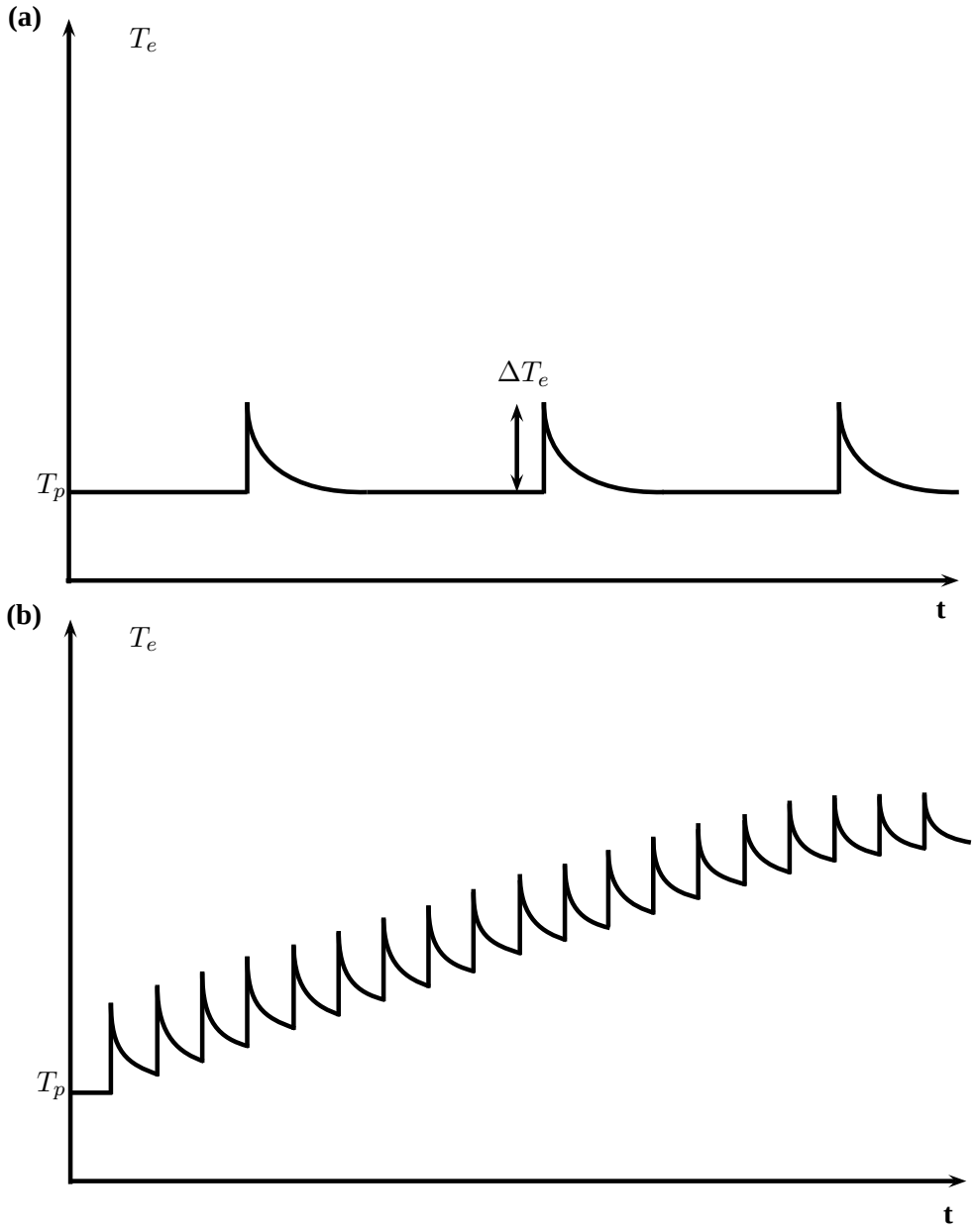

Figure 2.10: Electron temperature in the RSFQ device as a function of time. (a) If the frequency of the driver circuit is sufficiently low to allow the dissipated heat to be transported away to the surrounding bath, the temperature increase due to the dissipation will be small. In this case the energy pulse generates an increase of the electron temperature and subsequent relaxation at a frequency equal to $1/\tau_{e-p}$. (b) If the next RSFQ pulse arrives before the electron temperature in the circuit has had time to reach thermal equilibrium with the surrounding bath, the average electron temperature increases.

Chapter 3

Experiments

3.1 Fabrication of samples

The fabrication of samples took place in Micronova clean room facilities. The first samples were made for studies of the effect of double oxidation of tunnel junctions. These samples were CBTs with seven parallel arrays of 64 junctions in series with cooling fins in connection to the islands, see Fig. 3.1. The scheme for fabrication of the samples is summarized in Appendix A and below. Samples were fabricated on standard, undoped 4" silicon wafers (100) that had previously been thermally oxidized to a thickness of $\sim$ 300 nm.

Patterning was done with a Zeiss Supra 40 scanning electron microscope fitted with electrostatic beam blanker and pattern generator from Raith Gmbh [61]. Typical resist scheme was $\sim$ 2 μm thick copolymer (Polymethylmethacrylate-methyl acid acrylate) and 200 nm thick Polymethylmethacrylate (PMMA) on top. Exposure doses were typically $\sim 200\ \mu C/cm^2$. Exposed samples were developed in 10% DI water in IPA for 20-30 s at room temperature. In some cases the samples were further developed in a solution of methylglycol: methanol (1:3) for 5-15 s in order to increase the undercut. The bottom electrode was thermally evaporated in an e-gun evaporator with a base pressure $< 10^{-7}$ mbar. The bottom electrode was thermally oxidized in pure oxygen for 10 min at a pressure of 100 mbar. The top electrode was evaporated at an oblique angle. Lift-off was done in acetone bath heated to $\sim 60^\circ$ C, leaving the metallic patterns on the substrate surface. The procedure in the work related to paper II is summarized in Appendix A. In order to increase the resistance of large area tunnel junctions, a thin layer of aluminum (approximately 0.6 nm) was deposited on top of the already oxidized layer and the oxidation step was repeated before depositing the top electrode.

The sample type described above also served as a basis for the first attempts of adding larger blocks of metal in order to improve thermalisation of the CBT.

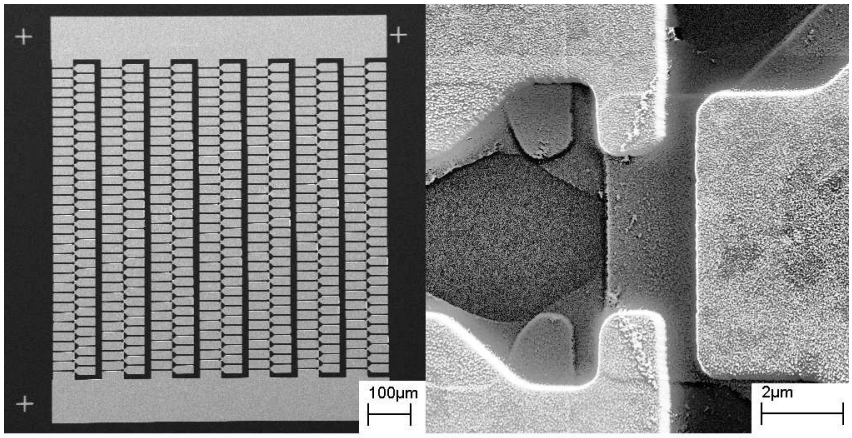

Figure 3.1: Test structure for the double oxidation sample. The sample consists of seven rows of 64 junctions in series. (a) An overview of the whole structure. The crosses in the corners of the structure are alignment marks for overlay exposures. (b) Two junctions with higher magnification.

However, as the work progressed to involve the use of mechanical shadow masks instead of the standard lift-off techniques, samples with fewer junctions were used instead. Attempts were made to improve thermalisation of the CBT by depositing a second layer of copper on top of the cooling fins of the double oxidation samples (see Appendix A). Another resist layer with the same specifications as for the fabrication of CBTs was deposited on top of the existing CBTs and it was exposed and developed to open up areas on top of the cooling fins. Another layer of copper was then deposited orthogonally to the surface to a total thickness of 1.7 μm after being subjected to argon plasma in order to clean the surface. Figure 3.2(a) shows that the alignment procedure for overlay exposures using the alignment marks seen in Fig. 3.1 (a) works well enough for our purposes. This procedure for achieving thicker additional layers is limited by the electron penetration depth in PMMA. Due to this limit, we aligned a mechanical mask to an underlying structure consisting of a 30 junction CBT instead. The deposition was performed with a suitable spacer (bonding wire with a diameter of 20 μm) between the evaporation mask and the substrate. The mask consisted of a silicon membrane that was etched out to a thickness of 20 μm [62]. The openings in the membrane were lithographically defined to match the layout of the CBT layer. The silicon membrane was etched either in a heated KOH bath at 70° C for a specified amount of time or by cryogenic reactive ion etching. After making the membrane, the openings were defined by optical lithography. They were then dry

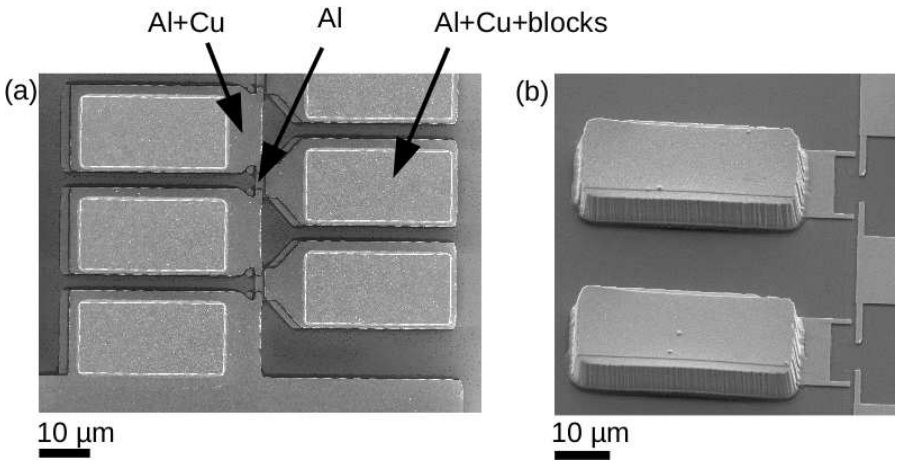

Figure 3.2: (a) Test structure for the double oxidation sample with 1.5 μm copper on top of the cooling fins textcolorredwith 0.2 μm copper deposited in the same vacuum cycle as the junction layers. This second layer was deposited after an overlay exposure utilizing the alignment marks shown in Fig. 3.1. (b) CBT with thick copper blocks ($\sim$ 5.7μm thick) deposited through a mechanical mask aligned to the underlying CBT structure.

etched at low temperatures (-110° C) to produce vertical sidewalls.

In order to investigate the influence of the electromagnetic environment of the tunnel junctions, SJT samples were fabricated using the standard procedure outlined above. Since they were not intended for measurements at the lowest temperatures, the cooling fins were omitted in this case.

The RSFQ samples were fabricated by VTT. They utilised a tri-layer Nb process resulting in Josephson junctions with a current density of 30 A/cm^2. For this purpose the fabrication process was based on optical lithography, sputtering of the Nb layers and etching of the lithographically defined structures, instead of the lift-off process used for the other structures presented in this thesis.

3.2 Measurements

Low temperature measurements were performed in ^{3}He/^{4}He dilution refrigerators. The doubly oxidized samples were first measured in a fridge with a base temperature of < 20 mK. Measurement lines were filtered with 2 m of thermocoax cable. In order to verify the effect of large copper blocks on the cooling fins, measurements of these samples were performed on a dilution refrigerator equipped

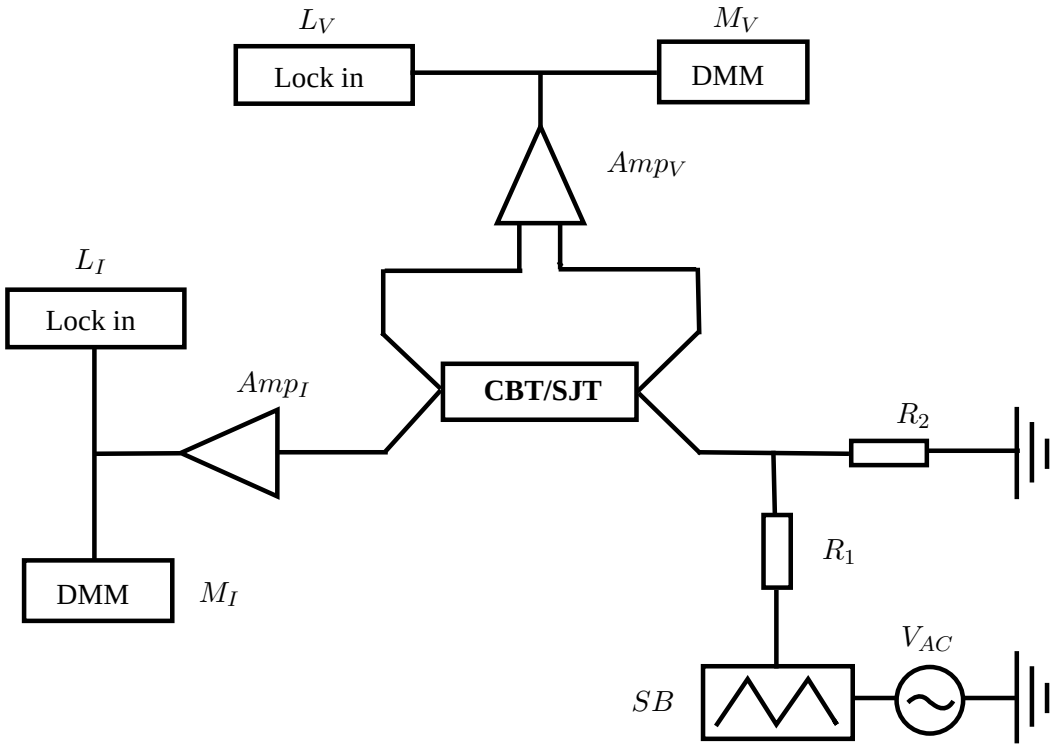

Figure 3.3: Circuit for temperature measurements. In the diagram Amp_I is current amplifier, Amp_V is voltage amplifier, L_I and L_V are lock in amplifiers (Stanford Reasearch SR 830) where the ac signals dI and dV were measured respectively. M_I and M_V are digital multimeters and R_1 and R_2 are resistors that together form a voltage divider for adjusting the range of the voltage source, SB. V_{AC} is the alternating voltage provided by the internal oscillator of the lock in amplifiers.

with a ^{3}He melting curve thermometer, which extended the measurement temperature range to below 6 mK. The available measurement lines consisted of coaxial cables. All other low temperature measurements were performed in a plastic dilution refrigerator (PDR 50) with a base temperature of about 30 mK. The measurement lines were all filtered with 2 m of thermocoax cable in this case as well. Here we could control the bath temperature that was measured with a ruthenium oxide resistor calibrated against a CBT thermometer.

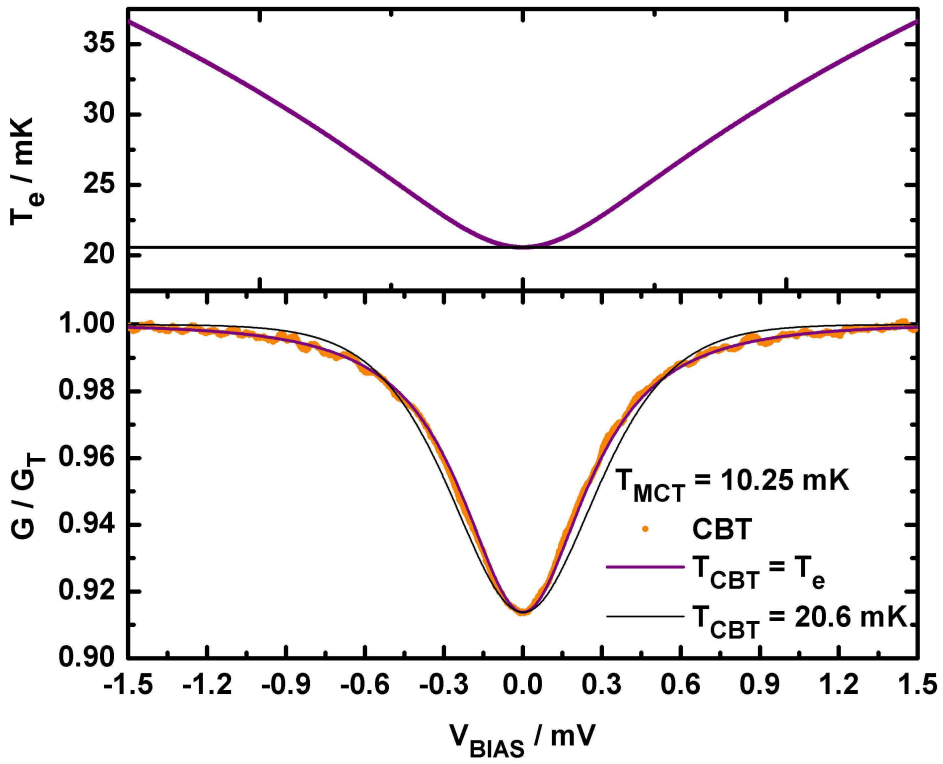

Figure 3.4: Measurement of one double oxidation sample with extra copper blocks at constant bath temperature, $T_{MCT} = 10.25$ mK, determined by a melting curve thermometer. This sample was of the type shown in Fig. 3.2 (a) and consisted of seven parallel arrays of 64 junctions. (Top) Electronic temperature of the CBT calculated as a function of applied bias voltage with added noise heating. (Bottom) CBT measurement using the scheme shown in Fig. 3.3. The measured data points (orange dots) compared with the calculated conductance curve for constant electron temperature, $T_e = 20.6$ mK(thin black line). The CBT showed a temperature $T_{CBT} = 20.6$ mK determined by noise heating. Solid magenta line is calculated curve for $T_{CBT} = T_e(V_{bias})$ from top panel. (Unpublished M. Meschke, T. Holmqvist, H. Junes and I. Todoshchenko)

3.2.1 Thermalisation

The low temperature measurements were performed in order to verify if the added cooling fins had the intended effect. The samples were of the type shown in Fig. 3.2 and they were fabricated as outlined in Appendix A. If thermalisation is insufficient we expect to see a a decreased half width and somewhat suppressed depth of the conductance curve due to noise heating [63]. Self heating due to biasing of

the thermometer will be minimal at zero bias, thus the electronic temperature of the thermometer is affected only by external noise. As the bias voltage increases the thermometer heats up and the conductance curve is gradually changed to a curve with smaller depth and larger half width, corresponding to this higher temperature. This typically results, counterintuitively, in a lower temperature reading than expected if the temperature is measured via the half width of the conductance curves [63].

The electronic temperature of each island with respect to the lattice temperature is determined, in a uniform array, approximately by Eq. (2.23) with $\dot{Q} = (V/N)^2/R_J + \dot{Q}_n$, where R_J is the resistance of one junction and $\dot{Q}_n$ is the heating power due to noise. The explicit expression for the electron temperature is

$$T_e = \left(\frac{(V/N)^2}{R_J \Sigma \Omega} + \frac{\dot{Q}_n}{\Sigma \Omega} + T_{ph}^5 \right)^{\frac{1}{5}}. \tag{3.1}$$

For copper $\Sigma = 2 \cdot 10^9$ WK^{-5}m^{-3} [11, 48]. The volume of the cooling fins is deduced from a fit using the calculated conductance curve according to [9] with $T_e(V_{bias})$ from (3.1) and the measured curve at a fixed bias point. This method gives the volume of the copper in the cooling fin to $\Omega = 225$ μm^3 within a confidence interval of ± 10 μm^3 in the case of the double oxidation samples. This is comparable to the estimated volume of the Cu cooling fins under the thick copper blocks (~ 2000 μm^3), thus suggesting that the added extra copper blocks did not have the desired effect. The noise power can be determined at the zero bias point. $\dot{Q}_n$ is found to be 1.6 fW in the performed measurements.
The use of the mechanical mask resulted in sufficiently thick copper blocks with good aspect ratio as can be seen in Fig. 3.2 (b), but due to poor adhesion to the underlying structure these samples were not measured at low temperatures.

3.2.2 Characterisation of junctions

One method of determining the quality of a tunnel junction is to measure the temperature dependence of its resistance. A generally accepted rule of thumb is that an aluminum - aluminum oxide junction should exhibit an increase of resistance of approximately 15 % when cooled from room temperature to liquid helium temperature (4.2 K) in order to possess good tunneling characteristics [64–66]. A comparison between single and double oxidation samples is summarized in Table 3.1. The double oxidation step resulted in larger resistance by close to one order of magnitude, while still meeting the criterion for quality.

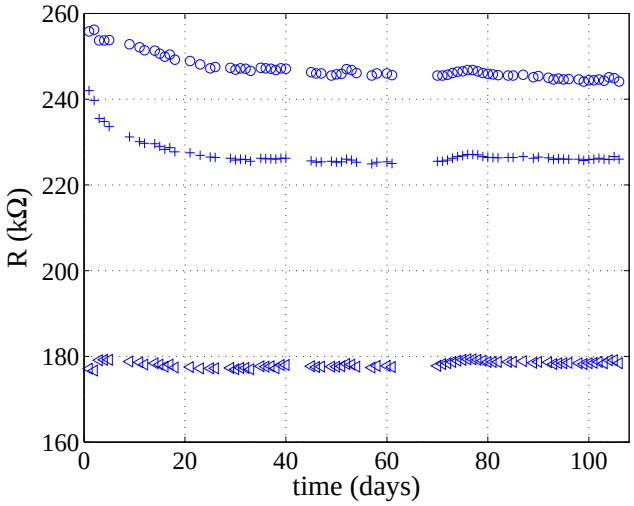

Figure 3.5: Room temperature resistance of three doubly oxidized samples against time as they were stored in air at room temperature.

Long term drift of junction parameters is a problem general to all metal tunnel junctions. This drift can be attributed to diffusion of oxygen from the oxygen rich compound formed on the surface during oxidation to the underlying metal, and subsequent relaxation to the stoichiometricly stable Al_2O_3. In order to test whether doubly oxidized junctions are robust against aging effects, three samples fabricated in the same vacuum cycle were monitored over a period extending about 100 days while the junctions were stored in ordinary air at room temperature. The corresponding resistance data are plotted in Fig. 3.5. The largest change in resistance happens during the first 5-10 days, and thereafter the junc-

Table 3.1: Samples fabricated and characterised to test double oxidation. The two first batches were fabricated with the standard single oxidation of aluminum. R_C^{RT} is the characteristic resistance at room temperature, and R_C^{LHe} that at 4.2 K. ΔR_C is defined as $\Delta R_C = R_C^{LHe} - R_C^{RT}$.

Batch	Oxidation pressure	Oxidation time	R_C^{RT}	R_C^{LHe}	$\Delta R_C/R_C^{RT}$
1	100 mbar	10 min	3.24 k$\Omega\mu$m^2	3.78 k$\Omega\mu$m^2	17 %
2	200 mbar	60 min	6.14 k$\Omega\mu$m^2	7.60 k$\Omega\mu$m^2	24 %
3	100 mbar	10 min	37.12 k$\Omega\mu$m^2	45.22 k$\Omega\mu$m^2	22 %
4	100 mbar	10 min	33.3 k$\Omega\mu$m^2	39.82 k$\Omega\mu$m^2	16 %
5	100 mbar	10 min	58.3 k$\Omega\mu$m^2	71.5 k$\Omega\mu$m^2	23 %

tions are stable.

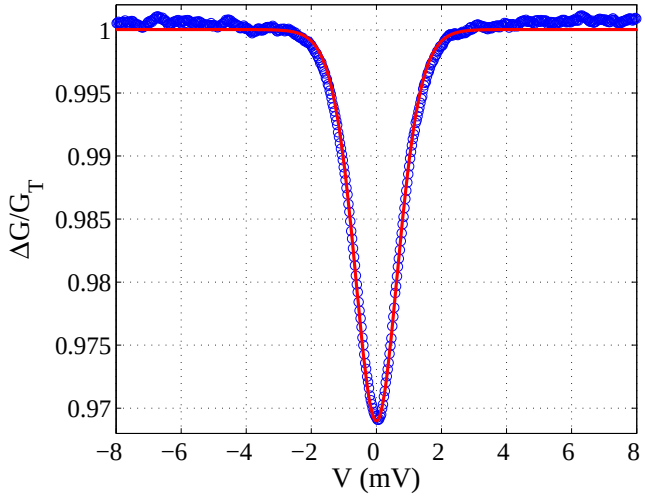

Figure 3.6: Conductance peak of a doubly oxidized sample with 64 junctions from batch 3 in Table 3.1 . The blue circles are the measurement data and the red line is the fittted curve. The fit yields a temperature of 48.5 mK. The capacitance is in this case approximately 90 fF/μm^2 giving a charging energy of $E_C = 5$ mK.

In order to extract the capacitance of the tunnel junctions Coulomb blockade peaks were measured at low temperatures, see Fig. 3.6. The capacitance of the junctions can be determined from Eq. (2.19). The capacitance per area was found to be 68 fF/μm^2 which is in line with values found in literature for Al/AlO$_x$/Al junctions [67–72]. To determine the thickness and height of the barrier formed by double oxidation technique the Simmons model was applied to conductance data measured at 77 K. The resulting curve, shown in Fig. 3.7, was used to fit a parabola, see Eq. (2.2). The fitting of the measured data yielded a barrier height of 3 eV and a barrier thickness of 12 Å wich is not inconsistent with values in literature [66].

3.2.3 Temperature measurement (CBT and SJT)

Temperature was measured by the SJT and CBT by acquiring the conductance versus bias voltage data in a four probe configuration and determining $V_{1/2}$. The measurement set up is shown in Fig. 3.3. The influence of the junction environment was experimentally verified by comparing conductance peaks of the embedded one and two junction samples with the same structures but without

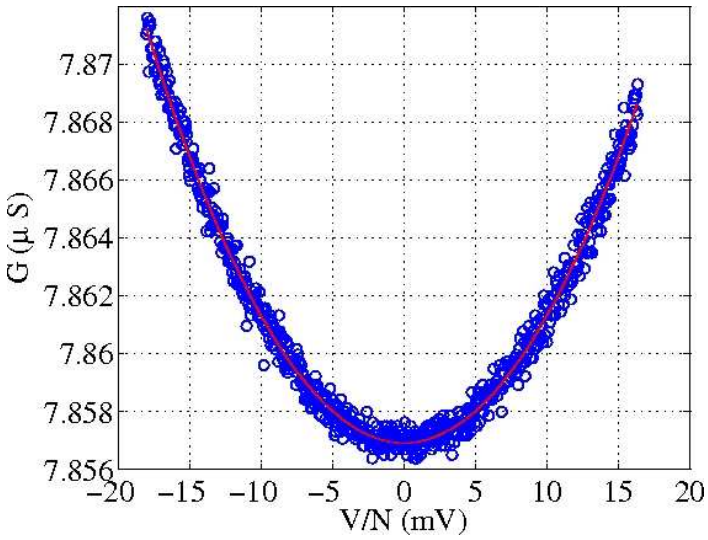

Figure 3.7: Measured conductance curve of the doubly oxidized structure measured at 77 K (blue symbols). The red line shows the parabolic fit to extract barrier parameters. The barrier height was 3 eV and the barrier thickness was 1.2 nm.

the embedding junctions, as shown in Fig. 3.8. Calculations show that errors due to environment noise in the background can be suppressed by embedding the thermometer in a high impedance circuit, see publications **IV** and **V**. As a proof of the concept, the SJT measurements were also done to demonstrate the functionality of the SJT and validate that the embedding junction arrays had the intended effect on the accuracy of the temperature measurements.

The cryostat was equipped with a resistance thermometer (CERNOX) but to ensure that there are minimal temperature gradients between the SJT and the thermometer, regular CBT measurements were performed on one of the embedding arrays ($N = 20$) and this was used as reference thermometer.

The sample made to verify the concept of the SJT is shown in Fig. 3.8 (a). It is a single junction with an area of 0.6 μm^2. The top panel show a junction with four metal leads, the middle panel shows a junction embedded in four arrays of 20 junctions each to provide a controlled electromagnetic environment. In Fig. 3.8 (c) a measured conductance curve of this sample at 0.3 K is shown for both the junction embedded in an array of tunnel junctions (green line) and the junction without this protective environment (red line). The curves are normalized to the assymptotic conductance. The measured widths of the curves compare well with the calculated ones assuming environment of $R = 80\ \Omega$, shown as solid lines in

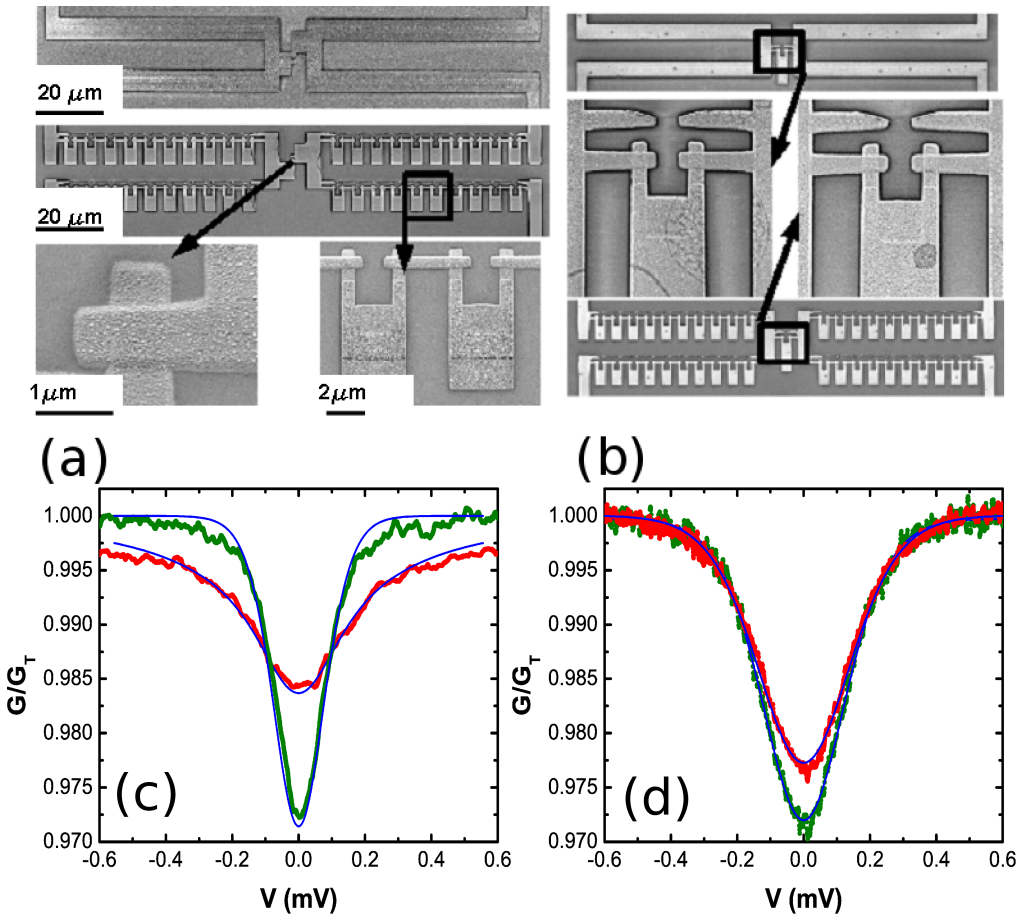

Figure 3.8: (a) An SJT sample both without (top) protective junction environment and with it (middle). In the bottom panel a zoom of the single junction (left) and junctions in the array (right) are shown. (b) The corresponding two junction sample. (c) Normalized conductance peaks of protected (green line) and unprotected (red line) SJT measured at 0.3 K. Solid lines are curves fitted according to Eq. (2.22). (d) Corresponding normalized conductance peaks for a two junction system measured at 0.32 K.

Fig. 3.8 (a) with $N = 1$ for the unprotected junction and with $N = 21$ for the protected one. A two junction system was also investigated in the same way. The structure is shown in Fig. 3.8 (b). The width of the conductance curve for the unprotected system shown in Fig. 3.8 (d) also compares well with the calculated one, now for $N = 2$ and $R = 80\ \Omega$. Figure 2.5 shows the rapid decrease in the deviation from $T = V_{1/2}e/5.439Nk_B$, as the number of junctions forming the

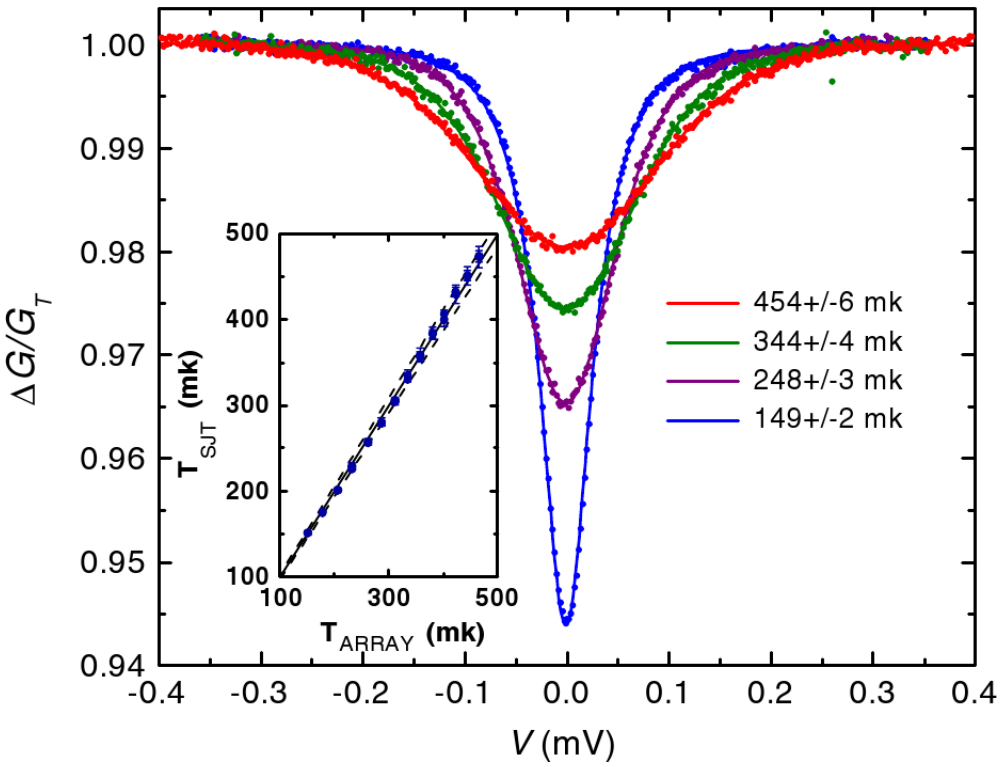

Figure 3.9: Four SJT conductance peaks measured within the range 150 mK - 500 mK on a SJT protected with arrays of junctions. A model for overheating was incorporated in the fitting procedure as described in the text. The insert shows temperature measurements of the SJT vs temperature measured with one of the arrays as a regular CBT. Over the whole range between 100 mK - 500 mK the discrepancy between the two thermometers is well within 5 % indicated by the dashed lines.

electromagnetic environment increases. This is thus fully demonstrated by the measurements in Fig. 3.8 (c) and (d). For the protected single and two junction samples (green lines in Fig. 3.8 (c) and (d) respectively) there is good agreement in temperature reading with Eq. (2.20), as one would expect.
Too large excitation voltage of the lock-in amplifier induces a smearing of the peaks resulting in a higher temperature reading while too low excitation level results in a noisy measurement. As a general rule of thumb an excitation of $1-10$ % of $V_{1/2}$ is considered good. The model used for the fitting of measured conductance curves to the theoretical curve, incorporated a model for self heating were the fact that the peaks become shallower and wider as temperature increase is incorporated as described in [63]. As can be seen in Fig. 3.9 the fitting to

the measured data was very good in the measured range between 150 mK and 500 mK. The temperature derived from the fits differed from the ones obtained from the reference CBT measurements by less than 5 %. Measurements at lower temperatures were not considered since these samples did not include cooling fins for thermalisation.

3.2.4 Grey-zone measurements of the balanced comparator

Presently the most well known source of commercial RSFQ circuits is based on design rules developed by HYPRES. There are some limitations in these design rules. An obvious one is that the smallest allowed critical current for their Josephson junctions is about $I_c = 30$ μA. As mentioned before it is of prime interest to reduce the critical current in order to achieve a smaller grey zone. Balanced comparators were developed and manufactured by VTT and grey zone measurements were performed on the comparators. The results are presented in paper **I**.

During the measurements the driving frequency of the SFQ pulses was kept

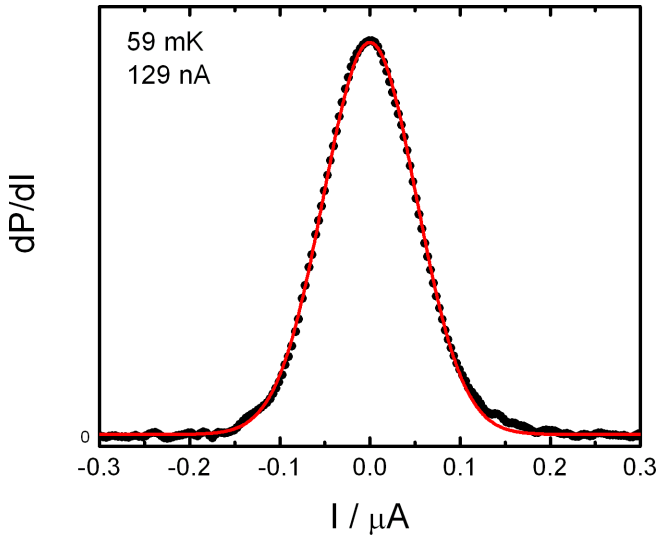

Figure 3.10: A typical result of a greyzone measurement. This experiment was done at 59 mK on a sample with cooling fins.

constant at $\nu = 2$ GHz. The measurements were performed at cryostat temperatures from 50 mK up to above 4.2 K. The measured comparators had a critical current of $I_{c0} = 2.1$ μA, shunt resistances were $R_s = 15.4$ Ω and the volume of the cooling fins attached to the shunt resistors were $V = 4 \cdot 10^5$ μm^3. These values yield a crossover temperature of $T_0 = 120$ mK, see Eq. (2.38). The grey

zone was measured by lock-in technique. One such measurement is presented in Fig. 3.10 where a grey zone measurement is shown for a bath temperature of 59 mK. This sample was a comparator with added cooling fins on the shunting resistors. Measurements of the grey zone were done both on comparators with cooling fins attached to the resistors, and comparators without cooling fins, see Fig. 3.11. The grey zone for the samples without cooling fins saturate slightly below 300 nA at a temperature of about 0.5 K. For the samples with enhanced thermalisation the grey zone deviates from the theoretical thermal dependence (marked as dashed line in Fig. 3.11) below temperatures of 200 mK and saturates at about $\Delta I = 130$ nA.

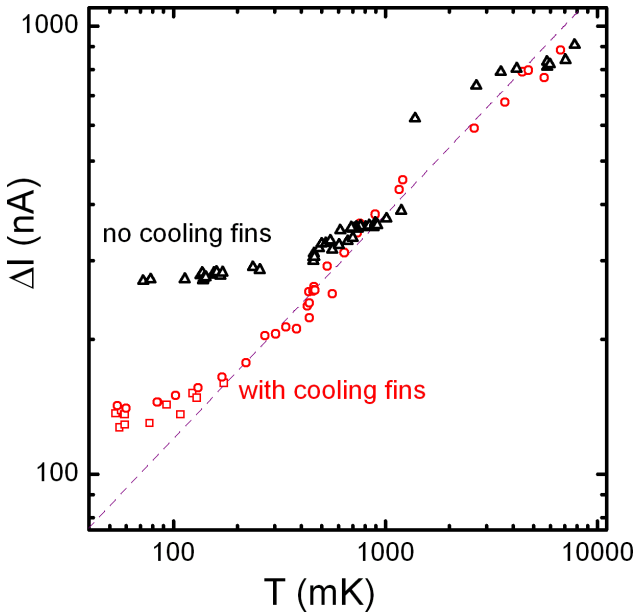

Figure 3.11: Greyzone of the RSFQ comparators as a function of temperature. Triangles show greyzone for comparator without cooling fins. Circles and squares show comparators with a cooling fin. The devices without cooling fins have a larger greyzone at low bath temperatures.

3.3 Conclusions and outlook

3.3.1 Thermalisation

In the case of the balanced comparator the cooling fins attached to the shunting resistors served to thermalize them. In this case an increase of the volume of

the shunting resistors had the desired and expected effect. Due to the relatively high operating temperature of these devices (200 mK - 500 mK) the samples could be manufactured with essentially the same technology as that used for standard Integrated Circuit (IC) fabrication. In the case of the CBTs, noise heating prevented us from reaching the limit of thermalisation for the volume of copper without extra blocks, i.e. $0.75 \cdot 10^{-15}$ m^3. The thermometer saturated at around 20 mK. In order to reach 10 mK saturation temperature, a volume of $3{\cdot}10^{-15}$ m^3, or a thickness of 5 μm would have been needed. We made an attempt to realize such blocks. The result was not satisfactory because of the adhesion problems still to be solved. The CBT saturated as if there were no extra copper blocks. This could indicate that even if the copper blocks did not actually fall off from the cooling fins, there is still an interface formed between the thin (~ 0.2 μm) copper layer deposited in the same vacuum cycle as the CBT layer and the extra copper blocks, even after cleaning the underlying layer in Ar plasma. The samples with copper blocks deposited through a mechanical mask were not characterized at low temperature as the adhesion problem was obvious by visual inspection. A successful method for thermalizing a CBT with large volume cooling fins would be directly applicable to the SJT as well.

3.3.2 Double oxidation

The method of double oxidation resulted in high quality tunnel junctions with increased specific resistance as planned. Barrier thickness, barrier height and capacitance of these junctions were in line with what is normally achieved with conventional fabrication methods while the resistance was one order of magnitude larger than using conventional techniques. The double oxidation gives a possibility to adjust the resistance of tunnel junctions without compromising the junction quality.

3.3.3 Junctions as thermometers

The environment of the SJT was controlled by embedding the thermometers within arrays of tunnel junctions. A comparison between measured conductance curves in Fig. 3.8 and calculated curves in Fig. 2.5 show that for both the SJT and the two junction system, embedding them effectively leads to results that are consistent with the basic thermometer formulas. The difference between the unprotected one and two junction samples is also noteworthy and follows the predictions from the environment theory. As expected from Fig. 2.5 (a) already one additional junction has a noticable effect on the conductance curves. The SJT does not suffer from the uncontrolled error common in standard CBTs, i.e. spread of junction parameters. It is also possible to effectively reduce the impact

of environmental noise by embedding the device in a controlled environment of tunnel junctions. The drawback of the SJT as compared to CBT is the smaller width of the conductance peak, which is directly proportional to the number of junctions. This makes measurements more demanding, in particular at very low temperatures.
At the time of writing this thesis there are unpublished developments in collaboration between TKK and NEC Nanotechnology Laboratory to make an SJT for measurements up to 77 K. Such a device is shown in Fig. 3.12 with preliminary measurements. One challenge is making the tunnel junction sufficiently small for this temperature range. As the spread in junction parameters is not an issue for SJT, this is quite feasible. Another problem arising at higher temperatures is that the environment must be placed closer to the junction for it to be effective. This is also in essence a fabrication problem that appears to be manageable.

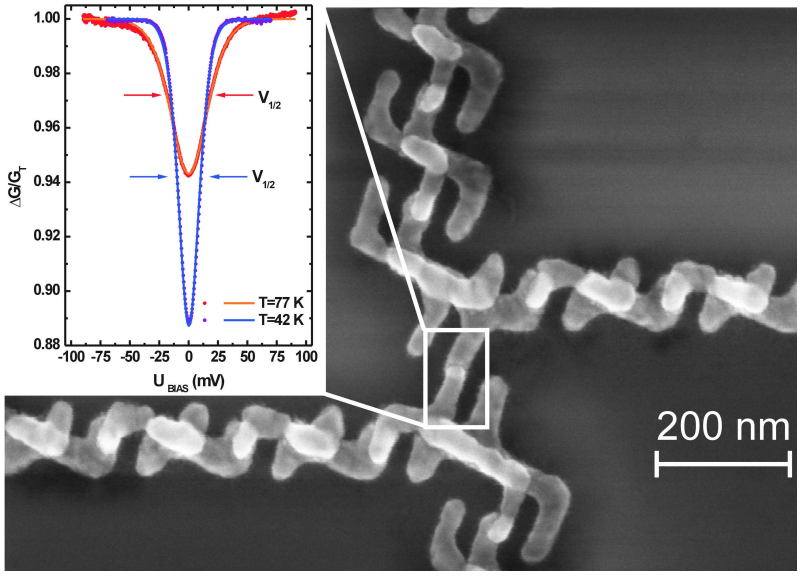

Figure 3.12: SJT made with sub 100 nm junctions, intended for temperature measurements up to 77 K. The insert shows preliminary measurements of the SJT. (Unpublished M. Meschke, J.P. Pekola and Yu. Pashkin.)

Ongoing efforts to verify the SJT against present temperature standards are also under way. Preliminary results, in a collaboration between TKK and PTB, shown in Fig. 3.13 appear promising.

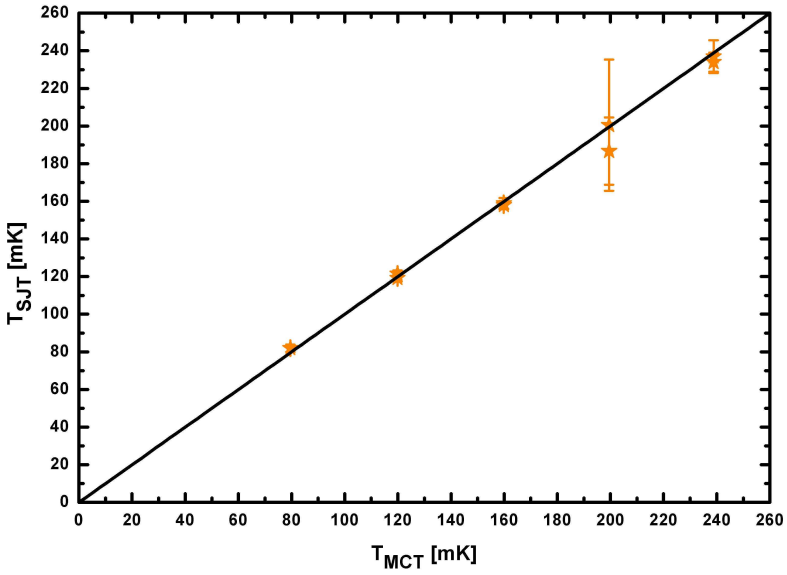

Figure 3.13: An SJT measured against a MCT at PTB Berlin. (Unpublished M. Meschke, J.P. Pekola and J. Engert.)

Appendix A

Fabrication of the double oxidation samples

This recipe was used for fabrication of the double oxidation sample.

1. Spin 3 layers of copolymer (PMMA-MAA 8.5 % in ethyl lactate) at 4000 rpm for 40 s. Bake on hot platefor 10 min. at 180°C after every layer. This gives a thickness of approximately 1.7 μm.
2. Spin top layer (PMMA 2 % in anisole) at 4000 rpm for 40 s. Bake for 10 min. at 180° C. The top layer has a thickness of approximately 100 nm.
3. Expose sample with an area dose of $\sim$ 200 μC/cm^2.
4. Develop for approximately 30 s at room temperature in a solvent consisting of 10 volume % DI water in isopropanol (IPA).
5. Develop for 5-15 s in a solvent of 25 volume % methylglycol in methanol.
6. Evaporate aluminum at an obligue angle to a thickness of 45 nm when the pressure in the vacuum chamber reaches $1{\cdot}10^{-7}$ mbar.
7. Oxidize in pure oxygen at a pressure of 100 mbar for 10 min.
8. Evaporate $\sim$ 0.6 nm aluminum without changing angle.
9. Repeat step 7.
10. Change angle and evaporate 50 nm aluminum to form the top electrode.
11. Evaporate 0.2 - 0.5 μm copper without changing the angle.
12. Lift-off in acetone heated to 60° C.

For samples with additional copper blocks on top of this structure, the following steps were employed.

- Repeat steps 1 and 2
- Align writefield to the sample using alignment marks on the sample [28].
- Expose fields on top of the structure where the thick copper blocks are meant to be.
- Develop according to steps 4 and 5.
- Clean sample in Ar plasma.
- Evaporate 1.5 μm copper at an angle perpendicular to the sample surface.
- Lift-off in acetone heated to 60° C.

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