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Millimeter-Wave Integrated Circuits in 65-nm CMOS

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***Abstract*—We present the design and measurement results of millimeter-wave integrated circuits implemented in 65-nm baseline CMOS. Both active and passive test structures were measured. In addition, we present the design of an on-chip spiral balun and the transition from CPW to the balun and report transistor noise parameter measurement results at V-band. Finally, the design and measurement results of two amplifiers and a balanced resistive mixer are presented. The 40-GHz amplifier exhibits 14.3 dB of gain and the 1-dB output compression point is at +6-dBm power level using a 1.2 V supply with a compact chip area of 0.286 mm^2. The 60-GHz amplifier achieves a measured noise figure of 5.6 dB at 60 GHz. The AM/AM and AM/PM results show a saturated output power of +7 dBm using a 1.2 V supply. In downconversion, the balanced resistive mixer achieves 12.5 dB of conversion loss and +5 dBm of 1-dB input compression point. In upconversion, the measured conversion loss was 13.5 dB with −19 dBm of 1-dB output compression point.**

***Index Terms*—Amplifiers, baluns, downconversion, millimeter-wave integrated circuits, MMICs, noise-parameter measurements, resistive mixers, silicon, slow-wave transmission lines, upconversion, 65-nm.**

I. Introduction

RECENTLY, there has been enormous development in the field of silicon integrated circuits operating at millimeter-wave frequencies. High performance millimeter-wave amplifiers in 130-nm and 90-nm CMOS technologies have been reported in [1]–[5]. The demand for high-speed short-range communications and the unlicensed wide bandwidth around 60 GHz have motivated the development of CMOS-circuits at V-band. Receiver circuits fabricated in 130-nm and 90-nm CMOS operating at V-band have been reported in [6]–[8]. A transmitter including an on-chip antenna and a transceiver in 130-nm CMOS have been demonstrated in [9] and [10], respectively.

As the device scaling of nanoscale CMOS technologies results in a higher unity gain frequency and maximum frequency of oscillation of the transistor, improved performance at millimeter-waves is expected. However, the continuing scaling of bulk CMOS process produces typically some challenges for the designer such as lower supply voltage, stringent metal density requirements and thinner dielectric layers above the substrate leading to higher substrate losses of passives. In this paper, we examine the suitability of 65-nm baseline CMOS technology for millimeter-wave operation. No additional options were employed in the fabrication process. The presented results are from the first design cycle.

We motivate the study by first presenting the measured noise parameter data of a $\mathrm{W/L} = 90/0.07$-sized transistor at V-band. Measurement results of passive elements such as conventional and slow-wave coplanar waveguides and standard finger capacitors are presented. In addition, we present the design of a wideband spiral transmission line balun and a transition from CPW to the balun in a deep submicron CMOS. We use the spiral transmission line balun in a highly linear V-band balanced resistive mixer that is suitable for both up- and downconversion [11]. In downconversion, the mixer achieves 12.5 dB of conversion loss and +5 dBm of 1-dB input compression point. In upconversion, the measured conversion loss was 13.5 dB with −19 dBm of 1-dB output compression point. We also demonstrate millimeter-wave amplifiers achieving state-of-the-art-performance in CMOS [12]. The 40-GHz amplifier exhibits 14.3 dB of small-signal gain occupying a chip area of 0.286 mm^2 only. The 1-dB output compression point is at +6-dBm power level using a 1.2 V supply. The 60-GHz amplifier achieves better than 11 dB of small-signal gain from 45 to 65 GHz. The measured noise figure is 5.6 dB at 60 GHz. The AM/AM and AM/PM characteristics of the 60-GHz amplifier chip were extracted from the large-signal S-parameter measurement results. The saturated output power is +7 dBm at 60 GHz using a 1.2 V supply.

II. Active and Passive Circuit Blocks

A. Transistor

The cascode topology achieves good isolation, high gain, good stability and low power consumption. As the operation frequency increases, the effect of the capacitances of the transistors becomes more pronounced. For example, resonating out the capacitances at the drain of the input transistor stage may improve performance. By using a common source topology the output voltage and current swings can be maximized. Thus, a high output power and good linearity can be achieved. This is especially beneficial when using a lower supply voltage. Although, the weak isolation of the common source topology makes the design challenging, low noise figure and good gain are feasible at millimeter wave frequencies. Anyhow, the choice of the transistor at millimeter-wave frequencies is not obvious because the transistor geometries and this way the parasitic capacitances have a strong influence on the millimeter wave performance of the chosen topology.

In this work, the selection of the transistor topology is based on a limited set of common-source transistors, which were available for preliminary measurements before the first

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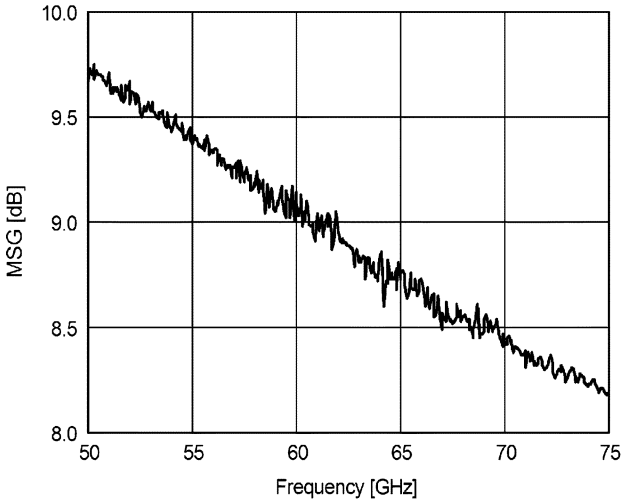

Fig. 1. Measured maximum stable gain of the $\mathrm{W/L} = 90/0.07$-sized transistor at V-band. $V_{DS} = 1.2$ V, $I_{DS} = 18$ mA.

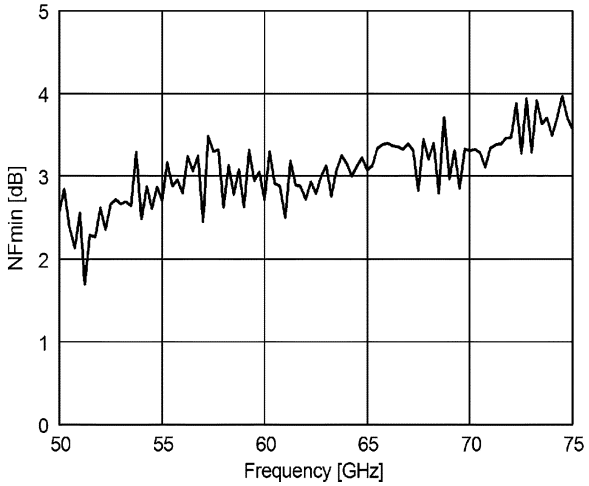

Fig. 2. Measured minimum noise figure of the $\mathrm{W/L} = 90/0.07$-sized transistor. $V_{DS} = 1.2$ V, $I_{DS} = 18$ mA.

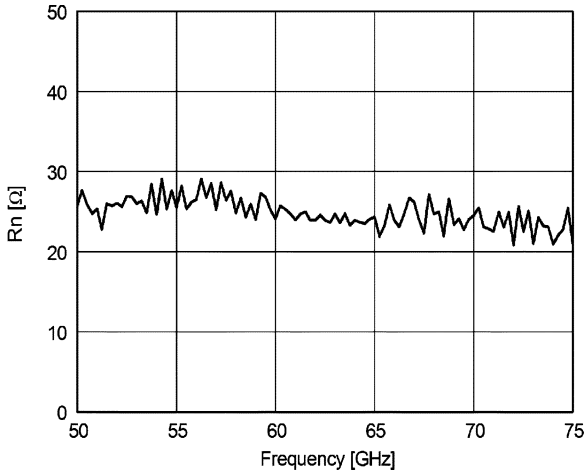

Fig. 3. Measured noise resistance of the $\mathrm{W/L} = 90/0.07$-sized transistor. $V_{DS} = 1.2$ V, $I_{DS} = 18$ mA.

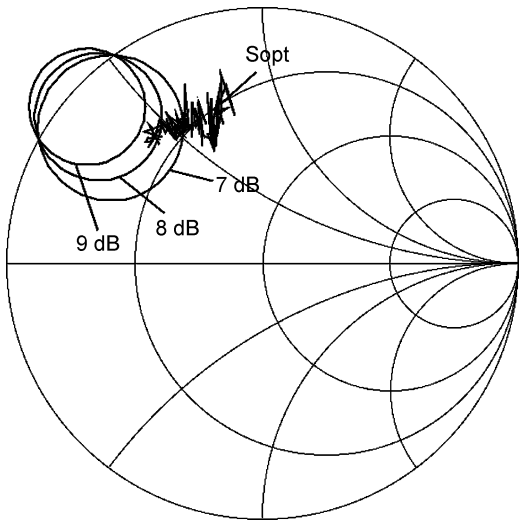

Fig. 4. Measured optimum noise match (S_{opt}) at V-band (50–75 GHz) of the $\mathrm{W/L} = 90/0.07$-sized transistor. Gain circles are drawn for 7, 8, and 9 dB levels at 60 GHz.

design cycle. Based on these test transistor measurements, a $\mathrm{W/L} = 90/0.07$-sized transistor was chosen as a suitable device for the amplifier designs. The same transistor size was used in the mixer design as well.

To capture the millimeter-wave behavior of the transistor, a coplanar waveguide test-structure for the transistor as well as corresponding open and short structures were developed. The measured S-parameters were open-short de-embedded [13]. The measured maximum stable gain is shown in Fig. 1. The maximum stable gain is 9 dB at 60 GHz.

To model the noise behavior of the transistor, the noise parameters of the transistor test-structure were measured and de-embedded. The noise contributions of the shunt admittances and series impedances of the test structure were subtracted from the measured data by using the correlation matrix method [14]. The on-wafer noise parameter measurement setup is described in [15]. The measured minimum noise figure, noise resistance and optimum noise match are presented in Figs. 2–4 for the chosen transistor size and 18 mA bias point. The minimum noise figure is around 3.0 dB at 60 GHz.

B. Conventional Coplanar Waveguide and Slow-Wave Coplanar Waveguide

A coplanar waveguide (CPW) was chosen as a suitable topology for on-chip matching and interconnections operating at millimeter waves. The top metal layer is used for the center conductor as shown in Fig. 5. In order not to distort the coplanar waveguide mode, dummy metal is not allowed around the center conductor at any metal layer. On the other hand, the metal density requirement has to be fulfilled which means that there has to be enough metal at all metal layers. This is accomplished by strapping all the other metal layers together with vias to form the ground plane for the CPW. The unwanted slotline mode is suppressed by connecting the ground planes of the CPW together around the discontinuities using the lower metal layers. This way the ground planes at the opposite sides of the center conductor remain at the same potential.

In the conventional coplanar waveguide, presented above, the electromagnetic field penetrates into the silicon substrate, which increases losses. A metal shield structure can be drawn

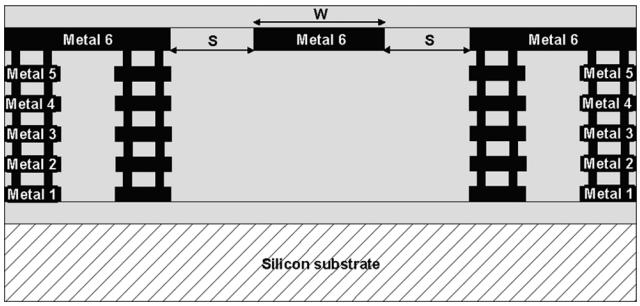

Fig. 5. Simplified cross-section of the conventional coplanar waveguide.

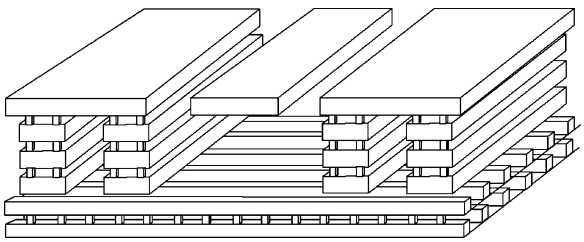

Fig. 6. Simplified cross-section of the slow-wave coplanar waveguide. Two lowest metal layers are strapped together with vias to form the floating shield strips.

using the lowest metal layers to prevent the electromagnetic fields from penetrating into the lossy silicon substrate. An efficient way to realize the shield is the slow-wave structure employing floating shield strips [16]. The simplified cross section of the slow-wave coplanar waveguide implemented in this work is shown in Fig. 6. Two lowest metal layers are strapped together with vias to form the floating shield strips. The shield is designed using minimum design rules, i.e. minimum metal strip width and spacing, in order to suppress the induced current flow in the direction of the propagating RF-signal. This minimizes the ohmic losses and maximizes the reactive energy storage per unit length. The smallest allowable shield strip spacing minimizes the exposure of the overlying CPW to the conductive substrate. In addition to shielding the substrate, the dielectric constant and thus the wavelength of the slow-wave CPW are adjustable by changing the signal-to-ground-gap spacing allowing more compact implementation of transmission lines for impedance transformation and phase shifting applications [16].

To characterize the on-chip coplanar waveguides, a conventional CPW and a slow-wave coplanar waveguide were implemented as test structures and measured on-wafer. The transmission line parameters were extracted using a method described in [17]. A test structure for a conventional CPW is shown in Fig. 7. A width of 12 μm was used for the center conductor. The signal-to-ground gap spacing was 9 μm resulting around 45 Ω characteristic impedance for this conventional CPW. The measured attenuation and quality factor of the conventional waveguide are shown in Fig. 8 and Fig. 9, respectively. Measured attenuation is around 2.8 dB/mm at 60 GHz.

In the slow-wave CPW the same width for the center conductor and signal-to-ground-gap spacing were used as for the

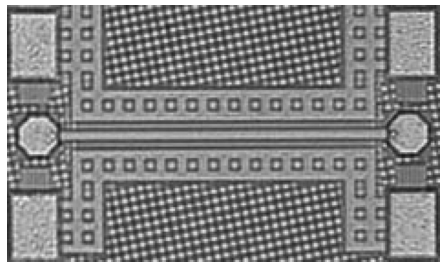

Fig. 7. Test structure for the conventional CPW. The length of the CPW is 375 μm.

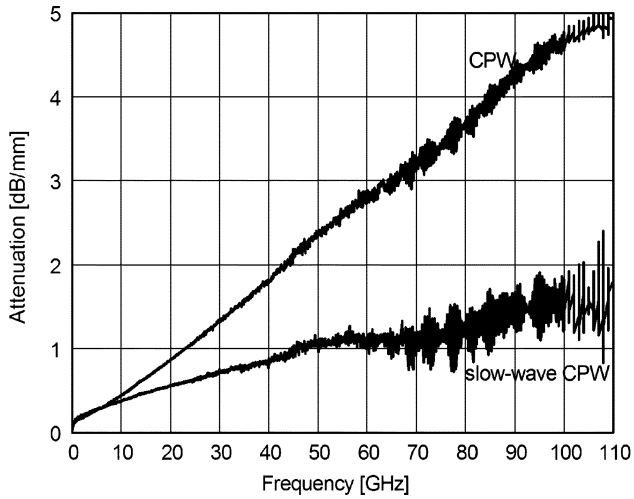

Fig. 8. Attenuation per unit length of the conventional ($Z_0 = 45\ \Omega$) and slow-wave CPW ($Z_0 = 35\ \Omega$).

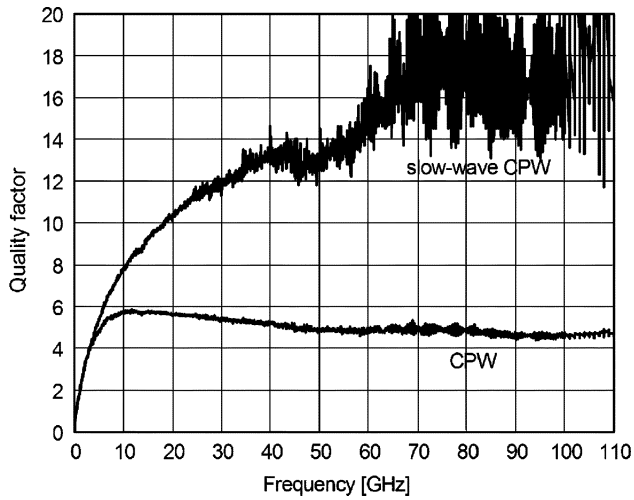

Fig. 9. Quality factor of the conventional ($Z_0 = 45\ \Omega$) and slow-wave CPW ($Z_0 = 35\ \Omega$).

conventional CPW. Because of the shield strips, the relative dielectric constant for the slow-wave CPW is higher. Therefore, the characteristic impedance of the slow-wave version is lower (around 35 Ω). The measured attenuation and quality factor of the slow-wave CPW are shown in Fig. 8 and Fig. 9, respectively. The measured attenuation is around 1.1 dB/mm at 60 GHz,

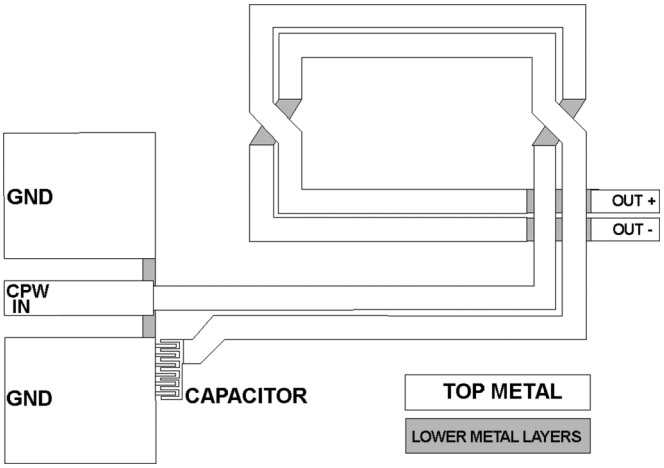

Fig. 10. Principal layout of the spiral balun and the transition from CPW-input to the balun.

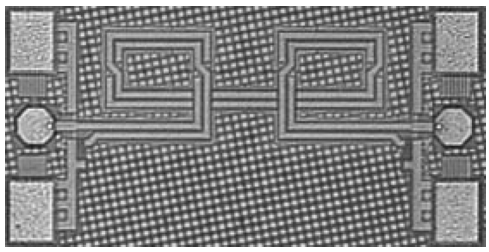

Fig. 11. Test structure for the balun. The utilized chip area is 0.57 mm × 0.30 mm.

which suggests that the shielding of the substrate is effective in the case of the realized structure.

C. Spiral Transmission Line Balun

At millimeter-wave frequencies the integration of a balun is feasible. A spiral transmission line transformer is a compact and wide-bandwidth balun [18]. The balun is used for matching the input impedance Z_0 of the circuit to the impedances Z_L of the loads. The circuit is properly matched, providing that the electrical length of the coupled lines in the odd mode is $\lambda/4$ at the design frequency and the odd-mode impedance of the quarter-wave transformer $Z_{\rm odd}$ is

$$Z_{\rm odd} = \sqrt{2Z_L Z_0} \tag{1}$$

For the signal to propagate in the odd mode, the balun has to suppress the even mode propagation. This means that the even mode impedance has to be as high as possible. Because of the conductive substrate of a typical CMOS technology, the return currents of a complicated circuit may not be explicit, which makes the exact analysis of the even-mode impedance at millimeter waves challenging. The even mode impedance can be increased by wrapping the balun in a spiral as explained in [18]. The spiral should have a minimal effect on the odd-mode impedance. In practice, the number of turns of the spiral is limited by the parasitic capacitance, which may cause undesired resonances. Thus, the presented balun incorporates one turn.

The EM analysis of the balun was divided into two parts as proposed in [18]. The even-mode characteristic impedance was

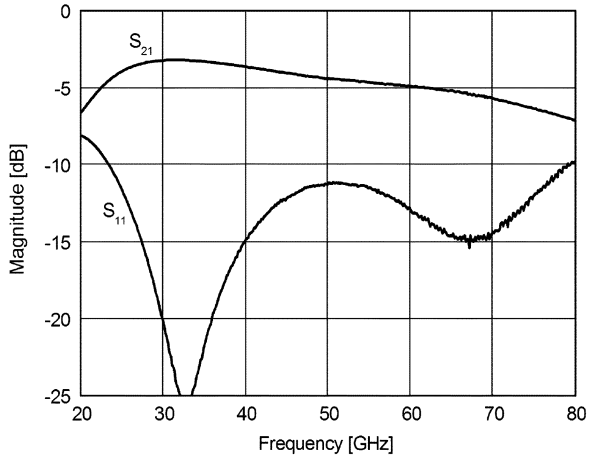

Fig. 12. Measured back-to-back response of the balun test structure.

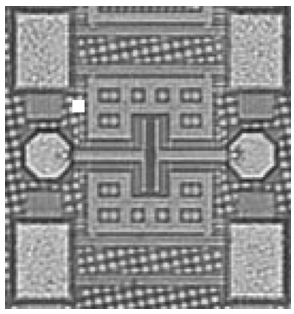

Fig. 13. Test structure for the series capacitor.

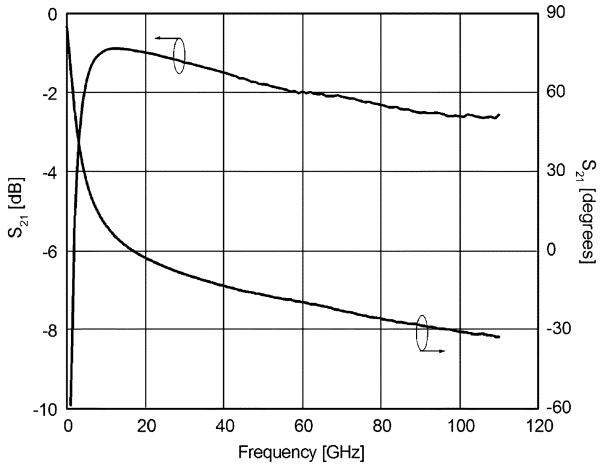

Fig. 14. Measured S_{21} of the series capacitor.

evaluated from the simulation of a spiral inductor in which the lines of the balun are joined. The odd-mode impedance and effective permittivity were modeled by calculating the odd-mode properties of a straight section of coupled lines. The balun was then treated as a lossy coupled transmission line in the circuit simulator.

The balun is fed from a coplanar waveguide input as shown in Fig. 10. To ensure a proper excitation for the balun, the ground planes of the CPW are connected together with lower metal layers at the transition point from CPW to the spiral balun. In order to prevent the DC from being grounded, multiple finger

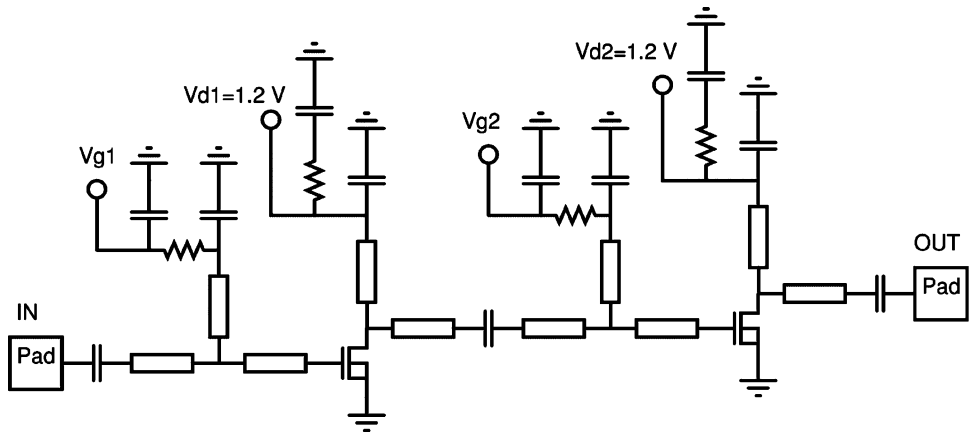

Fig. 15. Simplified schematic of the 40-GHz amplifier.

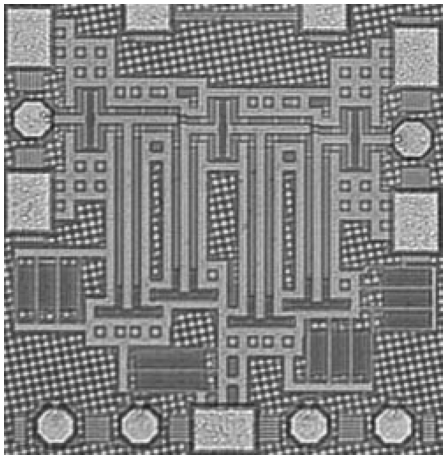

Fig. 16. Micrograph of the 40-GHz amplifier. The chip area is 0.52 mm × 0.55 mm.

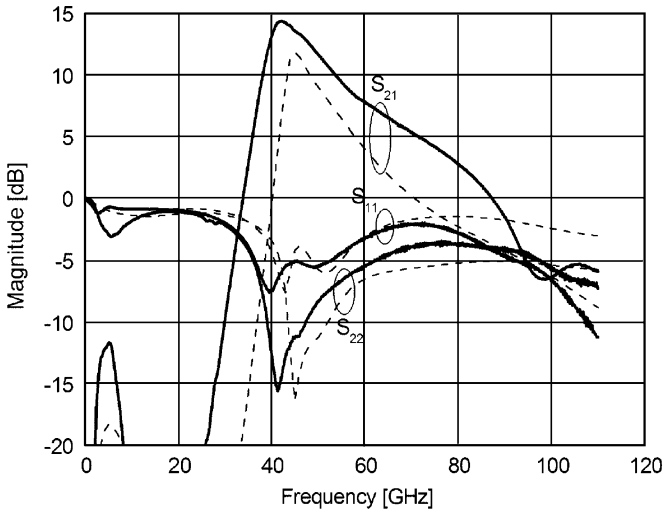

Fig. 17. Measured and simulated (dashed lines) S-parameters of the 40-GHz amplifier. $V_{\mathrm{supply}} = 1.2\ \mathrm{V}$, $I_{\mathrm{total}} = 36$ mA.

capacitors are used in parallel at the ground connection of the spiral balun.

The top metal layer is used for the balun lines. To prevent the dummy metal from occupying areas in the vicinity of the balun and to fulfill the metal density requirements at the lower metal layers, narrow metal paths were drawn perpendicular to the strips of the balun and it also enables the removal of the dummy metal directly under the balun by raising the local metal density to a suitable level. The narrow perpendicular strips have a minimal effect on the performance of the balun.

The test structure for the balun is shown in Fig. 11. The widths of the transmission lines of the balun are 9 μm and the lines are separated by a 2 μm gap. The size of the test structure including pads is 0.57 mm × 0.3 mm. Two baluns are connected together for measuring the back-to-back response. The results are shown in Fig. 12. The measured insertion loss including pads is less than 5 dB from 50 to 60 GHz; thus, less than 2.5 dB for a single balun.

D. Capacitors

Multiple standard finger capacitors were used in parallel to achieve reasonably high capacitance for on-chip short circuit and DC-blocking capacitors. Three six-capacitor blocks are in parallel resulting in 450 fF total capacitance. A CPW test structure for the series capacitor is shown in Fig. 13. Measured S_{21} of the series capacitor is shown in Fig. 14. The S-parameters were de-embedded by subtracting the pad admittance and the effect of the connecting CPW-lines.

III. Amplifiers

In the amplifier designs $\mathrm{W/L} = 90/0.07$-sized transistors are used in common-source configuration. Preliminary transistor S-parameter measurement data was available at the time of the design. On-wafer matching networks were implemented using conventional CPWs. Extensive electromagnetic simulations were used to capture the high frequency behavior of the conventional CPW-line and finger capacitors in parallel (Ansoft HFSS, Agilent ADS Momentum). Simplifications to the layouts were needed in order to decrease simulation time and computer memory usage. The main simplifications included the removal of metal layers having only a minor effect on the overall performance. In the simulations, the capacitor was divided into three identical parts.

TABLE I
PERFORMANCE COMPARISON OF CMOS AMPLIFIERS AROUND 40 GHz

CMOS process	Gain [dB]	Noise figure [dB]	Chip area [mm^2]	OCP [dBm]	Saturated output power [dBm]	Power dissipation	Circuit topology	Reference
180-nm CMOS	7 @ 40 GHz	N/A	2.04	N/A	10.4	100 mA @ 3 V	3-stage cascode	[20]
130-nm CMOS	20 @ 43 GHz	6.3 @ 41 GHz	0.525	4	8	24 mA @ 1.5 V	3-stage CS	[3]
130-nm CMOS	19 @ 40 GHz	N/A	1.43	-0.9	N/A	24 mA @ 1.5 V	3-stage cascode	[21]
90-nm CMOS	6 @ 40 GHz	N/A	0.7	-5.75	N/A	12.7 mA @ 1.5 V	2-stage CS	[22]
90-nm CMOS	18.6 @ 33 GHz	3 @ 33 GHz	0.856	1.6	N/A	8.3 mA @ 1.2 V	2-stage cascode	[5]
90-nm SOI*	11.9 @ 35 GHz	3.6 @ 35 GHz	0.18	4	N/A	17 mA @ 2.4 V	1-stage cascode	[23]
120-nm SOI*	14 @ 40 GHz	3.6 @ 40 GHz	N/A	N/A	N/A	16 mA 1.2 V	2-stage cascode	[24]
65-nm CMOS	14.3 @ 42 GHz	6 @ 50 GHz	0.286	6	9.6	36/60 mA @ 1.2 V	2-stage CS	This work

*SOI: Silicon on Insulator.

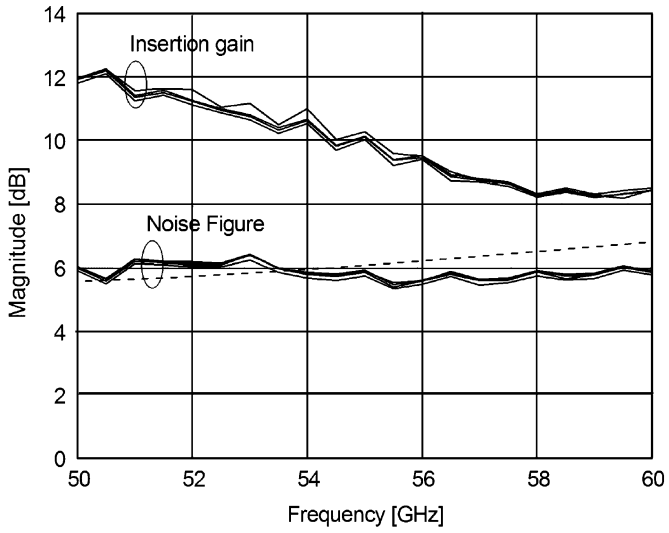

Fig. 18. Measured noise figure and insertion gain of four samples of the 40-GHz amplifier. The dashed line represents simulated noise figure. $V_{\mathrm{supply}} = 1.2$ V, $I_{\mathrm{total}} = 36$ mA.

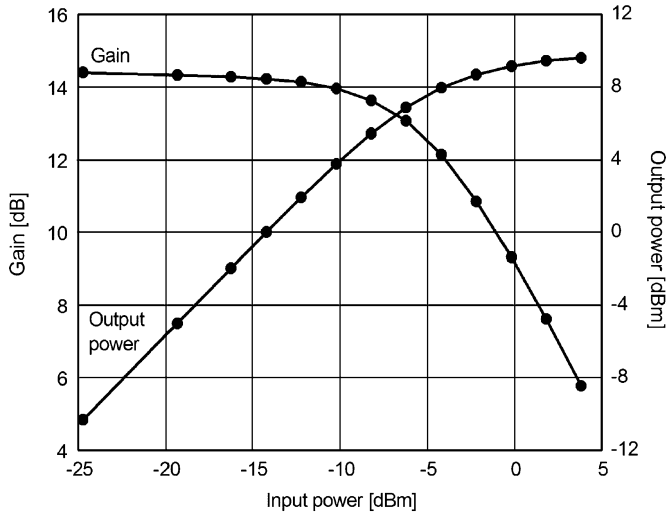

Fig. 19. Measured large-signal performance of the 40-GHz amplifier. $V_{\mathrm{supply}} = 1.2$ V, $I_{\mathrm{total}} = 60$ mA.

A. 40-GHz Amplifier Design and Measurement Results

The amplifier is a two-stage single-ended design. A simplified schematic and a micrograph of the amplifier are shown in Fig. 15 and Fig. 16, respectively. The chip size is 0.52 mm $\times$ 0.55 mm including pads. Series CPW-lines and short-circuited CPW-shunt stubs are used for matching the input and output of a single stage to 50-Ω impedance. A short-circuit at the end of the stub at 40 GHz is implemented using multiple finger capacitors in parallel. This is a low impedance point and suitable for bias insertion. Because the transistor is conditionally stable around 40 GHz, the matching networks were designed to obtain unconditionally stable operation for a single stage and the entire amplifier. The low frequency stability is ensured by resistor-capacitor networks that are placed in the vicinity of the short-circuit of the shunt stub.

The on-wafer measured and the simulated S-parameters of the 40-GHz amplifier are shown in Fig. 17. For a first design cycle circuit, a good agreement between simulated and measured results was achieved. The small-signal gain is better than 10 dB from 38 to 54 GHz and 14.3 dB at 42 GHz. The noise figure and insertion gain were measured on-wafer using a measurement setup that is described in [19]. Due to the measurement setup, it was only possible to measure noise figure starting from 50 GHz. Results for four amplifier chips are shown in Fig. 18. The measured noise figure is 6 dB at 50 GHz. The measured on-wafer large-signal performance at 42 GHz is shown in Fig. 19. The 1-dB output compression point (OCP) is at $+6$ dBm power level and the amplifier exhibits 9.6 dBm of output power using a 1.2 V supply. The measured performance of the 40-GHz amplifier is compared to previously published results in Table I. As can be seen, our two-stage common-source design achieves good gain and noise performance, highest 1-dB output compression point and miniature chip size, when compared to the previously reported bulk CMOS designs.

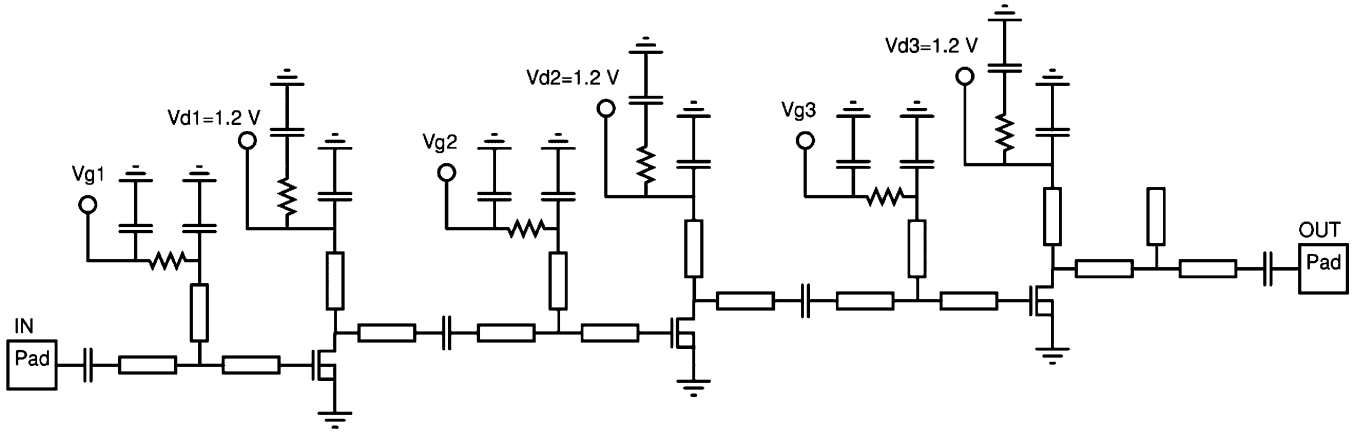

Fig. 20. Simplified schematic of the 60-GHz amplifier.

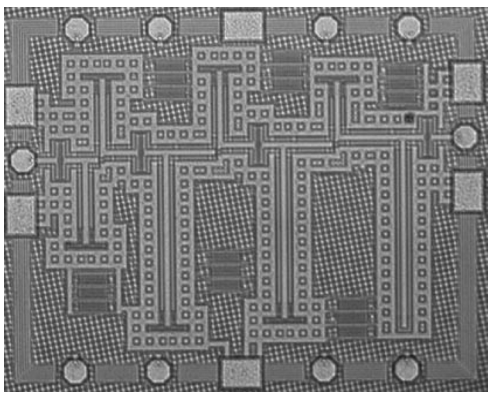

Fig. 21. Micrograph of the 60-GHz amplifier. The chip area is 0.87 mm × 0.70 mm.

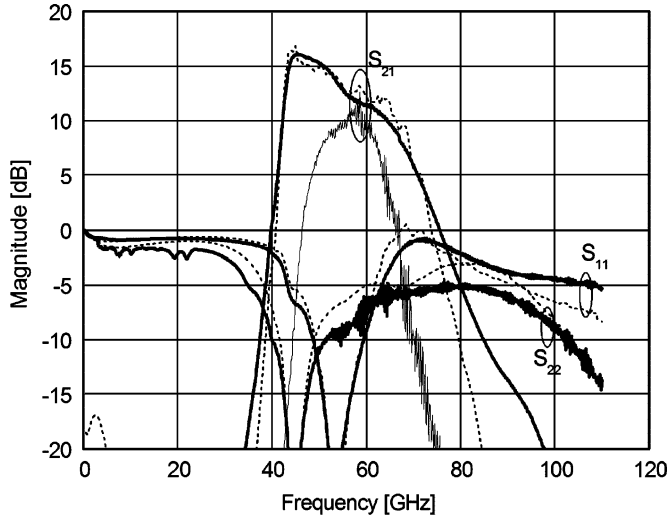

Fig. 22. Measured S-parameters (thick solid lines) and the simulated S_{21} (thin solid line) of the 60-GHz amplifier. The dashed lines represent re-simulated S-parameters. $V_{\mathrm{supply}} = 1.2$ V, $I_{\mathrm{total}} = 54$ mA.

B. 60-GHz Amplifier Design and Measurement Results

The amplifier is a three-stage single-ended design. A simplified schematic and a micrograph of the amplifier are shown in Fig. 20 and Fig. 21, respectively. The chip area is 0.87 mm × 0.70 mm including pads. Series CPW-lines and short-circuited CPW-shunt stubs are used for input, output and interstage matching. At the output, an open-ended shunt stub is needed to complete the output match to 50-Ω impedance. As with the 40-GHz design, multiple finger capacitors are used in parallel for the on-chip short circuit and DC-blocking capacitors. The low frequency stability is ensured by resistor-capacitor networks. The preliminary measured transistor data was used in the design of the amplifier.

The on-wafer measured S-parameters and the simulated S_{21} of the 60-GHz amplifier are shown in Fig. 22. As can be seen, the frequency response has shifted downwards. The frequency shift can be modeled by re-simulating the amplifier using the new measured data from individual circuit blocks i.e. the capacitor, transistor and CPW, which were presented in Section II. This way a good agreement between simulated and measured results was achieved.

The noise figure and insertion gain were measured on-wafer. Results for four amplifier chips are shown in Fig. 23. The amplifier achieves more than 11 dB of gain from 45 to 65 GHz. At 60 GHz, the measured noise figure is between 5.55 and 5.7 dB and below 6 dB from 55 to 65 GHz. The AM/AM and AM/PM characteristics were obtained from the large-signal S-parameter measurement data. The on-wafer measurement results are shown in Fig. 24. At 60 GHz, the measured 1-dB output compression point is at 1.5-dBm power level and the amplifier exhibits +7 dBm of output power using a 1.2 V supply. The measured performance of the 60-GHz amplifier is compared to previously published results in Table II. Our design achieves the lowest reported noise figure in CMOS with reasonable gain. In addition, the output power performance is competent even, when compared to the reported CMOS power amplifiers.

IV. Balanced Resistive Mixer

The mixer is one of the key components in a millimeter wave transceiver. In the transmitter, the local oscillator (LO) signal has to be adequately suppressed. To achieve wide-bandwidth LO operation the balanced mixer topology is preferred.

The resistive mixer can achieve high linearity. The field-effect transistor (FET) resistive mixer was first described in [25] and a balanced version was reported in [26]. In addition to the very low distortion, the advantages of the resistive FET mixer are low

TABLE II
PERFORMANCE COMPARISON OF V-BAND CMOS LOW-NOISE AMPLIFIERS AND POWER AMPLIFIERS

	CMOS technology	Frequency [GHz]	Gain [dB]	Noise figure [dB]	OCP [dBm]	Saturated output power [dBm]	Power dissipation	Chip size [mm^2]	Reference
CMOS low noise amplifiers	130-nm	56	24.7	7.1	1.8	5	72 mW	0.72 x 0.67	[2]
	130-nm	60	12	8.8	2	N/A	54 mW 1.5 V	1.3 x 1.0	[21]
	90-nm	58	14.6	N/A	N/A	N/A	24 mW @ 1.5 V	0.35 x 0.40	[4]
CMOS power amplifiers	90-nm	62	12.2	N/A	4	N/A	10.4 mW @ 1 V	N/A	[1]
	90-nm	61	5.2	N/A	6.4	9.3	40 mW @ 1.5 V	0.35 x 0.43	[4]
	65-nm	60	11.5	5.6	-	-	72 mW @ 1.2 V	0.87 x0.70	This work
			12.8	-	1.5	7	104 mW @ 1.2 V		

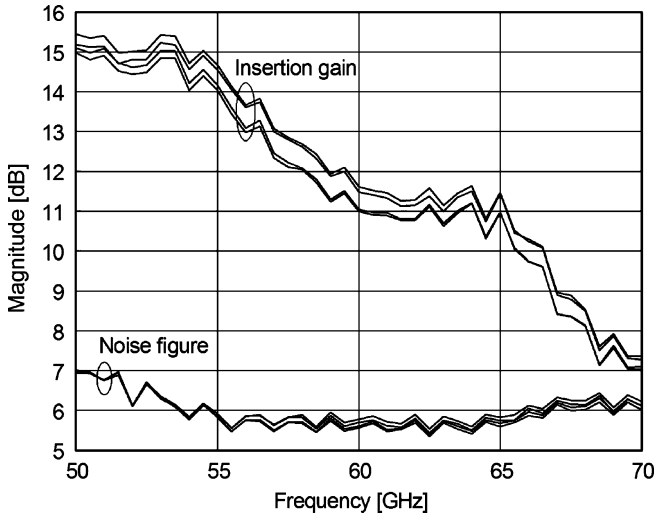

Fig. 23. Measured noise figure and insertion gain of four samples of the 60-GHz amplifier. $V_{\rm supply} = 1.2$ V, drain current per stage is 20 mA.

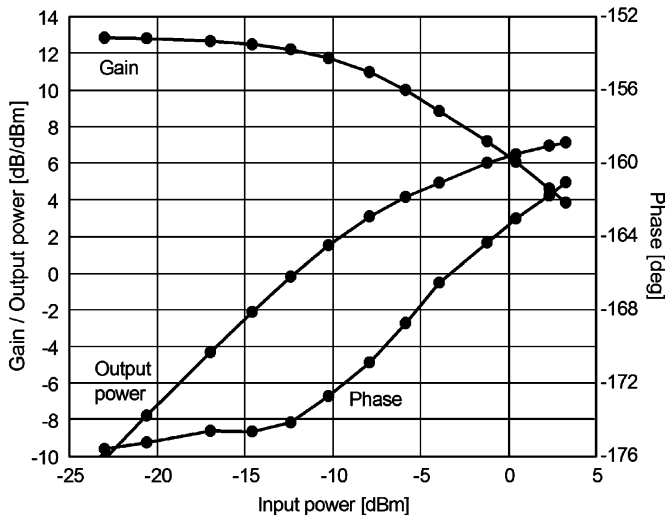

Fig. 24. Measured AM/AM and AM/PM characteristics of the 60-GHz amplifier. $V_{\rm supply} = 1.2$ V, drain current per stage is 29 mA.

1/f noise, stability, no shot noise and, in practice, no DC power consumption.

A simplified schematic of the balanced resistive mixer is presented in Fig. 25. The design is intended for upconversion. However, the topology is suitable for both up- and downconversion. On-wafer matching networks were implemented using conventional CPWs. Electromagnetic simulations were used to capture the high frequency behavior of the conventional CPW-line and multiple finger capacitors in parallel. The mixer consists of two $\mathrm{W/L} = 90/0.07$-sized transistors. The local oscillator is applied from a coplanar waveguide to a spiral transmission-line balun, presented in Section II, to generate the required 180° phase shift at the transistor gates. The drains are connected together through small valued finger-capacitors. This node is a virtual ground for the LO and an open circuit at the intermediate frequency (IF). In order to obtain the desired balanced mixing operation, the IF-current at the drains are out of phase and thus an external (off-chip) balun or a hybrid must be used to combine them. The IF is fed through a short-circuited CPW-line. The IF-ports are unmatched and no drain DC-bias voltage is applied to the transistors. The RF-port is matched to 50 Ω with a series CPW-line and a short-circuited shunt CPW-stub. The gates of the transistors are biased through the balun lines. At LO-port a short-circuited shunt stub is used for biasing the transistor gate and it is a part of the LO-port matching network. A micrograph of the mixer is shown in Fig. 26. The chip area including pads is 0.70 mm × 0.67 mm.

A. Upconversion Simulation and Measurement Results of the Mixer

The LO of the mixer is used to pump the channel resistance of the FET. The required drive level can be reduced when the transistor is biased near the threshold voltage. Therefore, the gate voltage was set to 0.5 V.

The measured on-wafer conversion loss and the LO-to-RF isolation as a function of RF-frequency are shown in Fig. 27. The desired RF-signal is at upper sideband (USB). The IF is fixed at 2 GHz. A LO-power varying from 5 to 9 dBm for LO frequencies from 51 to 62 GHz is delivered to the chip. The conversion loss is 13.5 dB at 60 GHz and it is better than 15 dB from 53 to 62 GHz. The local oscillator suppression is better than 33.7 dB, which suggests that the generated 180° degree LO signal phase shift and the LO virtual ground on the drain side were realized successfully.

The measured conversion loss can be modeled using the new measurement data obtained from the test structures presented in Section II. As can be seen in Fig. 27, a good agreement between the re-simulated and the measured conversion loss is achieved.

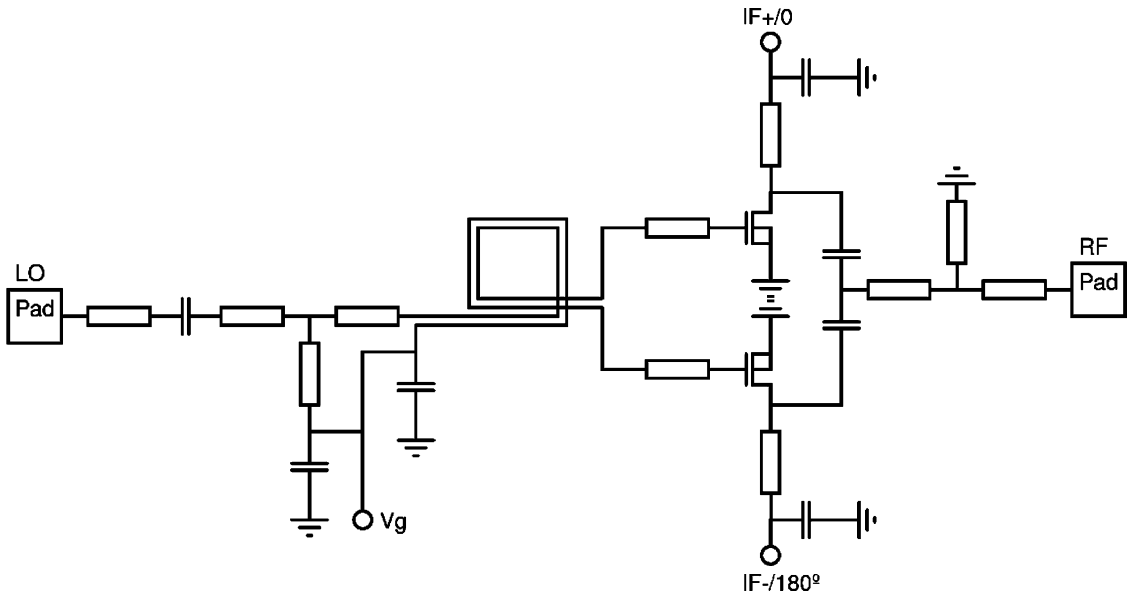

Fig. 25. Simplified schematic of the singly balanced resistive mixer. The IF+ and IF- ports are connected to an off-chip IF hybrid. The capacitors are short circuits at RF and LO frequencies and open circuits at IF-frequency.

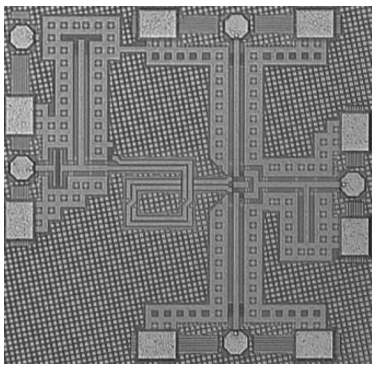

Fig. 26. Micrograph of the balanced resistive mixer. The chip area is 0.70 mm $\times$ 0.67 mm.

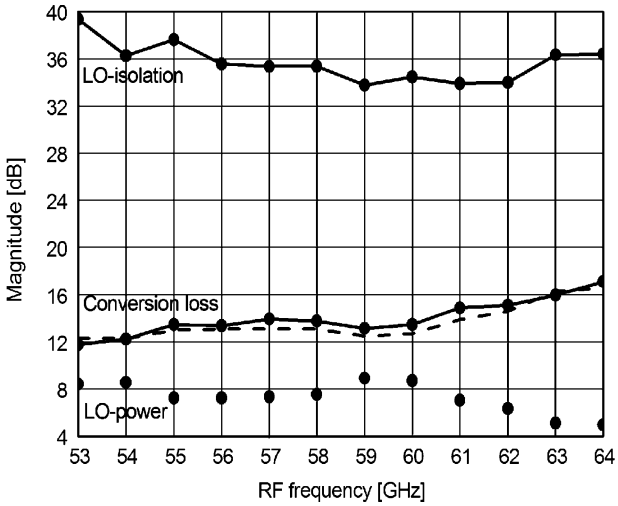

Fig. 27. Measured upconversion loss and corresponding LO-to-RF isolation as a function of the RF frequency. The dashed line represents re-simulated upconversion loss. The IF is fixed at 2 GHz. The LO is swept from 51 to 62 GHz. The corresponding LO power delivered to the chip is also shown.

The measured conversion loss at fixed LO frequency (58 GHz) is presented in Fig. 28. The conversion loss is better than 15.2 dB for IF frequencies from 1 to 5 GHz. In Fig. 29, the measured and simulated large-signal performance in upconversion is presented. At 60 GHz, the measured 1-dB output compression point (OCP) is at -19 dBm power level.

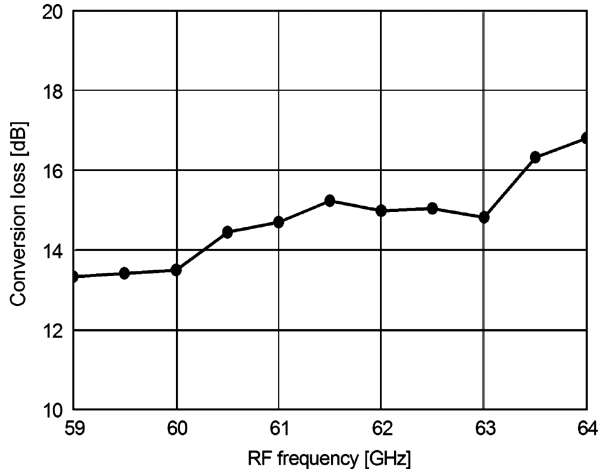

Fig. 28. Measured upconversion loss at a fixed LO frequency (58 GHz). The IF is swept from 1 to 6 GHz.

B. Downconversion Simulation and Measurement Results of the Mixer

As with the upconversion measurements, the gate voltage was set to 0.5 V and the LO power varies from 5 to 9 dBm for LO frequencies from 52 to 62 GHz. Measured conversion losses with fixed IF and LO frequencies are shown in Figs. 30 and 31, respectively. At 60 GHz, the measured conversion loss is 12.5 dB. The conversion loss is better than 15 dB for RF frequencies from 54 to 63 GHz. For IF bandwidth from 1 to 5 GHz, better than 14.4 dB conversion loss is achieved. The measured and simulated large-signal performances are shown in Fig. 32.

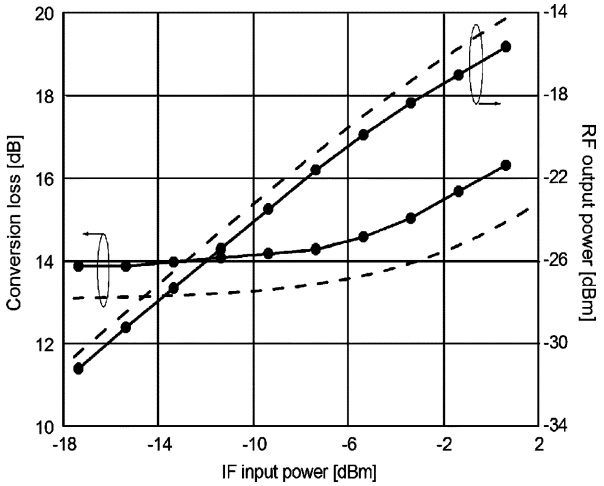

Fig. 29. Measured and re-simulated (dashed lines) upconversion loss and RF output power as a function of the input power.

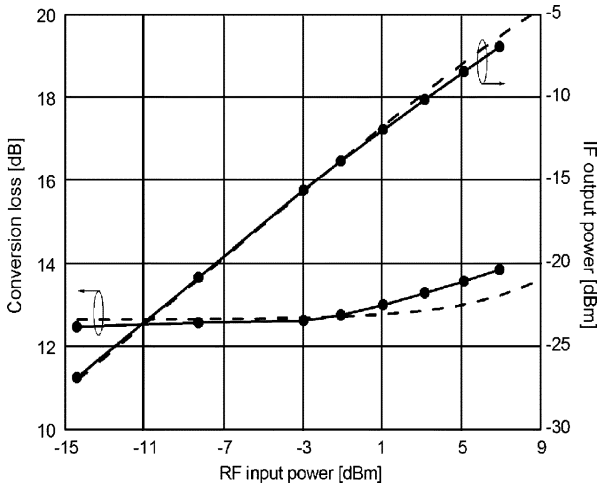

Fig. 32. Measured and re-simulated downconversion loss and IF output power as a function of the RF input power at 60 GHz. The LO is at 58 GHz.

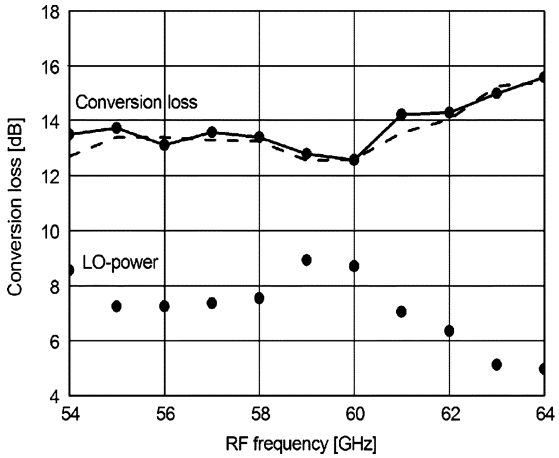

Fig. 30. Measured and re-simulated downconversion loss with a fixed IF frequency (2 GHz). The LO is swept from 52 to 62 GHz. The corresponding LO power delivered to the chip is also shown.

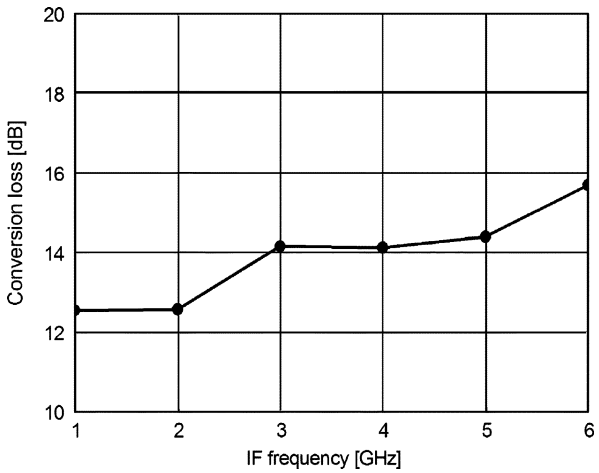

Fig. 31. Measured downconversion loss as a function of the IF frequency. The LO is fixed at 58 GHz.

At 60 GHz, the measured 1-dB input compression point (ICP) is at +5 dBm power level.

The measured and simulated return losses of the LO and RF ports are shown in Fig. 33. The return loss of the RF-port is around 5 dB at 60 GHz. The low return loss of the RF port increases the conversion loss of the mixer around 1.5 dB. The measured return loss of the LO-port is better than 10 dB from 55.5 to 72 GHz. Although the LO-port matching is good, the applied 8 to 9 dBm LO power level is difficult to achieve on chip. It should be also noted that because of the lossy passive components, the insertion loss of the LO-input network is around 7 to 8 dB. This means, that the required LO-power for the mixing devices is less than 3 dBm. Nevertheless, in this configuration a buffer amplifier is needed to generate enough LO power.

The measured downconversion results are compared to previously published CMOS mixers in Table III. The performance in upconversion is compared to results of a SiGe BiCMOS mixer in Table IV. The presented mixer is highly linear both in up- and downconversion and occupies only 0.47 mm^2 of chip area. Although the mixer dissipates no DC power, in this configuration relatively high LO-power is needed to obtain a reasonable conversion loss.

V. Conclusion

We presented the design and measurement results of millimeter-wave amplifiers and a V-band balanced resistive mixer in 65-nm baseline CMOS. Electromagnetic simulations were used to model the high frequency behavior of individual circuit blocks such as the conventional CPW-line, spiral transmission line balun and multiple finger capacitors in parallel. Successful results were obtained from the circuits of the first design cycle.

The new measurement results, which were obtained from the test structures, aid the design of millimeter wave integrated circuits using a 65-nm baseline CMOS. By using the measurement data it is possible to improve the performance of the circuit blocks. It was shown that the results obtained from the test structures enable fairly accurate characterization of the frequency response of the 60-GHz amplifier. Moreover, the V-band extrinsic noise parameters of the transistor were presented. Finally, the low attenuation of the slow-wave CPW may be beneficial when trying to reduce substrate losses.

TABLE III
PERFORMANCE COMPARISON OF CMOS DOWNCONVERSION MIXERS AT 60 GHz

Downconversion							
CMOS process	*Circuit topology*	*Conversion gain [dB]*	*ICP [dBm]*	*LO power [dBm]*	*Power dissipation [mW]*	*Chip size [mm^2]*	*Reference*
90-nm	Active Gilbert Cell	2	-4.5	-	93	0.3	[27]
90-nm	Active cascode	-1.2	0.2	1.5	29	0.49	[28]
130-nm	Active Gilbert cell	3 (voltage gain)	-15	0	-	0.81	[29]
130-nm	Active quadrature balanced	-2	-3.5	0	2.4	2.72	[30]
90-nm	Resistive single ended	-11.6	6	4	0	4	[31]
65-nm	Resistive singly balanced	-12.5	5	8.7	0	0.47	This work

TABLE IV
PERFORMANCE COMPARISON OF SILICON INTEGRATED UPCONVERSION MIXERS AT 60 GHz

Upconversion								
Technology	*Circuit topology*	*CL [dB]*	*OCP [dBm]*	*LO isolation [dB]*	*LO power [dBm]*	*Power dissipation [mW]*	*Chip size [mm^2]*	*Reference*
180-nm SiGe BiCMOS	Active Gilbert cell	7	-25 @ 40 GHz	40	5	14	0.28	[32]
65-nm CMOS	Resistive singly balanced	13.5	-19 @ 60 GHz	34	8.7	0	0.47	This work

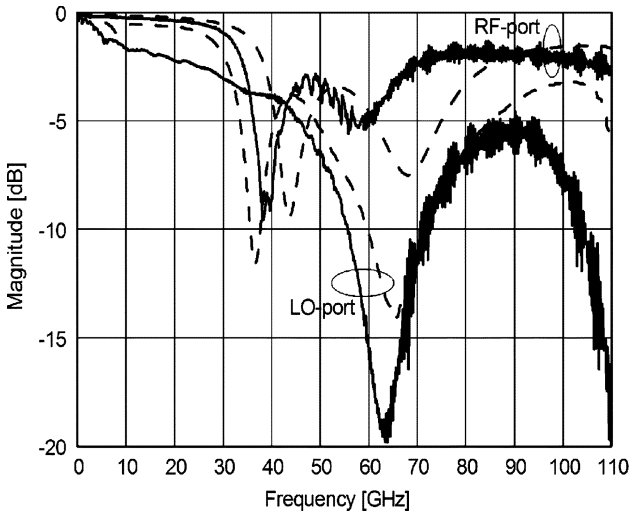

Fig. 33. Measured and re-simulated return losses of LO and RF ports of the balanced resistive mixer.

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