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Low noise amplifiers for D-band

Mikko Kantanen[1], Mikko Kärkkäinen[2], Mikko Varonen[2], Mikko Laaninen[3], Timo Karttaavi[1], Rainer Weber[4], Arnulf Leuther[4], Matthias Seelmann-Eggebert[4], Tapani Närhi[5], Janne Lahtinen[6] and Kari A. I. Halonen[2]

Abstract – Four low noise amplifiers for D-band (110-170 GHz) operation are presented. The amplifier circuits have been manufactured using a 100-nm gate length metamorphic high electron mobility transistor technology. A good agreement between simulations and measurements is verified by on-wafer measurements. Selected amplifiers have been assembled into a split-block waveguide module. The design and performance of the amplifier modules are presented. The amplifier modules exhibit better than 15-20 dB small signal gain with 6.0-7.5 dB noise figure. The bandwidths range from 141-152 GHz to 130-170 GHz.
Index Terms – Millimeter wave amplifiers, MMIC amplifiers, Integrated circuit packaging, Metamorphic high electron mobility transistors (MHEMT).

I. Introduction

Advances in the manufacturing of millimeter-wave monolithic integrated circuits (MMICs) can open new possibilities to exploit large bandwidths available above 100 GHz. Low noise amplifiers have been developed up to 260 GHz and the first circuits exhibiting gain at 300 GHz have been reported [1]-[4]. Future applications above 100 GHz may include wideband communication, environmental monitoring and millimeter-wave imaging.

An example application is the atmospheric water vapor profiling using a radiometer for simultaneous measurements at the water vapor resonance frequency 183 GHz and at a window frequency within 140 to 165 GHz. In the current generation of atmospheric sounders, heterodyne radiometer architecture is used with Schottky mixers as the first component after the antenna. The sensitivity of these instruments could be improved with a low noise amplifier (LNA), and even direct detection architecture is possible.

Traditionally, the manufacturing of low noise millimeter-wave integrated circuits has relied on the use of high electron mobility transistors (HEMT) implemented with gallium arsenide (GaAs) or indium phosphide (InP). While best noise performance has been achieved using InP HEMT technology there are some drawbacks. These include higher manufacturing cost, lower breakdown voltage, more fragile structure, and device reliability when comparing to GaAs technology. Few InP HEMT based LNAs operating at D-band have been reported [5]-[10].

To overcome some of drawbacks with InP, the possibility to process indium channel devices on GaAs carrier wafer has been introduced in pseudomorphic (PHEMT) and MHEMT technologies. In MHEMT technology, a metamorphic buffer layer is grown on the GaAs substrate, to enable the growth of the channel layer having 30-80 % indium content. This leads to cost reduction and manufacturability improvement over pure InP technology [11], [12]. So far, few PHEMT and MHEMT LNAs operating at D-band have been reported [13]-[18].

Packaging of MMICs operating above 100 GHz is challenging. Typically, the MMIC is mounted inside a waveguide module and a transition is used to couple the signal from the rectangular waveguide to the MMIC. Transitions can be manufactured on a separate substrate, which are then connected to MMIC using wire bonding or flip-chip technique. As frequency increases, the wire bonding becomes more demanding and the length of the wire has to be minimized [19], [20]. The use of flip-chip technique has been demonstrated with MMICs up to 100 GHz [21]-[24]. In addition, the integration of the transition on MMIC has been studied in [6].

With the water vapor profiling as a background application, the aim of this work was to study the possibilities of using metamorphic high electron mobility transistors (MHEMTs) for low noise amplification in the D-band (110-170 GHz). Four low noise amplifiers were designed and selected chips were assembled in an E-plane split-block package. Package design including transitions from coplanar to rectangular waveguide is presented. Results on both on-wafer and packaged module measurement are shown.

II. Fabrication technology and modelling

The manufacturing process used in this work is the 100-nm GaAs based MHEMT technology of the Fraunhofer IAF, Freiburg, Germany. The process is suitable for coplanar waveguide (CPW) designs [3]. The process features NiCr thin film resistors, metal-insulator-metal (MIM) capacitors and backside metallization. Unwanted substrate modes are

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[1]MilliLab, VTT Technical Research Centre of Finland, P.O. Box 1000, FI-02044 VTT, Finland Phone: +358 207226501; Fax: +358 207227012;
E-mail: mikko.kantanen@vtt.fi
[2] MilliLab, SMARAD2 / Electronic Circuit Design Laboratory TKK Helsinki University of Technology, P.O. Box 1000, FI-02015 TKK, Finland;
[3] Elektrobit Microwave Ltd., FI-02150 Espoo, Finland;
[4] Fraunhofer Institute for Applied Solid-State Physics, D-79108 Freiburg, Germany;
[5] European Space Agency (ESTEC), NL-2200 AG Noordwijk, The Netherlands;
[6] Ylinen Electronics, FI-31600 Jokioinen, Finland.

suppressed using ground via holes through the GaAs substrate. As a result of extensive modelling work the Fraunhofer IAF provided reliable models for CPW components and transistors. A transistor with a gate width of 2x15 μm was chosen as a suitable device for D-band operation. The ft of the transistor is about 200 GHz and it is used in common source configuration. All designs were optimized for high stable gain rather than low noise, because the noise model extracted from lower frequencies was considered unreliable at these frequencies.

III. Low noise amplifier designs

Four low noise amplifiers were designed using different design goals or design methodologies. More detailed description of LNA designs is presented in [25]. The basic schematic of the first design (LNA1) is shown in Fig. 1.

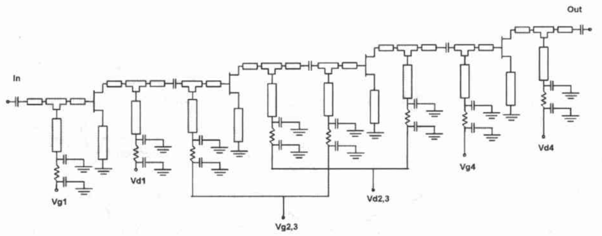

Fig. 1. Principal schematics of the LNA1.

LNA1 is a narrowband amplifier. Matching networks are designed using conventional reactive matching technique. Stability is improved using inductive source feedback. A micrograph of the LNA1 is presented in Fig. 2. The on-wafer measurement results and simulations are shown in Fig. 3. The measurements show peak gain of 22.7 dB at 152 GHz with a noise figure of 6.0 dB. The S-parameters were measured using two systems. The Agilent PNA series network analyzer was used over the range 1-110 GHz and the HP8510C network analyzer with G-band extension modules was applied for 130-200 GHz range. The noise figure measurement setup for the G-band consists of in-house assembled external downconverter and Agilent N8973A noise figure analyzer.

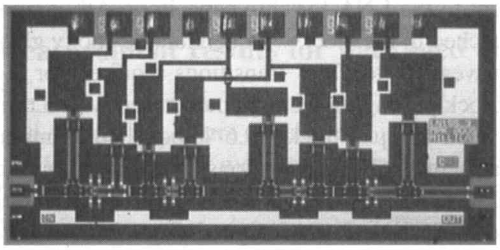

Fig. 2. Micrograph of the LNA1 MMIC. The chip size is 1.0 × 2.0 mm^2.

The second design (LNA2) is a narrowband four-stage amplifier. Input, output and interstage matching is based on series transmission lines. Bias voltage for the transistor is fed through λ/4 short circuited shunt stubs.

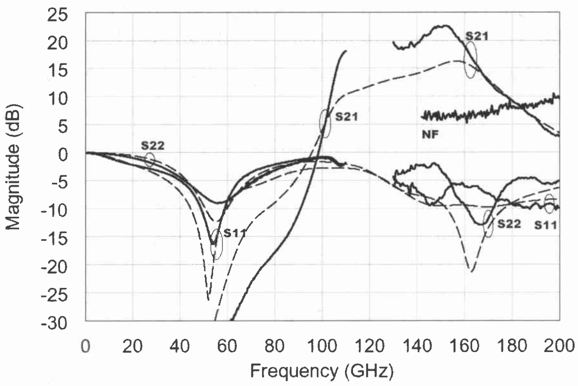

Fig. 3. Measured (solid) and simulated (dashed) S-parameters and noise figure (measurement only) for LNA1. The peak gain of 22.7 dB with the noise figure of 6.0 dB is achieved at 152 GHz. Vd = 1.09 V, Id = 36 mA. Data from [25].

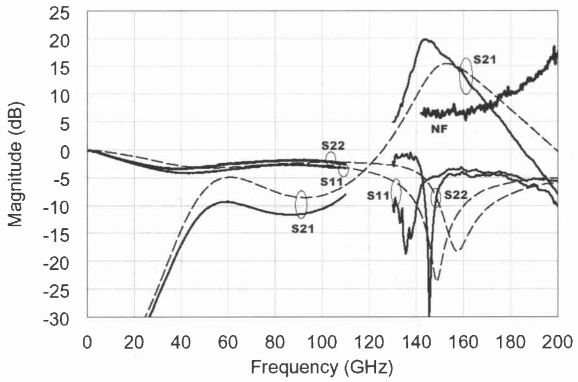

Fig. 4. Measured (solid) and simulated (dashed) S-parameters and noise figure (measurement only) for LNA2. The peak gain of 19.8 dB with the noise figure of 6.3 dB is achieved at 143 GHz. The applied bias values were Vd = 1.54 V, Id = 36 mA. Data from [25].

Stability is improved by using inductive source feedback and small series resistors in shunt stubs. The on-wafer measurement results and simulations are shown in Fig. 4. The measurements show a peak gain of 19.8 dB at 143 GHz with a noise figure of 6.3 dB.

The third design (LNA3) is a wideband amplifier. The input and output matching networks are designed using the reactive matching technique. The double resonant matching technique is used for interstage matching, in order to obtain wideband match. Stability is improved using inductive source feedback. The on-wafer measurement results and simulations are shown in Fig. 5. There is an unwanted gain peak with a poor output return loss at around 105 GHz, making the amplifier only conditionally stable. Otherwise, average gain of 18.0 dB is achieved over a wide bandwidth.

The fourth design (LNA4) is also a wideband amplifier. To suppress gain below 100 GHz, an interdigital capacitor is placed in two interstage networks. This capacitor provides smaller capacitance than MIM capacitors. Otherwise, the

Table 1. Comparison of reported HEMT MMIC LNAs at D-band.

Frequency (GHz)	Gain (dB)	NF (dB)	Number of Stages	Technology	Reference
150-215	12	N.A.	3	70-nm InP HEMT	[5]
150-215	20±6	8	6	80-nm InP HEMT	[6], [7]
150-205	17±2	N.A.	8	100-nm InP HEMT	[8]
140	30	N.A.	3	100-nm InP HEMT	[9]
90-140	15±3	N.A.	6	100-nm InP HEMT	[10]
150	5	N.A.	1	120-nm InP HEMT	[12]
164	6	N.A.	2	70-nm InP PHEMT	[13]
120-124	10-12	N.A.	2	100-nm InP PHEMT	[14]
142	9	N.A.	2	100-nm InP PHEMT	[15]
155	10.1	5.1	3	100-nm InP PHEMT	[16]
148	12	N.A.	2 cascode stages	150-nm GaAs PHEMT	[17]
155-160	15	N.A.	2 cascode stages	70-nm GaAs MHEMT	[18]
152	22.7	6.0	4	100-nm GaAs MHEMT	This work, on-wafer
143	19.8	6.3	4	100-nm GaAs MHEMT	This work, on-wafer
130-154	18.0-19.0	5.5-7.0	4	100-nm GaAs MHEMT	This work, on-wafer
130-171	17.6-20.6	5.5-7.0	4	100-nm GaAs MHEMT	This work, on-wafer

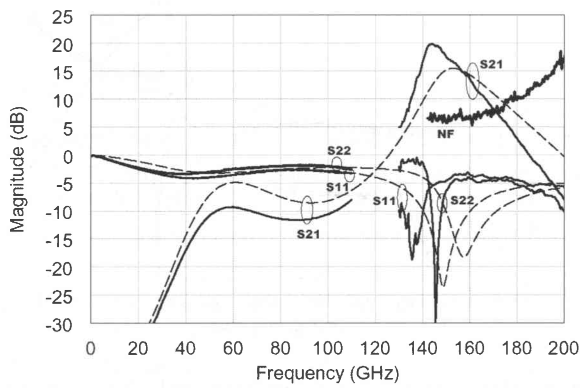

Fig. 5. Measured (solid) and simulated (dashed) S-parameters and noise figure (measurement only) for LNA3. A flat gain of 18 dB was achieved at D-band with noise figure of 5.5-7.0 dB. Vd = 1.36 V, Vg = 36 mA. Data from [25].

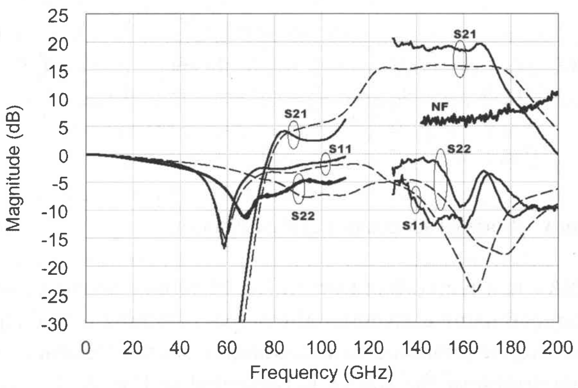

Fig. 6. Measured (solid) and simulated (dashed) S-parameters and noise figure (measurement only) for LNA4. The peak gain of 20.6 dB was achieved at 130 GHz. The 3 dB bandwidth is 130-171 GHz. The noise figure is less than 7.0 dB at 142-175 GHz range. Vd = 1.18 V, Id = 36 mA. Data from [25].

reactive matching technique was used for matching network design and inductive source feedback improves stability. The on-wafer measurement results and simulations are shown in Fig. 6. The maximum gain is 20.6 dB with a 3 dB bandwidth of 130-175 GHz. The measured noise figure is 5.5-7.0 dB between 142-175 GHz.

As a summary, the measured gain was found to be higher than simulated ones. The on-wafer performance of the designed amplifiers has been compared to previously reported MMIC LNAs at D-band in Tab. 1. The LNAs reported in this paper show comparable or better performance than the previously published amplifiers.

IV. Packaging

The mechanical design of the module used in this work is based on an E-plane split-block package, originally described in [26]. The concept is illustrated in Fig. 7, showing both halves of a WR-6 (110-170 GHz) block with the amplifier MMIC and two waveguide to CPW transitions. The outer dimensions of the block (excluding waveguide alignment pins) are 16x19x19 mm. The block has a space for a 5-pin micro connector and a small PCB for installing a bias network (lowpass RC), as well as a smaller cavity adjacent to the LNA for chip capacitors. All components are attached to the block with conductive epoxy glue.

The waveguide to CPW transitions required for E-plane split-block packaging were manufactured with a thin-film process on 100 μm thick, 99.6 % polished alumina. The design method of the transitions follows the outline presented in [27], where general transitions from waveguide to microstrip have been designed. The simulation model for the transition is illustrated in Fig. 8. The height and width of the microstrip channel were designed to result in cutoff above 200 GHz for the first waveguide-like mode in the channel. For the WR-6 antenna probe it was possible to find a combination of the width and length of the probe as well as the backshort distance that resulted directly in 50 Ω real impedance. A transition from microstrip to CPW

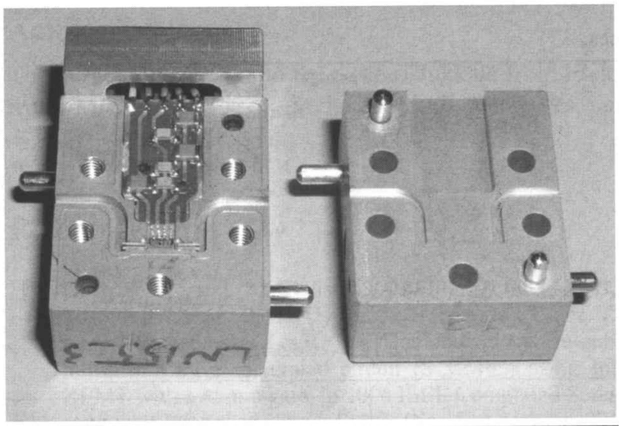

Fig. 7. Photograph of the split-block module with MMIC, waveguide to CPW transitions and DC-feeding network assembled.

is obtained with a short taper from the 50 Ω microstrip to the 47 μm wide center conductor of the CPW added to the transition. CPW structure is completed with two ground pads on the sides, which are connected to the backside metal by plated-through vias. For the transition, the simulations showed a transmission loss below 1 dB and the return loss above 20 dB over 20 GHz band around 150 GHz.

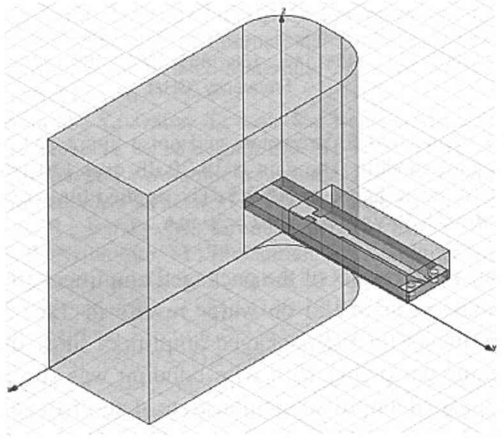

Fig. 8. Simulation model for waveguide to CPW transition.

V. Measurement results for packaged amplifiers

Selected amplifiers were packaged in a split-block waveguide package. The measurement range of packaged amplifiers was limited by the available test equipment. The S-parameters were measured using HP8510C with G-band extension modules, leading to a measurement range of 130-175 GHz. The upper frequency limit is due to the WR-6 package. The noise figures of the packaged amplifiers were measured using same measurement system as with the on-wafer measurements. It is noted that the meaningful noise measurement bandwidth depends on the gain of the amplifier.

First, the optimum bias conditions for each amplifier module were identified by sweeping the supply voltage and the drain current and measuring the noise figure and the insertion gain at a fixed frequency. As an example, the bias sweep for LNA3 is presented in Figs. 9 and 10 for noise figure and insertion gain, respectively.

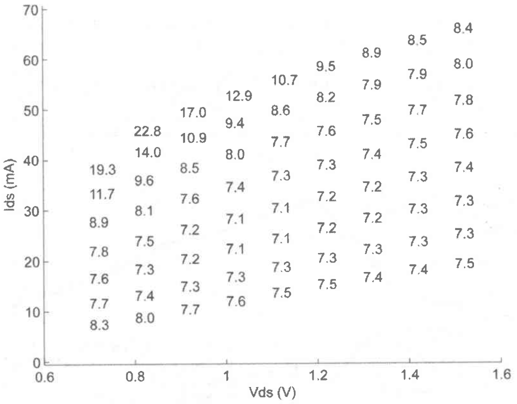

Fig. 9. Noise figure of the LNA3 in a waveguide module with different bias settings at 155 GHz. The gate voltage was swept from -0.1 V to 0.25 V with 0.5 V steps.

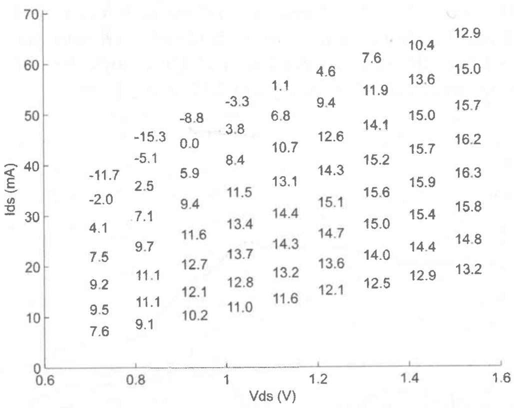

Fig. 10. Insertion gain of the LNA3 in a waveguide module with different bias settings at 155 GHz. The gate voltage was swept from -0.1 V to 0.25 V with 0.5 V steps.

The measurement results for a packaged LNA2 are presented in Fig. 11. With the tuned bias settings, the LNA2 exhibits a gain of 19.5 dB and a noise figure of 6.8 dB at 145 GHz. The values are not directly comparable to the on-wafer measurements due to different biasing conditions. Reasonable input and output match values (<-5 dB) are achieved over a wide bandwidth.

The measurement results for a packaged LNA3 are shown in Fig. 12. A peak gain of 18.9 dB and a noise figure of 6.7 dB are achieved at 151 GHz. Again, reasonable input and output match values are achieved up to 152 GHz. The gain is better than 15 dB at 130-140 GHz range.

Table 2. Comparison of on-wafer and packaged amplifier performances.

Design	On-wafer Frequency (GHz)	On-wafer Gain (dB)	On-wafer NF (dB)	On-wafer Bias	Package Frequency (GHz)	Package Gain (dB)	Package NF (dB)	Package Bias
LNA1	152	22.7	6.0	V_d = 1.09 I_d = 36 mA	N.A.	N.A.	N.A.	N.A.
LNA2	143	19.8	6.3	V_d = 1.54 I_d = 36 mA	145	19.5	6.8	V_d = 1.1 I_d = 24 mA
LNA3	130-154	18.0-19.0	5.5-7.0	V_d = 1.36 I_d = 36 mA	130-154	15.0-18.9	5.5-7.5	V_d = 1.1 I_d = 30 mA
LNA4	130-171	17.6-20.6	5.5-7.0	V_d = 1.18 I_d = 36 mA	130-161	15.0-19.5	5.5-7.5	V_d = 0.8 I_d = 30 mA

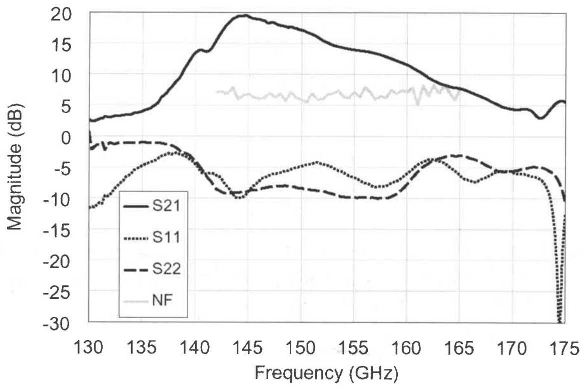

Fig. 11. Measured S-parameters and noise figure of LNA2 in a waveguide module. The peak gain of 19.5 dB with the noise figure of 6.8 dB was achieved at 145 GHz with the following bias conditions Vd = 1.1 V, Vg = 0.1 V, Id = 24 mA.

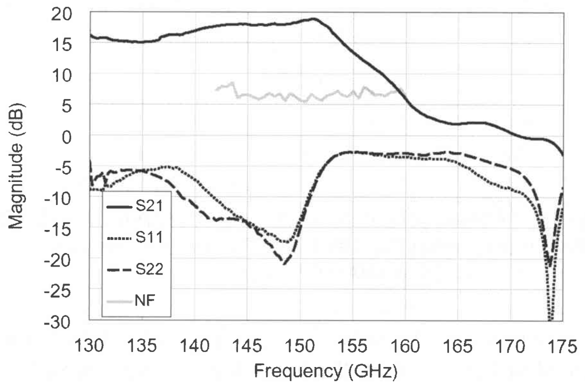

Fig. 12. Measured S-parameters and noise figure of LNA3 in a waveguide module. The peak gain of 18.9 dB with the noise figure of 6.7 dB was achieved at 151 GHz with the following bias conditions Vd = 1.1 V, Vg = 0.05 V, Id = 30 mA.

The measurement results of a packaged LNA4 are presented in Fig. 13. The gain is higher than 15 dB from 130 to 161 GHz and the noise figure values range from 5.5 to 7.5 dB at frequency range of 142-171 GHz.

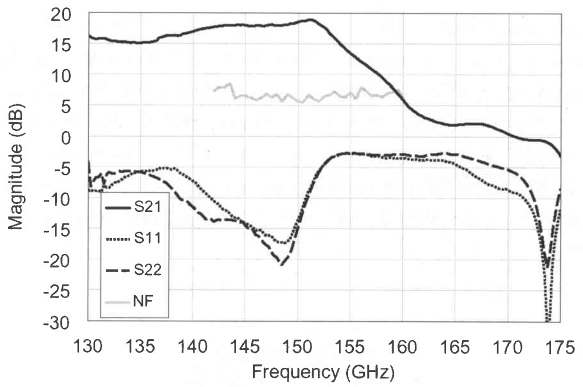

Fig. 13. Measured S-parameters and noise figure of LNA4 in a waveguide module. The gain is 14-20 dB over 130-161 GHz range with noise figure of 5.5-7.5. The applied bias conditions were Vd = 0.8 V, Vg = 0.0 V, Id = 30 mA.

The measured results of the packaged amplifiers are compiled and compared to on-wafer results in Tab. 2. The measurements for the packaged amplifiers show that the waveguide packaging with wire bonding was successful. The packaged amplifiers demonstrate state-of-the-art performance.

VI. Conclusion

Four amplifier designs for D-band operation and their performance have been presented. The on-wafer measurements showed larger gain than was predicted by the simulations. The measured results are comparable when compared to InP HEMT amplifiers. Selected amplifiers were packaged in a split-block waveguide package. The measurements for the packaged amplifier show that the waveguide packaging with wire bonding was successful. The MHEMT technology was found useful for D-band low noise applications. Using MMIC amplifiers the noise figure of D-band radiometers can be lowered, resulting better sensitivity compared to architectures with direct down conversion without preamplification.

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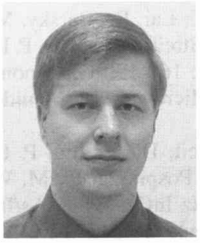
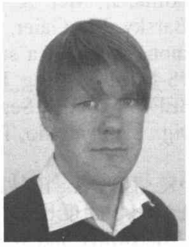


Mikko Kantanen received his M.Sc. and Lic.Sc. degrees in Electrical Engineering from the Helsinki University of Technology (TKK), Espoo, Finland 2001 and 2006, respectively. Since 2001 he has worked as a Research Scientist in MilliLab, VTT Technical Research Centre of Finland, Espoo, Finland, in the areas of millimetre wave integrated circuit design, millimetre wave measurements, and millimetre wave systems. He is a co-recipient of an Asia-Pacific Microwave Conference 2006 Prize.

Mikko Kärkkäinen was born in 1975. He received the Lic. Sc. and the M. Sc. degrees in electrical engineering from the Hel-sinki University of Technology, Espoo, Finland, in 2005 and 2000, respectively. He is currently working towards the Ph.D. degree at the Helsinki University of Technology. In 1998 he started working at the Electronic Circuit Design Laboratory, Helsinki University of Technology. His current research interests are in the field of CMOS millimetre-wave circuits for integrated radio front-ends. He is also a co-recipient of the APMC 2006 Prize for an outstanding contribution to the Asia-Pacific Microwave Conference held in Yokohama, Japan.

Mikko Varonen received the M.Sc. and Lic.Sc. degrees in electrical engineering from the Helsinki University of Technology (TKK), Espoo, Finland, in 2002 and 2005, respectively. He is currently working toward the D.Sc. degree in electrical engineering at the Electronic Circuit Design Laboratory, Helsinki University of Technology.

His research interests involve millimetre-wave integrated circuits. He is a member of the Finnish Graduate School of Electronics, Telecommunications and Automation (GETA). He was the co-recipient of the APMC 2006 Prize for the outstanding contribution to the Asia-Pacific Microwave Conference.



Mikko Laaninen received his M.Sc. from the Helsinki University of Technology in 2003, specializing in micro- and millimeter-wave measurements.

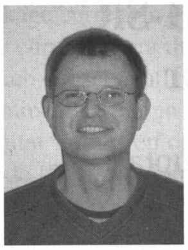
In 2003-2006 he participated in the design and testing of the ESA Planck satellite's 70GHz cryogenic receivers at Ylinen Electronics. Currently he works on commercial telecommunications equipment at Elektrobit, Finland.

Timo Karttaavi received M. Sc. (EE) and Lic. Sc (EE) degrees from the Helsinki University of Technology in 1989 and 2000, respectively.

He spent a year at the Swiss Federal Institute of Technology, Lausanne in 1990-91. From 1991 to 1993 he was with the University of Helsinki developing readout electronics for high energy physics experiments stationed at CERN in Geneva. From 1993 to 2008 he has been with VTT working on microwave and millimeter wave circuits and systems. During 2005-06 he spent a year with the Berkeley Wireless Research Centre in the USA working on millimeter wave CMOS circuits. Since 2008 he has been with Nokia Research Center.

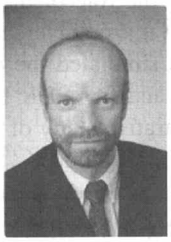
Rainer Weber was born in Offenburg, Germany, in 1978. He received the Dipl.-Ing. (FH) degree in electrical engineering from the University of Applied Sciences Offenburg, Germany, in 2003.

He then joined the High Frequency Devices and Circuits Department of the Fraunhofer Institute for Applied Solid-State Physics (IAF), Freiburg, Germany, where he is involved in the MMIC design of oscillators and amplifiers up to 220 GHz.



Arnulf Leuther received the Dipl. Phys. degree and the PhD degree in physics from the Technical University of Aachen.

He is with the Fraunhofer Institute for Applied Solid State Physics (IAF) since 1996. His research work was focused on the development of III/V-process technology for high frequency MMICs



Matthias Seelmann-Eggebert received his Diploma and Ph.D. degree in physics from the University of Tübingen in 1980 and 1986, respectively.

From 1980 to 1996 he was involved in R&D related to infrared detectors based on HgCdTe and developed electrochemical and surface physical methods for the characterization of compound semiconductor surfaces. From 1990 to 1991 he was a visiting scientist at Stanford University. From 1997 to 2000 he was engaged in the growth of CVD diamond. Since 2001 he is a member of the department of high frequency electronics of the IAF in Freiburg,Germany, and is concerned with the preparation and development of simulation models for active and passive III-V devices.

Tapani Närhi

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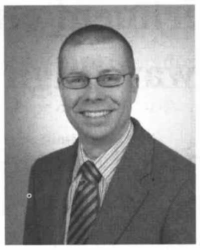

Janne Lahtinen received the M.Sc. (Tech.), Lic.Sc. (Tech.), and D.Sc. (Tech.) degrees from the Helsinki University of Technology (TKK), Finland, in 1996, 2001, and 2003, respectively.

Since 2007, he is the Managing Director of Harp Technologies Ltd, Espoo, Finland. From 2006 to 2007 he was the Director, Space at SF-Design Ltd, Jokioinen, Finland. From 2004 to 2006 he was with Elektrobit Microwave Ltd (Ylinen Electronics Ltd), Kauniainen, Finland serving in various positions, finally as the Manager, Space and Security. From 2002 to 2003 he was a Research Fellow at the ESA-ESTEC in Noordwijk, The Netherlands and from 1995 to 2002 with the TKK Laboratory of Space Technology. His research interests include microwave remote sensing systems and spacecraft hardware. He has authored or co-authored over 50 publications.

Dr. Lahtinen served as a Secretary of the Finnish National Committee of COSPAR from 1997 to 2002. From 2006 to 2007, he was an advisor of the Finnish Space Committee. He was welcomed as a Burgen Scholar by Academia Europaea in 2004, he won the Young Scientist Award of the National Convention on Radio Science (URSI) in 2001, and he received the third place in the IEEE GRS-S Student Prize Paper Competition in 2000.

Kari A. I. Halonen received the M.Sc. degree in electrical engineering from Helsinki University of Technology, Finland, in 1982, and the Ph.D. degree in electrical engineering from the Katholieke Universiteit Leuven, Belgium, in 1987.

Since 1988 he has been with the Electronic Circuit Design Laboratory, Helsinki University of Technology. From 1993 he has been an associate professor, and since 1997 a full professor at the Faculty of Electrical Engineering and Telecommunications. He became the Head of Electronic Circuit Design Laboratory year 1998.

He has been an associate editor of IEEE Transactions on Circuits and Systems I, a guest editor for IEEE Journal of Solid-State Circuits and the Technical Program Committee Chairman for European Solid-State Circuits Conference year 2000. He has been awarded the Beatrice Winner Award in ISSCC'02 Conference year 2002. He is a TPC- member of ESSCIRC and ISSCC. He specializes in CMOS and BiCMOS analog integrated circuits, particularly for telecommunication applications. He is author or co-author over two hundred international and national conference and journal publications on analog integrated circuits.