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Integrated Amplifier Circuits for 60 GHz Broadband Telecommunication

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Abstract. Wide frequency bandwidth has been internationally allocated for unlicensed operation around the oxygen absorption frequency at 60 GHz. A power amplifier and a low noise amplifier are presented as building blocks for a T/R-unit at this frequency. The fabrication technology was a commercially available 0.15 μm gallium arsenide (GaAs) process featuring pseudomorphic high electron mobility transistors (PHEMT). Using on-wafer tests, we measured a gain of 13.4 dB and a +17 dBm output compression point for the power amplifier at 60 GHz centre frequency when the MMIC was biased to 3 volts V_{dd}. At the same frequency, the low noise amplifier exhibited 24 dB of gain with a 3.5 dB noise figure. The AM/AM and AM/PM characteristics of the power amplifier chip were obtained from the large-signal S-parameter measurement data. Furthermore, the power amplifier was assembled in a split block package, which had a WR-15 waveguide interface in input and output. The measured results show a 12.5 dB small-signal gain and better than 8 dB return losses in input and output for the packaged power amplifier.

Key Words: millimetre wave amplifier, MMIC power amplifier, AM-PM conversion, broadband communication

1. Introduction

An increasing number of wireless multimedia applications demand high data rate radio systems. When high data rates are required, we will eventually need to broaden the signal bandwidth. A large amount of spectral space is more easily available at millimetre wave frequencies, because the relative bandwidth is reasonable even if the modulation occupies large amounts of spectrum. The possibilities of the 60 GHz frequency band are interesting because of the wide bandwidth that has been allocated globally for wireless networks. The available frequency bands for 60 GHz broadband networks are shown in Fig. 1. In Europe, the 62–63 GHz and 65–66 GHz bands are allocated for mobile broadband systems (MBS) and the 59–62 GHz band for wireless local area network (WLAN) applications. In the United States, the 59–64 GHz band is intended for general unlicensed applications, while in Japan the 59–66 GHz band is reserved for highspeed data communication. Therefore, 5 GHz of spectral space has been assigned for multimedia services around 60 GHz with a global overlap of 3 GHz (59–62 GHz) [1, 2].

This paper is organised as follows: Section 2 explains the fabrication technology. Section 3 concentrates on low noise amplifier design and Section 4 discusses the power amplifier design. Finally, some conclusions are presented at the end of the paper.

2. Manufacturing Process

The microchips were fabricated using commercial 0.15 μm GaAs PHEMT technology, for which the transistor f_t is 100 GHz. The passives include gold metallisation for interconnections, non-etched GaAs resistors, metal-insulator-metal (MIM) capacitors and ground-VIA-holes through GaAs-substrate. In addition, there are two capacitor plate metal layers, which can also be used for interconnections. It is possible to use air bridges for isolation between two metal layers that cross each other. The backside of the wafer is metallised. Both small-signal and large-signal models for the transistor are provided by the foundry. The measured non-pulsed drain current of a 4×50 μm PHEMT as a function of the drain voltage is shown in Fig. 2. The gate voltage is swept from -0.8 to 0.2 V using 0.1 V steps.

3. Low Noise Amplifier

At millimetre wave frequencies the available gain is often relatively low for a single transistor. The noise

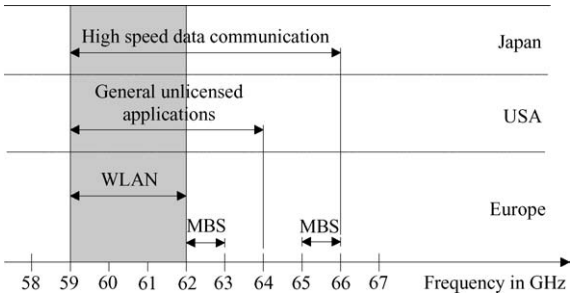

Fig. 1. Available frequency bands for 60 GHz wireless broadband networks.

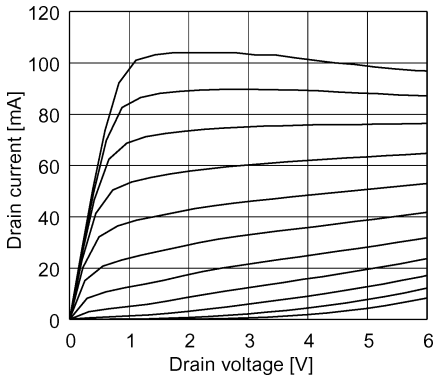

Fig. 2. Measured IV-curves for a 4 × 50 μm PHEMT.

contribution of the following stage becomes significant, which makes the LNA design more important. Furthermore, it becomes difficult to attain a total noise figure that would only be a small fraction larger than the minimum noise figure when designing a multistage amplifier. The overall gain of the low noise amplifier has to be large enough in order to make the noise produced in the following block as insignificant as possible when the total system noise figure is calculated.

Here we present a three-stage LNA that was designed and measured [3]. The first two stages are 2 × 25 μm transistors. The output stage is a 2 × 50 μm device in order to improve linearity and gain.

3.1. Noise Modelling

A simple model is fitted to simulate the noise parameters of the transistor. This model can be used for simulating the frequency dependence of the noise parameters [4]. Sometimes, a two or even three-parameter temperature noise model can be used [5]. The physical temperatures of the drain, gate and the gate-to-source resistances are raised in order to increase their noise power contribution in these models. The third parameter is needed if the gate Schottky-contact has a significant leakage current. The noise model is presented in Fig. 3.

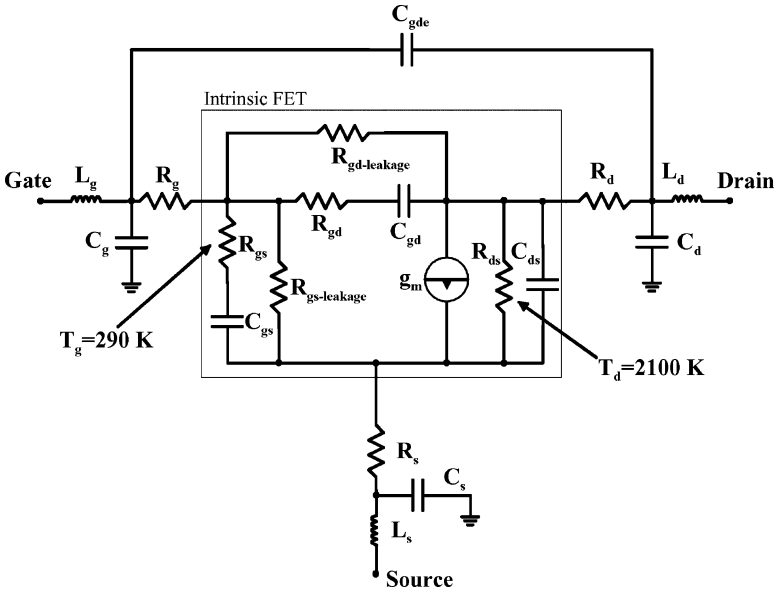

Fig. 3. Temperature noise model for a 2 × 25 μm pseudomorphic HEMT.

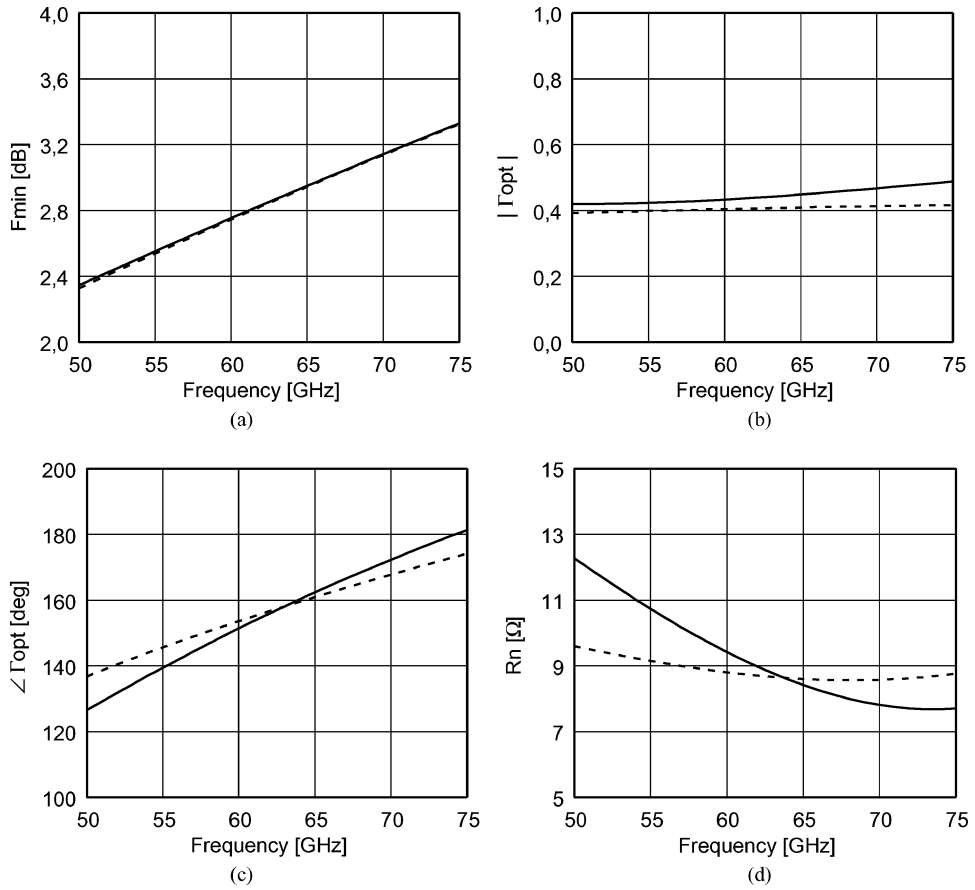

Fig. 4. Measured and simulated noise parameters. The dashed lines represent the modelled values. The minimum noise figure is presented in (a), the magnitude of the optimum noise match in (b), the angle of the optimum noise match in (c) and the noise resistance in (d).

There was no noise model provided by the foundry at the time of the LNA design. The noise parameters of the transistor were measured from 50 to 75 GHz and then the temperature noise model was adjusted to match the measured data. A single-parameter model proved adequate to model the noise characteristics of the transistor in our case. The temperature of the drain-to-source resistance was raised to 2100 K. The measured and simulated noise parameters of a 2×25 μm PHEMT biased at 0.0 V of gate voltage and 14 mA of drain current are presented in Fig. 4. The noise parameters and the results produced by the model are similar, but the noise resistance has the largest deviation from the measured values. This may be caused by the lack of correlation of the noise sources in the model; it is behaviour similar to that observed in [6]. The noise parameters of the transistor were measured using methods that are described in [7, 8].

3.2. Low Noise Amplifier Design

The input match of the amplifier was balanced between optimum noise and gain. Inductive series feedback was introduced by a lengthened and narrowed source ground-VIA connection, which can easily be realised with high precision on an MMIC. This helps in bringing the optimum noise and conjugate input gain match impedances closer to each other [9]. The input is matched with an open shunt stub and bias is inserted through a quarter wave short-circuited stub. The output is matched with a short-circuited shunt stub that is shorter than quarter wavelength and thus acts as an inductive shunt element. The supply is inserted to the vicinity of the short circuit capacitor and the ground-VIA-hole to make the DC-connections as invisible as possible at RF-frequency. The schematic of the low noise amplifier is presented

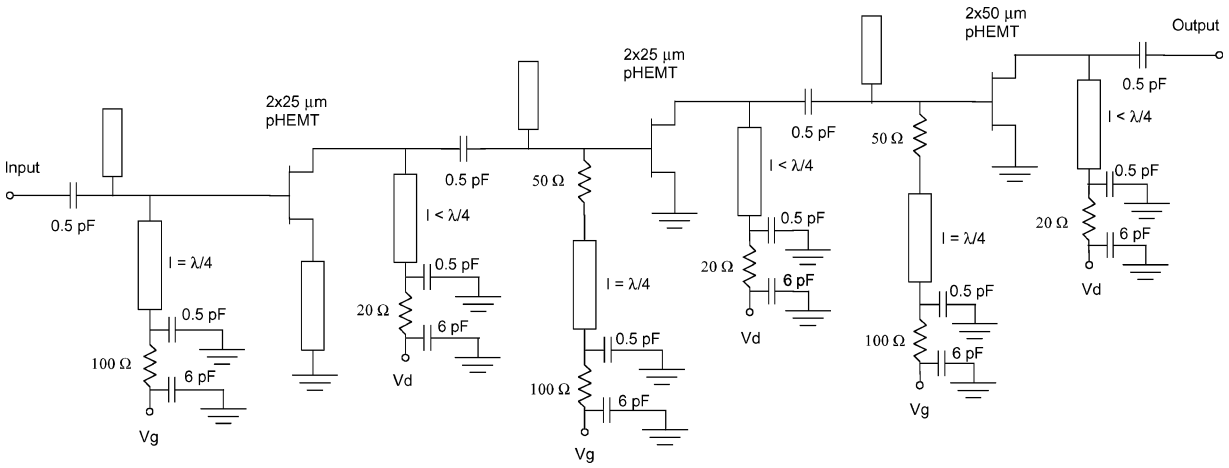

Fig. 5. Simplified schematic of the low noise amplifier.

in Fig. 5. Series microstrip lines are left out for simplicity.

Stabilisation RC-networks are attached to the bias lines to enhance out-of-band stabilisation. DC-decoupling and short-circuiting capacitors are 0.5 pF. The RC-stabilisation network consists of a 100 Ω series resistor and 6 pF shunt capacitor. For drain stabilisation, a 20 Ω series resistor is used. In addition, resistively loaded high impedance stubs with 50 Ω resistors were used in the gate biasing networks of the last two stages to further improve out-of-band stability. The first two stages are biased at 2.5 V/14 mA and the last stage at 4.5 V/30 mA (drain voltage/current).

3.3. Low Noise Amplifier Measurement Results

A photograph of the manufactured low noise amplifier is presented in Fig. 6. The LNA was mounted on a measurement jig in order to ensure low frequency stability. The bias pads were bonded to single layer capacitors, which were placed next to the microchip on the measurement jig. To further enhance stability, feed-through capacitors were used and series ferrites were connected to the bias feed lines, as can be seen in Fig. 7. The RF pads are not bonded for enabling coplanar RF-probe measurements. The measured scattering parameters, excluding S_{12}, are presented in Fig. 8. The S_{21} peaks at 55 GHz and it is significantly higher than in the simulations. The measured gain is 24 dB and the noise figure is 3.5 dB at 60 GHz. The noise measurement results can be seen in Fig. 9.

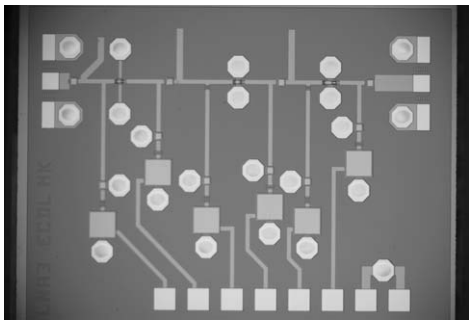

Fig. 6. Photograph of the manufactured LNA. The chip size is 2.0×1.5 mm^2.

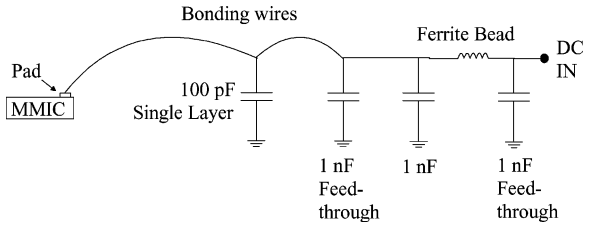

Fig. 7. The schematic of the jig stabilisation circuitry.

4. Power Amplifier

In order to obtain high output power from a MMIC amplifier, a large output device periphery is needed. A previously fabricated power amplifier design showed that a 14 dBm output compression point with a 15.5 dB overall gain can be achieved using a single transistor output stage [3].

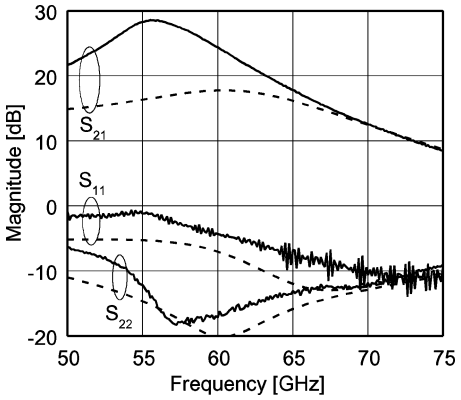

Fig. 8. Measured and simulated S_{11}, S_{21} and S_{22} of the low noise amplifier. Dashed lines represent simulated values.

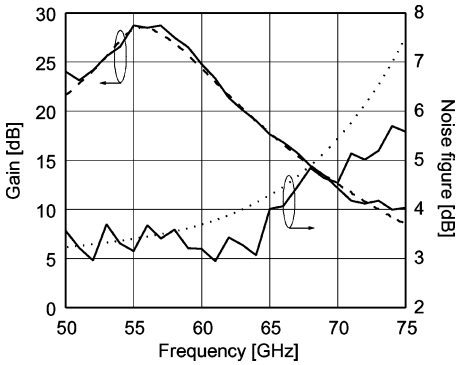

Fig. 9. Measured gain and noise figure. The S_{21} from the vector network analyser measurement is added for reference (dashed line). The dotted line represents the simulated noise figure.

4.1. Power Amplifier Design

To increase the output power, the size of the output stage of the power amplifier has to be enlarged. However, a large transistor has low gain. This means that the size of the driver and the gain stages have to be increased to ensure that these stages can drive the output stage into saturation. This may lead to low total gain for the amplifier. To achieve a high output power level without degrading the gain of the output stage, a large transistor can be divided into smaller devices. The power amplifier presented here is a three-stage single-ended amplifier with a total output periphery of 420 μm. The output stage consists of two 6×35 μm cells and the power is combined on chip. The driver and the gain stages were both chosen to have device peripheries of 6×35 μm [10].

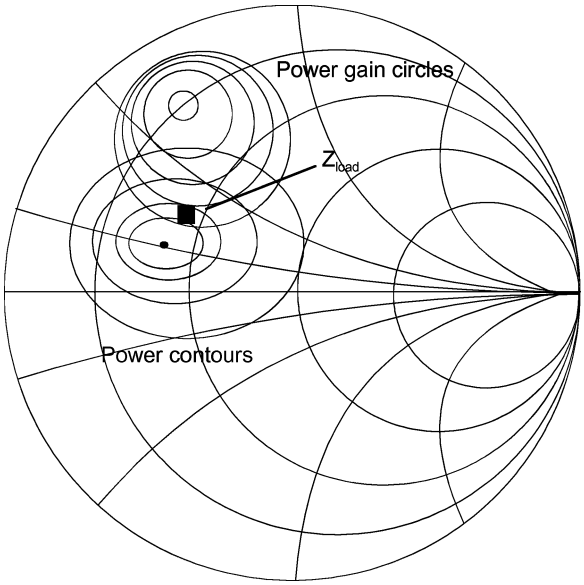

Fig. 10. Simulated power contours using 0.2 dB steps, power gain circles using 0.3 dB steps and the output match Z_{load} for a 6×35 μm PHEMT.

An appropriate output match had to be designed to utilise the power capability of the chosen transistor. This was accomplished by simulating the circuit using the large-signal model, which was provided by the foundry, and the harmonic balance technique. The results of the simulations are presented in Fig. 10, where the simulated power contours of a 6×35 μm transistor are drawn on a Smith chart. In addition, the chart includes the power gain circles of the transistor and the realised output match Z_{load}. It can be seen that the impedance for the maximum power and the maximum gain match differ from each other significantly.

The driver and the gain stages were designed to run with 2 dB back-off. This was accomplished by choosing both the driver and the gain stages to have device peripheries of 6×35 μm and by presenting a proper match to each amplifier stage, i.e. the driver stage output match was balanced between optimum power and gain and the gain stage was designed for maximum gain. The simulated gain compression curves for the three stages are presented in Fig. 11. All the stages operate in class A. The output stage reaches 1 dB compression with two decibel lower input power compared to the driver stage. Correspondingly, the driver stage reaches 1 dB compression with two decibel lower input power when compared to the gain stage.

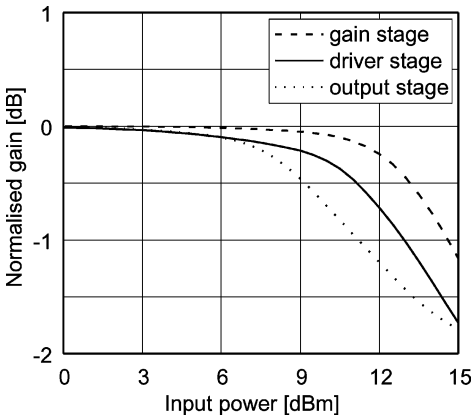

Fig. 11. Simulated gain compression of the power amplifier stages at 60 GHz. The gains are normalised.

Matching at 60 GHz is realised with open shunt stubs and series transmission lines as shown in the schematic in Fig. 12. The matching circuitry of the output stage performs both power combining and dividing as well as the matching of the output cells. The output match is realised in two parts. First, the 50 Ω load impedance is converted to a lower impedance level and then the impedance at the power combining point is matched to the desired impedance Z_{load} for the output transistors. A broadband output match is achieved.

The design of the bias networks is important when considering low frequency stability. The choice of decoupling elements and the bias insertion point are critical [11]. The biasing scheme of the amplifier is presented in detail in Fig. 13. The transistors are biased through high impedance quarter wave length shunt stubs, which are short circuited with a ground-VIA-hole. A small-valued metal-insulator-metal (MIM) capacitor (0.12 pF) is used to prevent the DC from being grounded. The capacitance forms a resonance circuit with the series inductance of the VIA-hole at 60 GHz design frequency. This is a low impedance point, which is suitable for bias insertion. A series resistor (30–50 Ω) is placed at the end of the gate biasing stub for out-of-band stabilisation. Low frequency stability is ensured with 40 Ω resistors that are in series with stabilising capacitors (5–8 pF). In addition, gate bias is fed through a 100 Ω series resistor.

The even mode stability of the power amplifier was simulated using μ-factor analysis [12]. Unconditional stability was required ($\mu > 1$). The stability of the individual stages and the overall stability of the amplifier were checked from a few megahertz to over the unity gain frequency of the transistor.

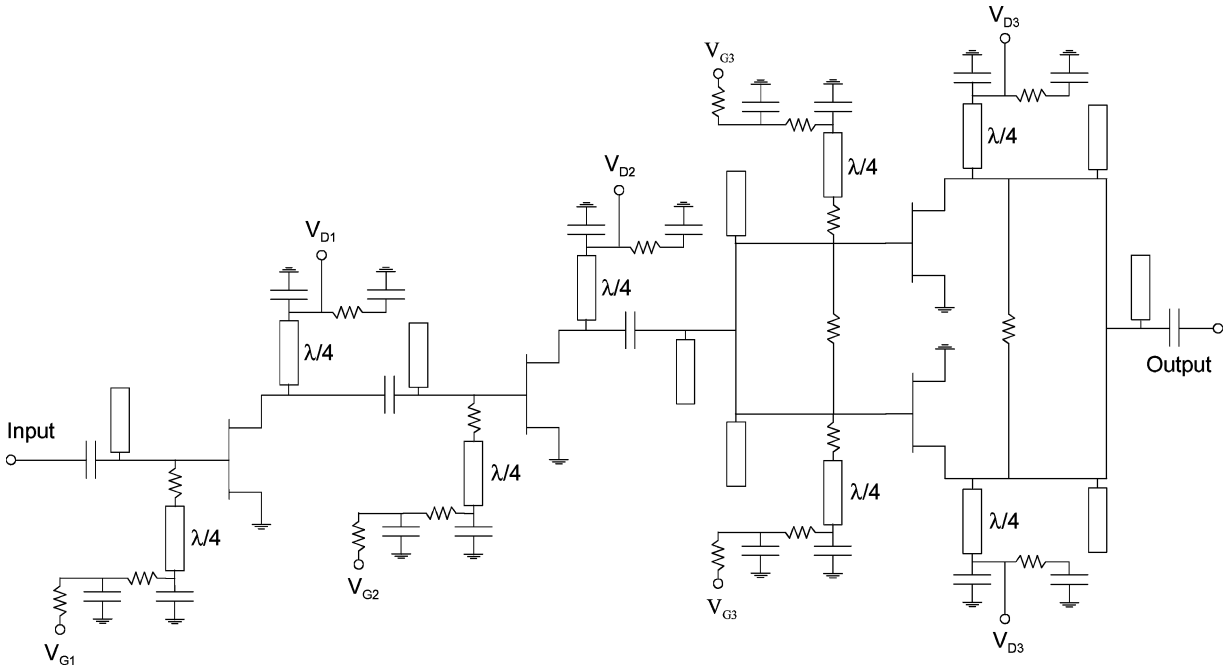

Fig. 12. Simplified schematic of the power amplifier.

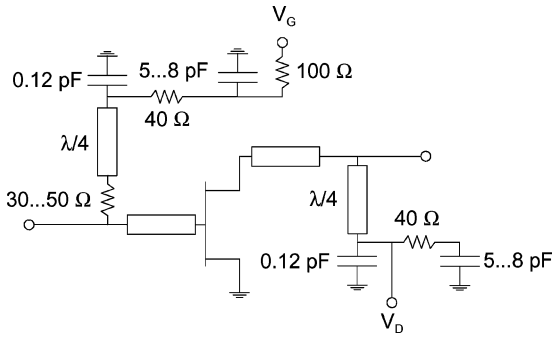

Fig. 13. Schematic of the power amplifier biasing network.

The power combining of the output stage may introduce a possible odd mode oscillation problem. To suppress odd mode oscillations, 80 Ω resistors were added between the output cells [13]. To further enhance the odd mode stability, the layout of the output stage was designed to be symmetrical [14]. Then the odd mode stability of the amplifier was carefully analysed using a CAD–suitable method described in [15].

A photograph of the manufactured power amplifier chip is presented in Fig. 14. After on-wafer measurements, the chip was assembled in a split block package. The package has WR–15 waveguide input and output interfaces. Alumina microstrip transitions are used to match the high impedance of the waveguide and the 50 Ω input and output impedances of the amplifier. The biasing circuit of the package includes additional RC-networks to improve low frequency stability. A photograph of the split block package is presented in Fig. 15.

4.2. Power Amplifier Measurements

The on-wafer small- and large-signal S-parameters were measured with coplanar RF-probes. The bias was

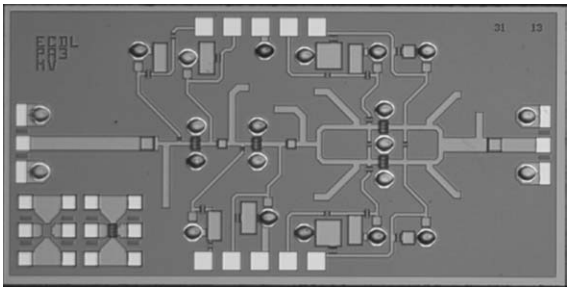

Fig. 14. Photograph of the power amplifier chip. The chip size is 3.0×1.5 mm^2.

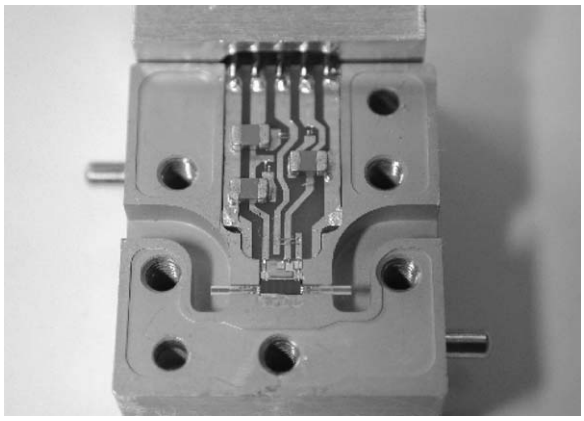

Fig. 15. Photograph of the split block package.

inserted with a DC-probe that has additional decoupling capacitors for enhanced bias circuit stability. The packaged power amplifier was measured in a WR-15 waveguide environment.

4.2.1. On-wafer Measurement Results The measured small-signal S-parameters and the simulated small-signal gain are presented in Fig. 16. The amplifier was biased to the nominal 3.0 V of drain voltage and 325 mA of total drain current. The drain currents are 162 mA, 81 mA and 82 mA for the power, driver and the gain stages, respectively. A small-signal gain of 13.5 dB is measured at 62 GHz. The corresponding input and output return losses are around 6.5 dB. Very good agreement between simulated and measured small-signal gain is achieved.

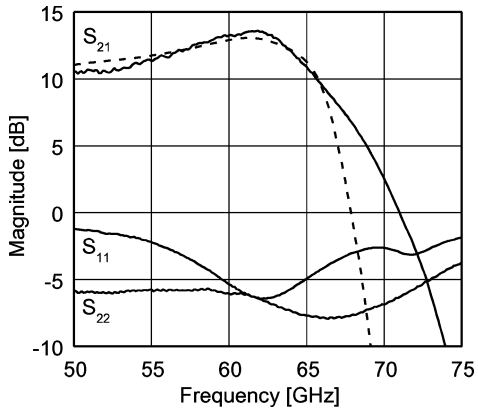

Fig. 16. Measured on-wafer small-signal *S*-parameters of the power amplifier. The dashed line represents simulated S_{21} (Supply voltage/total current: 3.0 V/325 mA).

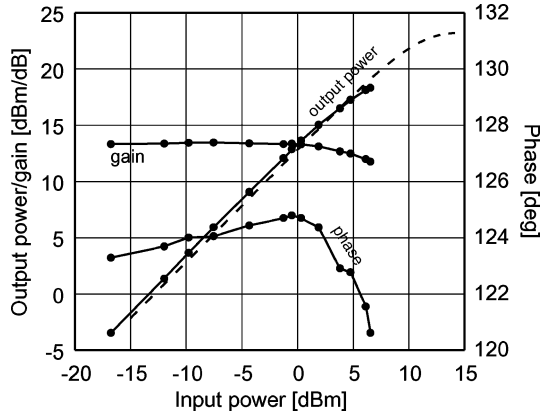

Fig. 17. Measured on-wafer AM/AM and AM/PM characteristics of the power amplifier at 60 GHz. The dashed line represents the simulated output power (Supply voltage/total current: 3.0 V/325 mA).

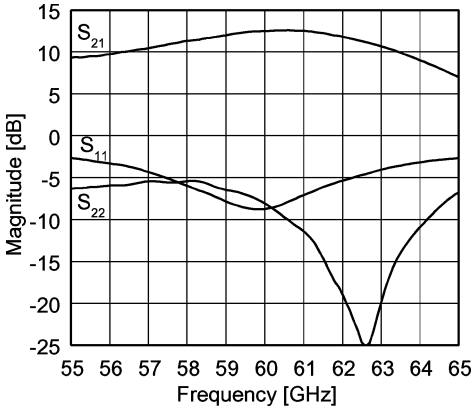

Fig. 18. Measured small-signal *S*-parameters of the packaged power amplifier (Supply voltage/total current: 3.0 V/320 mA).

The AM/AM and AM/PM characteristics were obtained from the large-signal S-parameter measurement data. Because of the high output power level obtained from the measurement system, it was possible to drive the power amplifier into a 2 dB compression during the large-signal S-parameter measurements, although the amplifier seems to be capable of delivering even more power when driven into deeper saturation. The measured amplitude and phase conversion at 60 GHz frequency are presented in Fig. 17. The equivalent simulated output power of the amplifier is also shown. The measured output compression point is at a +17 dBm power level and the large-signal gain is 13.4 dB. The power-added efficiency at 1 dB compression is approximately 5.5%. The phase response of the power amplifier shows good phase linearity.

Table 1 lists the largesignal characteristics of the power amplifier with different supply voltages at 60 GHz. When compared to the previous work [3], a 3 dB higher 1 dB output compression point was measured. Because of the designed 2 dB back-off used in the driver and the gain stages, a 2 dB lower gain was achieved. The gain could be improved by carefully optimising the size of these stages.

Table 1. Measured on-wafer large-signal performance of the power amplifier at 60 GHz.

Drain voltage (V)	Drain current (mA)	Gain (dB)	1 dB compression point (dBm)
This work			
2.5	324	14	16
3.0	325	13.4	17
3.5	325	12.4	17
4.0	327	11.8	16
Previous work [3]			
3.0	150	15.5	14

4.2.2. Module Measurement Results The measured small-signal S-parameters and large-signal characteristics of the packaged amplifier are shown in Figs. 18 and 19, respectively. The small-signal gain is approximately 12.5 dB. The packaged power amplifier exhibited less than a 1 dB lower small-signal gain when compared to the on-wafer measurements. The input

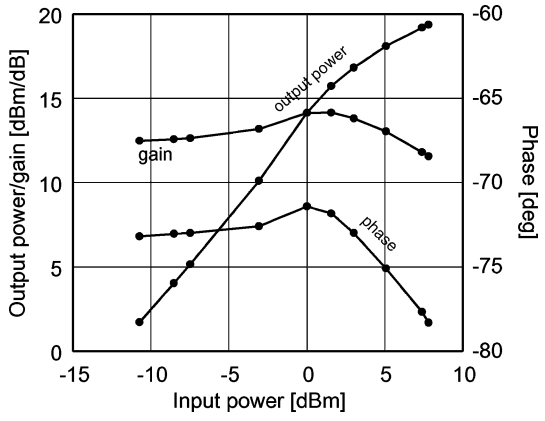

Fig. 19. Measured AM/AM and AM/PM characteristics of the packaged power amplifier at 60 GHz. The supply voltage is 3.0 V and the total drain current 320 mA.

and output return losses of the packaged power amplifier are better than 8 dB at 60 GHz.

5. Conclusions

In this paper, we present high-performance MMIC amplifier circuits for 60 GHz broadband telecommunications. The low noise amplifier has a noise figure of 3.5 dB and a 24 dB gain. A simple noise model was fitted to the measured noise data and the results show a good agreement between measured and simulated values. The accurate transistor noise model can be used for precise low noise amplifier design.

The power amplifier was designed using both linear and nonlinear methods. Extensive precautions were practised to ensure that the amplifier is stable in both cases of oscillation modes that can occur in a multidevice amplifier. The AM/AM and AM/PM conversion of the power amplifier was measured on-wafer and in a split block package environment. The measured phase and gain responses showed good linearity. The measured 1 dB output compression point was at a $+17$ dBm power level and the small-signal gain was 13.4 dB. The packaged amplifier had 12.5 dB of small-signal gain and better than 8 dB return losses in both input and output.

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