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Design Aspects of 65-nm CMOS MMICs

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***Abstract*—We present design aspects and techniques for millimeter-wave circuits implemented in 65-nm CMOS. Different transmission line topologies are discussed and measurement results for a conventional coplanar waveguide and slow-wave coplanar waveguide implemented in 65-nm CMOS are shown. The attenuation of the on-chip transmission lines can be reduced by using slow-wave coplanar waveguides. A 1-stage cascode amplifier in 65-nm CMOS employing inductors as matching elements is presented. On-chip interconnections of the amplifier are implemented and modeled using coplanar waveguides. The ground plane of the coplanar waveguide provides a good ground reference for the entire circuit.**

I. Introduction

There are many emerging millimetre wave applications, which demand for low unit cost manufacturing solutions. The complementary metal oxide semiconductor (CMOS) technology has received a lot of interest since it enables mass production and integration of both digital and analogue functions on the same microchip. The device scaling of CMOS technologies improves the performance of the transistors in terms of a higher unity gain frequency (f_T) and maximum frequency of oscillation (f_{MAX}). We have already demonstrated 40 GHz and 60 GHz amplifiers and a V-band balanced mixer in 65-nm baseline CMOS achieving state-of-the-art performance [1][2]. The continuing scaling of bulk CMOS process typically introduces some challenges to the designer. These include lower supply voltage, stringent metal density requirements and thinner dielectric layers above the substrate leading to higher substrate losses of passives. In this paper, we discuss design aspects for millimetre wave circuits implemented in 65-nm CMOS.

II. Transmission Lines in Nanoscale CMOS

A. Design Considerations and Simulations

Thinner dielectric layers above the substrate of a nanoscale CMOS process and stringent metal density requirements set limitations for implementing transmission lines on silicon. A way to realize a conventional coplanar waveguide in nanoscale CMOS is presented in Fig. 1. The top metal layer is used for the centre conductor. Dummy metal is not allowed around the centre conductor or in between the ground planes of the CPW at any metal level. On the other hand, the metal density requirement has to be fulfilled which means that there has to be enough metal at all metal levels. This is accomplished by strapping all the other metal layers together with vias to form the ground plane for the CPW. The width of the centre conductor W and the distance between the center conductor and the ground plane S can be used for realizing different characteristic impedances for the CPW. A wider centre conductor leads to lower conductor losses. In principle, the maximum width of the centre conductor is limited by the layout design rules of the chosen process. The metal density requirements set the limits for the maximum distance between the centre conductor and the ground plane for the CPW.

Because of the thin dielectric layers of a nanoscale CMOS process, the lossy silicon substrate is very close to the CPW, which causes increased substrate loss. One way to minimize the effect of the conductive substrate is to use the microstrip structure instead of the CPW. The microstrip line is realized between the top metal and lower metal planes. Ideally, this isolates the effect of the lossy silicon substrate. The removal of dummy metal from both underneath and the vicinity of the centre conductor can create a metal density problem. A way to realize a microstrip line in a CMOS technology is shown in Fig. 2 [3]. Drawing ground planes similar to a CPW-line fulfills the metal density requirements. These ground planes are then connected together using lower metal levels. The wide ground plane on the lower metal level must have longitudinal slots, which do not interfere with longitudinal ground currents of the microstrip line. When the height H of the dielectric material is rather low and when the top ground planes are located far from the center conductor, the signal propagates mostly in microstrip mode. In a nanoscale CMOS technology the more stringent metal density requirements render the design of millimeter wave circuits even more problematic. A rather large change in the width of the centre

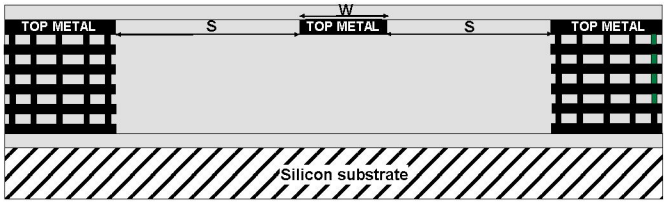

Fig. 1 Simplified cross-section of the conventional coplanar waveguide.

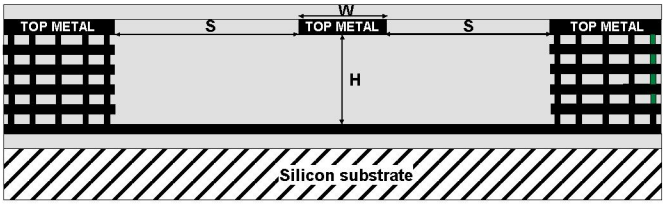

Fig. 2 Simplified cross-section of the microstrip line with sidewalls.

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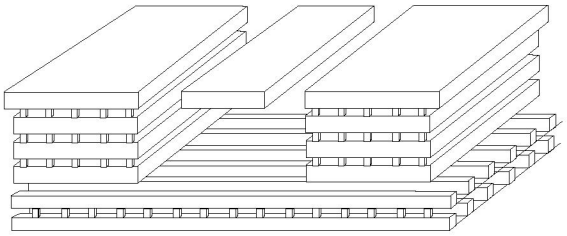

Fig. 3 Simplified cross-section of the slow-wave coplanar waveguide. Two lowest metal layers are strapped together with vias to form the floating shield strips.

conductor is needed to achieve a significant change in characteristic impedance, because of the low height of the dielectric layers. Thus, a wide range of impedances is difficult to realize, because the width of the centre conductor is limited by metallic losses in the narrow case and by the design rules in the wide case.

As discussed above, in the conventional coplanar waveguide the electromagnetic field penetrates into the silicon substrate, which increases losses. A metal shield structure can be drawn using the lowest metal levels to prevent the electromagnetic fields from penetrating into the lossy silicon substrate. An efficient way to realize the shield is the slow-wave structure employing floating shield strips [4]. The simplified cross section of the slow-wave coplanar waveguide implemented in this work is shown in Fig. 3. Two lowest metal layers are strapped together with vias to form the floating shield strips.

Electromagnetic simulations (Ansoft HFSS) were performed for the three different transmission line topologies presented above i.e. the conventional CPW, microstrip line and slow-wave CPW. For the transmission lines, a width W of a 12 µm was used for the centre conductor and the distance between the centre conductor and the ground plane S was 9 µm. The microstrip line was constructed by connecting sidewalls to the bottom metal ground plane and the height H was set to 2.4 µm. In the slow-wave CPW the width of the shield strip and the spacing between the strips was set to 1 µm.

The simulated attenuation α and phase constant β were calculated using equations found in [5]. The simulated attenuations per unit length are shown in Fig. 4. The Q-factor of a transmission line resonator can be calculated from

$$Q = \frac{\beta}{2\alpha}. \qquad (1)$$

The simulated Q-factors are shown in Fig. 5. The conventional CPW has the highest attenuation and lowest Q-factor. The attenuation per unit length reduces significantly when using a microstrip line. The slow-wave CPW has the lowest attenuation and highest resonator Q-factor.

B. Measurement Results

Test structures were realized on a 65-nm CMOS for characterizing a conventional CPW and a slow-wave CPW. A test structure for the conventional CPW is shown in Fig. 6. A width of 12 µm was used for the centre conductor and the distance between the centre conductor and the ground plane was 9 µm. The slow-wave CPW is constructed by strapping two lowest metal layers together to form the floating shield strips. The shield is designed using minimum design rules in order to suppress the induced current flow in the direction of the propagating RF-signal. This minimizes the ohmic losses and maximizes the reactive energy storage per unit length. The smallest allowable shield strip spacing minimizes the exposure of the overlying CPW to the conductive substrate [4].

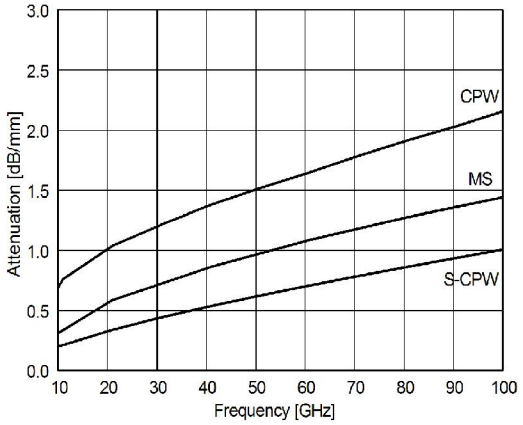

Fig. 4 EM-simulated attenuation per unit length dB/mm of the conventional coplanar waveuide (CPW), microstrip line (MS) and slow-wave coplanar waveguide (S-CPW).

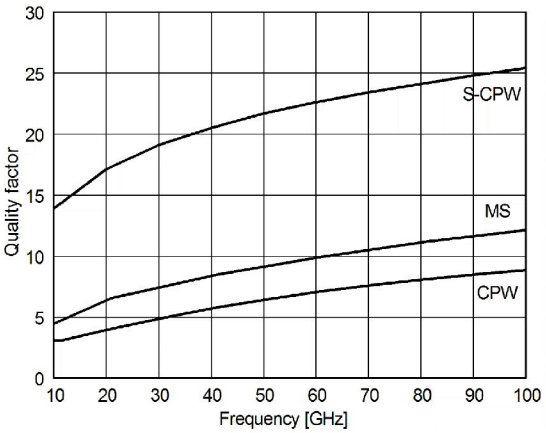

Fig. 5 EM-simulated Q-factor of the conventional coplanar waveuide (CPW), microstrip line (MS) and slow-wave coplanar waveguide (S-CPW).

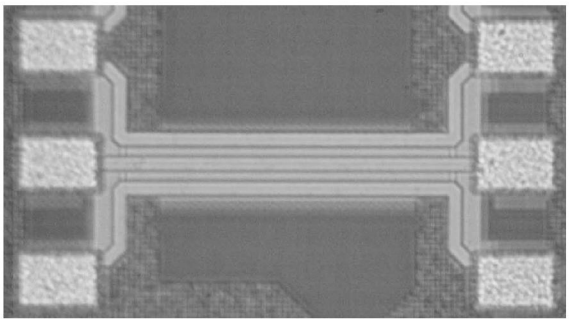

Fig. 6 Micrograph of a CPW test structure implemented in 65-nm CMOS.

The measured characteristic impedance of the conventional CPW is around 47 Ω. Because of the shield strips, the relative dielectric constant for the slow-wave CPW is higher and the resulting characteristic impedance for the slow-wave version is lower (around 35 Ω).

The measured attenuation per unit length and quality factor for both conventional and slow-wave CPW are shown in Fig. 7 and Fig. 8, respectively. Even though the direct comparison of the CPW structures having different impedances is difficult, the transmission line attenuation of the slow-wave coplanar waveguide is significantly lower when compared to the conventional coplanar waveguide.

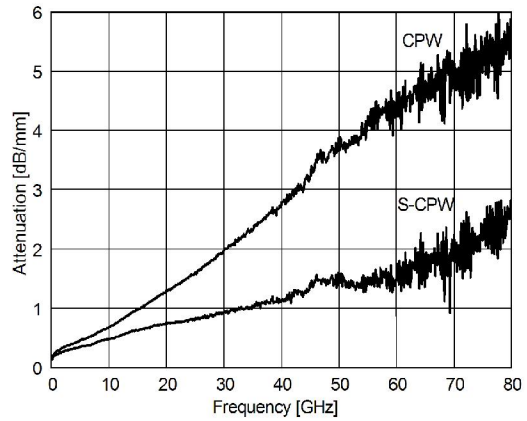

Fig. 7 Attenuation per unit length of the conventional and slow-wave CPW.

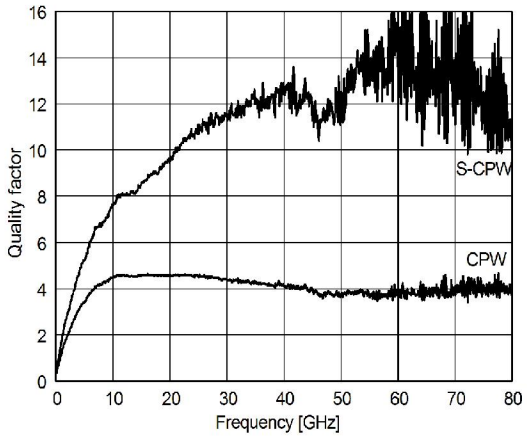

Fig. 8 Quality factor of the conventional and slow-wave CPW.

III. Active Test Structures in 65-nm CMOS

A. 30-GHz Amplifier

At millimeter waves, the transmission line matching networks provide a well-defined ground for the circuit. Another approach to perform on-chip matching is to use lumped elements such as inductors. At millimetre waves, the use of inductors becomes challenging, since the return currents of the circuit may not be explicit, which may result in inaccurate frequency response.

A principle layout/schematic and micrograph of a 1-stage cascode amplifier employing inductors as matching elements is presented in Fig. 9 and Fig. 10, respectively. On-chip interconnections are implemented and modelled using coplanar waveguides. The coplanar waveguide provides a ground reference for the circuit.

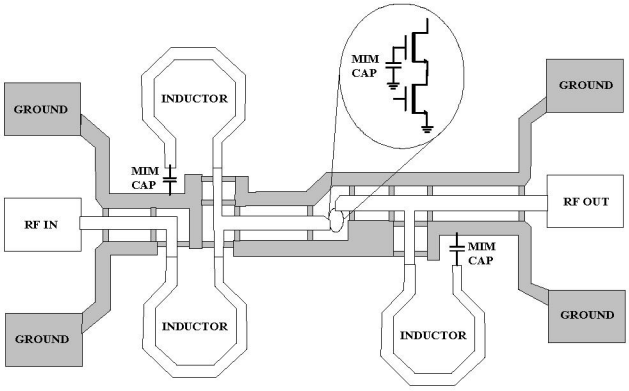

Fig. 9 Principle layout of the 30-GHz amplifier. Inductors are used for matching the cascode transistor. Coplanar waveguides are used for interconnections. The ground plane of the coplanar waveguide is used for ground reference for the circuit. Lower metal layers are used for connecting the ground planes of the CPW together around the discontinuities.

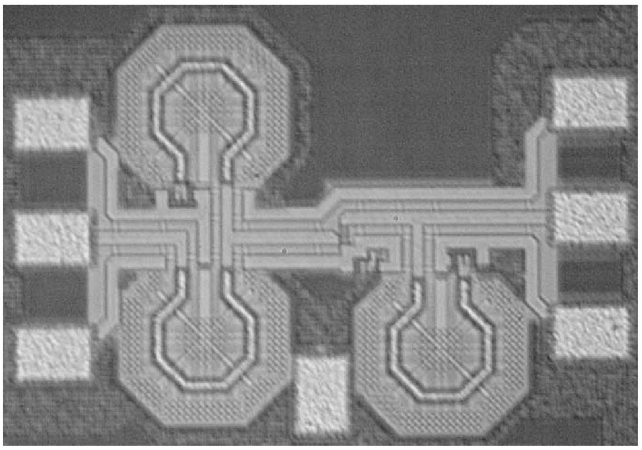

Fig. 10 Micrograph of the 30-GHz amplifier in 65-nm CMOS. Chip-area including pads is 0.54 mm x 0.36 mm.

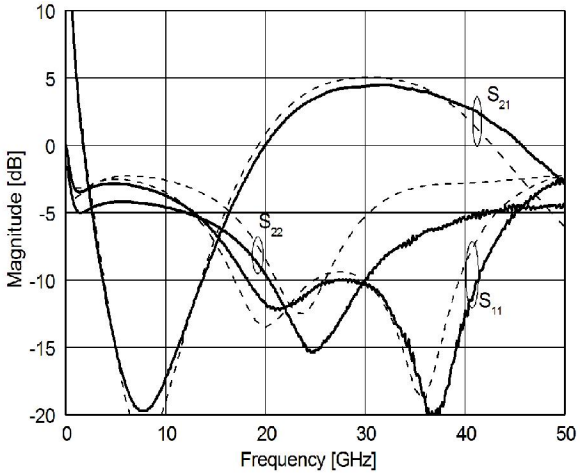

Fig. 11 Measured and simulated S-parameters of the 30-GHz amplifier implemented in 65-nm CMOS.

The input of the amplifier is matched to 50 Ω using a series and short-circuited shunt inductor. The short-circuit is implemented using a metal-insulator-metal capacitor (2 pF). The low frequency stability is ensured using resistor-capacitor networks. A short-circuited shunt inductor is used for matching the output of the amplifier to 50 Ω.

The simulated and measured S-parameters of the amplifier are shown in Fig. 11. Because of the use of CPWs as interconnections and the ground plane of the CPW as a ground reference for the circuit, there is a good agreement between measured and simulated response. The measured small-signal gain is 4.5 dB at 32 GHz.

B. Transistor test structure in 65-nm CMOS

A CPW test structure, shown in Fig. 12, was developed for characterizing a common-source NMOS-transistor up to at least 60 GHz. The transistor data was de-embedded using open and short de-embedding [6]. The measured maximum stable gain is 9.4 dB at 60 GHz.

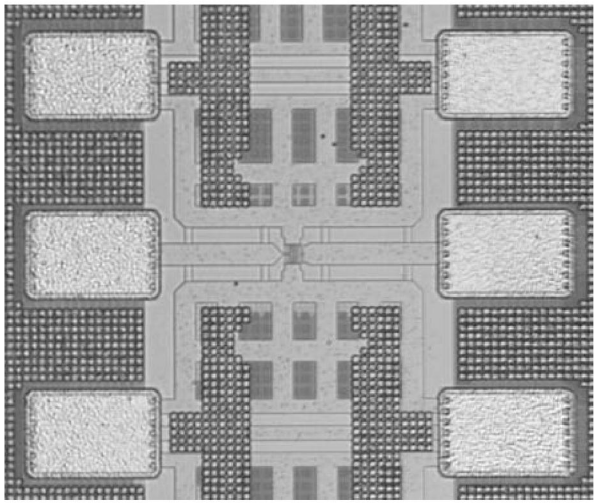

Fig. 12 A coplanar waveguide transistor test structure in 65-nm CMOS.

Although the design target was at 60 GHz the measurements were performed up to 110 GHz. The measured scattering-parameters of the test structure are shown in Fig. 13. As can be seen, a gain peak of 4.7 dB occurs at 97 GHz, which was not expected in the original design. The resonance is caused by the parasitic capacitance of the pad and by the length of the input and output CPWs. This can be simulated by using CPW and pad model for the test structure as presented in Fig. 14. Parasitic capacitances and resistances were extracted from the transistor layout. At millimeter wave frequencies, the effect of parasitic inductances becomes significant. Thus, small valued series inductors were used to model the access parasitic of the transistor. As can be seen from Fig. 13, a good agreement between simulations and measurements is achieved.

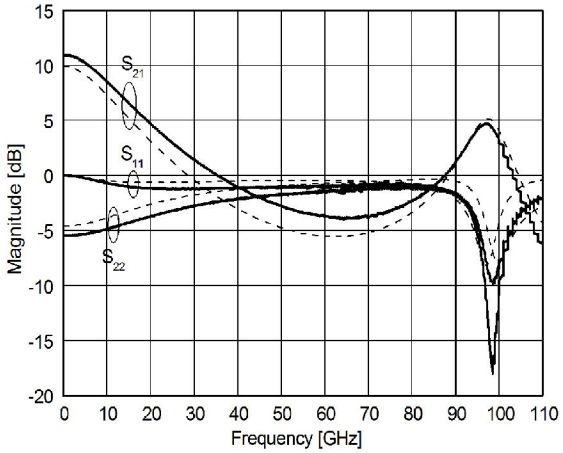

Fig. 13 Measured and simulated S-parameters of the transistor test structure.

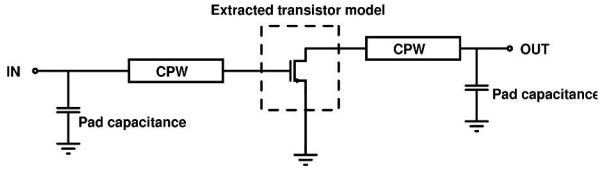

Fig. 14 The schematic for simulating the transistor test structure.

IV. Conclusions

In this paper we discussed and presented design aspects for implementing transmission lines in 65-nm CMOS. The attenuation of the on-chip transmission lines can be reduced by using slow-wave coplanar waveguides. A 30-GHz amplifier employing inductors and coplanar waveguides was presented. As the CPW provides a good ground reference for the circuit a good agreement between simulated and measured response is achieved.

Acknowledgment

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References

[1] M. Varonen, M. Kärkkäinen, and K. A. I. Halonen, "Millimeter-wave amplifiers in 65-nm CMOS," in *Proc. of the European Solid-State Circuit Conf.*, Munich, Germany. Sep. 2007, pp. 280-283.

[2] M. Varonen, M. Kärkkäinen, and K. A. I. Halonen, "V-band balanced resistive mixer in 65-nm CMOS," in *Proc. of the European Solid-State Circuit Conf.*, Munich, Germany. Sep. 2007, pp. 360-363.

[3] Y. Jin, M. A. T. Sanduleanu, E. Alarcon Rivero, and J. R. Long, "A millimeter-ave power amplifier with 25dB power gain and +8dBm saturated output power," in *Proc. of the European Solid-State Circuit Conf.*, Munich, Germany. Sep. 2007, pp. 276-279.

[4] T. S. D. Cheung, and J. Long, "Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 1183-1200, May 2006.

[5] W. R. Eisenstadt, and Y. Eo, "S-parameter-based IC interconnect transmission line characterization," in *IEEE Trans. on Comp., Hybrids, and Manufacturing Tech., vol. 15, pp. 483-490, Aug. 1992.*

[6] M. C. A. M. Koolen, J. A. M. Geelen, M. P. J. G. Versleijen, "An improved de-embedding technique for on-wafer high-frequency characterization," in *Proc. IEEE Bipolar Circuits and Techn. Meeting*, Minneapolis, MN, Sept. 1991, pp. 188-191.