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60 GHz amplifier employing slow-wave transmission lines in 65-nm CMOS

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Abstract A three-stage V-band amplifier implemented in 65-nm baseline CMOS technology is presented in this paper. Slow-wave coplanar waveguides are used for matching and interconnects to study the benefits of using this line type in amplifier design. Measured power gain, noise figure and 1 dB output compression point at 60 GHz are 13 dB, 6.3 dB and +4 dBm, respectively. The amplifier has 19.6 GHz of 3 dB bandwidth, thus covering entirely the unlicensed band around 60 GHz. The performance is achieved with a 1.2 V supply and 45 mA DC current consumption.

Keywords CMOS millimeter-wave integrated circuits · MMIC amplifiers · V-band · Slow-wave transmission lines

1 Introduction

The design of integrated circuits operating at millimeter wave frequencies (30-300 GHz) has gathered growing interest during the last few years. One reason for this is the rapidly scaling CMOS technology which has proved to be capable of operating at mm-wave frequencies from the 130 nm technology node [1]. The license free band around 60 GHz is especially interesting since it provides several gigahertz of world-wide bandwidth for implementing high-speed radio links, such as WLAN or wireless HDMI. These applications are commercially interesting only if the unit cost of components is kept low. Silicon CMOS process allows high level of integration and thus low cost of integrated components when produced in large volumes. While scaled CMOS technology offers performance improvements, such as higher maximum frequency of oscillation (f_{max}) of the active devices, it also adds several challenges to the design of active and passive circuit elements; thinner oxide layers increase leakage currents and decrease break-down voltages. Achieving high output power in scaled CMOS technology is more difficult because of lower allowable voltage swings and lower supply voltages. In addition, the strict metal density requirements and the close proximity of the silicon substrate add challenges in designing and modeling of the passives.

This paper presents a V-band amplifier implemented in a baseline, six metal layer 65-nm CMOS process. The matching circuitry and interconnects are implemented with slow-wave coplanar waveguides (SW-CPW) to study the feasibility of using this type of a transmission line in amplifier design. A floating shield of the SW-CPW line reduces substrate losses compared to the traditional CPW-structure [2]. The paper is organized as follows: Chapter 2 includes the design of transmission lines and capacitors in silicon, Chapter 3 explains the amplifier design and Chapter 4 shows the measurement results of the amplifier.

2 Passives

2.1 Transmission lines

The small inductance values required to match transistors at mm-wave frequencies can be implemented with transmission lines (TLs) and with spiral inductors. Even though spiral inductors provide higher inductance values for certain silicon area, they are more challenging to model

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accurately. Precise, easily scalable in length, inductance values can be implemented with TLs that can be characterized by four parameters: Characteristic impedance Z_0, relative effective permittivity $\varepsilon_{r,eff}$, attenuation constant α, and loss tangent $\tan(\delta)$. These parameters can be used to characterize the TL in ADS circuit simulator using the TLINP physical TL-model.

The traditional CPW-line, implemented in a modern CMOS process, suffers from shunt losses resulting from the close proximity of the conducting silicon substrate. To reduce this loss mechanism, a floating shield constructed of tightly spaced narrow metal strips can be implemented using the lowest metal layers. The wave velocity is reduced in this topology because $\varepsilon_{r,eff}$ is increased, thus the name *slow-wave coplanar waveguide* [2]. The electrical length of the line is also increased which can reduce the length of the transmission line stubs, for example. A simplified cross-section of the SW-CPW line is shown in Fig. 1, which shows how the ground planes are extended from metal six to metal three in order to fulfill the metal density requirements of a nanoscale CMOS process [3].

The impedance of the line is determined by the gap width *D* and the signal conductor width *S*. The ground planes should be kept at the same potential in order to suppress the unwanted slotline mode associated with discontinuities in the CPW-line. This is accomplished by using metal layers 3-5 since the lowest metals are already used for the floating shield. These underpasses are kept narrow to minimize their effect on the propagating electromagnetic wave, however, they can also be used to increase local metal density in, e.g.,

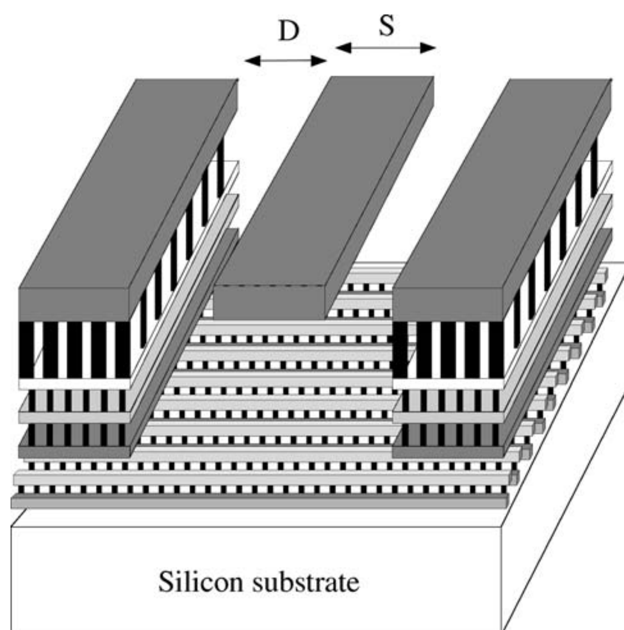

Fig. 1 Simplified cross-section of the SW-CPW line with the floating ground shield implemented with tightly spaced metal strips

transmission line T-junctions. A wide signal line width of 12 μm is chosen to reduce conduction losses, while the signal to ground spacing is maximized in order to increase the line inductance. The shielding allows the use of a wide gap width of 9 μm since the substrate losses are minimal. In a traditional CPW-line this will increase the substrate losses significantly. With this construction, the SW-CPW line has a characteristic impedance of 35 Ω and dielectric permittivity of 9 at 60 GHz.

To evaluate the performance of the slow-wave shielding two CPW test structures, with dimensions given above, were implemented and measured. The only difference between these TLs is the slow-wave metal grid, therefore the effect of the shielding can be identified. Figure 2 shows the transmission line parameters that are extracted from test structure measurements using the method presented in [4]. Although direct comparison of the two TL topologies is not straightforward since the impedance of the SW-CPW line differs from the impedance of the conventional CPW line ($\sim$45 Ω), some conclusion may be drawn on the performance.

The reduction in the line conductance indicates that the slow-wave shielding reduces shunt losses of the line. The line inductance is not changed, meaning that the return current path is not altered. The capacitive quality factor (Q_C) is increased since the line capacitance increases and line conductance decreases, but the inductive quality factor (Q_L) of the SW-CPW line is not improved. This means that the use of the SW-CPW line for matching active devices may not be beneficial. The positive effect of the SW-CPW line is smaller attenuation, reduced area as in [10], and more accurate modeling as the substrate is shielded from the propagating wave. The shielding reduces the line attenuation from 3 dB/mm to 1 dB/mm at 60 GHz. The drawback of the slow-wave shielding is the increased memory and time requirements of the electromagnetic simulations.

Substrate shielding can also be implemented by using the microstrip topology. Top metal layer is used for the signal line and the ground plane is located in the lower metal layers. To ensure a low-impedance ground return current path, two or several metal layers can be connected together. The ground plane is an effective substrate shield, but it is located very close to the signal line. Therefore a narrower signal line should be used to obtain same impedance values as with the CPW-topologies, which will increase conduction losses. The metal density requirements can be fulfilled by adding coplanar ground planes that are adjacent to the signal line. If the distance from the signal line to coplanar ground planes is much higher than the distance from the top metal layer to the microstrip ground plane, the main mode of propagation should be the microstrip mode. A microstrip line test structure with coplanar ground planes was also fabricated and characterized. The side-ground planes are located 9 μm away from

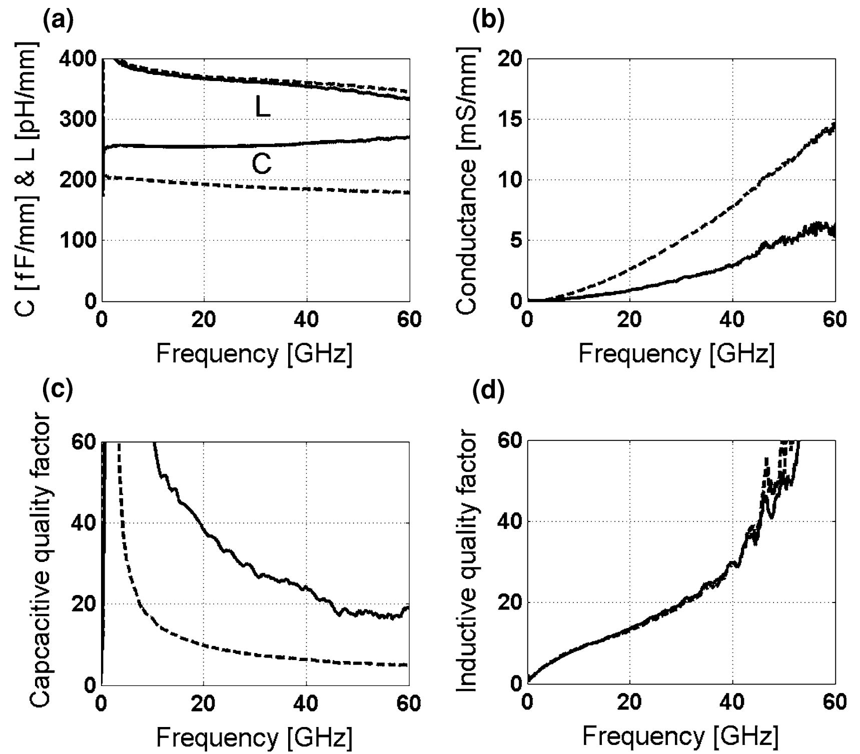

Fig. 2 Measurement results of a traditional CPW line (- -) and the SW-CPW line (—): **a** Line inductance [pH/mm] and capacitance [fF/mm], **b** Line conductance [mS/mm], **c** Capacitive quality factor and **d** Inductive quality factor

the 12 μm wide signal conductor and metal 1 and metal 2 layers are used for the actual microstrip ground plane. The performance is compared to the slow-wave shielded CPW-line in Fig. 3.

The measurement results indicate that the substrate shielding of the microstrip topology is as effective as with the SW-CPW line (same line conductance). The line inductance is, however, degraded since the return current path of the microstrip line is much closer to the signal line (typically less than 3 μm in baseline 65 nm CMOS).

A large inductance per unit length is desired when TLs are used to match transistors, i.e., when they store mostly

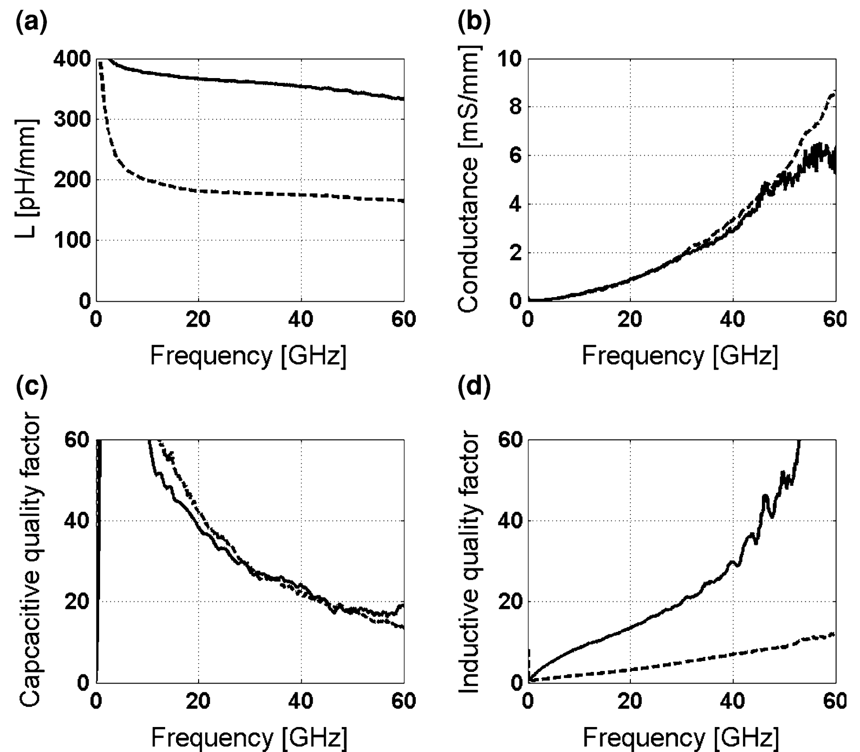

Fig. 3 Measurement results of a SW-CPW line (—) and the microstrip line (- -): **a** Line inductance [pH/mm], **b** Line conductance [mS/mm], **c** Capacitive quality factor and **d** Inductive quality factor

magnetic energy. For this reason, the inductive quality factor Q_L is more suitable for comparing TLs used in amplifier design than the resonator quality factor Q_{res}, or the capacitive quality factor Q_C [1]. These Q-values are given by:

$$Q_L = \omega_0 L/R \quad (1)$$

$$Q_C = \omega_0 C/G \quad (2)$$

$$1/Q_{res} \approx 1/Q_C + 1/Q_L \approx 2\alpha/\beta \quad (3)$$

where L, C, G and R are the inductance, capacitance, conductance and resistance per unit length, β is the phase constant and α is the attenuation constant, respectively. The SW-CPW combines the high line inductance of the CPW-topology with the same substrate shielding performance as the microstrip line. Therefore a SW-CPW line having the same signal conductor width as the microstrip line is more suitable for implementing matching networks.

2.2 Capacitors

Standard finger capacitors, shown in Fig. 4, were used in the amplifier design. Figure 4(a) shows a top-view of a DC-decoupling capacitor in CPW-environment and Fig. 4(b) shows how the RF short-circuit of the parallel matching stubs is implemented.

The length of the fingers must be kept short to maintain a high self-resonance frequency. The ground planes are slotted to fulfill metal density requirements of the process and they are connected together by narrow underpasses at the transmission line discontinuities. The slow-wave shield is not extended under the capacitor because the test structure, from which the model was extracted, did not utilize slow-wave structure. Model extraction was performed by subtracting the interconnects and the RF-pads from the measured capacitor test structure. The capacitance value of the DC-decoupling and the RF-short circuiting capacitor is around 450 fF.

3 Amplifier design

3.1 Topology

The two most commonly used amplifier topologies at mm-wave frequencies are the common-source (e.g. [5] and [6]) and the cascode topology (e.g. [7]). While the cascode topology provides good gain, better reverse isolation and stability, it has higher noise figure (NF) which is a result of the common-gate transistor [8]. The common-source topology (CS), on the other hand, suffers from poor reverse isolation but it has higher linearity that results from larger available voltage swing at the drain terminal. Achieving high output power with low supply voltages is therefore easier with the CS-topology.

Regardless of the chosen topology, the performance of the active device depends greatly on how the layout is drawn, and especially the effect of gate-, drain-, and source contact parasitics become more pronounced at mm-wave frequencies. In this work, the amplifier design is based on a limited set of common source test structures that were available for measurements before the first design cycle. Based on these measurements, a W/L = 90 µm/0.07 µm-sized device was chosen to be used in the amplifier design. The total gate width of 90 µm is divided to several narrow fingers in order to minimize the gate resistance, and thus maximize f_{max} (Fig. 5). The maximum stable gain (*MSG*) of the transistor is about 9 dB at 60 GHz. In practice, however, the losses of the passives and matching networks lower the achievable gain from one amplifier stage and thus three CS-stages needs to be cascaded to provide >12 dB power gain.

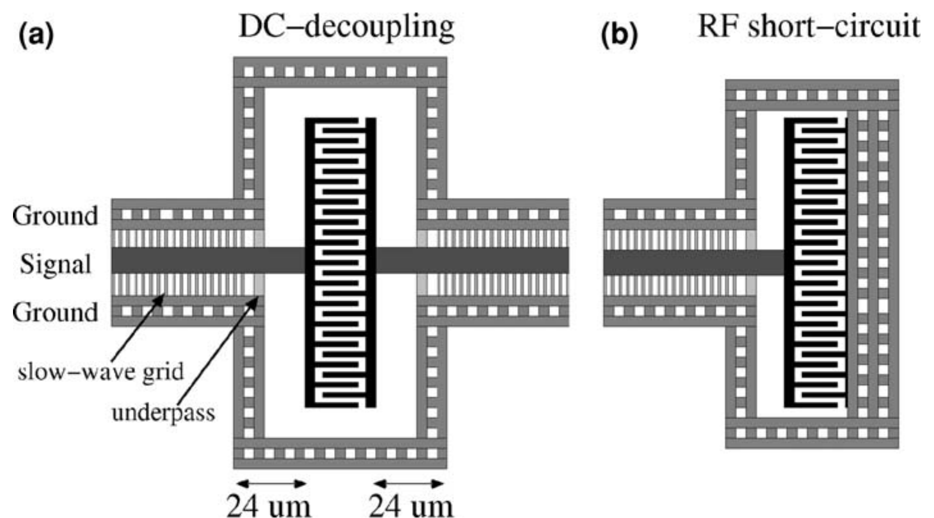

Fig. 4 Finger capacitor that was used in amplifier design: **a** DC-decoupling and **b** RF short-circuit

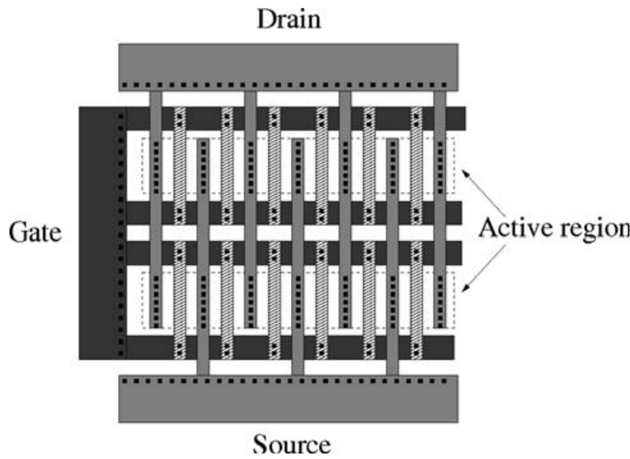

Fig. 5 Principle transistor layout used at millimeter-wave frequencies. Multiple fingers with double contacted gates are used to reduce gate resistance

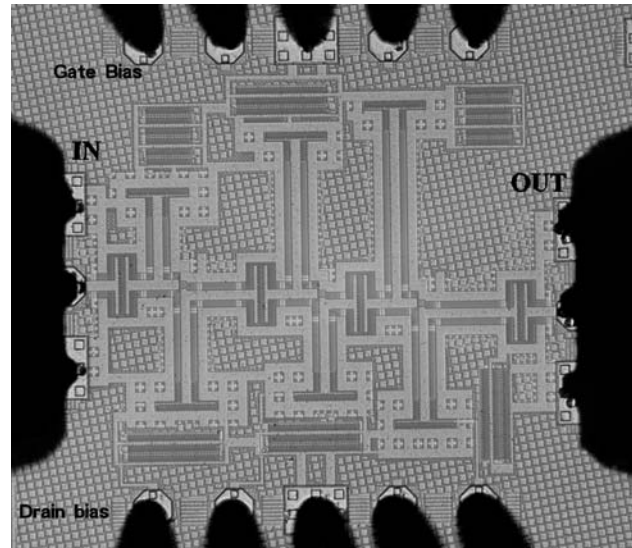

Fig. 7 Chip photograph with RF- and DC-probes. Size is 680 μm × 635 μm including pads

3.2 Matching

The schematic of the amplifier is presented in Fig. 6, which shows how the matching is performed using series- and short-circuited transmission line stubs.

Chip micrograph of the amplifier is shown in Fig. 7. The size of the chip is 680 μm × 635 μm, or 0.43 mm^2, including pads. Gate and drain terminals are biased through the pads located on top and below the amplifier core. The RF-short circuit at the end of the shunt matching stub is implemented using standard finger capacitors. This is a low impedance point at the design frequency and is therefore suitable for bias insertion. Low-frequency stability is ensured by resistor–capacitor networks at the end of the bias feed lines. Input and output are matched to 50 Ω for direct on-wafer probing and the RF-pads are taken into account in simulations as lumped capacitances.

Because the transistor is conditionally stable at 60 GHz, the input and output reflection coefficients of each stage have to be carefully chosen to avoid instability. These reflection coefficients can be chosen using the Smith's chart with help of stability circles that indicate the unstable region. The input match is therefore a compromise between gain, stability and noise figure as the lowest noise figure is not necessarily achieved with same impedance as the highest gain. Figure 8 shows how the input matching is performed on the Smith's chart taking into account the tradeoffs. Starting from the 50 Ω input, the pad- and the DC-blocking-capacitor move the impedance to point *p1* and *p2*. The matching is finalized with series and shunt transmission line stubs through points *p3* to *p4*. Optimum noise figure point *rho_opt* is not targeted as this would degrade the input return loss and reduce the gain and thus increase the noise contribution of the following amplifier stages.

The design of the output matching network is performed using the power gain circles together with the output stability circle to determine optimum matching point, as shown in Fig. 9. In addition, a load-pull simulation can be

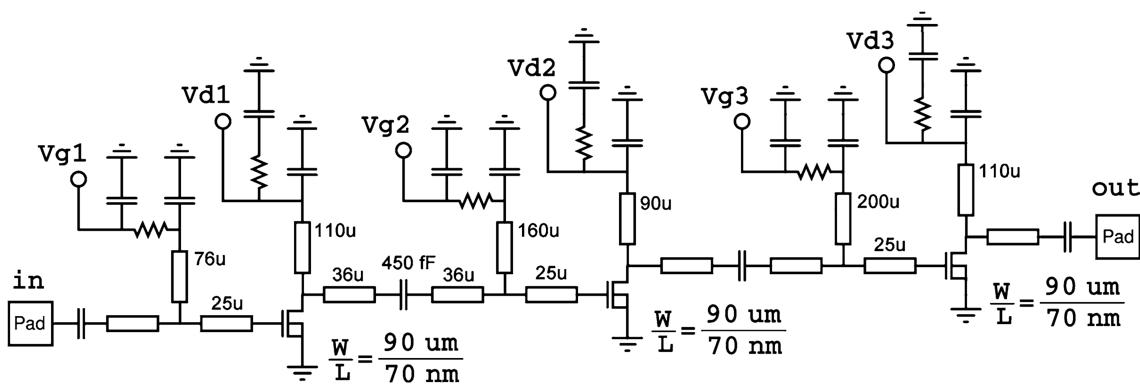

Fig. 6 Simplified schematic of the 60 GHz slow-wave amplifier

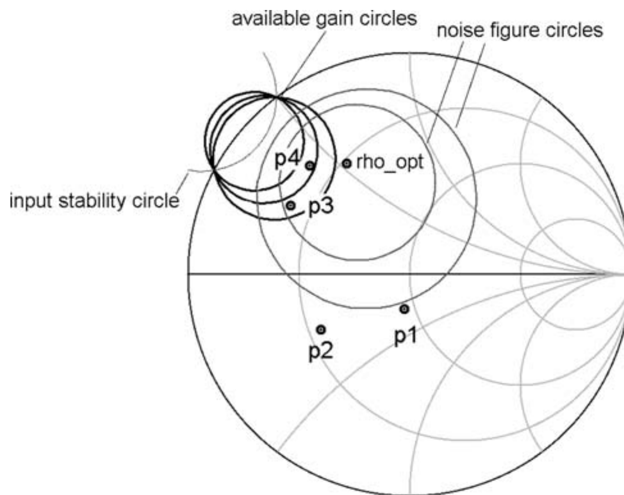

Fig. 8 Input matching at 60 GHz using circles of constant available gain and noise figure

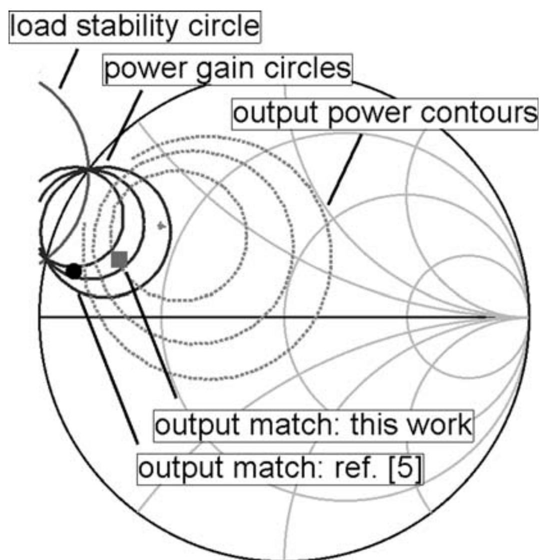

Fig. 9 Output matching at 60 GHz with power gain and stability circles. Load-pull contours are simulated after the measurements with foundry large signal model

performed to find the best compromise between gain and output power. The load-pull contours, shown in Fig. 9, are simulated with the foundry large-signal model after the measurements. This model predicts accurately the effect of the output parasitics and thus the output power, as can be seen in the next Chapter. The output matching point of the amplifier is shown on the chart together with the output matching point of the amplifier presented in [5]. The referenced amplifier is also a three stage common source amplifier that is designed with the same CMOS-technology, transistor size and supply voltage. The load-pull simulations explain the 1 dB higher saturated output power of the amplifier presented in this work when compared to amplifier in [5].

4 Measurement results

S-parameters were measured on-wafer and the results are compared to the simulations in Fig. 10. An excellent agreement to the simulations is observed. Each stage has been biased near the optimum noise figure current density. The ripple in the simulated S-parameters is a result of the measurement based S-parameter models. Measured gain is better than 11 dB from 51 GHz to 67 GHz and 13 dB at 60 GHz. A very wide 3 dB bandwidth of 19.6 GHz is achieved with TL-based matching. The measured S_{22} differs from the original simulation as shown in Fig. 10: Deviation results from the third stage drain terminal matching stub, which was accidentally drawn 40 μm longer than intended. Re-simulation of S_{22} was performed only by adjusting the stub length and it is in good agreement with the measured output return loss. The large signal model, which was used for load-pull simulation, predicts the input and output return losses accurately as can be seen in Fig. 11. This post-measurement simulation is performed to validate the accuracy of the load-pull simulation.

The noise figure was obtained with an automated V-band NF measurement setup described in [9]. The measured noise figure is compared to simulation in Fig. 12, which also shows the measured small signal gain at V-band. The simulation is based on the same noise parameters as in [3]. The measured noise figure is 6.3 dB at 60 GHz, while simulations indicated a noise figure of 7.1 dB. A lower noise figure could have been realized by

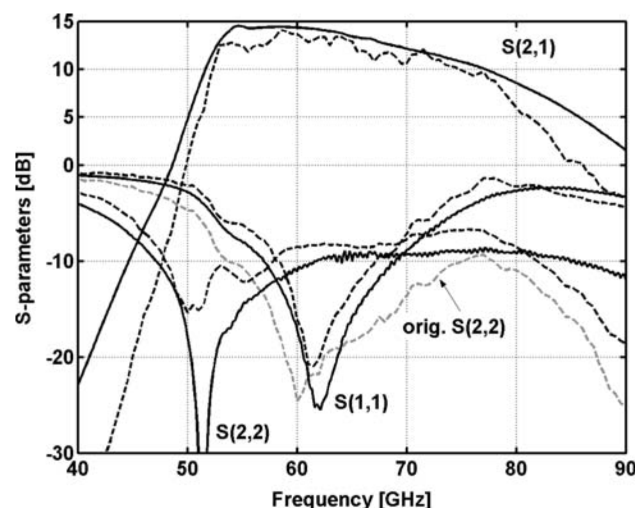

Fig. 10 Measured (*solid lines*) and simulated S-parameters (*dashed lines*). Original S(2,2) is indicated with *light grey line*

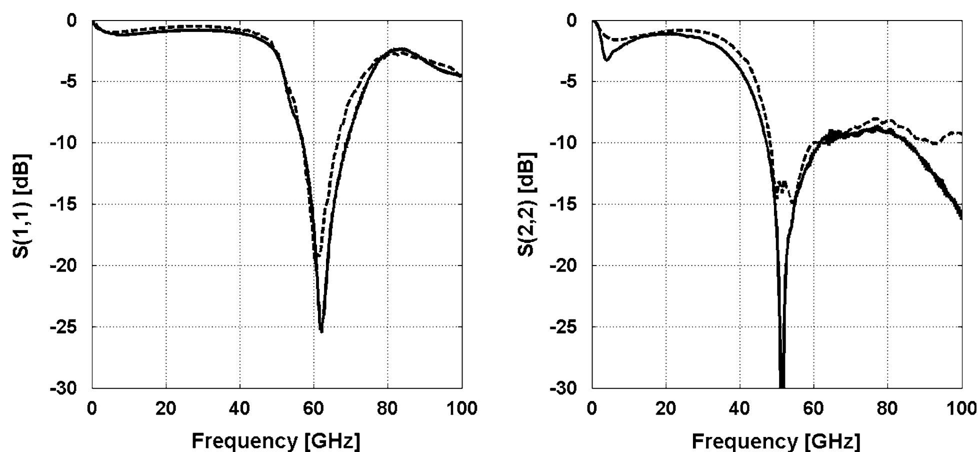

Fig. 11 Measured (*solid lines*) and simulated (*dashed lines*) S(1,1) and S(2,2). Simulation performed with large-signal transistor model and corrected output stub length

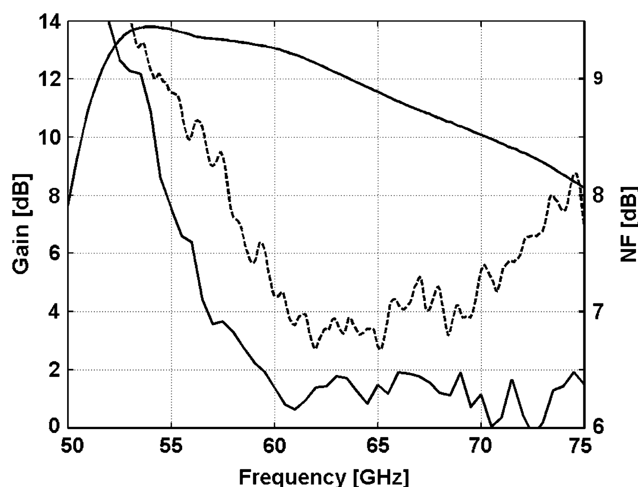

Fig. 12 Measured gain and noise figure (—) and simulated (- -) noise figure

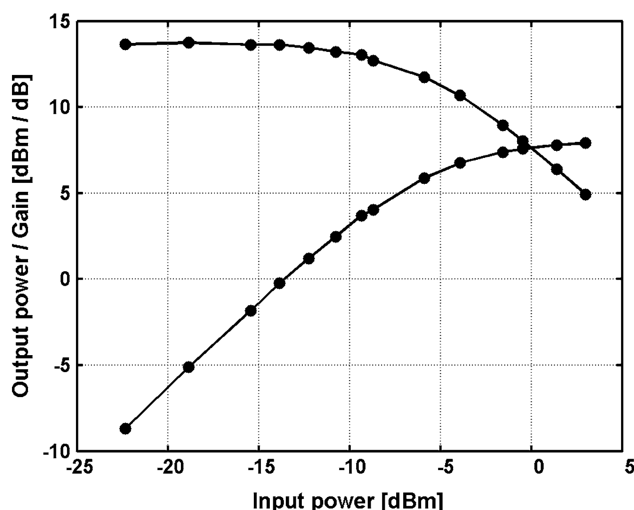

Fig. 13 Measured AM/AM characteristics of the amplifier (V_{DD} = 1.2 V, $I_{stage_1} = I_{stage_2}$ = 15 mA and I_{stage_3} = 20 mA)

degrading input return loss by designing the input reflection coefficient closer to ρ_{opt}.

Compression characteristics were measured at 60 GHz and the results are shown in Fig. 13. The 1 dB output compression point is +4 dBm and saturated output power is +7.9 dBm. For higher output power, the last stage was biased with a higher current density of 0.22 mA/μm, giving maximum PAE of 8%.

The measured performance of the SW-CPW amplifier compares well to other CMOS amplifiers operating near 60 GHz, as can be seen in Table 1. It is of special interest to compare the SW-CPW amplifier to the amplifier in reference [5], since it is a three stage CS amplifier implemented with conventional CPW TLs. The small signal performance is similar in both amplifiers, but the area has reduced from 0.6 mm^2 to 0.43 mm^2 partly because new models for the TLs and finger capacitors were used. The noise figure is actually lower in the referenced amplifier, resulting from different input match conditions of the SW-CPW amplifier.

5 Summary and conclusions

Slow-wave CPW TLs were used for matching and interconnects to study feasibility of using this line type in amplifier design. In general, substrate shielding with slow-wave metal grid is beneficial since it decreases substrate losses and increases the electrical length of the line, therefore matching stubs can become shorter as in [10].

Lower substrate losses implies a larger resonator quality factor (Eq. 3), however, when used to match capacitive loads, e.g. transistors, the ability to store magnetic energy is of greater interest [1]. A CPW, slow-wave CPW and a microsrip transmission line test structure were also implemented and measured. The measurement results indicate

Table 1 Previously published 60 GHz CMOS amplifiers

Reference	[5]	[6]	[7]	This work
Technology	65 nm	90 nm	90 nm	65 nm
Frequency [GHz]	60	58	64	60
Topology	3-stage CS	3-stage CS	2-stage cascode	3-stage CS
Supply [V]	1.2	1.3	1.65	1.2
BW [GHz]	NA	6	8	19.6
Gain [dB]	11.5	15	15.5	13
P_{DC} [mW]	72	4	86	54
NF [dB]	5.6	4.4	6.5	6.3
P_{1dB} [dBm]	1.5	−4	3.8	4 ($I_{tot} = 50$ mA)
Area [mm^2]	0.61	0.14	0.52	0.43

that the line inductance is not affected by the slow-wave shield, which was expected since the two CPW transmission lines have equal signal to ground spacing and signal line width. Q_L of the SW-CPW line is not improved, which means that the use of the SW-CPW line for matching active devices may not be beneficial. The microstrip line, with same signal line width, also offers substrate shielding as the slow-wave structure, but it has lower inductive quality factor.

The measurement results of the 60 GHz SW-CPW amplifier shows 13 dB of gain and 6.3 dB noise figure. The measured 1 dB output compression point is +4 dBm with saturated output power of +7.9 dBm.

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