Publication P4

Dan Sandström, Mikko Varonen, Mikko Kärkkäinen, and Kari A. I. Halonen. 2009. W-band CMOS amplifiers achieving +10 dBm saturated output power and 7.5 dB NF. IEEE Journal of Solid-State Circuits, volume 44, number 12, pages 3403-3409.

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W-Band CMOS Amplifiers Achieving +10 dBm Saturated Output Power and 7.5 dB NF

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***Abstract*—We present two W-band amplifiers, one implemented using conventional coplanar waveguides and unshielded passives and the other using slow-wave shielded waveguides and passives, realized in a 65-nm baseline CMOS technology. The measured results suggest that the slow-wave shielding of the passives is useful in achieving high performance and high frequency of operation. Our custom layout slotted plate capacitor employing slow-wave shield has low parasitic series resistance. Furthermore, as the substrate losses are minimal the modeling becomes more accurate. The measured slow-wave coplanar waveguide based amplifier achieves +10 dBm output power at 100 GHz with a 1.2 V supply and 70 mA total DC-current consumption. The noise figure and gain at 100 GHz are 7.5 dB and 13 dB, respectively. The chip size of the implemented slow-wave amplifier is 0.33 mm^2.**

***Index Terms*—CMOS millimeter-wave integrated circuits, MMIC amplifiers, slow-wave transmission lines, W-band.**

I. Introduction

THE scaling of CMOS technology has led to development of amplifiers up to 100 GHz and even beyond [1]. As the CMOS technology enables the integration of many functions on silicon and being suitable for mass production, the cost effective utilization of millimeter-wave frequencies becomes possible. This development has raised the interest of both academic institutions and the industry. The most promising millimeter-wave consumer applications are expected to utilize the unlicensed band around 60 GHz since it offers up to 7 GHz of bandwidth that is suitable for high-speed, short-range communication systems, such as wireless local area networks (WLAN) and wireless high definition multimedia interfaces (W-HDMI). Other applications include point-to-point links at 60 GHz and at E-band (71–76, 81–86 GHz) as well as collision avoidance car radars at 77 GHz. In addition, there are imaging and scanner applications that utilize the millimeter-wave frequency range.

Despite the possibilities, the millimeter-wave potential of the deep submicron CMOS technology is easily lost in the poor performance of the passive components around the transistors. The close proximity of the conductive silicon substrate results in substrate losses that are difficult to model accurately.

We demonstrate that the 65-nm baseline, 6 metal layer, CMOS technology is suitable for designing 100-GHz circuits having a competitive performance when compared to other published CMOS designs [2]–[5]. We present two amplifiers for W-band operation (75–110 GHz) and discuss the benefits of using slow-wave shielded passives for minimizing substrate losses. Moreover, the modeling of passive components becomes more accurate, as the complicated substrate effects are negligible. The paper is organized as follows. Section II includes the design of transmission lines and capacitors in silicon, Section III explains the amplifier design and Section IV shows the measurement results of the amplifiers.

II. Passives in CMOS

A. Transmission Lines

Distributed effects must be considered in the design of the passives when the wavelength of the operation frequency becomes comparable with the dimensions of the on-chip structures. Therefore, at millimeter-wave frequencies impedance matching is needed for maximum power transfer. In order to achieve high gain and output power, the parasitic capacitances and the intrinsic capacitances of the MOSFETs must be resonated by adding inductive elements to the matching networks. The utilization of millimeter-wave frequencies has a positive effect on the area required by these components; typically inductance values less than 100 pH are needed for matching networks of the transistors. These small inductance values can be implemented with transmission lines (TLs), spiral inductors or transmission line transformers. Even though higher inductance values can be implemented in compact size using spiral inductors, they might be more challenging to model accurately. Scalable inductance values can easily be implemented with TLs, thus allowing a wide range of inductance values to be realized by adjusting the length of the line. In the simulations a simple model can be used that accounts for the characteristic impedance Z_0, relative effective permittivity $\varepsilon_{r,\mathrm{eff}}$, attenuation constant A, and the loss tangent $\tan(\delta)$ [6]. These parameters can be used in the TLINP physical transmission line model in ADS circuit simulator.

Coplanar waveguide (CPW) topology was chosen to be used in amplifier design. Fig. 1 illustrates how the CPW-line is implemented in a multi-layer CMOS-technology. The ground planes consist of all metal layers that are connected together by vias. This structure provides a well defined ground return current path and also fulfills the metal density requirements. Therefore, there is no need for dummy metal filling in the vicinity of the center conductor. In the CPW-topology, a wide signal line width, W, can be used to lower conduction losses and thus the impedance of the line (and the line inductance) can be set by adjusting the distance D between the signal line and the coplanar ground

Manuscript received April 21, 2009; revised August 04, 2009. Current version published December 11, 2009. This paper was approved by Guest Editor Nikolaus Klemmer. This work was supported by the Finnish Funding Agency for Technology and Innovation (Tekes) under the Nastec and Brawe project, and also by the Academy of Finland under the UNCMOS project.

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Digital Object Identifier 10.1109/JSSC.2009.2032274

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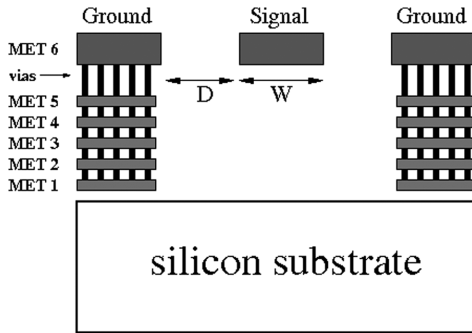

Fig. 1. CPW-line implemented in 6-metal layer CMOS technology. All metal layers are used for the coplanar ground planes to fulfill metal density requirements. The properties of the transmission line are set by choosing the signal line width W and the signal to ground spacing D. Figure is not to scale.

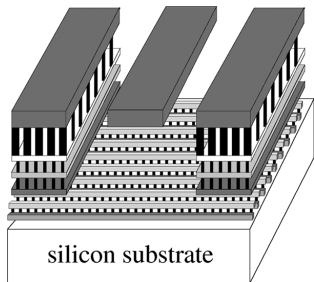

Fig. 2. Slow-wave coplanar waveguide in CMOS. The floating shield consists of narrow metal strips that are perpendicular to the signal line. Figure is not to scale.

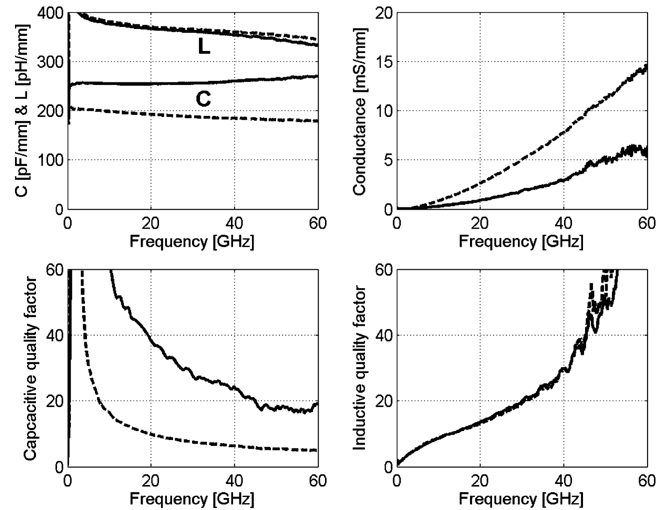

Fig. 3. Measurement results of the transmission line pair 1 ($W = 12$ μm, $D = 9$ μm), consisting of the conventional CPW-line (dashed lines) and the slow-wave shielded CPW-line (solid lines).

planes. However, increasing D increases shunt losses as the electromagnetic field can penetrate into the silicon substrate.

To reduce this loss mechanism, substrate shielding can be considered. One way to implement the shield, without affecting the ground return current path, is a floating shield constructed of tightly spaced narrow metal strips at the lowest metal layers [7]. This topology is called the *slow-wave coplanar waveguide* (SW-CPW), since the wave velocity decreases as a result of increased effective dielectric permittivity $\varepsilon_{\mathrm{r,eff}}$. Thus, the phase change per unit length increases, which means that the slow-wave shielded transmission line is electrically longer. Typically, this leads to smaller area of the matching elements or other transmission line based structures. A simplified cross section of the SW-CPW line is shown in Fig. 2, which illustrates how the floating shield strips are perpendicular to the signal line to minimize induced current flow in them [8], [9].

The ground planes of the CPW-lines should be kept at the same potential in order to suppress unwanted modes that may be produced at the discontinuities in the CPW-line. In the SW-CPW line, this is accomplished by connecting the ground planes together using metal layers 3–5 since the lowest metals are already used for the floating shield. These underpasses are kept narrow to minimize their effect on the propagating electromagnetic wave. In addition, they can also be used to increase local metal density in, e.g., transmission line T-junctions.

In order to compare the performance of the two line types described above, two pairs of transmission line test structures were implemented and measured on wafer. The first pair consists of a conventional CPW-line and a slow-wave shielded version of this same line. Both lines have a 12 μm wide center conductor and 9 μm signal-to-ground spacing. The second pair is otherwise identical to the first pair, but the signal-to-ground spacing has been reduced to 2 μm. The transmission line parameters were calculated from the measured S-parameters using the method described in [10]. The inductive and capacitive quality factors (Q_{L} and Q_C) are then calculated from the measured $RLGC$-parameters. These parameters are related to the self resonance quality factor Q_{res} according to the following equation [11]:

$$\frac{1}{Q_{res}} \approx \frac{2\alpha}{\beta} \approx \frac{1}{Q_C} + \frac{1}{Q_L} = \frac{G}{\omega_C} + \frac{R}{\omega L} \tag{1}$$

where α is the attenuation constant and β is the phase constant.

Fig. 3 shows the measurement results of the first pair of transmission lines. The shielding increases the line capacitance but does not affect the line inductance. This means that the return current path is not altered and no currents have been induced into the shield strips. As the line capacitance increases, the characteristic impedance reduces from 45 Ω to around 35 Ω. Even though the line impedances are not the same, the comparison is meaningful as the effect of the shielding can be identified. The reduction in line conductance shows how the shielding prevents the electromagnetic wave from penetrating into the substrate. The second pair of transmission lines was also characterized. The smaller signal to ground spacing reduces substrate exposure and thus the benefits of slow-wave shielding become smaller. This can be seen in Fig. 4, which shows the line inductance and conductance together with inductive and capacitive quality factors of the second transmission line pair.

Using a smaller gap width thus reduces the substrate losses, but the drawback is the reduced line inductance which lowers the inductive quality factor. The conventional CPW has an impedance of 30 Ω, while the impedance of the slow-wave shielded line is 25 Ω.

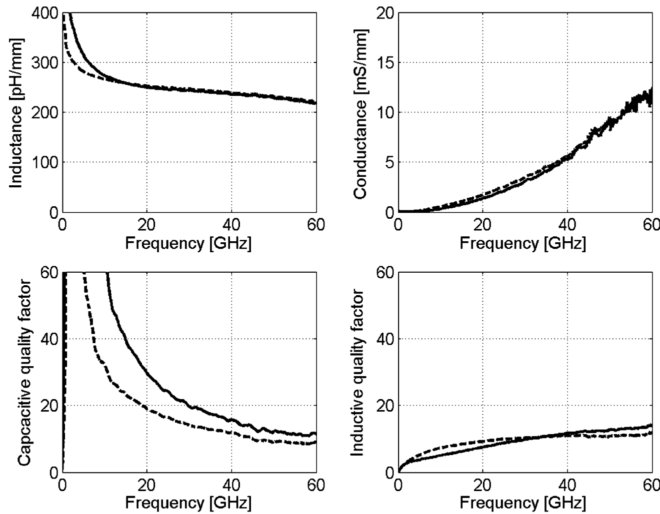

Fig. 4. Measurement results of the transmission line pair 2 ($W = 12\ \mu$m, $D = 2\ \mu$m), consisting of the conventional CPW-line (dashed lines) and the slow-wave shielded CPW-line (solid lines).

The advantages of the SW-CPW are lower attenuation and higher effective dielectric permittivity, which increases the electrical length of the line as in [12]. Because the substrate is shielded, the capacitive quality factor is increased when compared to the conventional CPW having the same W and D. However, in this case, the inductive quality factor remains the same, as the signal to ground spacing is the same in both topologies. In order to have same impedances for the conventional and the slow-wave CPW the signal-to-ground spacing D of the slow-wave CPW can be increased. Based on the measurement results of the transmission lines, it can be concluded that the inductive quality factor will be higher for the slow-wave CPW. As the inductive quality factor of a transmission line is more important figure of merit when designing amplifiers on silicon [11], the use of SW-CPW having the same characteristic impedance as the conventional CPW improves the performance of the matching networks. Furthermore, by extending the slow-wave shield below other passives the frequency dependent substrate effects of the matching networks are almost completely removed. As a result, the substrate losses of these passives become minimal. In addition, at millimeter-wave frequencies the modeling of passive structures becomes more accurate as the complicated substrate effects are negligible. This will be discussed in the next section.

B. Capacitors

The conventional amplifier uses standard finger capacitors for DC decoupling (Fig. 5, left side) and for implementing the RF short circuit for the shunt matching stubs. Since the SW-amplifier utilizes SW-CPWs, standard finger capacitors were replaced by a modified structure, shielded with the floating slow-wave metal grid. Only the lowest metal layer is used for the shield under the capacitor structure to spare metals 2 to 5 for the actual capacitor. The floating shield effectively reduces substrate losses and coupling, therefore the core capacitor model can be obtained from the RC-parasitic extraction tool. A plate capacitor structure was designed in order to reduce parasitic series

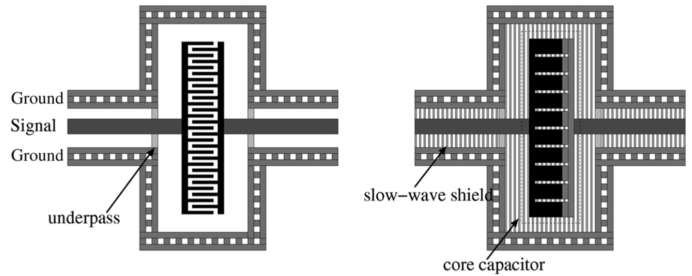

Fig. 5. Simplified presentation of a standard finger capacitor in CPW environment (left) and the modified capacitor structure with slow-wave shield in SW-CPW environment (right).

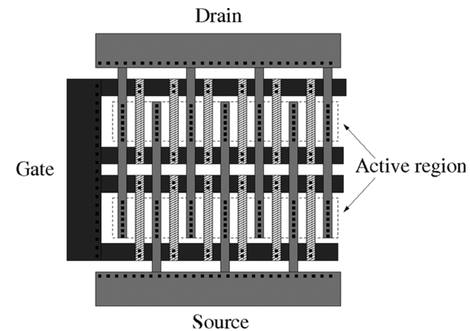

Fig. 6. Simplified layout of a multifinger transistor using double-contacted gates and two parallel devices.

resistance as shown in Fig. 5 (right side), which shows a principle presentation of the modified layout of a DC-decoupling capacitor in SW-CPW environment. The plates of the capacitor must have slots in order to fulfill the metal density requirements. Since metal 1 layer is used for the shield, the capacitance density decreases by approximately 20%. However, at 100 GHz there is no need for large capacitance values and thus the silicon area consumed by the modified capacitor structure is not increased. The parasitic series resistance is estimated to decrease to approximately 1/10 of the original value. Capacitor model used in the simulations consists of the core capacitor, obtained from parasitic extraction tool, and the interconnects which are modeled as transmission lines (as shown in Fig. 5).

III. Amplifier Design

A. Transistor

The transistor sizing is critical at mm-wave frequencies and the performance depends greatly on how the layout is drawn, since the parasitics become more dominant at mm-wave frequencies. The simplified equations for maximum frequency of oscillation $f_{\max}$, which is based on maximum available gain MAG and maximum stable gain MSG, can be used for evaluating the effect of parasitics to the gain performance of a transistor [13], [14]:

$$f_{\max} \approx \frac{f_t}{\sqrt[2]{(R_G + R_S)(g_{ds} + 2\pi f_t C_{gd})}} \tag{2}$$

$$\mathrm{MSG} \approx \sqrt{\left(\frac{g_m}{\omega C_{gd}}\right)^2 + 1} \approx \frac{g_m}{\omega C_{gd}} \tag{3}$$

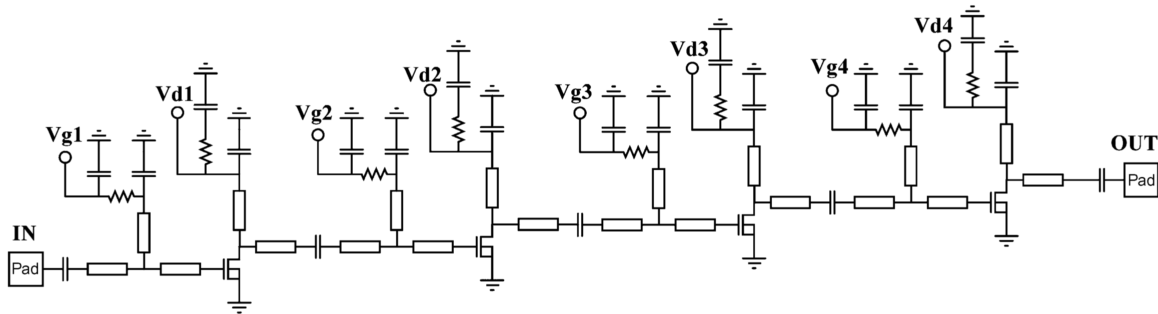

Fig. 7. Schematic of the amplifiers. The RF-pads are part of the matching networks.

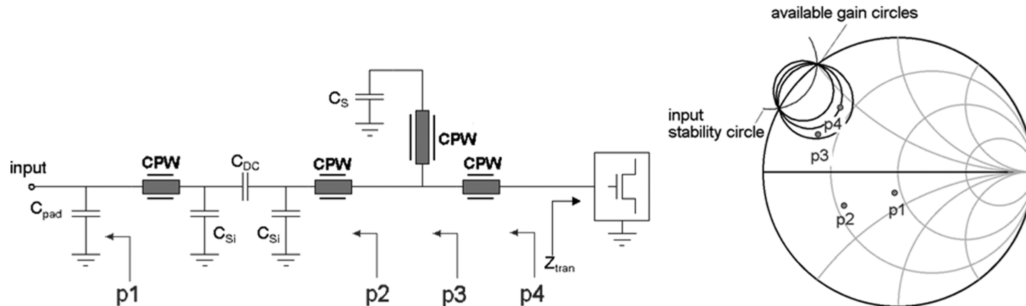

Fig. 8. Input matching of the amplifier. The impedance seen from point $p4$ is the complex conjugate of the input impedance of the transistor $\mathrm{Z_{tran}}$. $C_{\rm pad}$ represents the pad capacitance, $C_{\rm DC}$ is the DC-blocking capacitor and C_S is the capacitor for implementing the RF-short circuit for the parallel matching stub. $C_{\rm Si}$ represents the parasitic shunt capacitances of the DC-blocking capacitor.

where g_m, R_G, R_S, C_{gd}, and g_{ds} are transconductance, gate and source resistances, gate-to-drain capacitance and drain-to-source conductance, respectively. The $f_t = g_m/[2\pi(C_{gs} + C_{gd})]$ is the cut-off frequency, where C_{gs} is the gate-to-source capacitance. The width of the fingers must be short to minimize the gate resistance. Since also the noise figure (NF) is a function of the gate resistance, as shown in Fukui's equation, minimizing this parasitic is of great importance [15]:

$$\mathrm{NF_{min}} = 1 + K\omega C_{gs}\sqrt{\frac{R_G + R_S}{g_m}}. \tag{4}$$

In (4), K is an empirical fitting factor. Fig. 6 shows a way to realize a common source transistor. Several narrow fingers (around 1 μm) are connected in parallel and gates are connected on both sides. The drain and source are fed from opposite sides to minimize C_{gd}, C_{gs} and the drain-to-source capacitance C_{ds}. This will improve both the MSG and $f_{\max}$. Furthermore, as we use the transistor in coplanar waveguide environment, the positioning of the gate, drain and source access lines in this way gives the designer an opportunity to place a matching stub directly at the drain as shown in Fig. 7. This is important, because adding even a short series line at the drain node will easily result in a low impedance point, which complicates the matching. More details are presented in the amplifier design section. For higher current swings, multiple fingers can be used in parallel to obtain high output power with a low supply voltage. However, the gate width cannot be increased arbitrarily as low loss wideband matching may become unfeasible.

A $\mathrm{W/L} = 90/0.07$-sized transistor, constructed of several narrow fingers, was used in the design of both amplifiers. The same transistor size was used in all stages because S-parameter data was available for this transistor size from the previous process run. Since the contact parasitics have a large impact on the performance of the transistor at millimeter-wave frequencies, the S-parameter data is valid only for fixed layouts.

B. Amplifier Design

Both amplifiers are constructed of four cascaded common source (CS) stages, as shown in the schematic in Fig. 7.

Common source topology was adopted because it provides high gain, low noise figure and good output power at W-band. The CS topology suffers from poor reverse isolation that complicates the matching procedure: Changes made to the output matching networks are partly reflected to the input through the gate-drain capacitance. Simultaneous tuning of both matching networks is therefore required for optimum performance. Careful design of the source and load impedances is required since the transistor is potentially unstable below 90 GHz. Stability of the whole amplifier is guaranteed by designing each amplifier stage to be unconditionally stable at all frequencies, i.e., stability factor $K > 1$. The transistors are matched using series transmission lines and RF short-circuited transmission line shunt stubs. All transmission lines have 12 μm wide signal conductors and 9 μm signal-to-ground spacing. The conventional amplifier uses unshielded passives, while the passives of the slow-wave amplifier are shielded with the slow-wave shield. The DC-decoupling capacitors and the pad capacitances are part of the matching networks, therefore no de-embedding of the pad capacitances has been performed after the measurements. The input and output are matched to 50 Ω for direct on-wafer probe measurements. Fig. 8 shows how the input matching of the amplifiers is performed. The 50 Ω source impedance is transformed to the desired impedance using transmission lines, DC-blocking capacitor and the capacitance of the RF-pad.

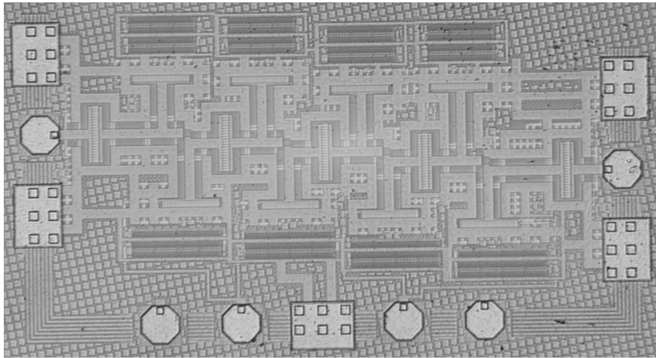

Fig. 9. Chip micrograph of the SW-amplifier. The size is 775 × 420 μm^2, or 0.33 mm^2 including bias and RF-probe pads. The size of the conventional amplifier is 0.42 mm^2.

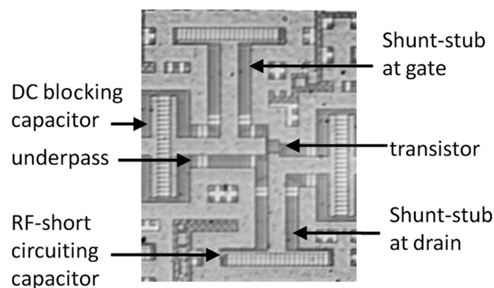

Fig. 10. Micrograph of a part of the transistor matching arrangement.

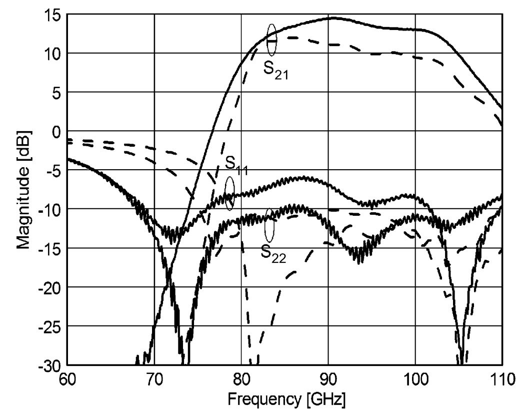

Fig. 11. Measured (solid lines) and simulated (dashed lines) S-parameters of the SW-amplifier.

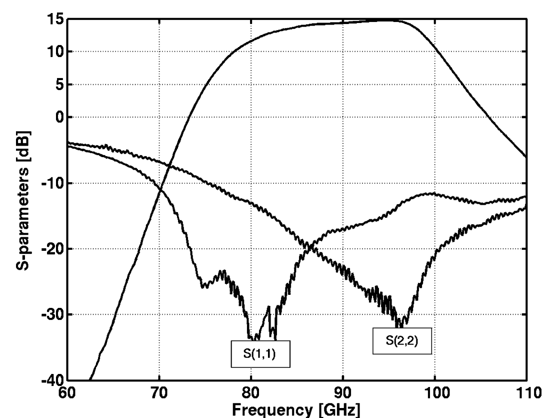

Fig. 12. Measured S-parameters of the conventional amplifier.

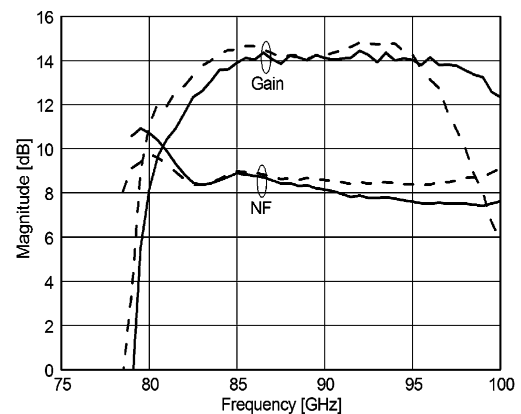

Fig. 13. Measured noise figure and insertion gain of the SW-amplifier (solid lines) and the conventional amplifier (dashed lines).

The bias voltages are applied through the RF short-circuited shunt matching stubs, where resistor capacitor networks are added to ensure low-frequency stability. Each transistor stage is biased close to a current density that gives a high f_{max} [16]. The chip micrograph of the SW-amplifier is shown in Fig. 9 and a more detailed micrograph of a part of the transistor matching arrangement is shown in Fig. 10. The shunt matching stubs can be clearly identified, note how the drain matching stub is placed directly at the drain-terminal as explained in Section III-A.

IV. Measurements

On-wafer measurements were performed for both amplifiers using a 1.2 V supply. Fig. 11 shows the measured and simulated S-parameters of the SW-amplifier biased with 18 mA DC current for all stages. The SW-amplifier has highest gain of 14.8 dB at 90 GHz and 13 dB at 100 GHz. Good correspondence between the simulated and measured results of the SW-amplifier indicate that the custom-layout capacitor has been accurately modeled by RC-parasitic extraction without the need of modeling the effects of the low-resistivity substrate. The 3-dB bandwidth of over 20 GHz was achieved by using transmission lines as matching elements and through careful design.

The measured S-parameters of the conventional amplifier are shown in Fig. 12. The frequency response is similar to the SW-amplifier with the highest gain of 15 dB at 96 GHz.

Fig. 13 shows the noise figure measurement results of the amplifiers. The automated noise measurement setup is described in detail in [17]. The measured NF of both amplifiers is less than 9 dB from 82 to 100 GHz. At 100 GHz, the SW-amplifier achieves the lowest noise figure of only 7.5 dB while the conventional amplifier has the lowest noise figure of 8.4 dB.

Fig. 14 shows the measured large signal characteristics of the amplifiers. The measurement is performed at 94 GHz, since both amplifiers have similar small signal gain at this frequency. DC bias currents of the third and fourth stage are adjusted to 20 mA for higher output current swing, and thus higher output power. The first two stages, on the other hand, are biased with 15 mA DC current as this value was sufficient to drive the last

TABLE I
RECENTLY PUBLISHED W-BAND CMOS AMPLIFIERS COMPARED TO THE SW-AMPLIFIER

Reference	[2]	[3]	[4]	[5]	**This work**
Technology	65nm GP CMOS	90nm RF-CMOS	90nm CMOS	90nm CMOS	**65nm CMOS**
Freq. [GHz]	95	96	94	104	**100**
Topology	3 stage casc.	3 stage casc.	2 stage casc.	3 stage CS	**4 stage CS**
Supply [V]	1.5	2.5	1.8	1.0	**1.2**
Gain [dB]	13	16	4.8	9.3	**13**
3dB BW	NA	22	NA	~1*	**21**
NF [dB]	6-7	NA	NA	NA	**7.5**
OCP [dBm]	NA	+2	NA	NA	**+6**
P_{sat} [dBm]	NA	+4	NA	NA	**+10**
P_{DC} [mW]	35	54	30	22	**86**
Area [mm^2]	NA	0.42	NA	0.36	**0.33**

* Value estimated from S-parameter measurement results.

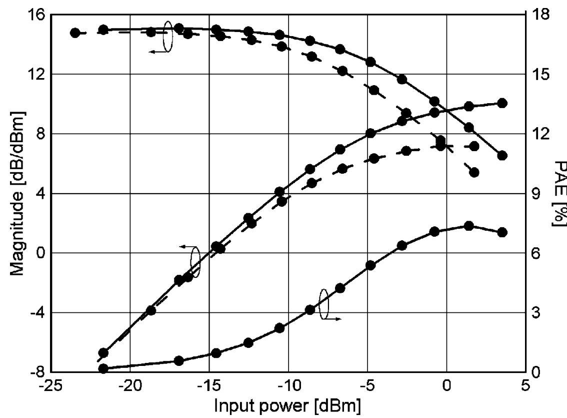

Fig. 14. Measured output power and gain with respect to input power. The power added efficiency is calculated for the SW-amplifier.

stage to saturation. The SW-amplifier achieves +10 dBm of saturated output power ($P_{\rm sat}$) reaching maximum PAE of 7.3%, while the conventional amplifier saturates at +7.2 dBm output power level. The 1-dB output compression points at 94 GHz are +3.7 dBm and +6.2 dBm for the conventional and the SW-amplifier, respectively.

The lower output power of the conventional amplifier can be explained by different output matching conditions and higher losses of the passives. At 100 GHz, the saturated output power and 1-dB output compression point of the SW-amplifier are at +9.7 dBm and +6 dBm power levels, respectively.

The measured gain, NF and output power of the SW-amplifier are comparable or better than previously published CMOS W-band amplifiers, as shown in Table I. The SW-amplifier achieves the highest reported output power of +10 dBm and the lowest reported noise figure of 7.5 dB at 100 GHz in CMOS.

V. CONCLUSION

Two CMOS amplifiers for W-band were implemented in a baseline 65-nm CMOS technology. The coplanar waveguide topology was chosen for interconnects and matching elements since it provides a well-defined ground return current path. To reduce substrate losses of the conventional CPW-line, the other amplifier utilized shielded passives. The shield has been implemented with a slow-wave structure that does not affect the line inductance, when considering lines with the same geometry (same W and D). If a conventional and a SW-CPW having the same characteristic impedances are compared, we conclude that the SW-CPW has higher inductive quality factor than the conventional one, which is important when matching transistors. A custom layout capacitor with a slow-wave shield was also presented and it was used in the design of the slow-wave amplifier. The floating shield effectively reduces substrate losses and coupling, therefore the core-capacitor model was obtained with the RC-parasitic extraction tool. The measured performance suggests that the substrate shielding of the passives is useful in achieving a low noise figure and high frequency of operation. The characterization of CPW, SW-CPW and transistor test structures up to 110 GHz [8] enabled accurate simulations and provided predictable results.

The amplifier with slow-wave shielded passives achieves the highest reported output power of +10 dBm in CMOS at W-band and the lowest reported noise figure of 7.5 dB at 100 GHz.

ACKNOWLEDGMENT

The authors would like to thank Hannu Hakojärvi and Mikko Kantanen for the on-wafer measurements at Millilab, The Millimetre Wave Laboratory of Finland.

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