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## 23.3 A W-Band 65nm CMOS Transmitter Front-End with 8GHz IF Bandwidth and 20dB IR-Ratio

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The nanoscale era of CMOS technology has enabled the integration of mm-Wave circuits and front-ends at W-band [1,2]. The possible applications range from telecommunications (71 to 76 & 81 to 86GHz) and collision avoidance radar for cars at 77GHz to imaging and sensing at 94GHz. Some of the benefits of using CMOS technology are low costs per unit in mass production and the possibility to integrate more functions on the same chip. This paper demonstrate a W-band transmitter front-end chip in 65nm baseline CMOS.

The topology of the integrated W-band transmitter front-end is presented in Fig. 23.3.1. It is suitable for both image-rejecting superheterodyne and direct-conversion transmission. The front-end uses two balanced mixers and quadrature IF signals, or baseband in-phase and quadrature signals, and in-phased balanced LO-drive signals. The image rejection or direct conversion is achieved when the RF signals are summed 90 degrees out of phase. Since the broadband Lange coupler provides both power combining and phasing, quadrature power combining in the RF path instead of LO-quadrature generation was chosen. Furthermore, as the needed LO power is relatively high compared to the RF power after mixing, it is more power efficient to use a Lange coupler in the RF chain where a small transistor can be used for compensating the loss of the coupler. The mixer should provide LO suppression and a wide IF bandwidth. Furthermore, it should achieve a high 1dB output compression point ($OCP_{1dB}$) for reducing the gain requirements of the mm-Wave power amplifier (PA).

The balanced resistive mixer topology, shown in the schematic in Fig. 23.3.2, is thus an attractive alternative since it has high linearity and consumes zero DC current. At RF frequency, the IF line is a quarter-wavelength short-circuited stub, which isolates the IF circuitry from the RF output. The capacitors are short circuits at RF- and LO frequencies and open circuits at IF frequency. Connection point at the drains of the mixing devices is a virtual ground for the LO signal. The quadrature IF signals are generated with off-chip hybrids and applied to the chip by GSGSG dual probes. The connection to the $\lambda/4$ stub is done by grounded coplanar waveguides that provide both substrate shielding and a well defined ground return current path. The on-chip spiral transmission line baluns, fed from a slow-wave coplanar waveguide (SW-CPW) input, are used to perform both the even-to-odd mode transformation, that is required for the balanced mixing operation, and power division for the LO signal [3]. Since the balun is a quarter-wave transformer at odd propagation mode it can be used for impedance matching over wide bandwidth. The impedance matching at the LO port was achieved both by using the balun parameters and by selecting a proper size for the mixing transistors. The balanced LO signal is used to pump the channel resistance of the transistors in the mixers. The mixing operation requires the LO power level to be relatively high, thus a single-stage common-source (CS) LO buffer was added before the baluns to lower the required LO power at the input and to compensate the losses of the baluns. For optimum mixer performance the gates of the mixing transistors are biased near to the threshold voltage at 0.5V

The Lange coupler provides accurate and wideband 90 degree phase shift between the through- and the coupled port. For good image rejection performance also the amplitude balance must be accurate. The 3dB power combining requires tight coupling between the branches of the coupler. As the Lange coupler is implemented in nanoscale CMOS technology, the distance from the top metal to the microstrip ground plane is very small, which means that the fingers must be narrow (around 1µm) and placed close to each other (0.5µm gap). The coupler was designed using even- and odd-mode analysis and simulated in 3D EM software.

The power level after the coupler is around -13dBm. Enough gain is needed to drive the output stage of the amplifier into compression. The gain of a single CS stage is around 3 to 4dB at W-band, thus six CS-stages were used in the PA. Smaller-sized transistors can be used in the first stages to reduce DC power consumption because of the low signal level. Therefore, a transistor with 48x0.9µm total gate width was chosen for the first three stages, while a large transistor of 100x0.9µm gate width was used in the last three stages. The total DC current consumption of the PA is 90mA and the LO buffer draws 10mA, thus the total power consumption of the transmitter front-end is 120mW with a 1.2V supply. Interconnects from the mixers to the coupler, as well as the matching stubs of the amplifiers, are implemented with slow-wave coplanar waveguides (SW-CPW) [4]. This line type provides substrate shielding and increased electrical length, which helps in reducing circuit area [5]. Metal-insulator-metal (MIM) capacitors were used for DC decoupling and for realizing the RF short circuit of the shunt matching stubs. The slow-wave shield of the transmission line was extended underneath the MIM capacitors and RF-, LO- and IF pads. This way the complicated substrate effects can be minimized. Furthermore, the MIM capacitor can be modeled simply by using the foundry model which utilizes a metal shield. In the simulations, the shield node is floating and the access to the MIM is modeled with SW-CPWs.

The transmitter front-end was measured on wafer. The LO power was set to +2dBm in all measurements. Figure 23.3.3 shows the measured conversion gain and IR ratio for upper sideband (USB) and lower sideband (LSB) with 2GHz IF frequency. The transmitter exhibits more than 5dB gain and 15 to 25dB image rejection for RF frequencies from 75 to 95GHz. Figure 23.3.4 shows the saturated output power, the LO power at the output, and the 1dB OCP at fixed 2GHz IF frequency. The output power is higher than +4dBm from 77 to 94GHz and the highest 1dB output compression point is +2.2dBm at 85GHz. At this frequency, the LO power is 20dB lower than the +6.6dBm maximum output power, which indicates a good LO suppression for the mixer. The transmitter front-end was measured with IF frequencies ranging from 1GHz to 8GHz with a fixed 85GHz LO frequency. The measured conversion gain and IR ratio are shown in Fig. 23.3.5. The result shows a wideband IF performance for the front-end. The measurement setup limited the IF bandwidth to 8GHz.

The measured performance of the transmitter front-end and a comparison to a previously published CMOS W-band transmitter are shown in Fig. 23.3.6. The presented design techniques resulted in wideband RF, IF and LO performances with good output power and image rejection. The transmitter silicon area with pads is approximately 1.2mm$^2$ and the chip micrograph is shown in Fig. 23.3.7.

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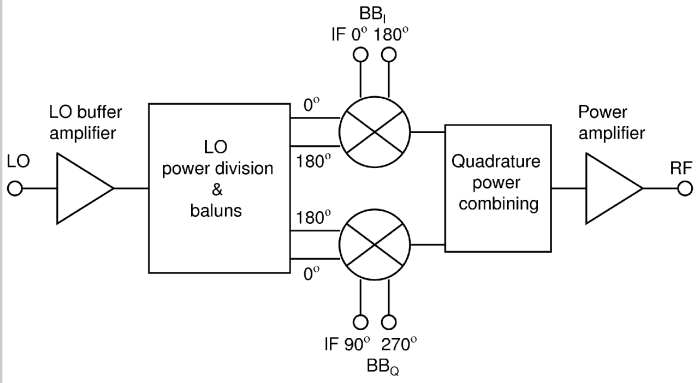


Figure 23.3.1: Block diagram of the transmitter front-end.

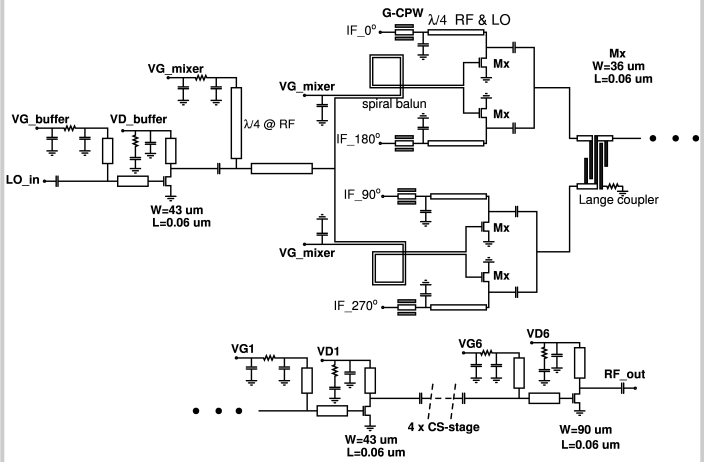


Figure 23.3.2: Schematic of the transmitter front-end. Two of the six CS stages of the PA are shown.

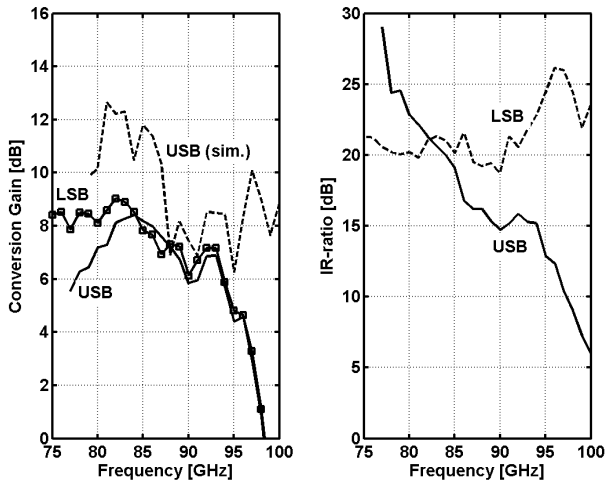


Figure 23.3.3: Measured and simulated conversion gain and measured USB and LSB IR ratio with 2GHz IF frequency.

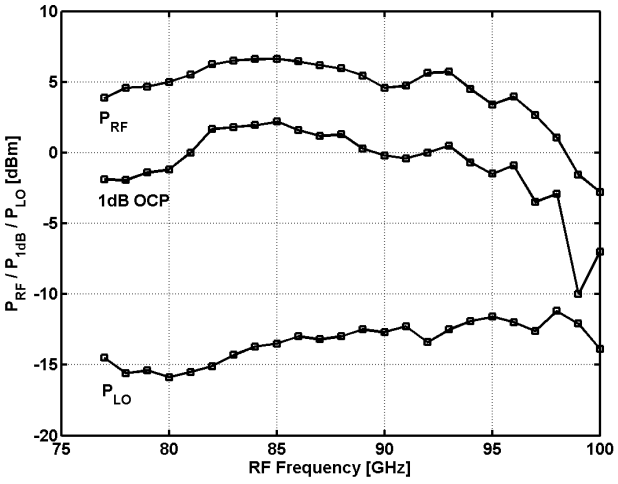


Figure 23.3.4: Measured 1dB OCP, RF and LO power of the front-end with 2GHz IF frequency.

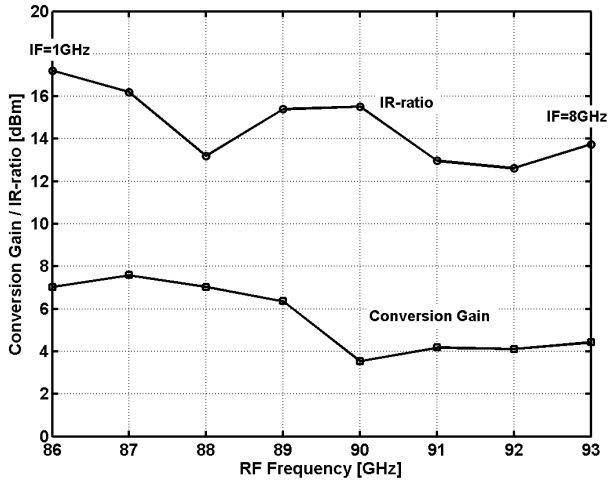


Figure 23.3.5: Measured conversion gain and IR ratio of the front-end with 85GHz LO frequency.

| | $P_{RF}$ max [dBm] | $OCP_{1dB}$ [dBm] | RF-BW [GHz] | IF-BW [GHz] | IR-ratio [dB] | Peak Gain [dB] | $P_{DC}$ [mW] |
|---|---|---|---|---|---|---|---|
| **This Work** | +6.6 | +2.2 | 75-95 | 1-8* | 15-20 | 8.5 | 120 |
| [6] | +3 | NA | 80-94 | NA | NA | 3.8 | 142 |

* Limited by the measurement setup

Figure 23.3.6: Measured performance of the transmitter front-end.

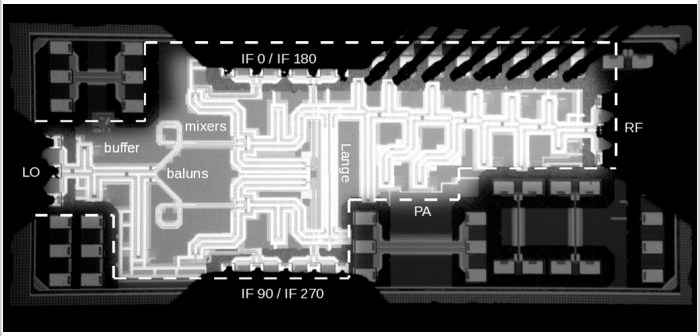


**Figure 23.3.7: Chip micrograph of the transmitter front-end. The core area (highlighted) is 1.2mm² including pads.**


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