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Resistive HEMT Mixers for 60-GHz Broad-Band Telecommunication

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***Abstract*—We report two resistive mixers, i.e., a balanced and a balanced image-rejection (IR) mixer for the 60-GHz frequency range. A compact and wide-band method for the local-oscillator (LO) power division is presented. The 56-GHz LO signal, which propagates in a coplanar-waveguide mode, is divided in between the lines of two spiral baluns. Consequently, a smooth and compact transition from even-to-odd propagation mode and an in-phase power division for two singly balanced unit mixers is achieved. As a result, the developed IR mixer occupies only 1.41mm^2 of chip area. The balanced design achieved 11.5 dB of conversion loss from 57 to 67 GHz with a fixed IF of 5.3 GHz. The corresponding LO suppression was better than 34 dB with 8 dBm of LO power. The IR mixer achieved better than 19 dB of IR ratio and better than 36 dB of LO suppression for an RF frequency from 57 to 66 GHz. The corresponding conversion loss varies from 13 to 16 dB. The measured 1-dB compression point of the IR mixer was at a −13-dBm output power level and the third-order intercept point was at a 4-dBm level.**

***Index Terms*—Baluns, MIMICs, resistive mixers.**

I. Introduction

THE possibilities open to the 60-GHz frequency band are interesting because of the wide bandwidth that has been allocated globally for wireless networks; 5 GHz of spectral space has been assigned for multimedia services around 60 GHz with a global overlap of 3 GHz starting from 59 GHz and extending up to 62 GHz [1], [2].

For millimeter-wave communication systems, low-cost, reliable, and high-performance circuits are required. The mixer is one of the key components in a millimeter-wave transceiver. In a receiver or transmitter, the problem with the image frequency that comes up in the mixing process must be solved. If there is no image rejection (IR) present in the receiver, noise, and possible interference from the image band will degrade the overall performance of the receiver. In the case of the transmitter, the image frequency or, alternatively, the mirror frequency, may double the power at the input of the power amplifier if it is not sufficiently suppressed. If a single-chip transmitter or receiver is to be developed, the filter has to be integrated on-chip. A compact sub-harmonic mixer integrated with an IR filter has been reported in [3]. However, it has a relative narrow passband at 60 GHz. Generally, the filter response determines the available local oscillator (LO) tuning range and prevents the overlapping of the desired RF and image bands. In addition, if the IF is low, the image band is close to the RF band, which makes the filter design more problematic. Therefore, the IR mixer configuration seems to be an appealing topology. Furthermore, by using a balanced design, we can suppress the LO leakage and spurious signals as well as reduce AM LO noise.

The field-effect transistor (FET) resistive mixer was first described in [4] and a balanced version was reported in [5]. Recently, a number of resistive mixers have been reported at V-band [6]–[10]. The advantages of the resistive FET mixer are very low distortion, low $1/f$ noise, stability, no shot noise, and, in practice, no dc power consumption. Additionally, the resistive mixer can operate with relatively low LO power levels [11].

The aim of this paper is to present broad-band monolithic-microwave integrated-circuit (MMIC) mixers that operate without filters. This enables a wide-band LO tuning range. The prototype balanced mixer was reported in [12]; here, we present the design in detail and new broad-band measurement results. The excellent results of the prototype mixer encouraged us to develop a small-size high-performance mixer that provides both high IR and LO suppression without filters. We also demonstrate how to employ spiral transmission-line baluns at V-band. We present a wide-band and compact method for the transition from even to odd mode and in-phase LO power division for the mixer. This resulted in a small chip area of 1.41 mm^2 for the balanced IR mixer. The mixers were fabricated using a commercial pseudomorphic high electron-mobility transistor (pHEMT) technology from OMMIC, France.

Some of the essential design issues concerning resistive mixers are discussed in the beginning of Section II following the detailed design of the balanced prototype and IR mixers. The measurement setup for up-conversion measurements and the measurement results are presented in Section III. Finally, we present conclusions in Section IV.

II. Mixer Design

In a resistive FET mixer, the transistor is operated in its linear ohmic region, where the LO of the mixer is applied to the gate. The IF (or RF) is applied to the drain and, consequently, the

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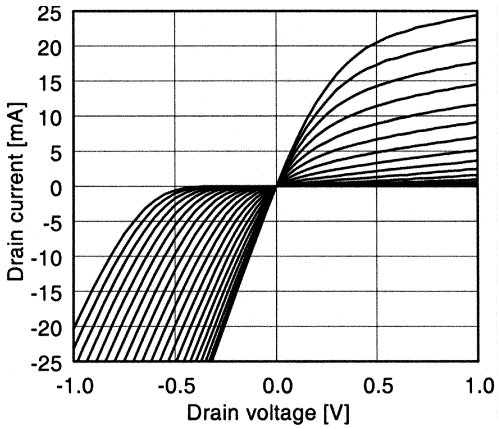

Fig. 1. Measured IV curves of a 2×50 μm HEMT.

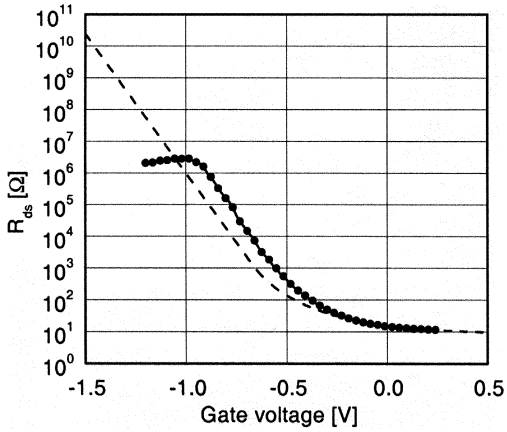

Fig. 2. Measured and simulated (dashed line) drain-to-source resistance of a 2×50 μm HEMT as a function of gate-to-source voltage ($V_d = 50$ mV).

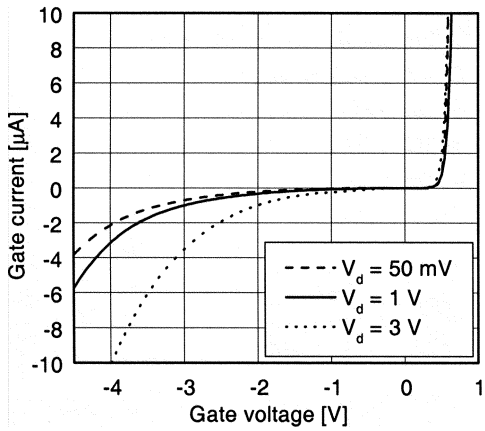

Fig. 3. Measured gate current of a 2×50 μm HEMT as a function of gate voltage for different drain voltages.

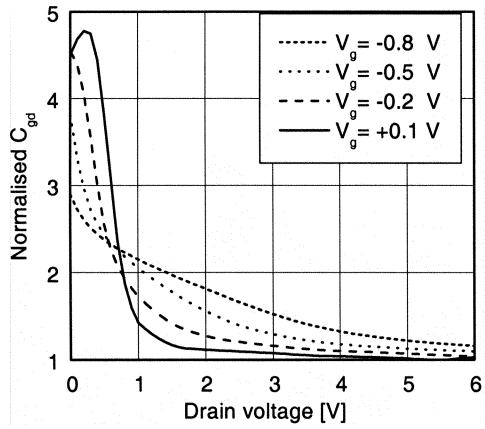

Fig. 4. Normalized gate-to-drain capacitance $C_{\rm gd}$ as a function of drain voltage for different gate bias voltages. The $C_{\rm gd}$ is normalized to open channel capacitance.

RF (or IF) is filtered from the drain. No drain dc-bias voltage is applied to the transistor. The LO of the mixer is used to modulate the channel resistance of an HEMT. The measured IV curves of a 2×50 μm high electron-mobility transistor (HEMT) are shown in Fig. 1. The gate voltage V_g is swept from -1.0 to 0 V in 0.05-V steps. The channel resistance $R_{\rm ch}$ can be found from

$$R_{\rm ch} = \frac{\partial V_d}{\partial I_d} \tag{1}$$

where V_d and I_d are the drain voltage and current, respectively. The measured and simulated drain-to-source resistance $R_{\rm ds}$ of a 2×50 μm HEMT is shown in Fig. 2. The measured gate current as a function of gate voltage is presented in Fig. 3. The minimum channel resistance is around $1\ \Omega \cdot$ mm. The measured $R_{\rm ds}$ saturates when the control voltage is set below -1 V. This is due to gate-leakage effects. The required drive level can be reduced if the gate is biased toward pinchoff. It can be seen that the appropriate gate bias of the device is around -0.5 V.

Since the drain of the transistor is unbiased, the gate-to-drain capacitance $C_{\rm gd}$ is greater than it would be if the drain were biased to the saturation region. This is shown in Fig. 4, where simulated normalized gate-to-drain capacitance as a function of the drain voltage for different gate bias voltages is shown. To prevent the LO from pumping the drain conductance, the RF- and IF-matching circuits have to be designed to short circuit the drain at LO frequency. A wide-band LO short can be realized by using a balanced design. Just as the LO couples through the gate-to-drain capacitance to the drain, so can the RF signal leak to the gate through this capacitance. However, it has been shown that the RF leakage is not a critical design factor [11].

A. Singly Balanced Resistive Mixer

The simplified circuit of the singly balanced resistive mixer is shown in Fig. 5. The LO is applied to a balun to generate the required 180° phase shift at the transistor gates. The drains are connected together through small valued metal–insulator–metal (MIM) capacitors. The connection point of the two drains is a virtual ground for the LO. In order to obtain the desired balanced mixing operation, the IF currents in the drains are out-of-phase and, thus, an external (off-chip) output balun or a hybrid must be used to combine them.

The circuit was designed using a 0.25-μm pHEMT process and coplanar waveguides (CPWs). In this design, the CPW technology was chosen because the grounding of the transistor sources is easy while the drains are kept close together. By employing this method, we can obtain a good virtual ground for the LO at the output.

The gatewidth of the pHEMTs was chosen to be 2×35 μm in order to achieve good impedance matching at the RF port.

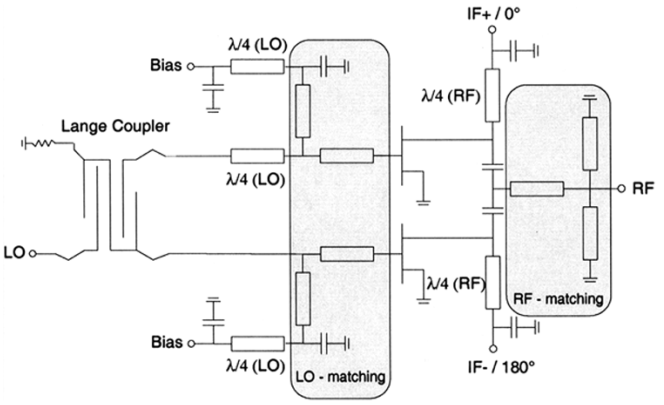

Fig. 5. Simplified schematic of the singly balanced resistive mixer. The IF+ and IF− ports are connected to an off-chip IF hybrid. The capacitors are short circuits at RF frequency and open circuits at IF frequency. A Lange coupler together with a $\lambda/4$ transmission line is used to generate the out-of-phase LO signal at the gate of the transistors.

The RF port is matched with a symmetrical short-circuited shunt stub. Due to the symmetry and the 180° phase shift between the IF lines, any low-frequency disturbance coupled from the RF line will cancel out when they are combined in the off-chip balun.

The transistor gates are matched with short-circuited shunt stubs to 50 Ω. A Lange coupler with 3-dB coupling in a microstrip configuration together with a $\lambda/4$-length CPW line were designed to realize the 180° phase shift of the LO signals at the transistor gates. In order to make the Lange coupler operate in microstrip mode, a gap of 75 μm to the ground-plane metallization was used.

A photograph of the fabricated singly balanced resistive mixer is shown in Fig. 6. The unwanted slotline mode is suppressed by placing air bridges around discontinuities [13]. Due to the relatively thin substrate and limited ground-plane width, the parasitic microstrip mode can be present. Vias are used for connecting the surface ground planes to zero potential to further reduce the possibility of propagating unwanted modes [14].

B. Balanced Resistive IR Mixer

The design principle of the developed balanced resistive IR mixer is presented in Fig. 7. An off-chip differential 90° divider is used for the IF signal. The unit mixers are fed with in-phased LO signals, whereas the IF signal is applied 90° out-of-phase. The desired upper sideband (USB) RF signals from the unit mixers are combined in-phase by the Lange coupler. The undesired lower sideband (LSB) signals are combined out-of-phase and cancelled out. The nominal LO and IF frequencies are 56.0 and 5.3 GHz, respectively. The desired RF frequency (USB) is 61.3 GHz.

The simplified schematic of the unit mixer is shown in Fig. 8. The singly balanced resistive unit mixer consists of two 2×50 μm pHEMTs. The LO is applied from the CPW to a spiral transmission-line balun to generate the required 180° phase shift at the transistor gates. The drains are connected together through small MIM capacitors. The connection point is a virtual ground for the LO and an open circuit for the IF. In order to obtain the desired balanced mixing operation, the IF

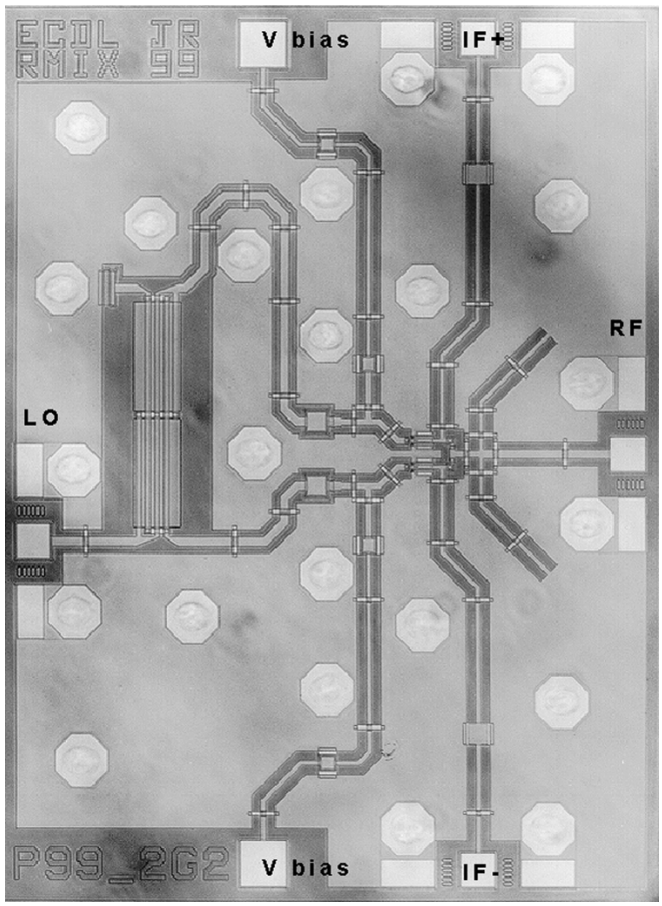

Fig. 6. Fabricated balanced resistive mixer (chip size: 1.5 mm × 2.0 mm) from [12].

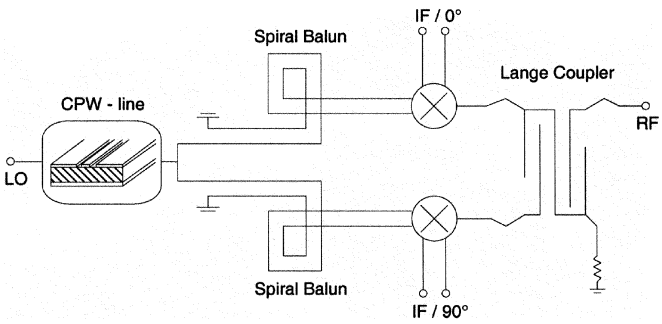

Fig. 7. Configuration of the balanced IR mixer.

signals are applied 180° out-of-phase to the drains. An off-chip hybrid is used for combining them. At RF frequency, the IF line is a quarter-wavelength short-circuited stub, which isolates the IF circuitry from the RF output. The RF short circuit is formed with a ground via-hole and a small valued capacitor.

The spiral transmission-line transformer is a compact and wide-bandwidth balun. The use of the spiral transmission-line transformers have been shown to be a successful solution in microwave mixer circuits [15]. We have demonstrated millimeter-wave frequency-doubler circuits using compact-size spiral baluns [16] and now apply these baluns in a V-band mixer.

The power division and the required 180° phase shift at the gates of the mixing devices are obtained by using two transmis-

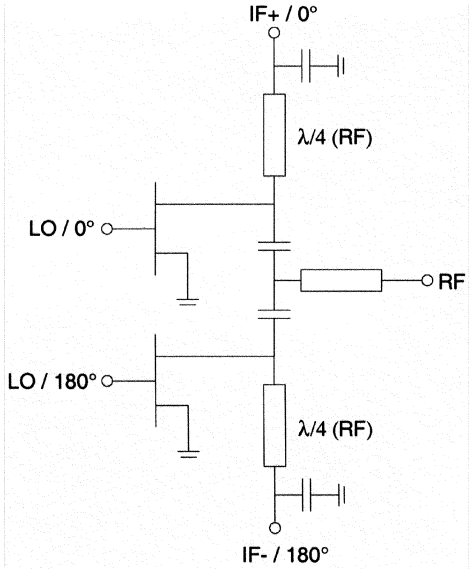

Fig. 8. Realization of the singly balanced unit mixer. The IF+ and IF− ports are connected to an off-chip IF hybrid. The capacitors are short circuits at RF frequency and open circuits at IF frequency.

sion-line baluns connected to CPW LO input. The LO signal propagates on-chip between the CPW slots. The propagating LO is smoothly divided in between the two lines of the spirals. For the signal to propagate in the odd mode, the balun has to rectify the even-mode propagation, which means that the even-mode impedance has to be several times higher than the odd-mode impedance. The even-mode impedance can be increased by wrapping the transmission-line balun in a spiral, as discussed in [15]. The spiral has a minimal effect on the odd-mode impedance. The number of turns of the spiral is limited by the parasitic capacitance, which may result in undesired resonances. This has to be taken into account, particularly at millimeter-wave frequencies. Therefore, we designed the spiral transformers to have one compact turn in order to minimize the parasitic capacitance.

The differential mode propagates in between the two lines of the spiral, thus, the characteristic impedance for these coupled lines should match the input impedance Z_0 of the circuit to the resistive impedances $Z_{\rm in}$ of the matched HEMTs. The circuit is properly matched provided that the electrical length of the coupled lines in the odd mode is $\lambda/4$ at the design frequency and the odd-mode impedance of the quarter-wave transformer $Z_{\rm odd}$ is

$$Z_{\rm odd} = \sqrt{2Z_{\rm in}Z_0}. \tag{2}$$

Since the exact values of even-mode and odd-mode impedances are not extremely critical, the analysis can be divided into two parts, as shown in Fig. 9. The even-mode impedance was calculated from the equivalent circuit of a characterized spiral inductor in which the lines of the balun are joined, and the odd-mode impedance and effective permittivity were calculated using finite-difference electromagnetic (EM) software for the coupled balun.

The connection of the CPW LO input and spiral baluns can be seen in Fig. 10, where a photograph of the test structure on

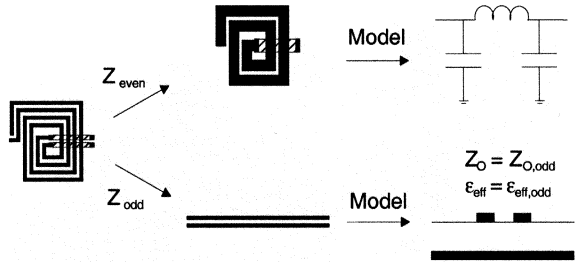

Fig. 9. Simulation of the spiral balun is divided to the characterization of the even-mode impedance $Z_{\rm even}$ with a spiral inductor and the EM analysis of the odd-mode impedance $Z_{\rm odd}$ by calculating the odd-mode properties of a straight section of coupled lines.

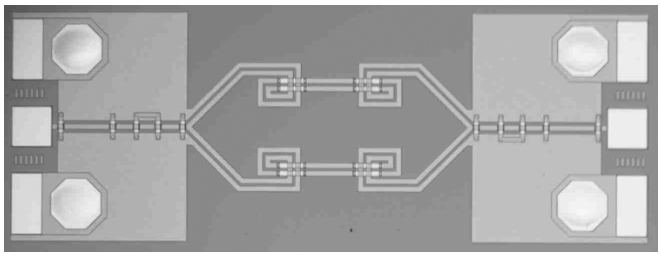

Fig. 10. Test structure on a microchip for the balun and power division of the balanced IR mixer.

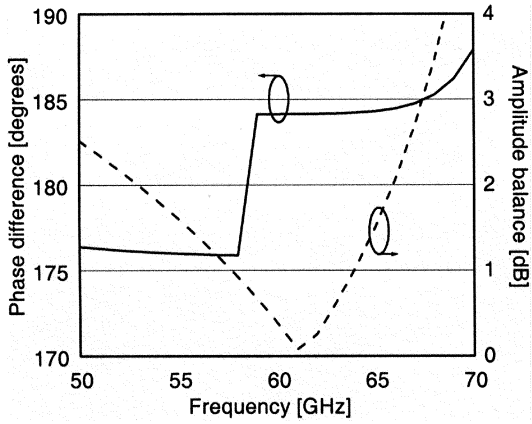

Fig. 11. Simulated phase difference and amplitude balance of the LO balun. The phase difference is $180° \pm 4°$ from 50 to 65 GHz. The amplitude balance is 1.4 dB at 56 GHz.

a microchip is presented. The test structure includes the implementation of the in-phase power division and the transition from even to odd mode for the balanced IR mixer design. In the structure, the divided signal is converted back to CPW mode to easily measure the performance of the even- to odd-mode transition and the power division with coplanar RF probes. The width of the transmission lines of the balun are 10 μm and the lines are separated by a 5-μm gap.

The phase and amplitude balances of the LO power division circuit were simulated using finite-difference EM software; the results are shown in Fig. 11.

The measured and simulated scattering parameters of the test structure at V-band are shown in Fig. 12. The measurement indicates that the power division and the balun are realized successfully and there are no undesired resonances within the LO-frequency range.

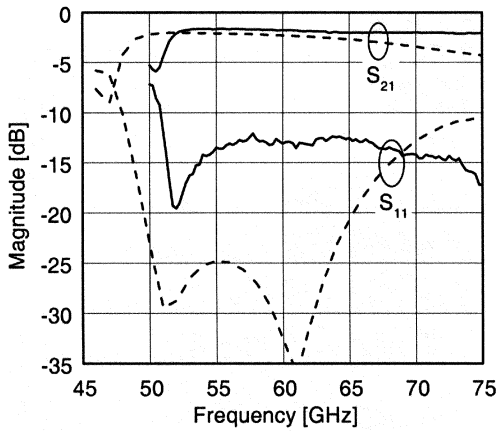

Fig. 12. Measured and simulated back-to-back response of the balun test structure. The dashed lines represent simulated values. The measured insertion loss of the test structure is 2 dB from 52 to 75 GHz.

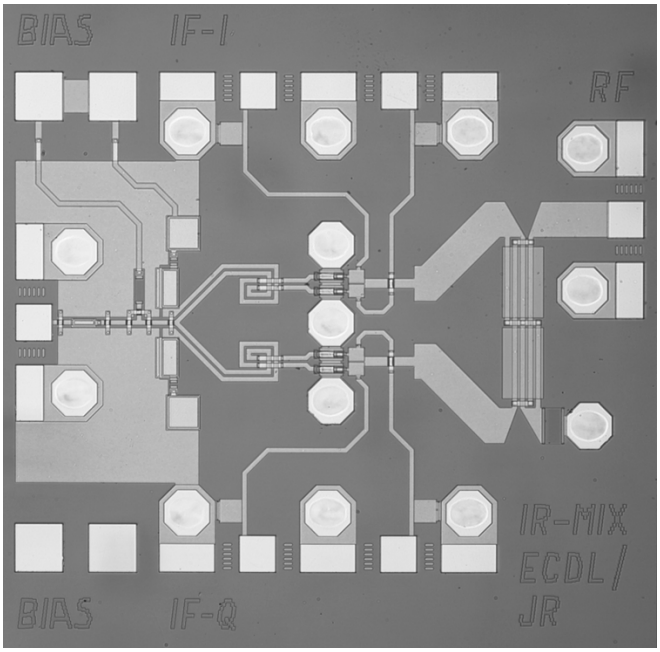

Fig. 13. Manufactured balanced IR mixer. The chip size is 1.5 mm × 1.5 mm. The mixer circuit fits within a 1.41-mm^2 area on chip.

A photograph of the balanced resistive IR mixer is presented in Fig. 13. The microchip was fabricated using a commercially available 0.15-μm GaAs pHEMT process. The chip size is 1.5 mm × 1.5 mm, but the occupied chip area is only 1.41 mm^2 on a standard chip in multiuser processing.

III. Measured Mixer Performance

The measurement setup for the on-wafer measurements of the balanced resistive IR mixer is shown in Fig. 14. The same setup was used when the singly balanced mixer was measured. A 180° IF hybrid was used instead of differential 90° divider in the singly balanced mixer measurement setup. Since only one millimeter-wave frequency source was available for making the measurements, the mixer was measured in the up-conversion configuration. The required LO power was generated by multiplying the signal generator signal using a V-band quadrupler.

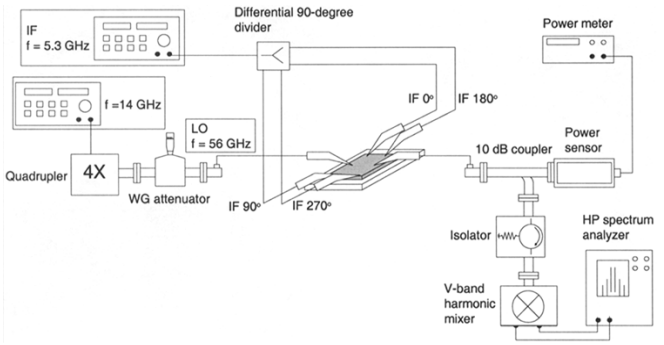

Fig. 14. Measurement setup for the balanced resistive IR mixer. The LO power was generated by multiplying the signal from the generator using a V-band quadrupler. An off-chip differential 90° divider was used for the IF signal. The RF spectrum is measured at the output with a spectrum analyzer. The bias (not shown) is brought to the chip with a dc probe.

The waveguide attenuator is used for power adjustment. The LO power was delivered to the chip using coplanar RF probes. The maximum output power of the quadrupler was approximately 10 dBm and the maximum LO power delivered to the chip was around 8 dBm.

An off-chip differential 90° divider was used for the IF signal. For test purposes, an external IF divider was fabricated on an FR4 substrate. The phase splitter consists of two 90° branch-line couplers and a 180° microstrip rat-race hybrid. The measured back-to-back attenuation of the hybrid was around 11 dB. The amplitude and phase imbalances of the splitter were 0.2 dB and 3.7° at 5.3 GHz, respectively. The loss of the external IF hybrid was subtracted from the measurement results. The output signal of the mixer was down-converted using an external V-band harmonic mixer and the RF spectrum was measured with a spectrum analyzer.

A. Measurement Results of the Singly Balanced Resistive Mixer

The mixer was measured as an up-converter having nominal 5.3-GHz IF frequency and 56-GHz LO frequency. Thus, the desired USB signal is at 61.3 GHz. The conversion loss was measured as a function of the applied gate bias and LO power in order to find the best up-conversion performance of the mixer. The measured and simulated results are presented in Figs. 15 and 16. The optimum conversion loss is achieved when the transistor is biased near the threshold voltage. When this happens, the LO pumps the channel resistance from its high value to its low value. The results show that the optimum gate voltage is around −0.55 V. The highest RF output power is achieved with 8 dBm of LO power, although the mixer seems to be capable of delivering even more RF power with higher LO power levels.

The measured conversion loss and LO-to-RF isolation as a function of RF frequency is presented in Fig. 17. The IF is fixed at 5.3-GHz frequency and the LO power delivered on-chip is around 8 dBm. The measured conversion loss is 11.5 dB with a flatness of 1.4 dB.

The LO-to-RF isolation is better than 34 dB, which suggests that the generated 180° LO signal phase shift and the LO virtual ground on the drain side were realized successfully. In Fig. 18, the measured conversion loss is presented when the LO is fixed.

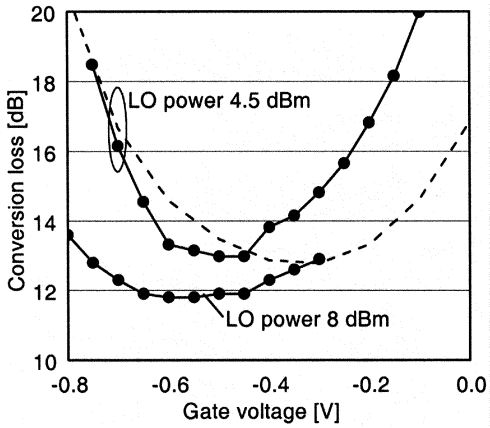

Fig. 15. Measured and simulated conversion loss of the singly balanced mixer as a function of applied gate bias. The dashed line represents the simulated value for LO power of 4.5 dBm.

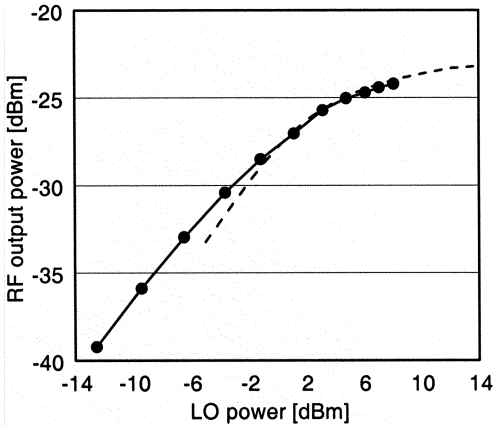

Fig. 16. Measured and simulated (dashed line) RF (61.3 GHz) output power of the singly balanced mixer as a function of applied LO power. The gate voltage is set to −0.55 V.

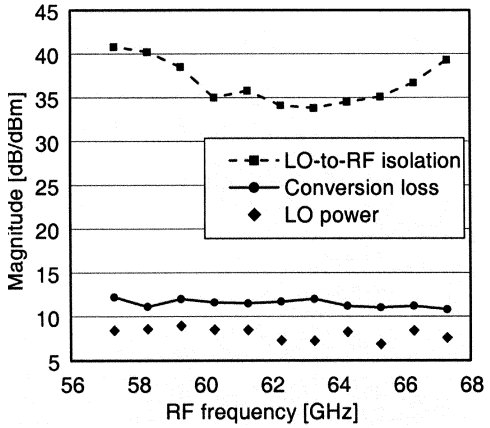

Fig. 17. Measured conversion loss and corresponding LO-to-RF isolation as a function of the RF frequency of the singly balanced mixer. The IF frequency is fixed at 5.3 GHz. The corresponding LO power delivered to the chip is also shown.

B. Measured Results of the Balanced IR Mixer

To find the optimum up-conversion performance of the balanced resistive IR mixer, the conversion loss, LO-to-RF port isolation, and IR were measured as a function of the applied gate bias and LO power. The measured results are shown in Figs. 19 and 20, respectively. As with the singly balanced mixer, the lowest conversion loss is achieved at a gate voltage of −0.55 V. On the other hand, the highest IR is achieved at a gate voltage of −0.45 V. In addition, the LO-to-RF isolation increases when the transistor gate is biased further above threshold voltage. Therefore, the gate bias of the mixer was set to −0.45 V for optimum mixer performance. The highest RF output power is achieved with LO power of 8 dBm, as shown in Fig. 20. The IR ratio improves at higher LO power levels. The return losses of the LO and RF ports were measured at V-band and the measurement results are shown in Fig. 21.

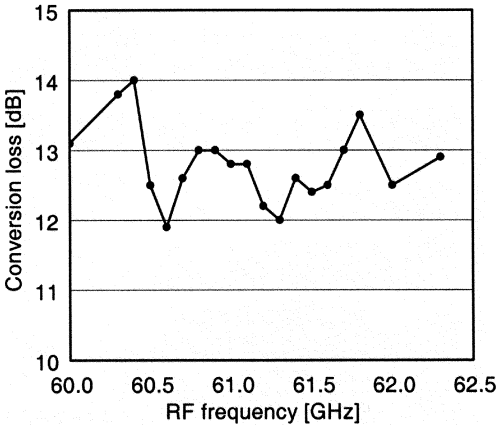

Fig. 18. Measured conversion loss at fixed LO frequency (56 GHz) of the singly balanced resistive mixer. The IF is swept from 4.0 to 6.3 GHz.

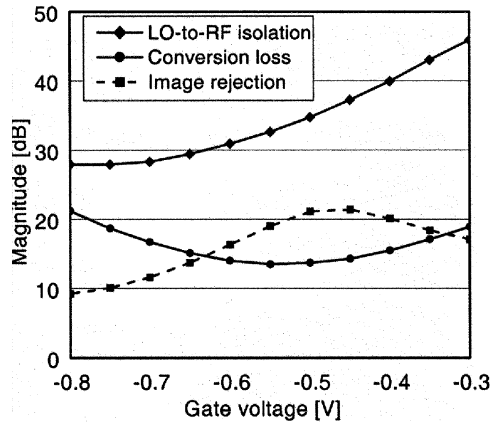

Fig. 19. Measured conversion loss, LO-to-RF isolation, and IR ratio of the balanced resistive IR mixer as a function of applied gate bias.

The measured conversion loss and IR ratio at a fixed IF frequency of 5.3 GHz are shown in Fig. 22 where the LO power delivered to the chip is also shown. The attenuation of the external IF splitter is not included in the measurement results. The conversion loss degrades as the LO power decreases and vice versa. With higher LO power levels, lower conversion loss and a flatter response are to be expected. The measured LO-to-RF isolation is presented in Fig. 23 and the measured conversion loss and IR ratio with fixed LO frequency (56 GHz) is shown in Fig. 24. Good LO suppression indicates that the power division and matching of the transistor gates using spiral transmission-line transformers and CPW input were realized successfully.

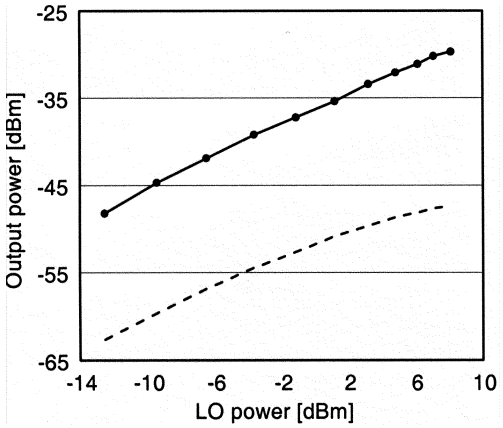

Fig. 20. Measured RF output power and image power (dashed line) of the balanced resistive IR mixer as a function of applied LO power. The gate voltage is set to −0.45 V.

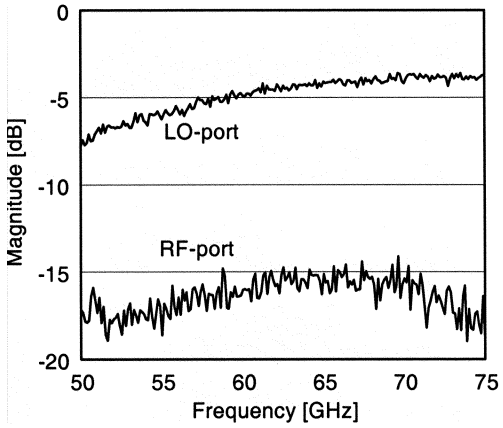

Fig. 21. Measured return losses of LO and RF ports of the balanced resistive IR mixer.

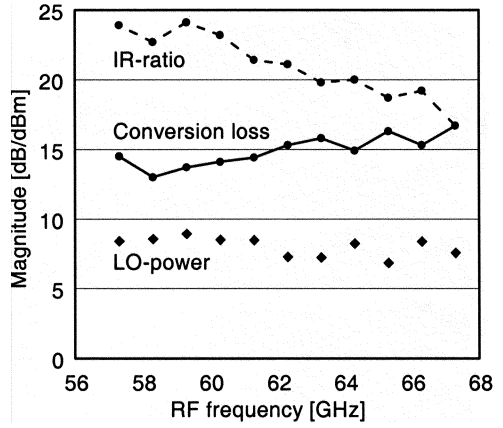

Fig. 22. Measured conversion loss and IR ratio at fixed IF frequency (5.3 GHz) of the balanced resistive IR mixer. The LO is swept from 52 to 62 GHz.

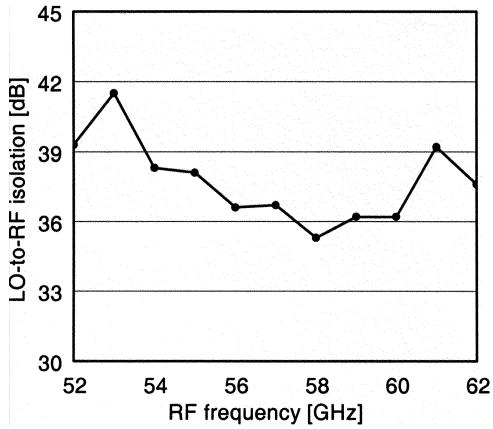

Fig. 23. Measured LO-to-RF isolation of the balanced IR mixer.

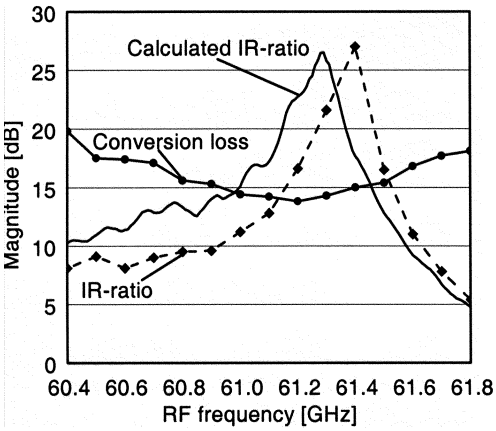

Fig. 24. Measured conversion loss and IR ratio at fixed LO frequency (56 GHz) of the balanced resistive IR mixer. The solid line represents the calculated IR ratio using the measured amplitude and phase errors of the IF test phase splitter. The IF is swept from 4.4 to 5.8 GHz.

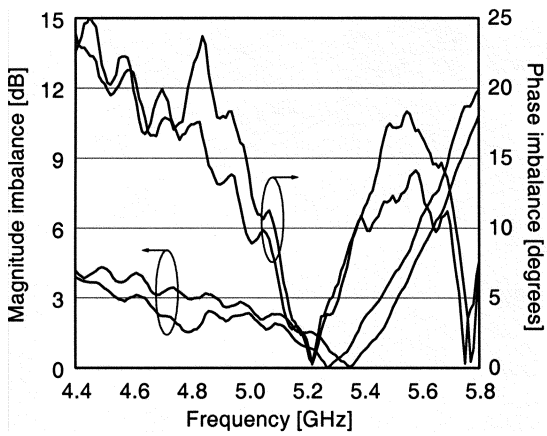

Fig. 25. Measured amplitude and phase error of the IF test phase splitter.

The measured amplitude and phase errors of the external FR4 test phase splitter are shown in Fig. 25, which are determined for the IF-input lines of the two unit mixer pairs. These results are used in the calculation of the IR ratio in Fig. 24; as expected, the IR is mostly determined by the external IF splitter.

The linearity of the balanced IR mixer was defined by measuring the output compression point and the output third order intercept point (OIP3) of the mixer. In Fig. 26, the output third-order intermodulation product at 61.27 GHz and the fundamental signal at 61.29 GHz as a function of applied input

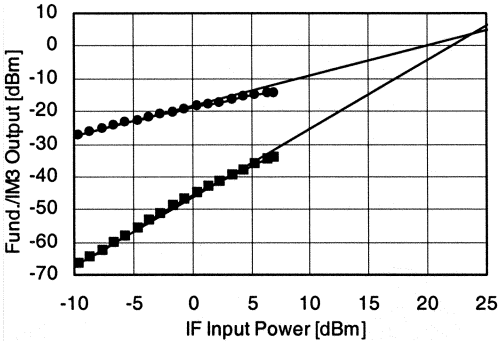

Fig. 26. Measured two-tone test result of the balanced resistive IR mixer. Two IF signals at 5.29 and 5.31 GHz were applied to the mixer. The LO frequency was set to its nominal value of 56 GHz. The OIP3 is at a 4-dBm power level. The measured 1-dB output compression point is at a −13-dBm power level.

TABLE I
SUMMARY OF MEASURED RESULTS OF THE BALANCED IR MIXER

RF frequency	57…66 GHz
Conversion loss	13…16 dB
IR-ratio	> 19 dB
LO suppression	> 35 dB
OIP3	+ 4 dBm
1 dB output compression point	– 13 dBm

power are shown. The measured results of the balanced IR mixer are gathered in Table I.

IV. CONCLUSIONS

In this paper, we have presented the design of broad-band MMIC resistive pHEMT mixers. Based on the successful design of the prototype mixer, we have designed a resistive IR mixer with balanced unit mixers. In this design, we have presented a compact circuit for LO power division and transition from even to odd mode for the pHEMTs in the unit mixers. This resulted in a small chip area of 1.41 mm^2.

The designed balanced IR mixer can significantly improve the performance and reduce the chip area of a 60-GHz telecommunication system. The high IR and LO suppression of the developed mixer enables the integration of the power amplifier and mixer on a single chip without a filter.

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REFERENCES

[1] P. Smulders, "Exploiting the 60 GHz band for local wireless multimedia access: Prospects and future directions," *IEEE Commun. Mag.*, vol. 40, pp. 140–147, Jan. 2002.
[2] J. Mikkonen, "Emerging wireless broadband networks," *IEEE Commun. Mag.*, vol. 36, pp. 112–117, Feb. 1998.
[3] A. Yamada, Y. Amano, Y. Motouchi, N. Takahashi, E. Suematsu, and H. Sato, "A compact 60 GHz sub-harmonically pumped mixer MMIC integrated with an image rejection filter," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Seattle, WA, Jun. 2002, pp. 1733–1736.
[4] S. A. Maas, "A GaAs MESFET mixer with very low intermodulation," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-35, no. 4, pp. 425–429, Apr. 1987.
[5] S. Maas, "A GaAs MESFET balanced mixer with very low intermodulation," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Las Vegas, NV, Jun. 1987, pp. 895–898.
[6] H. Zirath, "Development of 60 GHz front end circuits for high data rate communication systems in Sweden and Europe," in *IEEE Gallium Arsenide Integrated Circuit Symp. Dig.*, San Diego, CA, Nov. 2003, pp. 93–96.
[7] M. Kimishima, T. Ataka, and H. Okabe, "A family of Q, V, and W-band monolithic resistive mixers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Phoenix, AZ, May 2001, pp. 115–118.
[8] K. S. Ang, M. Chongcheawchamnan, and I. D. Robertson, "Monolithic resistive mixers for 60 GHz direct conversion receivers," in *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, Boston, MA, Jun. 2000, pp. 35–38.
[9] T. Kashiwa, T. Katoh, T. Ishida, T. Ishikawa, and Y. Nakayama, "A V-band drain injected/resistive dual-mode monolithic mixer," in *IEEE Gallium Arsenide Integrated Circuit Symp. Dig.*, Monterey, CA, Oct. 1999, pp. 117–120.
[10] M. Schefer, U. Lott, W. Patrick, H. Meier, and W. Bachtold, "Passive, coplanar V-band HEMT mixer," in *IEEE Int. Indium Phospide and Related Materials Conf. Dig.*, Cape Cod, MA, May 1997, pp. 177–180.
[11] S. Maas, *Nonlinear Microwave and RF Circuits*, 2nd ed. Norwood, MA: Artech House, 2003.
[12] J. Riska, P. Kangaslahti, M. Kärkkäinen, and V. Porra, "Amplifiers and signal generation circuits for 60 GHz wireless broadband systems," presented at the Eur. Microwave Conf., Paris, France, Oct. 2000, Paper EuMc_P3.
[13] Y. Baeyens, L. Verweyen, W. Haydl, W. Marsetz, and M. Schlechtweg, "Design of compact millimeter-wave MMICs using CPW," in *IEE Design of RFICs and MMICs Tutorial Coll.*, 1987, Ref. 1997/391, pp. 3/1–3/6.
[14] O. Salmela, "Wideband, single-mode coplanar waveguide operation," in *Proc. Asia–Pacific Microwave Conf.*, Yokohama, Japan, Dec. 1998, pp. 827–829.
[15] S. Maas, F. Kintis, F. Fong, and M. Tan, "A broadband planar monolithic ring mixer," in *IEEE Microwave Millimeter-Wave Monolithic Circuits Symp. Dig.*, San Francisco, CA, Jun. 1996, pp. 51–54.
[16] P. Kangaslahti, J. Riska, M. Kärkkäinen, P. Alinikula, and V. Porra, "Low phase noise signal generation circuits for 60 GHz wireless broadband system," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Boston, MA, Jun. 2000, pp. 43–46.

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