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A 60-GHz CMOS Receiver With an On-Chip ADC

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***Abstract* — A broadband 60-GHz receiver implemented in a 65-nm baseline CMOS technology is presented. A millimeter-wave front-end, including a single-ended low noise amplifier and a balanced resistive mixer, an IF-stage and an analog baseband circuit with an analog-to-digital converter are integrated on a single chip. The receiver achieves a measured 7.0-dB noise figure at 60 GHz and the voltage gain can be controlled between 45 to 79 dB. The measured 1-dB input compression point is –38.5 dBm.**

***Index Terms* — ADC, CMOS, MMIC receivers.**

I. Introduction

The development of deep-submicron CMOS processes and the limited spectrum below 10 GHz has increased interest towards transceivers operating in the unoccupied millimeter-wave frequencies. For example, the 60-GHz unlicensed band is seen as a viable choice for high-data-rate applications like high quality video streaming. In the last few years, various millimeter-wave CMOS blocks and RF front-ends operating at 60-GHz have been published [1]-[3]. The aim of this paper is to demonstrate a 60-GHz single-chip receiver. The millimeter-wave front-end and IF-stage circuits are designed to achieve high performance and wideband operation for 60-GHz reception. The baseband circuit with a programmable gain amplifier (PGA) ensures optimal input signal level for the analog-to-digital converter (ADC) and supports wireless MB-OFDM ultra wideband (UWB) system data reception [4]. The receiver is implemented in a 65-nm baseline CMOS technology. No additional options were employed in the fabrication process and the receiver layout fulfills all the required technology specific design rules.

II. Receiver Design

The block diagram of the single-chip 60-GHz receiver is shown in Fig. 1. The dual-conversion architecture was chosen to minimize the number of blocks operating at millimeter-wave frequencies. The 60-GHz front-end consists of a single-ended LNA and a balanced resistive mixer, which downconverts the signal to intermediate frequency (IF). A differential two-stage cascode amplifier follows the resistive mixer before the IF signal separation into I/Q baseband signals with a quadrature mixer. The balanced quadrature signals for the mixer are generated on-chip with an active poly-phase filter for which the resistors are replaced with transconductors. The baseband circuit contains a merged 275-MHz low-pass filter and a programmable gain amplifier and is followed by a 6-bit 600-MS/s flash-ADC. In this test chip, both local oscillator (LO) signals are external and one complete baseband chain with the ADC is integrated on chip. The other baseband channel includes a wideband buffer for testing purposes.

A. Millimeter-Wave Front-End

The simplified schematic of the millimeter-wave front-end is shown in Fig. 2. To minimize the noise-contribution of the resistive mixer and the following stages, the LNA uses four common-source stages. Although the weak reverse isolation of the common-source topology makes the design challenging, low noise figure and sufficient gain can be achieved at millimeter-wave frequencies.

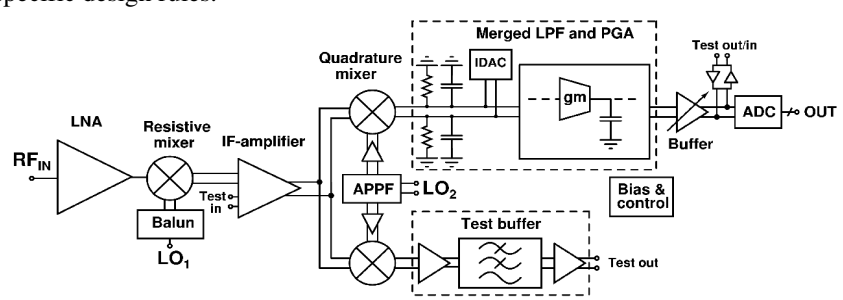

Fig. 1. Receiver block diagram.

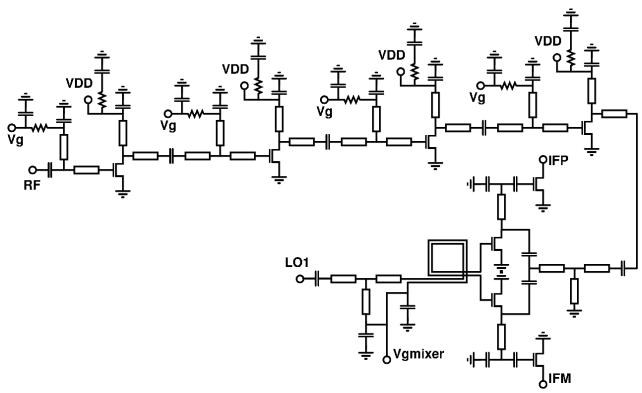

Fig. 2. Simplified schematic of the millimeter-wave front-end.

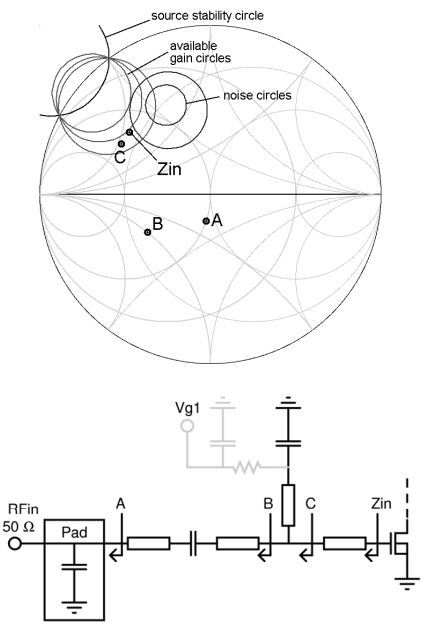

Fig. 3. Input matching principle of the millimeter-wave LNA. Impedance after each circuit block is plotted on the Smith-chart. Available gain circles and noise circles of a 90/0.07-sized transistor are plotted for 7, 8, and 9 dB and 3.1 and 3.4 dB levels, respectively.

Coplanar waveguides (CPWs) are used for on-chip matching. The transmission lines provide a well-defined ground return current path and, hence, enable accurate simulations and very predictable performance of the 60-GHz front-end. To fulfill metal density requirements, the ground planes of the CPWs are formed by strapping all metal layers together with via-matrices. The RF short-circuits of the matching stubs and the DC decoupling are realized with standard finger capacitors. For accurate simulations, both active and passive components were characterized using test structures from the previous process run [5]. The input matching principle of the millimeter-wave LNA is shown in Fig. 3. Available gain circles, noise circles and a source stability circle of a 90/0.07-sized transistor are plotted on the Smith-chart at 60 GHz. As can be seen, all the passives have a strong influence on the matching and for example, the effect of parasitic capacitances has to be well modeled. The simulated gain and noise figure (NF) of the LNA at 60 GHz are 19 dB and 6 dB, respectively.

The detailed design of the mixer is presented in [5]. The balanced resistive mixer configuration establishes a broadband conversion from the single-ended 60-GHz input to the differential IF. In the mixer an on-chip spiral transmission line balun converts the coplanar LO_1 input into differential signal, which is then fed to the gates of the mixing transistors. The drains are connected together using capacitors, which are short-circuits at RF- and LO-frequencies and open circuits at IF-frequency. The interface to the IF-stage is implemented using CPWs, which are short-circuited at 60 GHz using small valued capacitors. This isolates millimeter-wave signals from the IF-stage.

B. IF-Stage and Baseband

A two-stage amplifier with a cascode configuration is utilized in the IF-stage to reduce the noise contribution of the remaining receiver chain. The first amplifier stage has a shunt-peaked load to guarantee a broadband response. An enhanced source-follower output buffer is designed to drive the following quadrature mixer. The buffer output is directly connected to the sources of double-balanced Gilbert-cell mixing transistors. When compared to a conventional high-impedance mixer input, this low-impedance node suffers less from parasitic capacitance. A common-mode feedback circuit at the mixer output biases the mixing transistors and sets the DC input voltage for the baseband.

The 5th-order baseband low-pass filter, similar as in [6], has a digitally programmable gain to amplify received in-band signals with a wide power range to the desired full-scale level of the following ADC. The filter circuit consists of a real pole realized at the filter input with the passive load components of the preceding quadrature mixer, a 4th-order gm-C leapfrog filter having embedded voltage gain, and an output buffer designed to drive the ADC. The DC offset of the receiver is compensated with a 6-bit current-steering digital-to-analog converter (IDAC) at the filter input. The measured –3dB bandwidth and variable gain range of the filter with the output buffer are 275 MHz and 34 dB, respectively.

The block diagram of the 6-bit full-flash ADC is shown in Fig. 4. Active interpolation is used before the second preamplifier stage and the comparator stage. Interpolation reduces the input capacitance of the ADC as well as power consumption. Reference voltages

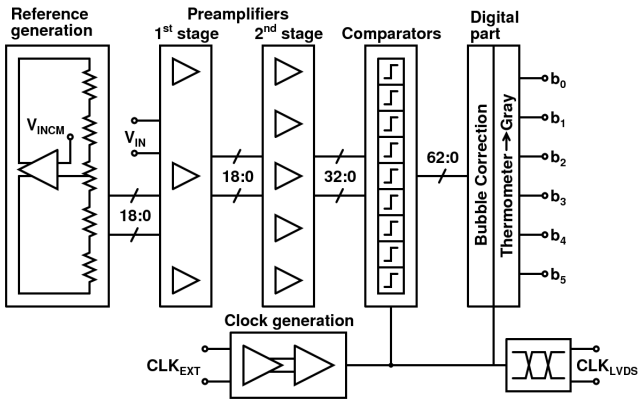

Fig. 4. Block diagram of the ADC.

for the ADC are generated with a separate amplifier, which forces the common-mode of the resistor ladder to follow the common-mode voltage of the baseband filter. Data is driven out of the chip using single-ended outputs, while the clock output uses LVDS.

III. Measurement Results

The receiver is fabricated in a 65-nm baseline CMOS technology and chips were directly bonded onto a PCB excluding the millimeter-wave inputs. The micrograph of the receiver is shown in Fig. 5. The total silicon area including pads is 2.8 mm^2. The receiver measurements were performed from the output of the ADC with the exception of the 1-dB input compression point (ICP), which was measured from the analog test output. The millimeter-wave signals were fed to the chip via RF-probes. The performance of the whole receiver was characterized with a combination of a fixed LO_2 frequency of 4 GHz, baseband frequencies of both 10 MHz and 100 MHz, and an ADC sampling rate of 600 MS/s. The measured noise and gain performance of the receiver, with LO_1 between 59 to 64 GHz and with the maximum baseband gain setting, are shown in Fig. 6. The measurement set-up limited the RF input to 60 GHz. The NF, which is dominated by the LNA, is 7.0 dB at 60 GHz and 7.9 dB at 55 GHz, showing a relatively flat noise figure over the measured frequency range. The receiver chain achieves a total maximum gain of 79 dB at 60 GHz and it remains flat within 2 dB over the measured band. As shown in Fig. 7, there is a good agreement between the measured and simulated input matching S_{11} of the receiver. Input matching is observed to be below –12 dB from 55 to 62 GHz. The measured ICP of the receiver is –38.5 dBm with receiver minimum gain of 45 dB. Fig. 8 shows the output spectrum of the ADC at 600 MS/s with a 10 MHz baseband signal.

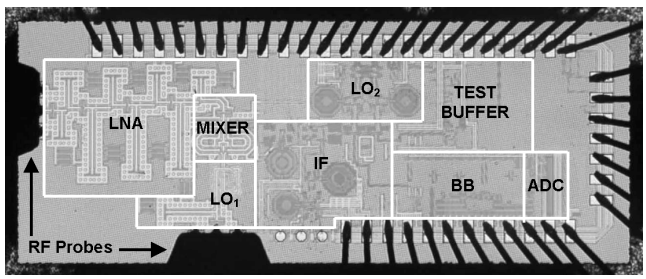

Fig. 5. Micrograph of the receiver.

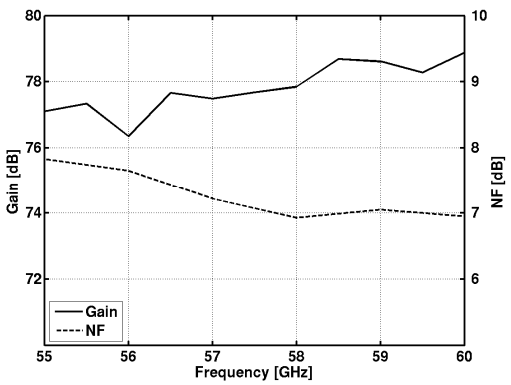

Fig. 6. Measured voltage gain and noise figure of the receiver.

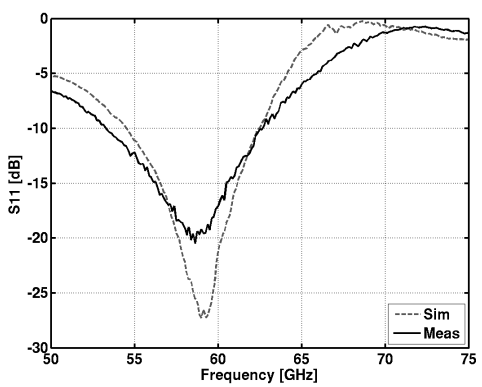

Fig. 7. Measured and simulated S_{11} of the receiver.

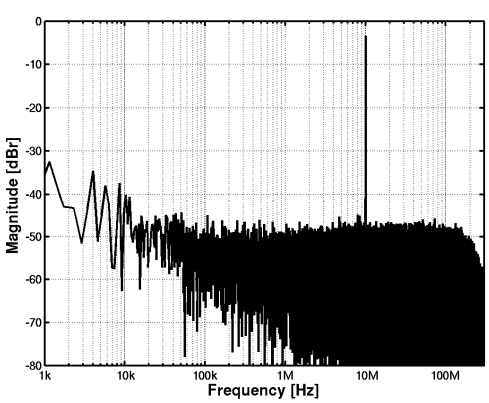

Fig. 8. Spectrum of the whole receiver measured from the output of the 600-MS/s ADC with a 10 MHz signal at the baseband.

The total power consumption of the receiver with one baseband channel is 198 mW from a 1.2 V supply. Table 1 summarizes the experimental results of the whole receiver and the performance is compared to recently published 60-GHz receiver front-ends in Table 2.

TABLE I
MEASURED PERFORMANCE OF THE 60-GHZ CMOS RECEIVER

Technology	65nm CMOS
Supply voltage	1.2 V
Range of operation*	55 to 60 GHz
NF**	7.0 dB
Voltage gain**	79 to 45 dB
Gain control step	1 dB
ICP** with min gain	–38.5 dBm
S11***	< –12 dB
BB –3dB frequency	275 MHz
ADC sampling rate	600 MS/s
ADC ENOB	> 4.0 bits
ADC SFDR	> 30 dB
Power dissipation	198 mW
Chip area	2.8 mm^2

* Limited to 60 GHz by the measurement set-up
**RF/IF at 60/4GHz
***Over the entire range of operation

VII. CONCLUSION

In this paper, a broadband 60-GHz receiver, with an analog baseband circuit and an A/D converter, implemented in a 65-nm baseline CMOS technology is presented. As a result of the accurate modeling of the millimeter-wave circuit blocks and careful system level design, wideband performance and as low as 7-dB noise figure were achieved. The dynamic range of the receiver is considerably increased by embedding voltage gain with 34-dB variable gain range into the baseband low-pass filter. The experimental results demonstrate the feasibility of a broadband single-chip 60-GHz receiver with an ADC in deep-submicron CMOS. Despite the high level of integration, this receiver compares favorably to existing state-of-the-art millimeter-wave front-ends.

ACKNOWLEDGEMENT

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TABLE II
COMPARISON TO PUBLISHED 60GHZ CMOS RECEIVER FRONT-ENDS

	[1]	[2]	[3]	This work
Technology	90-nm CMOS	90-nm CMOS	90-nm CMOS	65-nm CMOS
Integrated Blocks	Antenna, LNA, mix, TIA, VCO, synth.	LNA, polyphase, 2xmix, LO	LNA, mix, VGA, buffer	LNA, mix, IF amp, IF mix, IF IQ-gen, BB LPF+PGA, ADC
Max. gain	22.5 dB*	22 dB	55.5 dB*	79 dB
NF	8.4 dB**	5.7 to 8.8 dB	6.1 to 6.35 dB**	7.0 dB
$P_{1dB,IN}$	---	–27.5dBm	–26dBm	–38.5dBm
S11	< –6.25 dB	---	< –10 dB	< –12 dB
Supply	1.2 V	1.2 V	1.0 V	1.2 V
P_d	144 mW	36 mW	24 mW	198 mW
Area	2.64 mm^2 ***	0.185 mm^2 ***	1.55 mm^2	2.8 mm^2

*Power gain instead of voltage gain
** DSB NF
***Active area without pads