Publication P8

Mikko Kärkkäinen, Mikko Varonen, Dan Sandström, and Kari A. I. Halonen. 2009. 60-GHz receiver and transmitter front-ends in 65-nm CMOS. In: 2009 IEEE MTT-S International Microwave Symposium Digest (IMS 2009). Boston, MA, USA. 7-12 June 2009, pages 577-580.

60-GHz Receiver and Transmitter Front-Ends in 65-nm CMOS

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***Abstract* — In this paper, 60-GHz receiver and transmitter front-ends implemented in 65-nm baseline CMOS are presented. Both down- and upconversion mixers employ a spiral transmission line balun for the local oscillator input, thus, creating a balanced mixer topology. The receiver has a balanced active mixer and a low noise amplifier on the same chip. The measured results show that the receiver has a 14.5-dB gain and a 9.2-dB double sideband noise figure with 53-GHz local oscillator and 1.5-GHz intermediate frequencies. The transmitter front-end consists of a balanced resistive mixer and a five-stage medium power amplifier. The mixer topology enables wideband LO-suppression as well as IF and RF responses. The measured upconversion gain and 1-dB output compression point at 60 GHz are 12 dB and –3 dBm, respectively. The saturated output power is +2 dBm. The chip sizes are 0.90 and 1.00 mm^2 for the receiver and transmitter front-end, respectively.**

***Index Terms* — MMIC receivers, MMIC transmitters, MMIC amplifiers, MMIC mixers, CMOS integrated circuits.**

I. Introduction

The large bandwidth around the 60-GHz range and the integration possibilities of silicon technology has gathered a lot of interest in CMOS based millimetre wave integrated circuits. The device scaling of CMOS technologies improves the performance of the transistors in terms of a higher unity gain frequency (f_T) and maximum frequency of oscillation (f_{MAX}). However, the scaling of a bulk CMOS process typically introduces some challenges to the designer. These include lower supply voltage, stringent metal density requirements and thinner dielectric layers above the substrate leading to higher substrate and ohmic losses of passives.

Recently, receiver and transmitter front-ends for the 60-GHz range have been implemented in 90-nm CMOS technology [1]-[4]. The aim of this paper is to demonstrate the performance of integrated receiver and transmitter front-ends for the 60 GHz band in 65-nm baseline CMOS. The receiver front-end has an active mixer whereas the transmitter front-end uses a passive mixer topology. No additional options were employed in the fabrication process.

II. Receiver Front-End

A simplified schematic of the receiver front-end is presented in Fig. 1. The receiver consists of a 5-stage low noise amplifier and an active mixer including buffers at the balanced IF output. The design of the amplifier is presented in section IV.

The mixer topology is similar to a half of a Gilbert type mixer having a transconductance stage below the mixer core. The balanced mixer operation is realised by placing a spiral transmission line balun at the LO-input, which also provides an impedance match to the mixing transistors. The IF-outputs have source followers to provide buffering to a 50-ohm measurement system. Coplanar waveguides are used in the amplifier and mixer, except the coupled lines in the LO path. The IF-outputs have a balanced topology with ground metal strip in between the signal lines. The matching between the LNA output and mixer input as well as inductive compensation at the drain of the transconductance stage are realized with short circuited shunt stubs. The short circuit is created with standard finger capacitors. The gate bias voltage and the boost current for the transconductance stage are provided through the shunt stubs.

The small-signal characteristics of this transistor as well as the coplanar waveguide were characterized earlier using separate test structures [5]. The large signal model is provided by the foundry.

The balanced IF-output signals are combined in an external coupler. The gate bias for the source followers is set by the circuit topology and the main supply for the mixer is 2.3 V. This way the total current flowing through the source followers is around 20 mA. The drain current of the amplifier stages is 18 mA per stage from a 1.2 V supply.

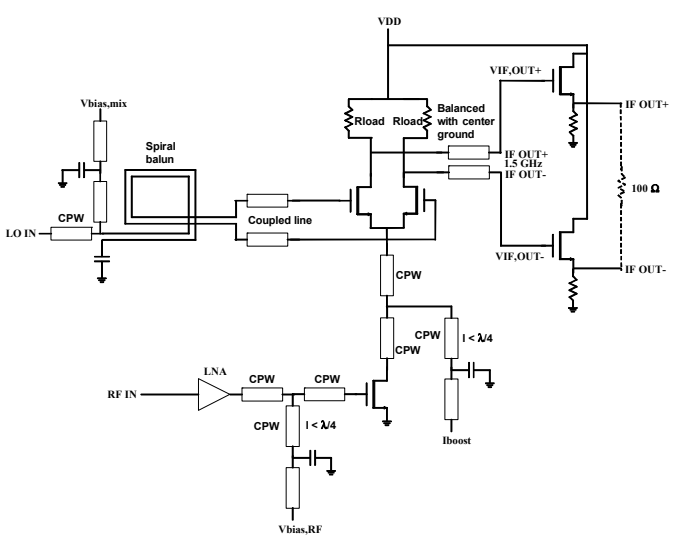

Fig. 1. Simplified schematic of the receiver front-end.

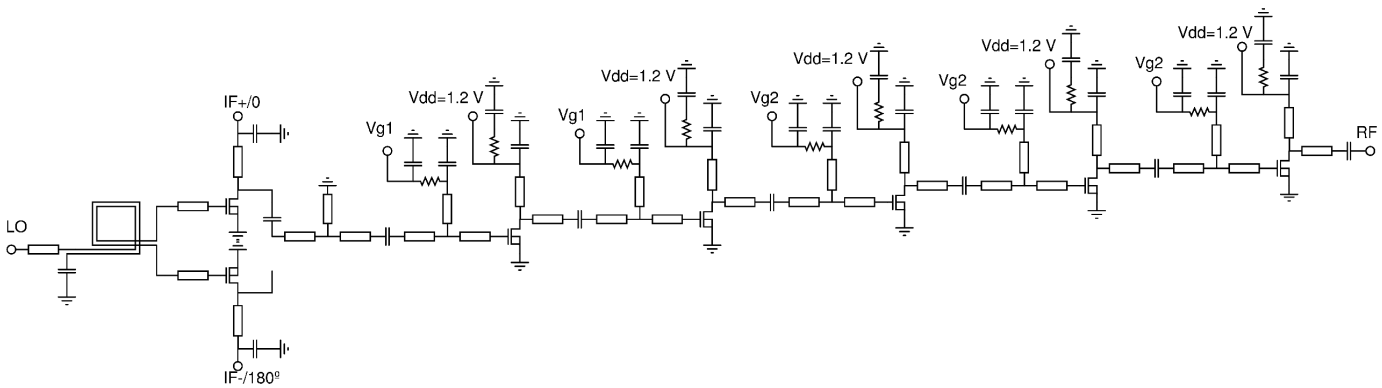

Fig. 2. Simplified schematic of the transmitter front-end.

III. Transmitter Front-End

In the transmitter, the local oscillator signal has to be adequately suppressed. Furthermore, the 1-dB output compression point of the mixer should be high to reduce the gain requirements of the power amplifier. Therefore, the balanced resistive mixer seems to be an appealing topology.

A simplified schematic of the transmitter front-end is presented in Fig. 2. It consists of a balanced resistive mixer and a five stage amplifier. The detailed design of the mixer is presented in [5]. In the mixer, spiral transmission line balun is used to transform the single-ended LO fed from CPW-input to 180 degree LO-signal for the gates of the mixing devices. The drains are connected together using small-valued capacitors. The connection node is a virtual ground for the LO-signal enabling a wideband LO suppression. Differential IF-signal is fed to transistor drains through CPW-lines. The CPW-lines are short circuited using capacitors at RF. The RF-signal port is matched to the input of the amplifier using a short-circuited shunt stub. For the desired upper sideband signal at 60 GHz, the measured 1-dB output compression point (OP1dB) and conversion loss of the mixer are –19 dBm and 13.5 dB, respectively. The measured LO-supression is better than 34 dB for LO-fequencies from 51 to 62 GHz.

IV. Amplifier Design

The two most commonly used transistor configurations at mm-wave frequencies are the common-source and the cascode topology. The cascode topology achieves good isolation, high gain, good stability and low power consumption. As the operation frequency increases, the effect of the parasitic capacitances of the transistors becomes more pronounced. For example, resonating out the capacitances at the drain of the input transistor stage may improve performance. By using a common source topology the output voltage and current swings can be maximized. Thus, a high output power and good linearity can be achieved. This is especially beneficial when using a lower supply voltage. Although, the weak isolation of the common source topology makes the design challenging, low noise figure and good gain are feasible at millimeter wave frequencies. Regardless of the chosen topology, the performance depends greatly on how the layout is drawn, since the contact parasitics become more dominant at mm-wave frequencies. The transistor sizing is critical at mm-wave frequencies: The width of the fingers must be short (in order of 1μm) to minimize the gate resistance and thus maximize f_{max} and gain and simultaneously minimizing the noise figure. For higher current swings, multiple fingers can be used in parallel to obtain high output power with a low supply voltage. However, the gate width cannot be increased arbitrarily as low loss wideband matching becomes difficult.

In this work, the same amplifier is used in both transmitter and receiver RF front-ends. Based on measurements, a W/L = 90/0.07 μm-sized transistor, constructed of several narrow fingers, was used in the amplifier design. It provides both low noise figure and high output power.

In the case of the transmitter front-end, enough gain is needed to drive the output stage of the amplifier into compression. The measured OP1dB of the mixer and amplifier are -19 dBm and 1.5 dBm, respectively. This means that the amplifier should provide more than 20 dB gain. Therefore, a five-stage amplifier was chosen for the transmitter front-end circuit. When considering the receiver front-end, enough gain is needed from the low noise amplifier to reduce the noise contribution of the mixer, and, thus, to improve receiver sensitivity. The same 5-stage amplifier is used in the receiver front-end circuit, although, in practice, by using smaller transistors a similar performance could be achieved with lower power consumption. Also, the power consumption of the transmitter front-end could be improved by carefully resizing the gain and driver stages of the amplifier. The amplifier is matched using series and short-circuited CPW shunt stubs as shown in Fig. 2. Standard finger capacitors are used for implementing DC-blocking and short-circuiting capacitors.

V. Measured Results

The RF front-end circuits were measured on-wafer using coplanar probes for the RF-, LO, and IF-ports. An external hybrid is used for dividing and combining the IF-signals. All

cable losses in the measurement setup were measured and subtracted from final results.

A. Receiver front-end

The micrograph of the receiver front-end is shown in Fig. 3. The measured results show a gain of 14.5 dB and a double sideband (DSB) noise figure of 9.2 dB for the receiver front-end, as seen in Fig. 4. The LO frequency is 53 GHz and the lower sideband (LSB) RF is at 51.5 GHz. The LO power delivered to the chip is around +5 dBm over the measured range and at 53 GHz an LO power sweep showed that a power level of +4.4 dBm is enough to obtain optimal performance. The IF was swept from 500 to 2000 MHz with LSB RF. The measured results show that the IF response remains practically unchanged up to 1.5 GHz and even at 2 GHz the gain is still around 13 dB with 53 GHz LO, as seen in Fig. 5.

The 1-dB input compression point (ICP) is at -24.4 dBm level, as seen in Fig. 6. The total power consumption of the receiver front-end is 174 mW of which 120 mW is dissipated in the amplifier and 40 mW in the output buffers. The size of the receiver front-end chip is 0.90 mm^2 including pads.

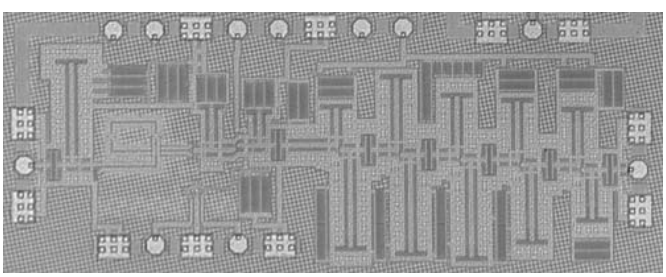

Fig. 3. A die micrograph of the receiver front-end chip. The chip size is 0.90 mm^2 including pads.

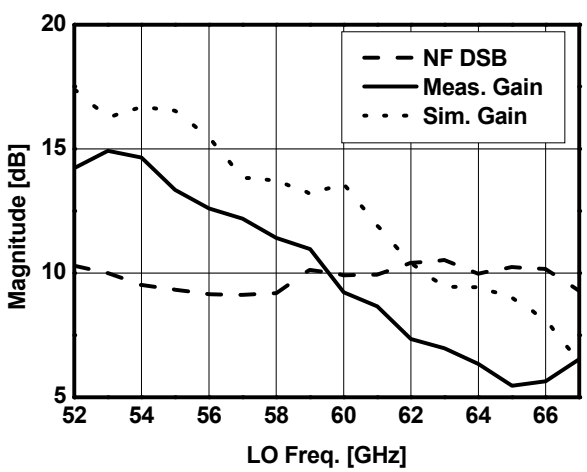

Fig. 4. Measured and simulated gain as well as measured double sideband noise figure of the receiver.

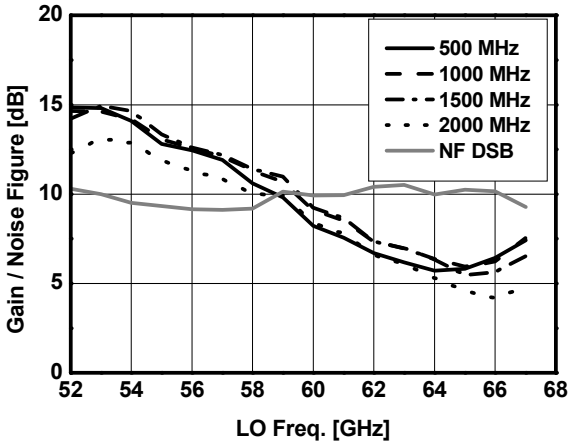

Fig. 5. Measured receiver front-end gain with IF at 500, 1000, 1500 and 2000 MHz. The DSB noise figure is measured with 1500 MHz IF.

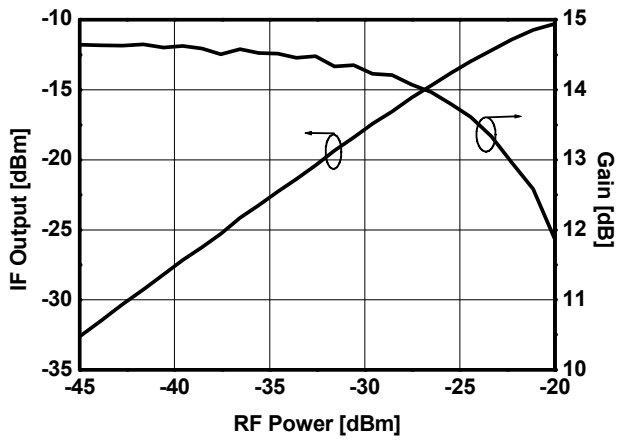

Fig. 6. Measured 1-dB input compression point (ICP) for the receiver front-end. The LO is at 53 GHz and IF at 1.5 GHz.

B. Transmitter front-end

The micrograph of the transmitter is shown in Fig. 7. The transmitter chip was assembled on a PCB-substrate and DC-bias pads were bonded to the PCB. Otherwise, the performance of the transmitter was measured on-wafer. The gate voltage of the resistive mixer was set to 0.56 V for optimum conversion loss. All the amplifier stages were biased to same drain bias of around 20 mA per stage using a 1.2 V supply. It is possible to bias the first two stages and the last three stages of the amplifier separately.

The measured conversion gain and RF output power at 60 GHz are shown in Fig. 8. The desired RF signal is at upper sideband (USB) and a LO power of 8.7 dBm is delivered to the chip. The measured 1-dB output compression point is at –3 dBm power level. The saturated output power is around 2 dBm. The measured LO power at RF-port is below the desired RF-signal which means that the LO virtual ground at the drains of the mixer was realized successfully. In Fig. 9, the measured and simulated conversion gain with fixed LO-frequency of 57 GHz are shown. The IF is swept form 1 to 6 GHz. The measurement shows very wideband IF and RF-

response. Also, the simulations are in agreement with the measurements. The measured conversion gain as a function of the LO and IF frequencies is shown in Fig. 10. The LO is swept from 51 to 62 GHz while the IF is swept fom 1 to 6 GHz. The measurement results show a wideband IF, RF and LO performance.

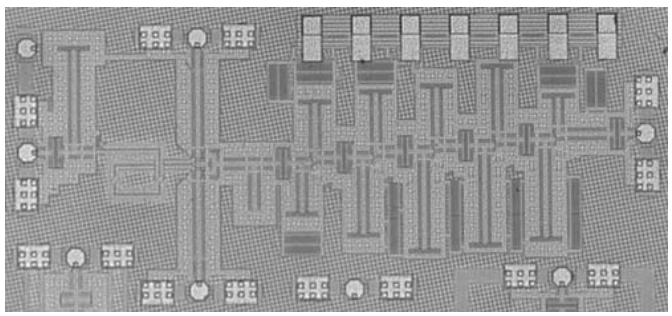

Fig. 7. A die micrograph of the transmitter front-end chip. The chip size is 1.0 mm^2 including pads.

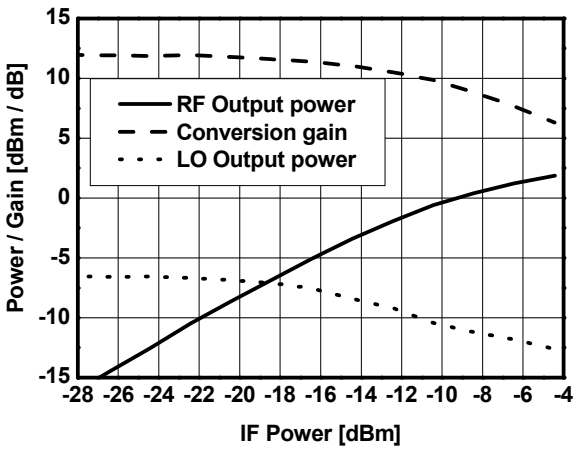

Fig. 8. Measured conversion gain and RF output power of the transmitter front-end chip. The LO and RF frequencies are at 58 and 60 GHz. The measured LO power at the RF output port is also shown. V_{supply} = 1.2 V, I_{total} = 110 mA.

VI. Conclusions

Integrated receiver and transmitter RF front-ends were presented for the 60 GHz range. The receiver front-end has an active mixer whereas the transmitter front-end uses a passive mixer topology. The measured results show that these relatively compact designs achieve high performance and demonstrate the millimetre wave capability of the 65-nm baseline CMOS technology.

Acknowledgement

We want to thank ESA external laboratory MilliLab for performing the on-wafer measurements of the receiver front-end. This work was funded by the Finnish Funding Agency for Technology and Innovation under Nastec-project.

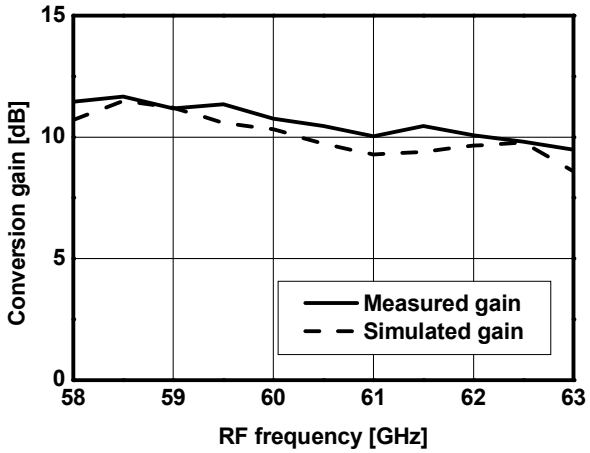

Fig. 9. Measured and simulated conversion gain at a fixed LO frequency (57 GHz) of the transmitter front-end chip. The IF is swept from 1 to 6 GHz. V_{supply} = 1.2 V, I_{total} = 100 mA.

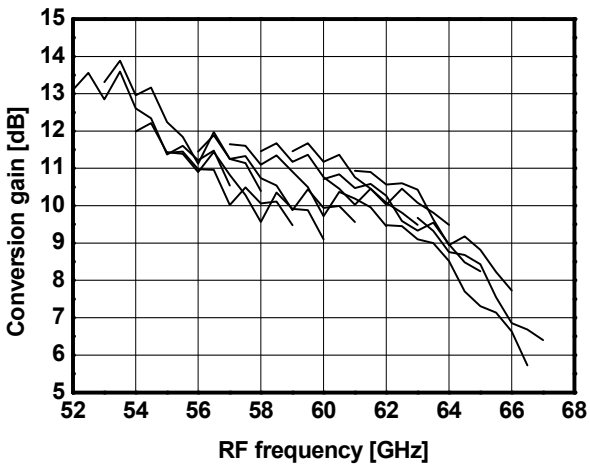

Fig. 10. Measured conversion gain of the transmitter front-end chip. The LO and IF are swept from 51 to 62 GHz and 1 to 6 GHz, respectively. V_{supply} = 1.2 V, I_{total} = 100 mA.

References

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