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DESIGN AND CHARACTERIZATION OF MONOLITHIC MILLIMETER-WAVE ACTIVE AND PASSIVE COMPONENTS, LOW-NOISE AND POWER AMPLIFIERS, RESISTIVE MIXERS, AND RADIO FRONT-ENDS

Doctoral Dissertation

Mikko Varonen

Aalto University
School of Science and Technology
Faculty of Electronics, Communications and Automation
Department of Micro and Nanosciences

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School of Science and Technology
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Instructor	

Abstract

This thesis focuses on the design and characterization of monolithic active and passive components, low-noise and power amplifiers, resistive mixers, and radio front-ends for millimeter-wave applications. The thesis consists of 11 publications and an overview of the research area, which also summarizes the main results of the work. In the design of millimeter-wave active and passive components the main focus is on realized CMOS components and techniques for pushing nanoscale CMOS circuits beyond 100 GHz. Test structures for measuring and analyzing these components are shown. Topologies for a coplanar waveguide, microstrip line, and slow-wave coplanar waveguide that are suitable for implementing transmission lines in nanoscale CMOS are presented. It is demonstrated that the proposed slow-wave coplanar waveguide improves the performance of the transistor-matching networks when compared to a conventional coplanar waveguide and the floating slow-wave shield reduces losses and simplifies modeling when extended below other passives, such as DC decoupling and RF short-circuiting capacitors. Furthermore, wideband spiral transmission line baluns in CMOS at millimeter-wave frequencies are demonstrated. The design of amplifiers and a wideband resistive mixer utilizing the developed components in 65-nm CMOS are shown. A 40-GHz amplifier achieved a +6-dBm 1-dB output compression point and a saturated output power of 9.6 dBm with a miniature chip size of 0.286 mm^2. The measured noise figure and gain of the 60-GHz amplifier were 5.6 dB and 11.5 dB, respectively. The V-band balanced resistive mixer achieved a 13.5-dB upconversion loss and 34-dB LO-to-RF isolation with a chip area of 0.47 mm^2. In downconversion, the measured conversion loss and 1-dB input compression point were 12.5 dB and +5 dBm, respectively. The design and experimental results of low-noise and power amplifiers are presented. Two wideband low-noise amplifiers were implemented in a 100-nm metamorphic high electron mobility transistor (HEMT) technology. The amplifiers achieved a 22.5-dB gain and a 3.3-dB noise figure at 94 GHz and a 18-19-dB gain and a 5.5-7.0-dB noise figure from 130 to 154 GHz. A 60-GHz power amplifier implemented in a 150-nm pseudomorphic HEMT technology exhibited a +17-dBm 1-dB output compression point with a 13.4-dB linear gain. In this thesis, the main system-level aspects of millimeter-wave transmitters and receivers are discussed and the experimental circuits of a 60-GHz transmitter front-end and a 60-GHz receiver with an on-chip analog-to-digital converter implemented in 65-nm CMOS are shown. The receiver exhibited a 7-dB noise figure, while the saturated output power of the transmitter front-end was +2 dBm. Furthermore, a wideband W-band transmitter front-end with an output power of +6.6 dBm suitable for both image-rejecting superheterodyne and direct-conversion transmission is demonstrated in 65-nm CMOS.

Keywords balun, CMOS, low-noise amplifier, millimeter-wave receiver, millimeter-wave transmitter, MMIC, power amplifier, resistive mixer, slow-wave shield, transmission line

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Millimetriaaltoalueen monoliittisten aktiivi- ja passiivikomponenttien, vähäkohinaisten vahvistimien, tehovahvistimien, resistiivisten sekoittimien ja radioetupäiden suunnittelu ja karakterisointi

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Tiivistelmä

Tässä väitöskirjassa on tutkittu millimetriaaltoalueen integroituja aktiivi- ja passiivikomponentteja, vähäkohinaisia vahvistimia, tehovahvistimia, resistiivisiä sekoittimia ja radioetupäitä. Väitöskirja koostuu 11:sta julkaisusta sekä niistä laaditusta yhteenvedosta. Aktiivi- ja passiivikomponenttien suunnittelussa on keskitytty CMOS-komponentteihin ja piirisuunnitteluteknikoihin, joilla voidaan toteuttaa piirejä yli 100 GHz:n taajuuden käyttäen nanomittaluokan CMOS-teknologioita. Työssä on suunniteltu testipiirejä komponenttien mittauksia ja analysointeja varten. Työssä on esitetty koplanaariselle siirtojohdolle, mikroliuskalle ja hitaan aallon suojalla toteutetulle koplanaariselle siirtojohdolle rakenteet, joita voidaan käyttää nanomittaluokan CMOS-teknologioissa. Työssä on demonstroitu, että hitaan aallon suojalla toteutettu koplanaarinen siirtojohto vähentää transistorien sovituspiirien häviöitä verrattuna koplanaariseen siirtojohtoon. On myös osoitettu, että hitaan aallon suojan ulottaminen muiden passiivisten komponenttien alle vähentää häviöitä ja yksinkertaistaa mallinnusta millimetriaaltoalueella. Työssä demonstroidaan CMOS-teknologioilla toteutettujen kierukkasiirtolinjamuuntajien käyttöä millimetriaaltoalueella. Esitetyillä komponenteilla on suunniteltu vahvistimia ja laajakaistainen balansoitu resistiivinen sekoitin käyttäen 65 nm:n CMOS-teknologiaa. 40 GHz:n vahvistimesta mitattiin lähdön yhden dB:n kompressiopisteeksi 6 dBm:n tehotaso ja saturaatiotehoksi 9,6 dBm. Piirin pinta-ala on 0,286 mm^2. 60 GHz:n vahvistimen kohinaluvuksi mitattiin 5,6 dB:ä ja vahvistukseksi 11,5 dB:ä. V-alueen sekoittimen sekoitusvaimennukseksi mitattiin 13,5 dB:ä ylössekoituksessa ja lokaalivaimennukseksi RF-portissa 34 dB:ä. Piirin pinta-ala on 0,47 mm^2. Alassekoitusvaimennukseksi mitattiin 12,5 dB:ä ja tulon yhden dB:n kompressio-pisteeksi 5 dBm:n tehotaso. Työssä esitetään millimetriaaltoalueen vähäkohinaisten vahvistimien ja teho-vahvistimien suunnittelua. Kaksi laajakaistaista vähäkohinaista vahvistinta suunniteltiin ja toteutettiin 100 nm:n metamorfisella HEMT-teknologialla. Vahvistimien vahvistukseksi mitattiin 22,5 dB:ä 94 GHz:n taajuudella ja 18-19 dB:ä taajuusalueella 130-154 GHz:ä. Vastaavat mitatut kohinaluvut olivat 3,3 ja 5,5-7,0 dB:ä. Tehovahvistimen lähdön yhden dB:n kompressiopisteeksi mitattiin 17 dBm:n tehotaso ja vahvistukseksi 13,4 dB:ä. Vahvistin toteutettiin 150 nm:n pseudomorfisella HEMT-teknologialla. Työssä käsitellään millimetriaalto-alueen lähettimiä ja vastaanottimia systeemitasolla ja esitellään 65 nm:n CMOS-teknologialla toteutettujen 60 GHz:n ja W-alueen lähettimien sekä 60 Ghz:n vastaanottimen, joka sisältää analogiadigitaalimuuntimen, suunnittelu. Vastaanottimen kohinaluvuksi mitattiin 7 dB:ä ja 60 GHz lähettimen lähtötehoksi 2 dBm.

Asiasanat CMOS, hitaan aallon suoja, millimetriaaltoalueen lähetin, millimetriaaltoalueen vastaanotin, MMIC, resistiivinen sekoitin, siirtojohto, symmetrointimuuntaja, tehovahvistin, vähäkohinainen vahvistin

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Preface

The work for this thesis was carried out in the Electronic Circuit Design Laboratory of Helsinki University of Technology during 2001-2009. The work was funded by the Finnish Funding Agency for Technology and Innovation (Tekes) under the Nastec, Brawe, and LALAMO projects, by the Academy of Finland under the Millimono and UNCMOS projects and the Centre of Excellence program (SMARAD2), the Graduate School in Electronics, Telecommunication and Automation (GETA), by the European Space Agency, by Nokia Research Center, by Nokia Networks, and by Ylinen Electronics. I would like to thank the Nokia Foundation, Walter Ahlström Foundation, HPY Research Foundation, Ulla Tuominen Foundation, the Finnish Society of Electronics Engineers (EIS), and Telealan edistämissäätiö for awarding scholarships for my postgraduate studies.

I would like to thank my supervisor, Professor Kari Halonen, for the opportunity to write this thesis and encouragement during the study. I wish to thank both Professor Kari Halonen and emeritus Professor Veikko Porra for the opportunity to work on this interesting research area. I warmly thank Professor Henrik Sjöland and Professor Patrick Reynaert for reviewing my thesis.

I have been fortunate to work on many interesting research projects among very talented research engineers. The excellent research results reported in this thesis have been result of collaborative work and I am grateful to all co-authors for their valuable work. Especially, I wish to thank my colleague Mikko Kärkkäinen for managing the projects, which gave me the opportunity to concentrate on the research work and writing my thesis. I also thank D.Sc. Pekka Kangaslahti for instructing me in the early stage of my studies, advice during the research, and reading this thesis. I appreciate the work of Jan Riska in the area of MMIC design. It has inspired me in my own research. I am grateful to Dan Sandström for fruitful collaboration. I also thank Professor Jussi Ryynänen for advice, useful discussions about MMIC design, and good company during several conference trips. All the staff at the Electronic Circuit Design Laboratory deserves thanks for creating a pleasant working atmosphere. I warmly thank Ville Saari, Tero Tikka, Pasi Juurakko, and Mikko Kärkkäinen for sharing the same office with me in a good team spirit.

I wish to thank my friends for giving me something else to think than the research on electronics. The friendship that we share and our freetime activities have been playing important part in completing this thesis. I am grateful to my mother and Veikko, my grandparents and my parents-in-law for encouragement and support during my studies. Finally, I would like to thank my lovely wife Essi. Without her support I would never have been able to finish this work. Writing this thesis would have been a real burden without her and my daughter Emmi bringing sunshine to my life.

Espoo, April 2010

Mikko Varonen

Contents

List of Publications

This thesis is based on the work presented in the following papers:

[P1] M. Varonen, M. Kärkkäinen, M. Kantanen, and K. A. I. Halonen, ”Millimeter-wave integrated circuits in 65-nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 43, no. 9, pp. 1991-2002, Sep. 2008.

[P2] M. Kärkkäinen, M. Varonen, D. Sandström, T. Tikka, S. Lindfors, and K. A. I. Halonen, “Design aspects of 65-nm CMOS MMICs,” in *Proc. of the 3rd European Microwave Integrated Circuits Conference*, Amsterdam, the Netherlands, Oct. 2008, pp. 115-118.

[P3] D. Sandström, M. Varonen, M. Kärkkäinen, and K. A. I. Halonen, “60 GHz amplifier employing slow-wave transmission lines in 65-nm CMOS,” accepted to be published in *International Journal on Analog Integrated Circuits and Signal Processing*.

[P4] D. Sandström, M. Varonen, M. Kärkkäinen, and K. A. I. Halonen, “W-band CMOS amplifiers achieving +10dBm saturated output power and 7.5dB NF,” *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3403-3409, Dec. 2009.

[P5] D. Sandström, M. Varonen, M. Kärkkäinen, and K. A. I. Halonen, “A W-band 65nm CMOS transmitter front-end with 8GHz IF bandwidth and 20dB IR-ratio,” in *IEEE International Solid-State Circuits Conference Dig.*, San Francisco, CA, Feb. 2010, pp. 418-419.

[P6] M. Varonen, M. Kärkkäinen, J. Riska, P. Kangaslahti, and K. A. I. Halonen, “Resistive HEMT mixers for 60-GHz broadband telecommunication,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 4, pp. 1322-1330, April 2005.

[P7] M. Varonen, M. Kaltiokallio, V. Saari, O. Viitala, M. Kärkkäinen, S. Lindfors, J. Ryynänen, and K. A. I. Halonen, “A 60-GHz CMOS receiver with an on-chip ADC,” in *IEEE International Radio Frequency Integrated Circuits Symposium Dig.*, Boston, MA, June 2009, pp. 445-448.

[P8] M. Kärkkäinen, M. Varonen, D. Sandström, and K. A. I. Halonen, “60-GHz receiver and transmitter front-ends in 65-nm CMOS,” in *IEEE International Microwave Symposium Dig.*, Boston, MA, June 2009, pp. 577-580.

[P9] M. Varonen, M. Kärkkäinen, M. Kantanen, M. Laaninen, T. Karttaavi, R. Weber, A. Leuther, M. Seelmann-Eggebert, T. Närhi, J. Lahtinen, and K. A. I. Halonen, ”W-band low-noise amplifiers,” *Proceedings of the European Microwave Association*, vol. 3, issue 4, pp. 358-366, Dec. 2007.

[P10] M. Kantanen, M. Kärkkäinen, M. Varonen, M. Laaninen, T. Karttaavi, R. Weber, A. Leuther, M. Seelmann-Eggebert, T. Närhi, J. Lahtinen, and K. A. I. Halonen, ”Low noise amplifiers for D-band,” *Proceedings of the European Microwave Association*, vol. 4, issue 4, pp. 268-275, Dec. 2008.

[P11] M. Kärkkäinen, M. Varonen, P. Kangaslahti, and K. A. I. Halonen, “Integrated amplifier circuits for 60 GHz broadband telecommunication,” *International Journal on Analog Integrated Circuits and Signal Processing*, vol. 42, no. 1, pp. 37-46, January 2005.

Author's contribution

Paper [P1] was mainly contributed by the author. The author was responsible for writing the manuscript. The author designed all the test structures for the passive and active components. The topology for the conventional coplanar waveguide and the core capacitor was designed by the author and M. Kärkkäinen in co-operation. The author designed the slow-wave coplanar waveguide, the spiral transmission line balun, both amplifiers, and the mixer. The measurements of the S-parameters, the noise parameters of the transistor, the noise figures, and the power sweeps of the amplifiers, to which the author contributed, were carried out in the Millimetre Wave Laboratory of Finland. The author was responsible for the measurement setup and the measurements of the mixer. The analysis of the transistor S-parameter data was carried out by the author and M. Kärkkäinen in co-operation. M. Kärkkäinen was responsible for extracting the noise parameters of the transistor and the de-embedding of the S-parameters of the capacitor. Otherwise, the author is responsible for the analysis in the manuscript.

Paper [P2] is a result of collaborative work. The author contributed substantially to the writing of the manuscript. The electromagnetic simulations of the transmission lines were performed by D. Sandström under the instruction of the author and M. Kärkkäinen. The author designed the amplifier presented in the paper. The test structure was designed and the transistor was analyzed by the author in co-operation with T. Tikka. The measurements, to which the author contributed, were carried out in the Millimetre Wave Laboratory of Finland.

Paper [P3] is a result of collaborative work. The author contributed to the writing of the manuscript. The amplifier was designed by D. Sandström under the instruction of the author. The microstrip line was designed and the results analyzed by D. Sandström under the instruction of the author. The noise performance of the amplifier was simulated using the de-embedded transistor data calculated by M. Kärkkäinen. The models of the other active and passive components are based on the work presented in [P1].

Paper [P4] is a result of collaborative work. The author contributed to the writing of the manuscript. The two amplifiers were designed by D. Sandström under the instruction of the author. The author designed the test structures for the transmission lines. The author had the main responsibility for the analysis of the results of the transmission lines in co-operation with

D. Sandström. The original idea of extending the slow-wave shield under the other passives and under the capacitor was the author's. The realization of the shield under the capacitor was carried out by D. Sandström in co-operation with the author. M. Kärkkäinen was responsible for the realization and the analysis of the slotted plate capacitor in co-operation with D. Sandström. The models of the other active and passive components and the matching arrangement of the amplifiers are based on the work presented in [P1]. The measurements were carried out in the Millimetre Wave Laboratory of Finland.

Paper [P5] is a result of collaborative work. The author contributed to the writing of the manuscript. The author was responsible for the system-level design of the transmitter front-end. The circuit-level design of the transmitter front-end was carried out by D. Sandström and the author in co-operation. The measurements were carried out in the Millimetre Wave Laboratory of Finland.

Paper [P6] is a result of collaborative work. The author was responsible for writing the manuscript. J. Riska designed the circuits presented in this paper. The author was responsible for building the measurement setup and for the measurements and the analysis presented in the paper. M. Kärkkäinen contributed to the analysis of the measurement results.

Paper [P7] is a result of collaborative work. The author participated in the writing of the manuscript. The system-level analysis of the receiver was carried out by the author, M. Kaltiokallio and Prof. J. Ryynänen in co-operation. The author designed and implemented the millimeter-wave front-end for the receiver. The interface between the millimeter-wave front-end and the IF circuitry was designed and implemented by the author in co-operation with M. Kaltiokallio. M. Kaltiokallio designed and implemented all the IF circuits in co-operation with Prof. J. Ryynänen. V. Saari and O. Viitala designed and implemented the low-pass filter and the analog-to-digital converter, respectively, both in co-operation with Prof. S. Lindfors. The author participated in the building of the measurement setup and the measurements.

Paper [P8] is a result of collaborative work. The author was responsible for the design of the transmitter front-end and the amplifier for the receiver front-end. The spiral transmission line balun used in both front-ends is based on the work presented in [P1]. M. Kärkkäinen was

responsible for the downconverter mixer design. The author was responsible for the transmitter front-end measurements. The author wrote Chapters III, IV and V B.

Paper [P9] is a result of collaborative work. The author contributed to the writing of the manuscript. The author designed the wideband low-noise amplifier chip (LNA2) and participated in the on-wafer S-parameter measurements which were carried out in the Millimetre Wave Laboratory of Finland.

Paper [P10] is a result of collaborative work. The author designed the wideband low-noise amplifier chip (LNA3) and participated in the on-wafer S-parameter measurements, which were carried out in the Millimetre Wave Laboratory of Finland.

Paper [P11] is a result of collaborative work. The author designed the power amplifier chip. The power amplifier was packaged by Ylinen Electronics. The author was responsible for the power amplifier measurements, which were carried out in the Millimetre Wave Laboratory of Finland. The author wrote Chapter 4. Chapters 1, 2, and 5 were written by the author in co-operation with M. Kärkkäinen.

List of Abbreviations

AC	alternating current
ADC	analog-to-digital converter
ADPD	antiparallel diode pair
AlSb	aluminum antimony
AM	amplitude modulation
APPF	active poly-phase filter
ASK	amplitude shift-keying
BB	baseband
BiCMOS	bipolar complementary metal oxide semiconductor
C	carbon
CAD	computer-aided design
CG	conversion gain
CMOS	complementary metal oxide semiconductor
CPW	coplanar waveguide
CS	common source
DAC	digital-to-analog converter
DAT	distributed active transformer
DC	direct current
DFE	decision feedback equalizer
DSB	double sideband
ESD	electrical static discharge

FDD	frequency domain duplexing
FET	field-effect transistor
GaAs	gallium arsenide
GCPW	grounded coplanar waveguide
HEMT	high electron mobility transistor
I	in-phase
IF	intermediate frequency
InAs	indium arsenide
InP	indium phosphide
IR	image rejection
LNA	low-noise amplifier
LO	local oscillator
LPF	low-pass filter
LTCC	low temperature co-fired ceramic
MB-OFDM	multi band orthogonal frequency division multiplexing
MHEMT	metamorphic high electron mobility transistor
MIM	metal-insulator-metal
MMIC	monolithic microwave integrated circuit
MSG	maximum stable gain
NF	noise figure
OFDM	orthogonal frequency division multiplexing
OOK	on-off keying
PA	power amplifier

PCB	printed circuit board
PGA	programmable gain amplifier
PHEMT	pseudomorphic high electron mobility transistor
PLL	phase-locked loop
PM	phase modulation
Q	quadrature-phase
RC	resistor-capacitor
RF	radio frequency
SHP	subharmonically pumped
SiGe	silicon germanium
SOI	silicon on insulator
TDD	time-domain duplexing
TIA	transimpedance amplifier
USB	universal serial bus
UWB	ultra-wideband
VCO	voltage-controlled oscillator
VGA	variable gain amplifier

List of Symbols

B	bandwidth
BB_I	baseband in-phase
BB_Q	baseband quadrature-phase
C	shunt capacitance per unit length
C_{gd}	gate-to-drain capacitance
C_{gs}	gate-to-source capacitance
$e_{n,out}$	output noise voltage
F	noise factor
f_{max}	maximum frequency of oscillation
F_{min}	minimum noise factor
f_t	cut-off frequency
F_{tot}	total noise factor
G	shunt conductance per unit length
G	power gain
g_{ds}	drain-to-source conductance
g_m	transconductance
H	distance between the signal line and ground plane
ICP_{1dB}	1-dB input compression point
I_d	drain current
$IDAC$	current-steering digital-to-analog converter
I_{max}	saturation current

I_{swing}	current swing
k	Boltzmann's constant
K	empirical fitting factor
L	series inductance per unit length
OCP_{1dB}	1-dB output compression point
PAE_{max}	maximum power added efficiency
P_{DC}	power consumption
P_{sat}	saturated output power
Q_C	capacitive quality factor
Q_L	inductive quality factor
Q_{res}	self-resonance quality factor of a transmission line
R	series resistance per unit length
R_{ch}	channel resistance
R_{ds}	drain-to-source resistance
R_g	gate resistance
r_n	equivalent normalized noise resistance
R_{opt}	optimum load line resistance
R_s	source resistance of a transistor
R_S	source resistance
S	signal-to-ground spacing
S_{11}	input match
SNR_{in}	signal-to-noise ratio at the input
SNR_{out}	signal-to-noise ratio at the output

T	absolute temperature
V_{brk}	device breakdown voltage
V_d	drain voltage
V_{dd}	supply voltage
V_g	gate voltage
V_{knee}	transistor knee voltage
V_{out}	output signal voltage
V_S	source voltage
V_{swing}	voltage swing
W	width of the center conductor
Z_0	input impedance
Z_L	load impedance
Z_{driver}	output match for the driver
Z_{even}	even-mode impedance
Z_{load}	output match
Z_{odd}	odd-mode impedance of the quarter-wave transformer
α	attenuation per unit length
β	phase delay
λ	wavelength
ρ_{opt}	optimum reflection coefficient
ρ_s	source reflection coefficient
ω	angular frequency

1 Introduction

The millimeter-wave region of the electromagnetic spectrum covers the wavelengths from 10 millimeters to 1 millimeter, which corresponds to radio frequencies of 30 to 300 GHz. Applications for this frequency band vary from scientific satellites to commercial high-data-rate wireless transfers. The most promising millimeter-wave consumer applications are expected to utilize the unlicensed band around 60 GHz since it offers up to 7 GHz of bandwidth, which makes possible various high-bandwidth applications such as the wireless transmission of uncompressed high-definition video streams and the wireless replacement of wired interconnections for example USB 3.0. Other applications include point-to-point links at 60 GHz and in the E-band (71-76 GHz, 81-86 GHz) as well as collision avoidance car radars at 77 GHz. Applications above and around 100 GHz include radar, wideband communication, environmental monitoring, and millimeter-wave active and passive imaging at the atmospheric windows at 94, 140, and 220 GHz. The imaging applications include for example atmospheric radiometers, airport safety in landing and taxiing, the detection of concealed weapons and explosives, and high-resolution collision avoidance car radars.

The monolithic microwave integrated circuit (MMIC) technology enables the fabrication of low-cost, high-performance, highly reliable, small-sized, and light-weight millimeter-wave radios. By using MMICs the production of millimeter-wave systems is feasible in large quantities with a high yield. Millimeter-wave integrated circuits have traditionally been implemented using technologies which are based on compound semiconductors such as gallium arsenide (GaAs) or indium phosphide (InP). Recently, there has been enormous development in the field of silicon integrated circuits operating at millimeter-wave frequencies. Circuits and subsystems have been demonstrated in silicon germanium (SiGe) and complementary metal oxide semiconductor (CMOS) technologies even beyond 100 GHz. However, the high electron mobility transistor (HEMT) technology provides the best high-frequency noise, gain, and output power performance. An example application where optimum performance is required is atmospheric water vapor profiling using a radiometer for simultaneous measurements at the water vapor resonance frequency of 183 GHz and at a window frequency within 140 to 165 GHz. In the current generation of atmospheric sounders, a heterodyne radiometer architecture is used with Schottky mixers as the first component after the antenna. The sensitivity of these instruments could be improved with an HEMT low-noise amplifier. Silicon-based technologies

have the potential to enable front-end, baseband, analog-to-digital and digital-to-analog converters, and digital signal processing circuitry to be integrated on a single chip. When targeting high-volume commercial applications, for example, in the 60-GHz band, CMOS technology can provide the highest integration level at low cost when produced in large volumes.

1.1 Objectives and contents of this thesis

Regardless of the MMIC technology, appropriate transceiver architectures, circuit topologies, and circuit design methods must be selected and developed to take full advantage of the potential of the chosen technology and to meet the requirements of the target application. This thesis focuses on the design and characterization of active and passive MMIC components and the circuit design of integrated low-noise and power amplifiers, resistive mixers, and radio front-ends for millimeter-wave applications.

In the first part of this thesis, an overview of the research area is given and the main results of the work are summarized. In Chapter 2, the design of active and passive millimeter-wave components are discussed. The main focus is on realized CMOS components and techniques for pushing nanoscale CMOS beyond 100 GHz. Furthermore, test structures for measuring and analyzing these components are shown. In Chapter 3, the design of millimeter-wave low-noise and power amplifiers and the experimental results of amplifiers implemented in GaAs pseudomorphic and metamorphic HEMT and 65-nm CMOS are shown. Chapter 4 concentrates on the design and experimental results of resistive mixers. In Chapter 5, the main system-level aspects of millimeter-wave transmitters and receivers are discussed and the experimental circuits of a 60-GHz transmitter front-end and single chip 60-GHz receiver implemented in 65-nm CMOS are shown. Furthermore, a wideband W-band transmitter front-end suitable for both image-rejecting superheterodyne and direct conversion transmission is demonstrated. The main contributions of this work are summarized in the chapter on Conclusions.

The second part of this thesis contains the published papers, where the theoretical and experimental results of this research work are reported.

2 Millimeter-wave active and passive components

2.1 Design flow for millimeter-wave circuits in CMOS

Millimeter-wave integrated circuits have traditionally been implemented using compound semiconductor technologies such as gallium arsenide or indium phosphide. For these technologies circuit models have been available for basic active and passive components in standard computer-aided design (CAD) packages. The foundries or institutions have developed their own compact models which enable accurate simulations well beyond 100 GHz [1]. However, active and passive millimeter-wave models for CMOS components are not readily available. Because of the lossy silicon substrate, thin dielectric layers above the substrate, and metal density requirements of CMOS technologies, the traditional models, for example, for transmission lines, metal-insulator-metal (MIM) capacitors, or resistors are not applicable for circuit design. Furthermore, the available models for transistors in CMOS are limited to RF frequencies [2]. Therefore, a systematic approach is needed for developing models that take into account the distributed effects and the challenges in CMOS described above. We used the design flow shown in Fig. 1, which resulted in state-of-the-art performance for the first design cycle circuits.

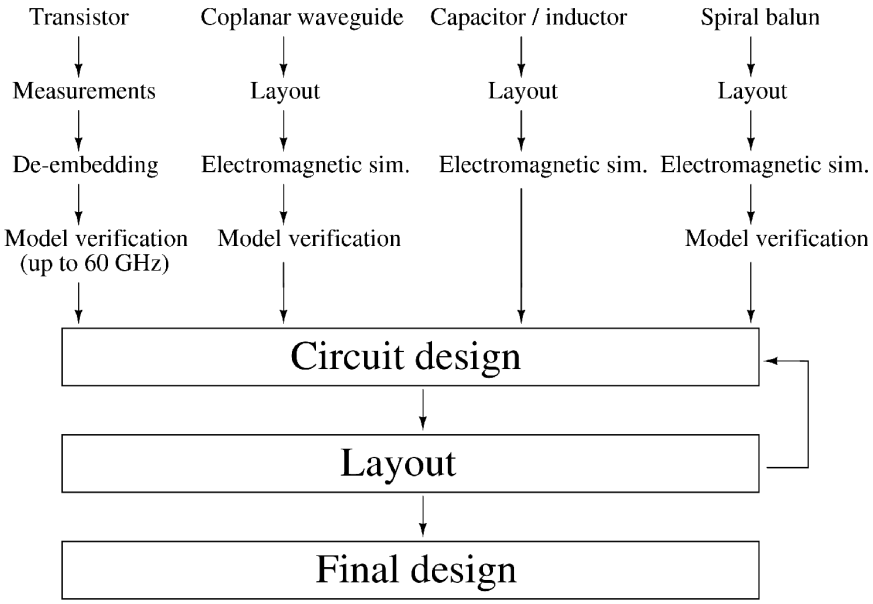

Fig. 1. Design flow for successful first design cycle in CMOS.

The flow includes preliminary test transistor measurements, electromagnetic simulations and parasitic extractions to capture the high-frequency behavior of the transmission lines, capacitors, and, balun structures and the circuit design of the amplifiers and mixers. We also included test structures in the first run for the accurate verification of the active and passive components. Using the data of these test structures, we have been able to design CMOS circuits beyond 100 GHz, with state-of-the-art results.

2.2 Transmission lines in CMOS

Equation-based models derived for microwave transmission lines are not applicable for lines integrated on silicon substrates. The models typically assume thin conductors, ground planes which are far from the signal lines, and high-quality dielectrics [3]. Furthermore, thin dielectric layers above the substrate of a CMOS technology and stringent metal density requirements set limitations for implementing transmission lines on silicon. In Papers [P1] and [P2], we presented topologies for a coplanar waveguide (CPW), microstrip line, and slow-wave coplanar waveguide that are suitable for implementing transmission lines in nanoscale CMOS. Furthermore, test structures were developed for these lines and, to the best of the author's knowledge, we were the first to present measurement results for a slow-wave coplanar waveguide in 65-nm CMOS. We also showed that the proposed slow-wave CPW improves the performance (i.e. reduce losses) of the transistor-matching networks when compared to a conventional coplanar waveguide.

2.2.1 Coplanar waveguide in CMOS

A way to realize a conventional coplanar waveguide in nanoscale CMOS was proposed in [P1] and is shown in Fig. 2. The top metal layer is used for the center conductor. Although it is possible to design transmission lines that allow dummy metal filling around the signal conductor [4], in our case, dummy metal is not allowed around the center conductor or in between the ground planes of the CPW at any metal level. On the other hand, the metal density requirement has to be fulfilled, which means that there has to be enough metal at all metal levels. This is accomplished by strapping all the other metal layers together with vias to form the ground plane for the CPW. The width of the center conductor W and the signal-to-ground spacing S can be used for realizing different characteristic impedances for the CPW. A wider

center conductor leads to lower conductor losses. In principle, the maximum width of the center conductor is limited by the layout design rules of the chosen process. The metal density requirements set the limits for the maximum signal-to-ground spacing for the CPW. The unwanted slotline mode can be suppressed by connecting the ground planes of the CPW together around the discontinuities using the lower metal layers. In this way the ground planes at the opposite sides of the center conductor remain at the same potential.

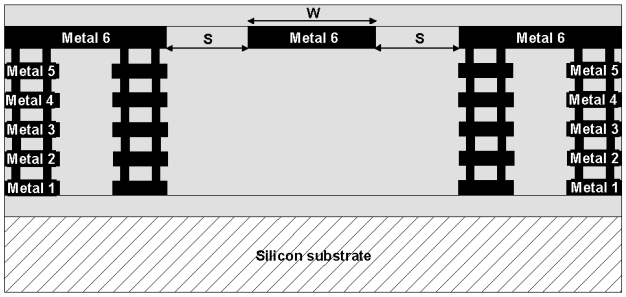

Fig. 2. Simplified cross-section of the conventional coplanar waveguide (© 2008 IEEE, with permission from [P1]).

2.2.2 Microstrip line in CMOS

The microstrip line is realized between the top metal and lower metal planes. This isolates the effect of the lossy silicon substrate. The removal of dummy metal from both underneath and in the vicinity of the center conductor can create a metal density problem. A way to realize a microstrip line in a CMOS technology was proposed in [5] and is shown in Fig. 3.

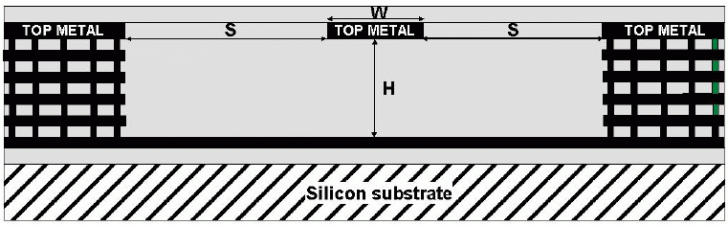

Fig. 3. Simplified cross-section of the microstrip line with sidewalls (© 2008 EuMA, with permission from [P2]).

Adding ground planes similar to a CPW line fulfills the metal density requirements. These ground planes are then connected together using lower metal planes. Because of the metal density requirements the wide ground plane on the lower metal level must have longitudinal slots which do not interfere with the longitudinal ground currents of the microstrip line. When the distance between the signal line and ground plane *H* is rather low and when the side ground planes are located far from the center conductor, the signal propagates mostly in microstrip mode.

2.2.3 Slow-wave coplanar waveguide in CMOS

In the conventional coplanar waveguide, presented above, the electromagnetic field penetrates into the silicon substrate, which increases losses. A metal shield structure can be drawn using the lowest metal levels to prevent the electromagnetic fields from penetrating into the lossy silicon substrate. An efficient way to realize the shield is a slow-wave structure employing floating shield strips [6]. A simplified cross-section of the slow-wave coplanar waveguide proposed in [P1] is shown in Fig. 4. The two lowest metal layers are strapped together with vias to form the floating shield strips. The shield is designed using minimum design rules, i.e. minimum metal strip width and spacing, in order to suppress the induced current flow in the direction of the propagating RF signal. This minimizes the ohmic losses and maximizes the reactive energy storage per unit length. The smallest allowable shield strip spacing minimizes the exposure of the overlying CPW to the conductive substrate.

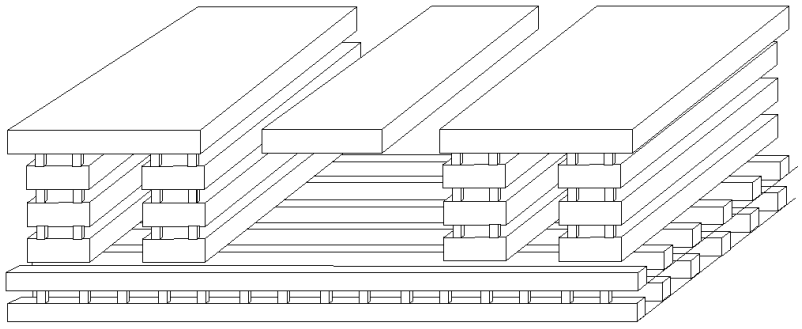

Fig. 4. Simplified cross-section of the slow-wave coplanar waveguide. The two lowest metal layers are strapped together with vias to form the floating shield strips (© 2008 IEEE, with permission from [P1]).

In addition to shielding the substrate, the dielectric constant and thus the wavelength of the slow-wave CPW are adjustable by changing the signal-to-ground spacing, allowing more compact implementation of transmission lines for impedance transformation and phase-shifting applications [6]. The electromagnetic simulation of the slow-wave CPW is challenging, typically time consuming, and memory intensive. Different methods have been developed for accurate and fast electromagnetic simulations of slow-wave CPWs in CMOS [7], [8]. To characterize slow-wave CPWs and on-chip transmission lines, we developed on-wafer test structures for the lines.

2.2.4 Characterization of transmission lines in CMOS

A test structure for a conventional CPW is shown in Fig. 5.

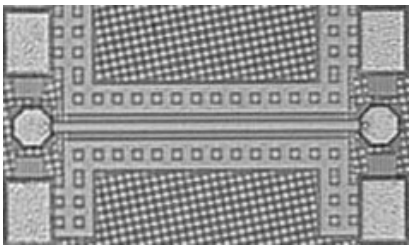

Fig. 5. Test structure for the conventional CPW in 65-nm CMOS (© 2008 IEEE, with permission from [P1]).

The self-resonance quality factor Q_{res} of a transmission line can be calculated using the attenuation per unit length α and the phase delay along the line β. The inductive and capacitive quality factors (Q_L and Q_C) can be calculated from the distributed transmission line parameters, series resistance per unit length R, series inductance per unit length L, shunt conductance per unit length G, and shunt capacitance per unit length C. These are related to the self-resonance quality factor according to the following equation [9]:

$$\frac{1}{Q_{res}} \approx \frac{2\alpha}{\beta} \approx \frac{1}{Q_L} + \frac{1}{Q_C} = \frac{R}{\omega L} + \frac{G}{\omega C} \quad . \tag{1}$$

The ground plane of the microstrip line is an effective substrate shield, but it is located very close to the signal line yielding to a very small distributed inductance. This significantly degrades the inductive quality factor which is a more important figure of merit when transmission lines are used to resonate with the intrinsic capacitances of the transistors [9]. The technology scaling even exacerbates the problem, since the distance between the signal line and ground plane typically decreases. This means that a narrower line width is needed for a high-impedance line. This will increase the metal losses of the signal line, degrading the inductive quality factor even more. Furthermore, the ground plane of the microstrip produces more metal losses since it has to be realized using thinner lower metal layers rather than the thick top metal layer in the case of the coplanar waveguide. Since the coplanar waveguide offers a higher inductive quality factor, it seems to be an appealing transmission-line topology for transistor-matching networks [9]. Furthermore, the substrate losses can be minimized by using a slow-wave shield. Although it is difficult to compare transmission lines with different impedances, the measurement results showed that the attenuations for the conventional and slow-wave CPW with characteristic impedances of 45 Ω and 35 Ω are 2.8 dB/mm and 1.1 dB/mm at 60 GHz, respectively, and that the Q_{res} was improved by a factor of three. This suggests that the shielding of the substrate is effective in the case of the structure that was realized [P1]. It was also found that the substrate shielding of the proposed slow-wave coplanar waveguide is as effective as with the microstrip topology [P3]. Since the substrate is shielded, the capacitive quality factor is increased and the impedance of the line is reduced when compared to a conventional CPW with the same *W* and *S*. However, in this case, the inductive quality factor remains the same, as the signal-to-ground spacing is the same in both topologies. In order to have the same impedances for the conventional and slow-wave CPW, the signal-to-ground spacing of the slow-wave CPW can be increased. The measurement results in [P4] suggest that both the inductive quality factor and the capacitive quality factors will then be higher for the slow-wave CPW. Thus, in our case the use of slow-wave CPW with the same characteristic impedance as the conventional CPW should improve the performance (i.e. reduce losses) of the transistor matching networks. However, it should be noted that the slow-wave CPW has a more limited range of feasible characteristic impedances compared to a conventional coplanar waveguide. This is because the capacitance per unit length is increased, whereas the inductance is the same as for a conventional CPW with the same *W* and *S*. For a high impedance slow-wave CPW line the signal-to-ground spacing should be increased or the width of the signal line should be decreased. However, the signal-to-ground spacing is limited by the design rules and the width of the center conductor by metallic losses.

2.3 Capacitors in CMOS

On-chip capacitors are needed for DC decoupling and implementing an RF short circuit for shunt matching stubs. Two types of capacitor structures are usually used in MMIC circuits: a metal-insulator-metal (MIM) capacitor or a finger (interdigital) capacitor. MIM capacitors consist of two metal plates with a thin dielectric between them. The fabrication of the MIM capacitors typically requires an additional process step in CMOS. Finger capacitors can be realized in any modern CMOS process. They consist of many narrow fingers in parallel using all the available metal layers.

When CPWs are used for matching the capacitors should be implemented in a CPW environment, as shown in Fig. 6, where simplified layouts for DC decoupling and RF short-circuiting capacitors are shown. A micrograph of a CPW test structure for the series capacitor is shown in Fig. 7.

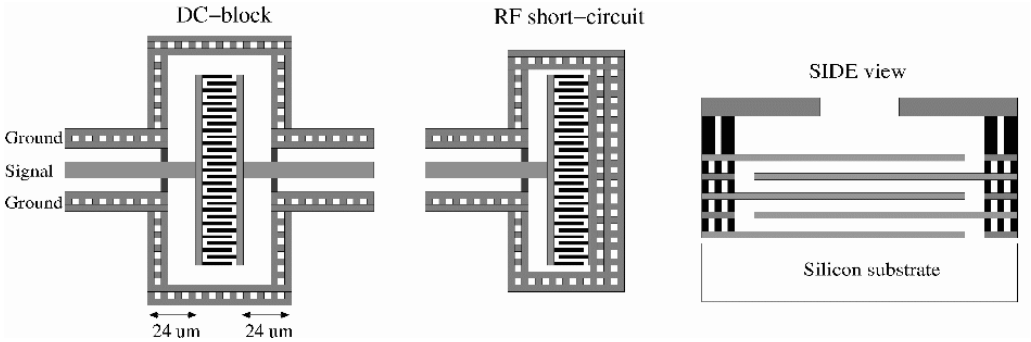

Fig. 6. Simplified layouts of a DC decoupling capacitor (left) and RF short-circuiting capacitor (middle) implemented using finger capacitors.

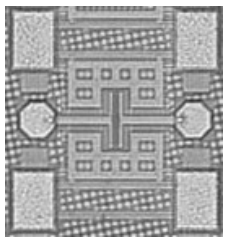

Fig. 7. Test structure for the series capacitor in 65-nm CMOS (© 2008 IEEE, with permission from [P1]).

The close proximity of the silicon substrate of the capacitor structures described above induces losses and complicates the modeling. By extending the slow-wave shield below the capacitors, as shown in Fig. 8, the frequency-dependent substrate effects of the matching networks can be almost completely removed. As a result, the substrate losses of these passives become minimal. Furthermore, at millimeter-wave frequencies the modeling of passive structures becomes more accurate as the complicated substrate effects are negligible. In Paper [P4] we presented a custom-designed plate capacitor utilizing a slow-wave shield. As the floating shield effectively reduces substrate losses and coupling, the capacitor model can be obtained from the RC-parasitic extraction tool. Furthermore, the MIM capacitor can be modeled simply by using the foundry model, which utilizes a metal shield. In the simulations, the shield node is floating and the access to the MIM is modelled with slow-wave CPWs [P5].

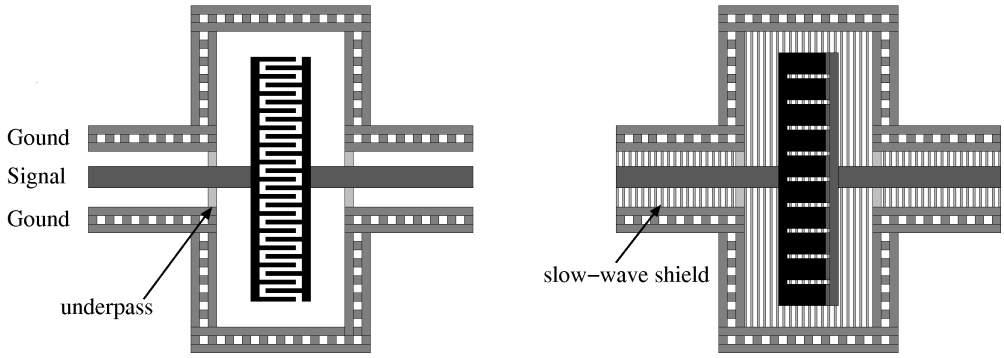

Fig. 8. Simplified presentation of a standard finger capacitor in the CPW environment on left and the modified capacitor structure with a slow-wave shield in the slow-wave CPW environment on right (© 2009 IEEE, with permission from [P4]).

2.4 Spiral transmission line baluns

At millimeter-wave frequencies the integration of a transformer or a balun is feasible. A spiral transmission line transformer is a compact and wide-bandwidth balun. The use of spiral transmission line transformers has been shown to be a successful solution in microwave mixer circuits [10]. In Paper [11], compact-sized spiral baluns were utilized in millimeter-wave frequency doubler circuits. In Paper [P6], we demonstrated how to employ and analyze spiral transmission line baluns at the V-band. In addition, we presented a wide band and a compact

method for the transition from even to odd mode with in-phase power division by feeding the signal from a coplanar waveguide input to two spiral transmission line baluns. The use of transformers in silicon technologies at millimeter-wave frequencies is a relatively new subject of study [12]. To the best of the author's knowledge, we were the first to demonstrate spiral transmission line baluns in CMOS at millimeter-wave frequencies [P1]. We also utilized the even-to-odd mode transition with in-phase power division described above for the LO signal in CMOS at 100 GHz [P5].

The balun is used for matching the input impedance Z_0 of the circuit to the impedances Z_L of the loads. The circuit is properly matched, providing that the electrical length of the coupled lines in the odd mode is $\lambda/4$ at the design frequency and the odd-mode impedance Z_{odd} of the quarter-wave transformer is

$$Z_{odd} = \sqrt{2 Z_L Z_0} \quad . \tag{2}$$

For the signal to propagate in the odd mode, the balun has to suppress the even-mode propagation. This means that the even-mode impedance Z_{even} has to be as high as possible. The even-mode impedance can be increased by wrapping the balun in a spiral, as explained in [10]. The spiral has a minimal effect on the odd-mode impedance. In practice, the number of turns of the spiral is limited by the parasitic capacitance, which may cause undesired resonances.

The electromagnetic analysis of the balun can be divided into two parts, as proposed in [10]. The even-mode characteristic impedance is evaluated from the electromagnetic simulation of a spiral inductor in which the lines of the balun are joined. The odd-mode impedance and the effective permittivity can be modeled by calculating the odd-mode properties of a straight section of coupled lines. Because of the semi-insulating substrate of compound semiconductor technologies, such as GaAs, this analysis is quite straightforward, since the return currents of the balun in both modes are well defined. In the even propagation mode the return current flows through the backside metallization, whereas in CMOS the return currents of a complicated circuit may not be explicit. In general, the return current in even propagation mode can flow through the lossy substrate or through a lower impedance return current path, for example, through other metallization layers connected between the source and load. However, at millimeter-wave frequencies the return current will flow underneath the structure because the

path has lower inductance [13]. Fig. 9 presents the simulated even-mode impedance of a straight section of coupled lines on CMOS and GaAs substrates used in this work. The even-mode impedance of the CMOS line is higher which is beneficial for the balun design.

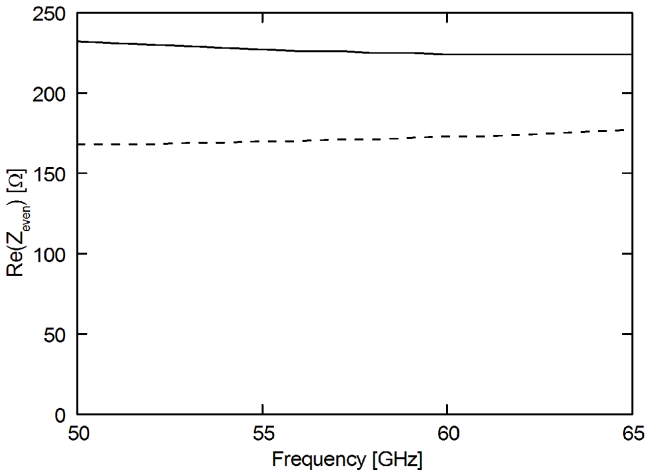

Fig. 9. Simulated even-mode impedance of a straight section of coupled lines on CMOS and GaAs (dashed line) substrates. The odd mode impedance for both lines is around 60 Ω.

The CMOS balun was verified by measuring it on-wafer in a back-to-back test structure shown in Fig. 10. The measured insertion loss including pads was less than 5 dB from 50 to 60 GHz; thus, less than 2.5 dB for a single balun including a pad. The result is comparable to insertion losses of transformers published in [12] and [14]. Furthermore, the balun was used in a balanced resistive mixer [P1], [P7], [P8] and in an active mixer [P8]. The simulations and measurements of these circuits were in excellent agreement, which suggests that the design methodology chosen for the balun is successful.

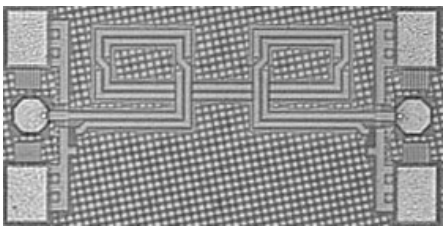

Fig. 10. Test structure for the balun (© 2008 IEEE, with permission from [P1]). The chip area utilized is 0.57 mm x 0.30 mm.

In Paper [P1], we presented a transition from CPW to the balun in a deep submicron CMOS. As shown in Fig. 11, the balun is fed from a coplanar waveguide input. To ensure a proper excitation for the balun, the ground planes of the CPW are connected together with lower metal layers at the transition point from CPW to the spiral balun. In order to prevent the DC from being grounded, multiple finger capacitors are used in parallel at the ground connection of the spiral balun.

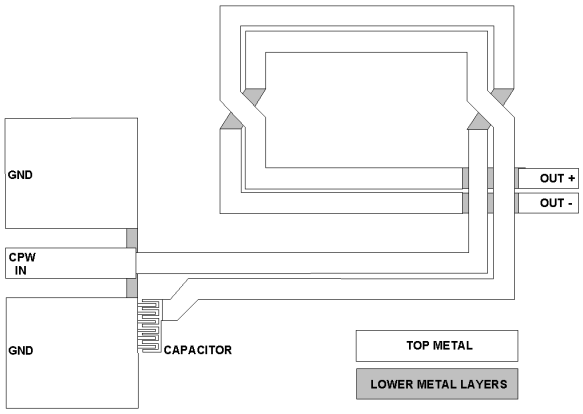

Fig. 11. Principle layout of the spiral balun and the transition from CPW input to the balun (© 2008 IEEE, with permission from [P1]).

2.5 Transistor layout considerations for millimeter-wave operation

The transistor sizing is critical at millimeter-wave frequencies and the performance depends greatly on how the layout is drawn, since the influence of the parasitics become more dominant at millimeter-wave frequencies. Furthermore, the chosen technology has an influence on the optimal layout of the transistor. The simplified equations for the maximum frequency of oscillation f_{max}, and maximum stable gain *MSG* calculated from the transistor small-signal equivalent circuit shown in Fig. 12 can be used for evaluating the effect of parasitics on the gain performance of a transistor [15], [16]:

$$f_{max} \approx \frac{f_t}{2\sqrt{(R_g + R_s)(g_{ds} + 2\pi f_t C_{gd})}} \tag{3}$$

$$MSG \approx \sqrt{\left(\frac{g_m}{\omega C_{gd}}\right)^2 + 1} \approx \frac{g_m}{\omega C_{gd}} \tag{4}$$

where g_m, R_g, R_s, C_{gd}, and g_{ds} are the transconductance, gate and source resistances, gate-to-drain capacitance, and drain-to-source conductance, respectively. $f_t = g_m/[2\pi(C_{gs}+C_{gd})]$ is the cut-off frequency, where C_{gs} is the gate-to-source capacitance.

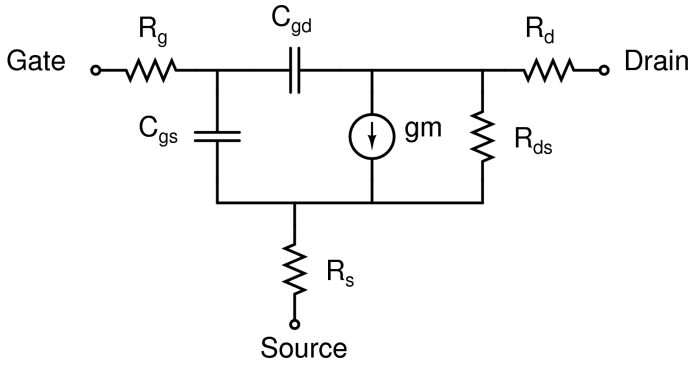

Fig. 12. Simplified small-signal equivalent circuit for a field-effect transistor (FET).

Because of the metal gates of HEMTs a few fingers of wide devices can be used to obtain a very high f_T and f_{max} for the transistor. Since polysilicon gates are used in CMOS-technology the width of the fingers must be kept short to minimize the gate resistance [13]. Because the minimum noise factor F_{min} is a function of the gate resistance, as shown in Fukui's equation, minimizing this parasitic is of great importance [17]:

$$F_{min} = 1 + K\,\omega\,C_{gs}\sqrt{\frac{R_g + R_s}{g_m}} \tag{5}$$

In Eq. (5), K is an empirical fitting factor. Fig. 13 shows a way to realize a common source transistor [P4], [18]. Several narrow fingers (around 1 um) are connected in parallel and the gates are connected on both sides to minimize the gate resistance. The drain and source are fed from opposite sides to minimize C_{gd}. As can be seen from Equations 3 and 4 this will improve both the *MSG* and f_{max}.

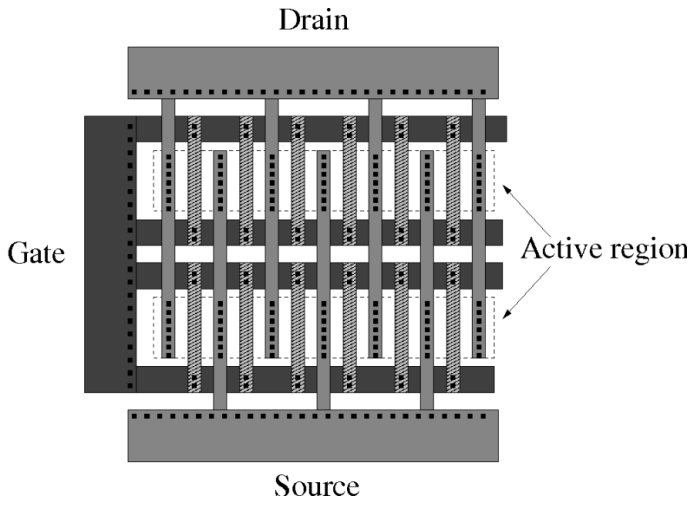

Fig. 13. Simplified layout of a multifinger transistor using double-contacted gates and two parallel devices in CMOS (© 2009 IEEE, with permission from [P4]).

Furthermore, as we use the transistor in a coplanar waveguide environment, the positioning of the gate, drain, and source access lines in this way gives the designer an opportunity to place a matching stub directly at the drain, as shown in Fig. 14. This is important, because adding even a short series line at the drain node will easily result in a low impedance point, which complicates the matching. For higher current swings, multiple fingers can be used in parallel to obtain high output power with a low supply voltage. However, the gate width cannot be increased arbitrarily as low-loss wideband matching may become unfeasible. This will be discussed in more detail in Chapter 3.

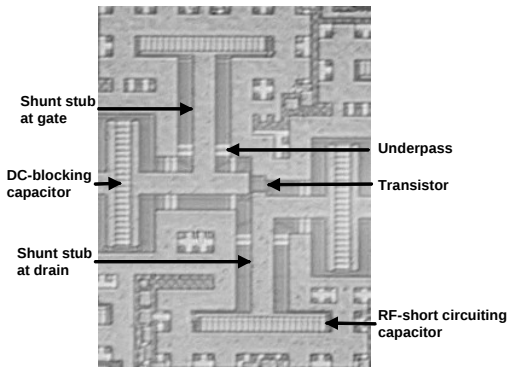

Fig. 14. Micrograph of a part of a transistor matching arrangement (© 2009 IEEE, with permission from [P4]).

2.5.1 Transistor de-embedding structures for millimeter-wave frequencies in CMOS

To capture the millimeter-wave behavior of a CMOS transistor, a coplanar waveguide test-structure for the transistor and the corresponding open and short structures for the de-embedding were developed [19]. A micrograph of the test structure is shown in Fig. 15.

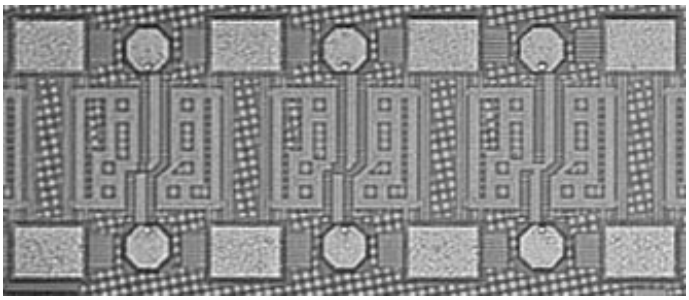

Fig. 15. Coplanar test structure including open (middle) and short (right) structures for measuring a transistor (left) in CMOS.

Based on the transistor test structure data [P1], we have been able to design circuits such as amplifiers beyond 100 GHz [P4].

3 Millimeter-wave amplifier design

In a transmitter, a power amplifier is needed to amplify the transmitted signal to a sufficient power level with reasonable linearity and efficiency. The gain, noise, and intermodulation properties of the low-noise amplifier have a strong influence on the receiver performance. At millimeter-wave frequencies the gain of a single transistor is relatively low. Therefore, there is little margin, with power amplifiers, for trade-off between linearity, output power, gain, and efficiency. Because of the low gain, the noise contribution of the following stages becomes significant. Therefore, in a low-noise amplifier several stages have to be cascaded in order to make the noise produced in the following blocks low enough when the total system noise figure is calculated. The requirements for the power and low-noise amplifiers are determined by the intended system and its system specifications. Power amplifiers and low-noise amplifiers as part of millimeter-wave systems are discussed in more detail in Chapter 5. In this chapter the focus is on the circuit-level design of these blocks.

3.1 Millimeter-wave low-noise amplifier design

The noise factor is defined as:

$$F = \frac{SNR_{\text{in}}}{SNR_{out}} = \frac{V_S^2/(4\,k\,T\,B\,R_S)}{V_{out}^2/e_{n,out}^2} \quad , \tag{6}$$

where SNR_{in} and SNR_{out} are the signal-to-noise ratios at the input and output, V_S is the source voltage, V_{out} and $e_{n,out}$ are the output signal and output noise voltages, k is the Boltzmann's constant, B is the bandwidth, and R_S is the source resistance. The Friis equation can be used for calculating the noise factor of the cascaded blocks [20]:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_n - 1}{\prod_{i=1}^{n-1} G_i} \tag{7}$$

where F_n and G_n are the noise factor and available power gain of the n^{th} stage. From Equation 7 it can be seen that to minimize the total noise figure *NF* (*NF=10log(F)*) the gain of the first block should be high so as to reduce the noise contribution of the following stages. However, at high frequencies the gain of a single transistor is relatively low, as shown in Fig. 16. Therefore, in a millimeter-wave low-noise amplifier several stages have to be cascaded in order to make the noise produced in the following blocks low enough when the total system noise figure is calculated.

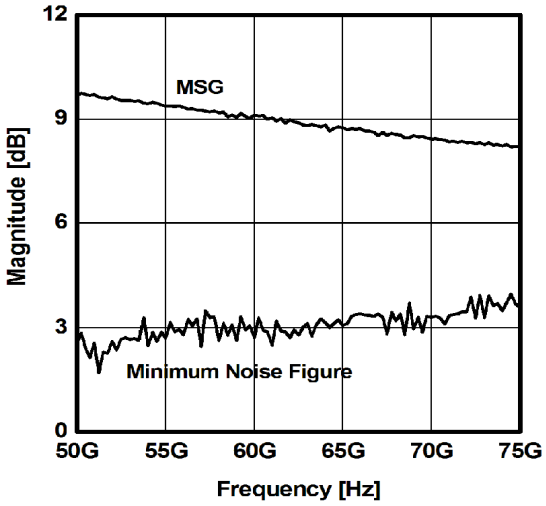

Fig. 16. Measured maximum stable gain and minimum noise figure of a W/L=90/0.07-sized transistor in 65-nm CMOS at V-band (data from [P1]).

The minimum noise figure of a two-port can be obtained by selecting the source reflection coefficient properly. For a two-port and a transistor the noise factor can be expressed as [21]:

$$F = F_{min} + 4 r_n \frac{|\rho_s - \rho_{opt}|^2}{(1-|\rho_s|^2)|1+\rho_{opt}|^2} \quad , \tag{8}$$

where r_n is the equivalent normalized noise resistance, ρ_s is the source reflection coefficient, and ρ_{opt} is the optimum reflection coefficient when the noise factor reaches its minimum value F_{min}. In general, matching the input of the transistor to the minimum noise figure does not lead to maximum gain for the transistor. Therefore, in the design of a low-noise amplifier there is a

trade-off between the noise, gain, and return loss. This is illustrated in Fig. 17, where the noise circles and the available gain circles of a 90/0.07-sized CMOS transistor are plotted on a Smith chart.

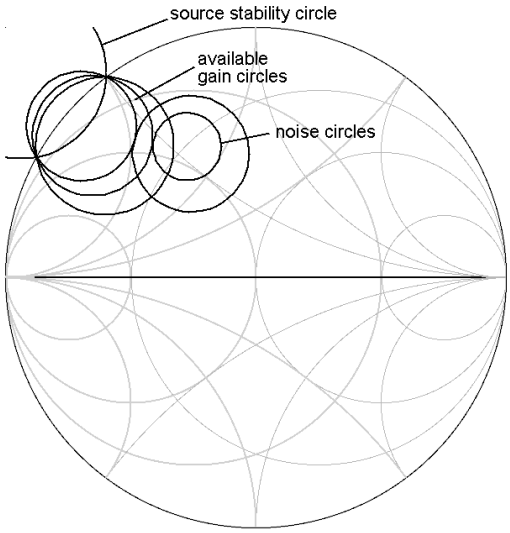

Fig. 17. Available gain circles and noise circles of a 90/0.07-sized CMOS transistor are plotted for the 7, 8, and 9 dB and 3.1 and 3.4 dB levels, respectively (data from [P7]).

Feedback can be used for bringing the conjugate of S_{11} and ρ_{opt} closer together. In a series feedback an inductor is placed between the FET source contact and ground. The conjugate of S_{11} depends on both the series feedback and the output loading, whereas ρ_{opt} is only affected by the feedback inductor. This means that by selecting a proper combination of the output loading and feedback inductor the minimum noise figure and conjugate match can be obtained simultaneously [22]. The series feedback reduces the gain and improves the stability.

3.1.1 Experimental results of millimeter-wave low-noise amplifiers

Two low-noise amplifiers for the W-band and D-band were designed [P9], [P10], [23], [1] and fabricated in a 100-nm GaAs-based metamorphic HEMT technology from Fraunhofer IAF, Freiburg, Germany. The simulation models were provided by Fraunhofer IAF. The simplified schematic and chip micrograph of the D-band amplifier are presented in Fig. 18 and Fig. 19, respectively. Both amplifiers were designed for wideband performance and flat gain response.

This was realized by using reactive matching elements implemented in grounded coplanar waveguides (GCPW) and using a double-resonance technique for interstage matching. The input is matched using a 30-Ω series line and a short-circuited shunt stub. The interstage matching can be divided into two parts. The drain of the transistor is loaded with a long 50-Ω series line and a short circuited shunt stub. The interstage matching is completed with a quarter-wavelength 30-Ω series line and a short-circuited shunt stub. Inductive series feedback is used in every stage to stabilize the amplifiers.

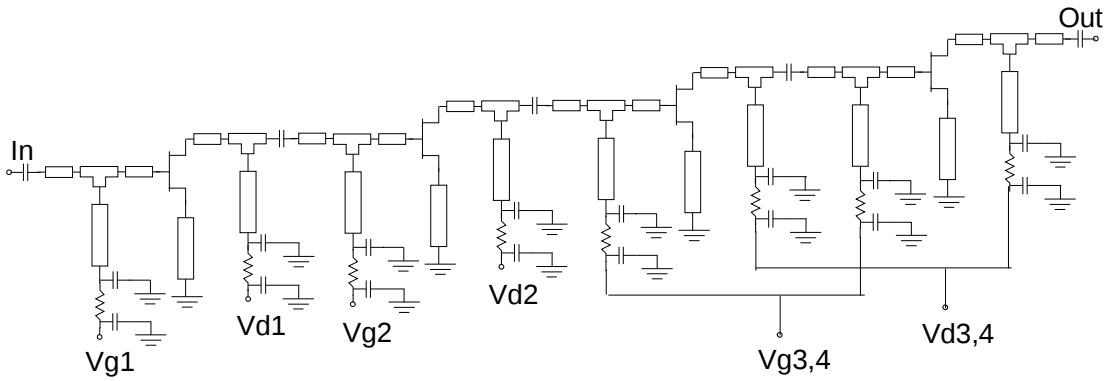

Fig. 18. Simplified schematic of the D-band amplifier.

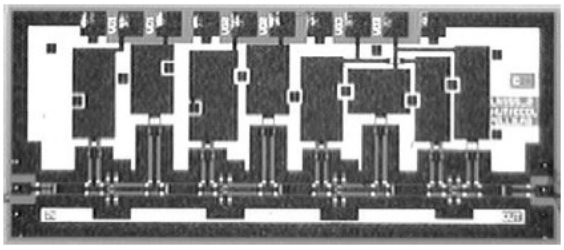

Fig. 19. Micrograph of the D-band amplifier. The chip size is 1.00 mm x 2.25 mm.

A comparison of published W-band and D-band HEMT MMIC amplifiers is presented in Table 1 and Table 2, respectively. The measured results demonstrate excellent noise and gain performance. In addition, both amplifiers were packaged in a split block package and the W-band packaged amplifier was measured at cryogenic temperatures.

Table 1. Comparison of published HEMT MMIC amplifiers for W-band.

Frequency [GHz]	Gain [dB]	NF [dB]	Technology	Ref.
95	20	2.5	InP HEMT	[24]
94	18	2.9	InP HEMT	[25]
94	33	3.2	130-nm InP HEMT	[26]
94	16	3.2	100-nm InP HEMT	[27]
94	12	3.3	100-nm InP HEMT	[28]
94	19.4	2.5	100-nm InP HEMT	[29]
65-86	26-30	3.1	35-nm InP HEMT	[30]
90	17	2.8	GaAs MHEMT	[31]
89	14	4.8	100-nm GaAs MHEMT	[32]
80-100	12	2.3	70-nm GaAs MHEMT	[33]
70-105	20	2.5	70-nm GaAs MHEMT	[34]
80-100	20	2.5	70-nm GaAs MHEMT	[35]
94	31	4.0	100-nm GaAs low noise PHEMT	[36]
90-100	10.3	3.6	100-nm GaAs power PHEMT	[37]
94	11	5.4	100-nm InAs/AlSb HEMT	[38]
94	20	3.9	200-nm InAs/AlSb HEMT	[39]
94	22.5	3.3	100-nm GaAs MHEMT	[P9]

Table 2. Comparison of published HEMT MMIC amplifiers for D-band.

Frequency [GHz]	Gain [dB]	NF [dB]	Number of Stages	Technology	Ref.
160	16	3.6	3	35-nm InP HEMT	[40]
150-220	18-26	-	3	50-nm InP HEMT	[41]
150-215	12	-	3	70-nm InP HEMT	[42]
150-215	20±6	8	6	80-nm InP HEMT	[43]
150-205	17±2	-	8	100-nm InP HEMT	[44]
140	30	-	3	100-nm InP HEMT	[45]
90-140	15±3	-	6	100-nm InP HEMT	[46]
150	5	-	1	120-nm InP HEMT	[47]
164	6	-	2	70-nm InP PHEMT	[48]
120-124	10-12	-	2	100-nm InP PHEMT	[49]
142	9	-	2	100-nm InP PHEMT	[50]
155	10.1	5.1	3	100-nm InP PHEMT	[51]
148	12	-	2 cascode stages	150-nm GaAs PHEMT	[52]
155-160	15	-	2 cascode stages	70-nm GaAs MHEMT	[53]
140-160	20	4.5	4	70-nm GaAs MHEMT	[35]
180-220	16	4.8	4	50-nm GaAs MHEMT	[54]
130-154	18.0-19.0	5.5-7.0	4	100-nm GaAs MHEMT	[P10]

3.2 Millimeter-wave power amplifiers

In power amplifier design, a suitable load impedance is presented to the transistor for delivering maximum output power. The maximum output power of a device in Class A can be derived from the load line theory [55]. The optimum load line can be calculated from the I-V characteristics of the transistor, as shown in Fig. 20. The maximum output power of a FET is delivered to the load when the output current I_{swing} and voltage swings V_{swing} are maximized. The optimum load line resistance R_{opt} is therefore

$$R_{opt} = \frac{V_{swing}}{I_{swing}} = \frac{V_{brk} - V_{knee}}{I_{max}} = \frac{2(V_{dd} - V_{knee})}{I_{max}} \tag{9}$$

It can be seen that the maximum voltage swing of a FET is limited by the device breakdown voltage V_{brk} and the transistor knee voltage V_{knee}. If the supply voltage V_{dd} is fixed, it might limit the swing. As the V_{brk} (or the V_{dd}, according to the specifications of the system) is fixed for each process, a larger current swing is needed to achieve higher output power. The current swing can be increased by using a larger device. This can be accomplished by placing identical devices in parallel. In principle, increasing the device size this way does not affect the gain performance of the transistor. However, the increased parasitics of the realized FET start to reduce the gain of the device and eventually, when the size of the device becomes significant when compared to the wavelength, the phase errors between the gate fingers start to reduce the gain performance.

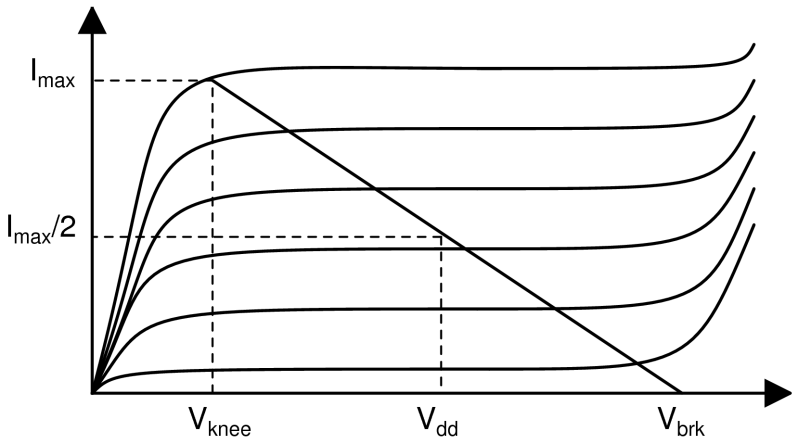

Fig. 20. I-V-characteristics and optimum load line of a FET.

Furthermore, a larger device has a lower output impedance, which makes the design of the output match difficult. As a result, the total width of the transistor cannot be increased arbitrarily as low-loss wideband matching becomes difficult. Therefore, at millimeter-wave frequencies the parasitics of the transistor have to be taken into account when the appropriate size for the transistor is being chosen. In a load-pull technique the power performance of the transistor is measured or simulated for different output impedances. As shown in Fig. 21, this technique takes the device parasitics into account and gives the designer the opportunity to trade off between the output power and gain performance and also the matching conditions.

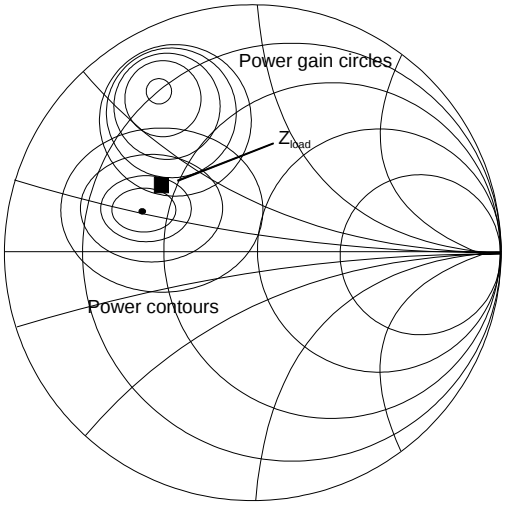

Fig. 21. Simulated power contours using 0.2-dB steps, power gain circles using 0.3-dB steps, and the output match Z_{load} for a 6x35-µm PHEMT chosen for the 60-GHz power amplifier presented in [P11] (© 2004 Springer Science + Business Media, Inc., with kind permission of Springer Science and Business Media).

Since the gain of the single transistor is low at millimeter-wave frequencies, several stages have to be cascaded in order to achieve sufficient gain from the amplifier. The equation for the 1-dB output compression point OCP_{1dB} of cascaded stages can be used to calculate the distribution of the power gain and linearity in a multistage power amplifier:

$$\frac{1}{OCP_{1\mathrm{dB}}} = \frac{1}{OCP_{1\mathrm{dB},n}} + \frac{1}{OCP_{1\mathrm{dB},n-1}G_n} + \frac{1}{OCP_{1\mathrm{dB},n-2}G_nG_{n-1}} + \ldots + \frac{1}{OCP_{1\mathrm{dB},1}\prod_{i=2}^{n}G_i} \quad , (10)$$

where $OCP1_{dB,n}$ and G_n are the output compression point and power gain of the n^{th} stage. From Equation 10 it can be seen that when the size of the output stage is enlarged for higher output power the size of the driver and the gain stages have to be increased to ensure that these stages can drive the output stage into saturation. Since increasing the size of the transistor lowers the gain, as explained above, this leads to a low total gain for the millimeter-wave amplifier. This happens more abruptly when compared to a lower-frequency power amplifier, where a high output power and feasible gain are available from a large transistor [56]. In addition, to ensure that the most nonlinear effects come from the output stage, the preceding stages, i.e. the driver stages, have to run with some backoff. Traditionally, a 3-dB backoff is used [55]. This amount of backoff is typically too demanding at millimeter wave frequencies and, as shown in Fig. 22, lower backoff has to be used to achieve sufficient gain.

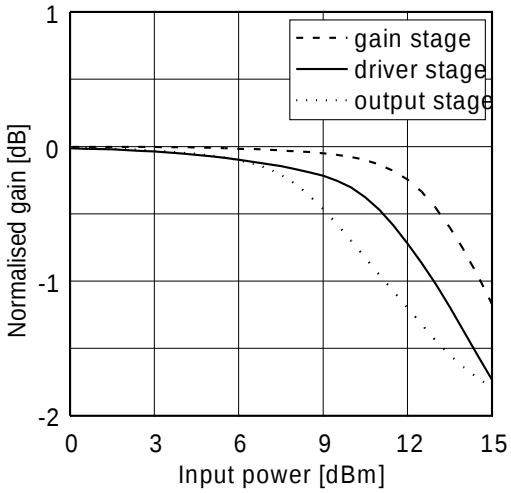

Fig. 22. Simulated gain compression of a three-stage power amplifier at 60 GHz. The gains are normalized (© 2004 Springer Science + Business Media, Inc., with kind permission of Springer Science and Business Media from [P11]).

To achieve a higher output power level without degrading the gain of the output stage, a large transistor can be divided into smaller devices and the power combined on-chip. There are several methods for power combining and they are well presented in the literature [57], [58]. A common technique is to use a Wilkinson combiner [59], in which the power is combined in-phase. The power can also be combined differentially using baluns or transformers. In a multistage amplifier, the use of transformers eliminates the need for AC coupling capacitors and

RF chokes, while differential operation reduces the amount of bypass capacitances needed [14]. In Paper [P11] and [60], we presented a 60-GHz three-stage single-ended power amplifier where the output consists of two cells. The power-combining principle is similar to a cluster matching technique [61]. In our design, we realize the output matching in two parts. As shown in Fig. 23, the 50-Ω load impedance is first converted to a lower impedance level and then the impedance at the power-combining point is matched to the desired impedance Z_{load} for the output transistors. As a result, a broadband output match is achieved. The input is matched in a similar way.

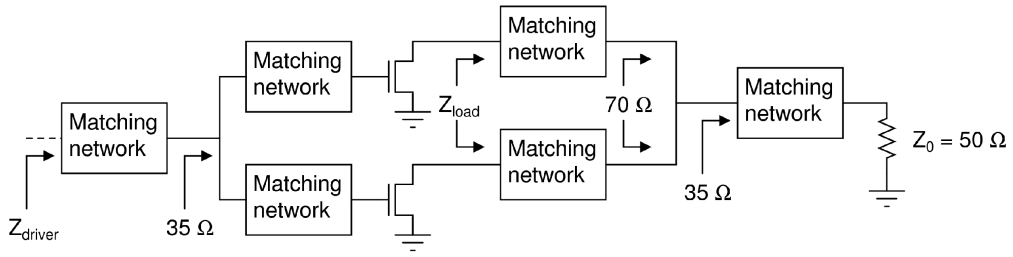

Fig. 23. Principle block diagram for realizing the output and input matching of the 60-GHz power amplifier.

The output matching circuitry is realized using series transmission lines and open shunt stubs, as presented in Fig. 24. At least in our case, this gave more freedom to choose the impedance levels during the design than using quarter-wave length transformers or Wilkinson power combiners. Furthermore, this led to smaller chip area. The power combining of the output stage may introduce a possible odd-mode oscillation problem. To suppress odd-mode oscillations, resistors can be added between the output cells [62]. The resistors for damping any odd-mode oscillations are shown in the simplified schematic in Fig. 24.

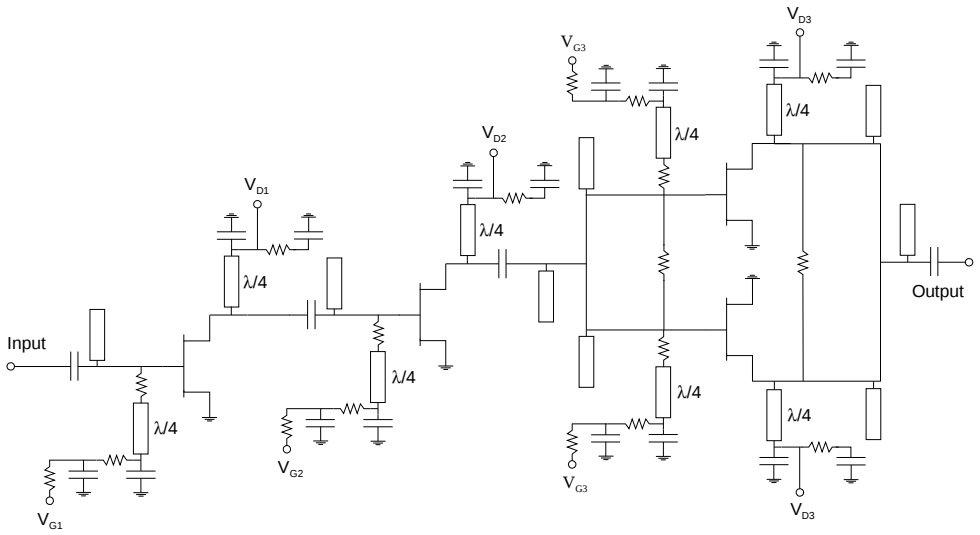

Fig. 24. Simplified schematic of the 60-GHz power amplifier (© 2004 Springer Science + Business Media, Inc., with kind permission of Springer Science and Business Media from [P11]).

3.2.1 Experimental results of the millimeter-wave power amplifier

The power amplifier was fabricated in a commercially available 0.15-µm GaAs pseudomorphic high electron mobility transistor (PHEMT) technology. The previous power amplifier design using a single transistor output stage presented in [63] and [64] showed that a 14-dBm 1-dB output compression point can be achieved using a single transistor output stage. The power amplifier in [P11] achieved a 1-dB output compression point 3 to 4 dB higher, which suggests that the chosen design methodology is successful. Furthermore, the chip was mounted in a split block package with WR-15 waveguide interfaces and alumina microstrip transitions. In addition, the packaged amplifier was assembled in a channel sounder [65]. We have also presented measured AM/PM results for both the packaged amplifier and the chip itself.

A comparison of recently published 60-GHz power amplifiers fabricated in different technologies is presented in Table 3. It can be seen that amplifiers manufactured in the GaAs and InP technologies provide the highest output power and SiGe designs achieve a saturated output power of more than 20 dBm. Because of the low breakdown voltage of scaled CMOS transistors, the design of CMOS power amplifiers is more challenging. Compared to the

published results, the power amplifier presented here achieves a good output power performance.

Table 3. Comparison of published 60-GHz power amplifiers.

Technology	Gain [dB]	OCP_{1dB} [dBm]	P_{sat} [dBm]	Power dissipation	PAE_{max} [%]	Topology	Area [mm^2]	Ref.
90-nm CMOS	5.6	9.0	12.3	1 V	8.8	2-stage differential CS	0.25	[14]
90-nm CMOS	14.3	10	11	150 mW @ 1.0 V	8.2	3-stage CS 2 cells output	0.18	[66]
90-nm CMOS	26	14.5	18	63 mW @ 3 V	12.2	DAT-combining	0.64	[67]
90-nm CMOS	15	10.2	12.5	84 @ 1.2 V	19.3	3-stage differential CS	0.15	[68]
90-nm CMOS	5.2	6.4	9.3	40 mW @ 1.5 V	7	3-stage CS	0.15	[69]
90-nm CMOS	10	8.8	12.6	213 mW @ 1 V	6.9	3-stage CS	0.64	[70]
90-nm CMOS	4.4	12.1	14.2	1 V	5.8	CS 4 cells output	1	[71]
90-nm CMOS	20	8.2	12	146 mW @ 1.2 V	9	4-stage 2 cells output	0.65	[72]
65-nm CMOS	15.8	2.5	11.5	43.5 mW @ 1.0 V	11	3-stage differential CS	0.053	[73]
45-nm CMOS	6	11	13.8	138 mW @ 1.1 V	7	2-stage differential CS	0.38	[74]
SiGe 0.25-µm BiCMOS	18.8	14.5	15.5	132 mW @ 3.3 V	19.7	2-stage cascode	0.795	[75]
SiGe 0.13-µm BiCMOS	20	-	23	1.2 W @ 4 V	6.3	DAT-combining	3.42	[76]
SiGe 0.13-µm BiCMOS	18	13.1	20	240 mW @ 4 V	12.7	Differential	0.975	[77]
SiGe:C 0.25-µm BiCMOS	24.8	17.2	18.9	800 mW @ 4 V	9.8	Differential cascode	0.58	[78]
0.15-µm GaAs PHEMT	-		28.5	-	31	-	-	[79]
0.15-µm GaAs PHEMT	17*	-	26	400 mW @ 5 V	24.5	2-stage 2 cells output	10.66	[80]
0.15-µm GaAs PHEMT	17	-	27.5	1.95 W @ 6 V	26	Balanced 3-stage	10.62	[81]
0.1-µm GaAs PHEMT	18.8	-	28.9	4.72 W @ 4 V	14.2	5-stage CS 8 cells output	16.1	[82]
0.1-µm GaAs PHEMT	13*	26*	27.5	-	21	Balanced 2-stage CS	10.35	[83]
0.1-µm InP HEMT	10.5*	-	23.5	3 V	43	Single stage 2 cells output	2.85	[84]
0.15-µm MHEMT	15	-	16	-	-	2-stage common source	2.5	[85]
0.12-µm MHEMT	10*	-	22.6	-	41.5	Single stage 2 cells output	2.85	[84]
0.15-µm GaAs PHEMT	13.4	17-18	24**	975 mW @ 3 V	24** (5.5 % @ OCP_{1dB})	3-stage common source 2 cells output	4.5	[P11]

* evaluated from the results presented in the publication

** simulated results

3.3 Millimeter-wave amplifier design in CMOS

The methods described in previous chapters for designing low-noise and power amplifiers are applicable for designing millimeter-wave CMOS amplifiers. In this chapter, the design of CMOS amplifiers and the effect of the circuit blocks that were developed are discussed.

3.3.1 Amplifier topology

Different topologies have been used for implementing millimeter-wave CMOS amplifiers [86], [87], [9], [69]. The cascode topology achieves good isolation, high gain, good stability, and low power consumption. As the operating frequency increases, the effect of the capacitances of the transistors becomes more pronounced. For example, resonating out the capacitances at the drain of the input transistor stage may improve performance. For a higher output power the supply voltage of the cascode topology can be increased from the nominal which is set by the process. By using a common source topology the output voltage and current swings can be maximized. Thus, a high output power and good linearity can be achieved when a relatively low supply voltage is used. Although the weak reverse isolation of the common source topology makes the design challenging, a low noise figure and good gain are feasible at millimeter-wave frequencies.

3.3.2 Impedance matching of millimeter-wave CMOS amplifiers

At millimeter-wave frequencies the distributed effects must be taken into account as part of the design process. For maximum power transfer impedance matching is needed and the parasitic capacitances and the intrinsic capacitances of the transistors must be resonated out by adding inductive elements to the matching networks. These small inductance values can be implemented with transmission lines, spiral inductors, or transmission line transformers. Even though spiral inductors have a better inductance-to-area ratio, they might be more challenging to model accurately. Scalable inductance values can easily be implemented with transmission lines, thus allowing a wide range of inductance values to be realized by adjusting the length of the line. The matching using transmission lines is illustrated in Fig. 25, where a simplified schematic of a 60-GHz CMOS amplifier presented in [P1] is shown. Series CPW-lines and

short-circuited CPW shunt stubs are used for input, output, and interstage matching. An open-ended shunt stub is used to complete the output match.

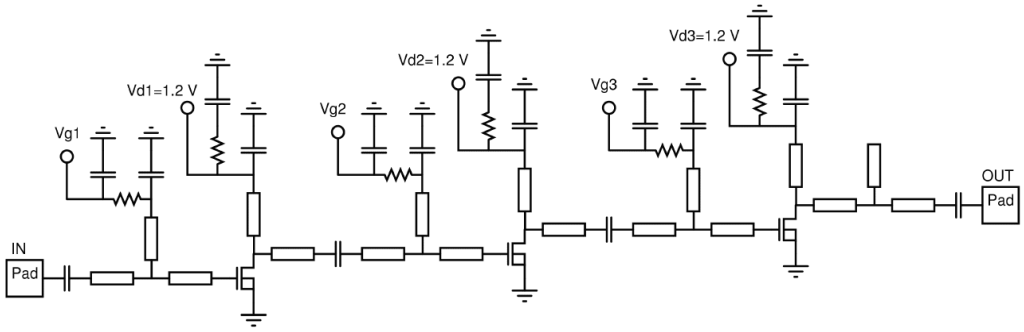

Fig. 25. Simplified schematic of the 60-GHz amplifier (© 2008 IEEE, with permission from [P1]).

The detailed input-matching principle of a low noise amplifier is shown in Fig. 26. Available gain circles, noise circles, and a source stability circle of a 90/0.07-sized transistor are plotted on the Smith chart at 60 GHz. As can be seen, all the passives have a strong influence on the matching and, for example, the effect of parasitic capacitances has to be well modeled.

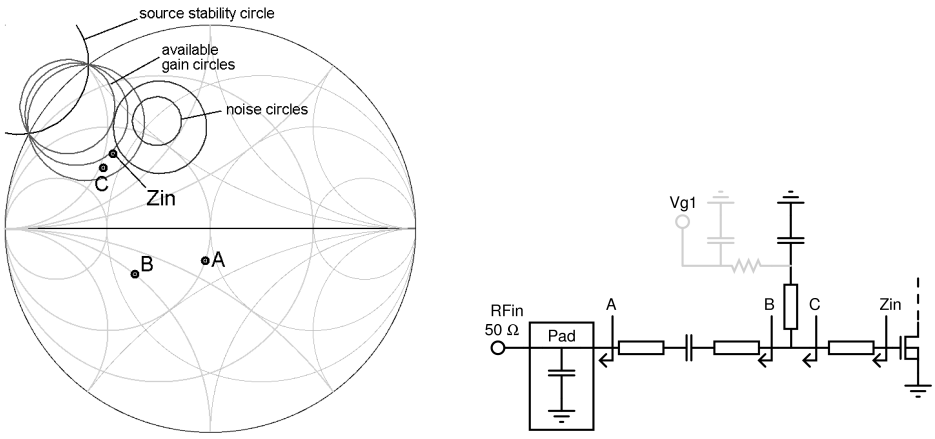

Fig. 26. Input-matching principle of the 60-GHz low noise amplifier (© 2009 IEEE, with permission from [P7]). Impedance after each circuit block is plotted on the Smith chart. The source stability circle and the designed input impedance are also shown. Available gain circles and noise circles of a 90/0.07-sized transistor are plotted for the 7, 8, and 9 dB and 3.1 and 3.4 dB levels, respectively.

3.3.3 Experimental results of millimeter-wave amplifiers in CMOS

The amplifiers were designed as stand-alone [P1] and as part of front-ends [P7], [P8]. In [88], the preliminary results of an 80-GHz amplifier implemented in 65-nm LP CMOS were presented. To the best of the author's knowledge, we were the first to present the detailed design and comprehensive measurement results of millimeter-wave amplifiers fabricated in 65-nm CMOS [89], [P1]. Furthermore, using the active and passive components and circuit design methods presented here, we have been able to design 100-GHz CMOS amplifiers with state-of-the-art results [P4], [90].

The measured performance of the 40-GHz amplifier is compared to previously published results in Table 4. The design achieves a good gain and high output power performance and small chip size when compared to the previously reported bulk CMOS designs. The measured performance of the 60-GHz amplifier is compared to previously published CMOS designs in Table 5. The design achieves a low noise figure and high output power.

Table 4. Performance comparison of CMOS amplifiers around 40 GHz.

CMOS process	Freq. [GHz]	Gain [dB]	NF [dB]	Area [mm^2]	OCP_{1dB} [dBm]	P_{sat} [dBm]	Power dissipation	Circuit topology	Ref
180-nm	40	7	-	2.04	-	10.4	100 mA @ 3 V	3-stage cascode	[91]
130-nm	43	20	6.3	0.525	4	8	24 mA @ 1.5 V	3-stage CS	[92]
130-nm	40	19	-	1.43	-0.9	-	24 mA @ 1.5 V	3-stage cascode	[9]
90-nm	40	6	-	0.7	-5.75	-	12.7 mA @ 1.5 V	2-stage CS	[93]
90-nm	33	18.6	3	0.856	1.6	-	8.3 mA @ 1.2 V	2-stage cascode	[94]
90-nm	44	13.5	-	0.7	7.5	10.6	66 mA @ 1.5 V	Balanced 2-stage CS	[95]
90-nm SOI*	35	11.9	3.6	0.18	4	-	17 mA @ 2.4 V	1-stage cascode	[87]
120-nm SOI*	40	14	3.6	-	-	-	16 mA 1.2 V	2-stage cascode	[96]
65-nm	42	14.3	6**	0.286	6	9.6	36/60 mA @ 1.2 V	2-stage CS	[P1]

* SOI: silicon on insulator

** at 50 GHz

Table 5. Performance comparison of CMOS amplifiers around 60 GHz.

CMOS technology	Freq. [GHz]	Gain [dB]	NF [dB]	OCP_{1dB} [dBm]	P_{sat} [dBm]	Power dissipation	Chip size [mm^2]	Ref
130-nm	56	24.7	7.1	1.8	5	72 mW @ 2.4 V	0.72 x 0.67	[97]
130-nm	60	12	8.8	2	-	54 mW 1.5 V	1.3 x 1.0	[9]
130-nm	60	20.2	7.2	-0.6*	5.2*	65 mW @ 2.4 V	0.72 x 0.67	[98]
130-nm	60	17.8	8.2	0.3	-	91.2 mW @ 2.4 V	1.1 x 0.69	[99]
90-nm	58	14.6	-	-	-	24 mW @ 1.5 V	0.35 x 0.40	[69]
90-nm	62	12.2	-	4	-	10.4 mW @ 1 V	-	[2]
90-nm	58	15	4.4	-	-	4 mW @ 1.3 V	0.44 x 320	[100]
90-nm	64	15.5	6.5	3.8	-	86 mW @ 1.65 V	1.3 x 0.4	[101]
90-nm	60	13	7-8	8	-	42 mW @ 1.2 V	0.7 x 0.43	[102]
65-nm	60	20.3**	7.6	-	-	37.2 mW @ 1.2 V	0.849 x 0.56	[103]
65-nm	60	15	5.9	0.6	-	31 mW @ 1.5 V	1.4 x 0.75	[104]
65-nm	60	22.3**	6.1	2.7	6	35 @ 1.2 V	0.46 x 0.46	[105]
65-nm	60	11.5	5.6	-	-	72 mW @ 1.2 V	0.87 x0.70	[P1]
65-nm	60	12.8	-	1.5	7	104 mW @ 1.2 V	0.87 x0.70	[P1]

* with ESD protection

**voltage gain

4 Millimeter-wave resistive mixer design

The mixer is one of the key components in a millimeter-wave transceiver. Early millimeter-wave mixers were based on Schottky barrier diodes [106]. FET mixers have been reported in both active and passive configurations. A relatively low conversion loss or even gain can be achieved with active topologies such as the single gate [107], [108], [109], the cascode [110], the balanced [86], [P8] and the Gilbert cell mixer [111], [112]. However, the linearity of these active mixers is low. The resistive mixer can achieve high linearity [113], [114]. Although the resistive mixer suffers from conversion loss, it has very low flicker noise, which is important in a direct conversion receiver [115]. Furthermore, the saved DC power can be used for adding an amplifier stage before the downconverting or after the upconverting mixer to compensate the conversion loss. Moreover, the resistive mixers can be designed for very wideband IF, RF, and LO performances, as presented in [P6], [P1].

4.1 Resistive mixer fundamentals

In a resistive FET mixer, the transistor is operated in its linear ohmic region, where the LO of the mixer is applied to the gate and used to pump the channel resistance of a FET, as shown in Fig. 27. In a shunt configuration, the source of the transistor is grounded and the IF (or RF) is applied to the drain and consequently the RF (or IF) is filtered from the drain.

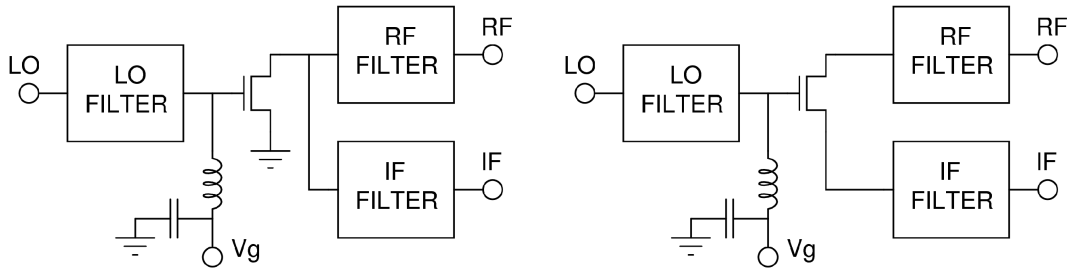

Fig. 27. The FET resistive mixer can be realized in a shunt configuration (left) or series configuration (right).

In a series configuration, the RF and IF are applied to the drain and source of the transistor. No drain DC bias voltage is applied to the transistor. Generally, no significant differences have been found between the series and shunt configuration of the channel resistance [116]. The channel resistance R_{ch} can be found from:

$$R_{ch} = \frac{\partial V_d}{\partial I_d} \tag{11}$$

where V_d and I_d are the drain voltage and current, respectively.

In Fig. 28, the measured and simulated drain-to-source resistance R_{ds} of a 2x50-µm HEMT is shown. The required drive level can be reduced if the gate is biased towards the threshold voltage. It can be seen that the appropriate gate bias of the device is around -0.5 V.

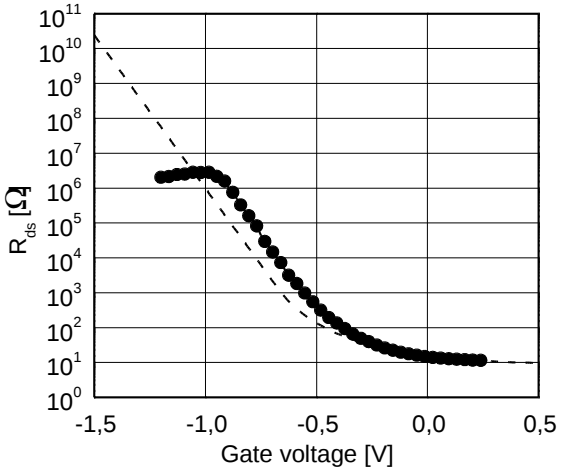

Fig. 28. Measured and simulated (dashed line) drain-to-source resistance of a 2x50-µm HEMT as a function of gate-to-source voltage (© 2005 IEEE, with permission from [P6]).

Because the drain of the transistor is unbiased, the gate-to-drain capacitance C_{gd} is greater than it would be if the drain were biased to the saturation region. This is shown in Fig 29, where simulated gate-to-drain capacitance as a function of the drain voltage for different gate bias voltages is shown.

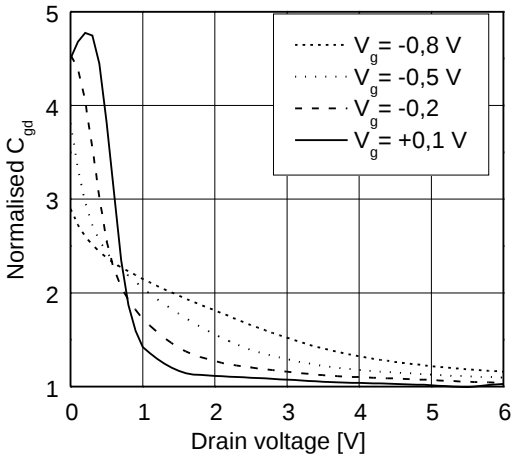

Fig 29. Normalized gate-to-drain capacitance C_{gd} as a function of drain voltage for different gate bias voltages of a 2x50-µm HEMT. The C_{gd} is normalized to open channel capacitance (© 2005 IEEE, with permission from [P6]).

To prevent the LO from pumping the drain conductance, the RF- and IF-matching circuits have to be designed to short-circuit the drain at the LO frequency. Just as the LO couples through the gate-to-drain capacitance to the drain, so the RF signal can leak to the gate through this capacitance. However, it has been shown that the RF leakage is not a critical design factor [117]. A wideband LO-short can be realised by using a balanced design.

4.2 Balanced resistive mixers

The principles, advantages, and disadvantages of balanced resistive mixers are similar to those of other balanced mixer designs (AM noise rejection properties, spurious response rejection, LO-to-RF-isolation) [106]. In Paper [P6], we presented a singly balanced resistive mixer and a balanced image rejection mixer for the 60-GHz frequency range in a GaAs pHEMT technology. In Paper [P1] and [118], we presented the design and measurement results of a broadband balanced resistive mixer at millimeter-wave frequencies for the first time in CMOS. Fig. 30 shows a simplified schematic of the balanced resistive mixer. The topology is suitable for both up- and downconversion and it achieves very wideband IF, RF, and LO performances. As demonstrated in [P7], the configuration also establishes a broadband conversion from the single-ended 60-GHz input to the differential IF.

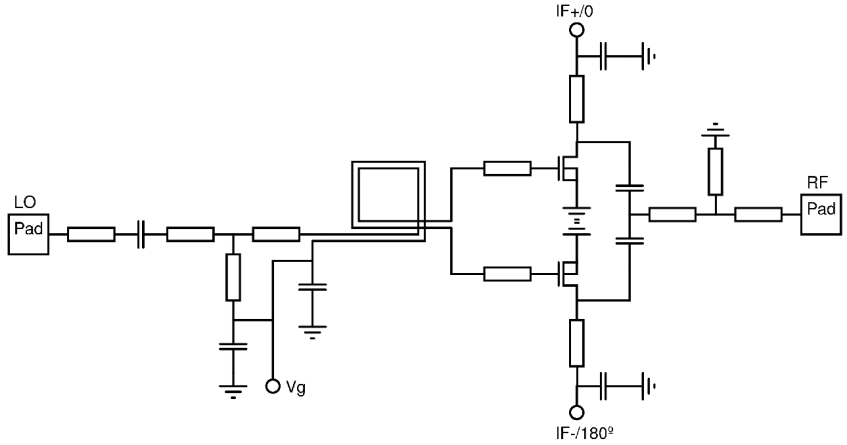

Fig. 30. Simplified schematic of the singly balanced resistive mixer (© 2008 IEEE, with permission from [P1]). The IF+ and IF- ports are connected to an off-chip IF hybrid. The capacitors are short circuits at the RF and LO frequencies and open circuits at the IF frequency.

In the mixer, the local oscillator signal is applied from a coplanar waveguide to a spiral transmission-line balun to generate the required 180-degree phase shift at the transistor gates. The drains are connected together using capacitors, which are short circuits at the RF and LO frequencies and open circuits at the IF frequency. The interface to the IF stage is implemented using CPWs, which are short-circuited at 60 GHz using capacitors with a small value. This isolates millimeter-wave signals from the IF circuitry.

4.2.1 Experimental results of the millimeter-wave balanced resistive mixer

The balanced resistive mixer was fabricated in a 65-nm baseline CMOS, first as a stand-alone circuit and then utilized in a 60-GHz single chip receiver [P7] and 60-GHz transmitter front-end [P8]. The measured downconversion results are compared to previously published CMOS mixers in Table 6. The performance in upconversion is compared to recently published mixers in Table 7. The experimental results demonstrate the feasibility of a balanced resistive mixer in deep-submicron CMOS. The mixer achieves wideband LO, RF, and IF operation with 34-dB LO-to-RF isolation and it occupies only 0.47 mm^2 of the chip area. Although the mixer dissipates no DC power, in this configuration relatively high LO-power is needed to obtain a reasonable conversion loss. A buffer amplifier can be added before the balun to relax the

impedance matching of the LO-port. In [P5] a single stage common-source amplifier stage consuming 12 mW reduced the LO power delivered to chip to +2 dBm.

Table 6. Performance comparison of CMOS downconversion mixers at 60 GHz.

CMOS process	Circuit topology	Conversion gain [dB]	ICP_{1dB} [dBm]	LO power [dBm]	P_{DC} [mW]	Chip size [mm^2]	Ref
130-nm	Active Gilbert cell	3 (voltage gain)	-15	0	-	0.81	[119]
130-nm	Active quadrature balanced	-2	-3.5	0	2.4	2.72	[109]
130-nm	Bulk-driven	1	-19	3	3	0.45	[120]
130-nm	Single balanced gate pumped	0.5	-6	3	7.5	0.56	[121]
130-nm	Single balanced diode	-15	-2	5	0.35	0.49	[121]
130-nm	Quandrature balanced current mode	1	2	0	3	1.4	[122]
90-nm	Active Gilbert Cell	2	-4.5	-	93	0.3	[111]
90-nm	Active cascode	-1.2	0.2	1.5	29	0.49	[123]
90-nm	Resistive single-ended	-11.6	6	4	0	4	[124]
65-nm	Resistive singly balanced	-12.5	5	8.7	0	0.47	[P1]

Table 7. Performance comparison of upconversion mixers around 60 GHz.

Technology	Circuit topology	RF freq [GHz]	CG [dB]	OCP_{1dB} [dBm]	LO-RF-isol. [dB]	LO power [dBm]	P_{DC} [mW]	Area [mm^2]	Ref
150-nm GaAs PHEMT	Balanced resistive	60	-11.5	-	34	8	0	3	[P6]
150-nm GaAs PHEMT	Balanced image rejection	60	-13.5	-13	36	8	0	1.41	[P6]
GaAs PHEMT	4xSHP APDP*	60	-16	-	-	15	-	4.4	[125]
150-nm GaAs mHEMT	2xSHP resistive mixer**	60	-8.4	-	37	8	0	4	[126]
150-nm GaAs MHEMT	4xSHP resistive mixer**	60	-15.5	-	36	8	0	4.5	[126]
250-nm SiGe BiCMOS	Gilbert micromixer	60	-6.5	-7.5	33	0	82.5	1.21	[127]
180-nm SiGe BiCMOS	Gilbert cell	40	-7	-25	40	5	14	0.28	[128]
130-nm CMOS	Gilbert cell	60	-0.7-4	-5.6	37	0	24	0.21***	[129]
130-nm CMOS	Gilbert cell	60	-5.6	-20.6	-	-	2.7	0.6****	[130]
90-nm CMOS	Gilbert cell	60	-4-(-7)	-	-	-	70*****	0.36	[88]
90-nm CMOS	Gilbert cell	51	-11	-11	26.5	0	13.2	0.63	[131]
65-nm CMOS	Gilbert cell	60	-6.5	-5	30	5	29	0.98	[132]
65-nm CMOS	Balanced resistive	60	-13.5	-19	34	8.7	0	0.47	[P1]

* ADPD: antiparallel diode pair
** SHP: subharmonically pumped
*** without LO or RF baluns
**** including frequency tripler
***** including LO buffer

5 Millimeter-wave receiver and transmitter front-end design

Millimeter-wave communications systems require a high-performance technology. The continuing progress of the GaAs, SiGe BiCMOS, and CMOS technologies has made possible low-cost radio transmitters and receivers operating at millimeter-wave frequencies including the 60-GHz band. In practice, the radio chip-set targeted to 60-GHz low-cost applications should achieve an integration level that is as high as possible and avoid off-chip components. The wide bandwidth available enables multi-gigabit per second data transmission using a variety of modulation formats, ranging from non-coherent amplitude shift-keying (ASK) to complex orthogonal frequency division multiplexing (OFDM) [133], which means that several architectures can be considered for high data rate transfer. Single-carrier systems with simple modulation schemes are tempting solutions, since analog-to-digital (ADC) and digital-to-analog (DAC) converters (both can consume large amounts of DC power when several Gb/s are desired) can be avoided [134]. However, if the delay spread of the underlying propagation channel is high, then an OFDM is an obvious choice of modulation [135]. For the 60-GHz systems and applications up to and beyond 100 GHz, different transceiver architectures and circuit topologies have to be studied and experimental results are needed to provide an understanding of the trade-offs between different implementations. Here, only the common transceiver architectures, the superheterodyne and direct conversion, are briefly introduced to support the experimental results of a 60-GHz single-chip receiver and 60-GHz and W-band transmitter front-ends fabricated in CMOS.

5.1 Transceiver architectures

5.1.1 Superheterodyne architecture

A block diagram of a superheterodyne transceiver with one intermediate frequency is shown in Fig. 31. This architecture was first introduced by E. Armstrong [136]. In the transmitter, the I (in-phase) and Q (quadrature-phase) baseband inputs are fed to the quadrature modulator for upconversion to IF. The following filter suppresses the harmonics of the IF signal. The IF is

mixed to RF and the unwanted sideband is filtered in an image rejection filter before the power amplifier. If the image frequency is not sufficiently suppressed it doubles the power at the input of the power amplifier. In this case the power amplifier will enter saturation at an input power that is 3 dB below that of the desired frequency component present.

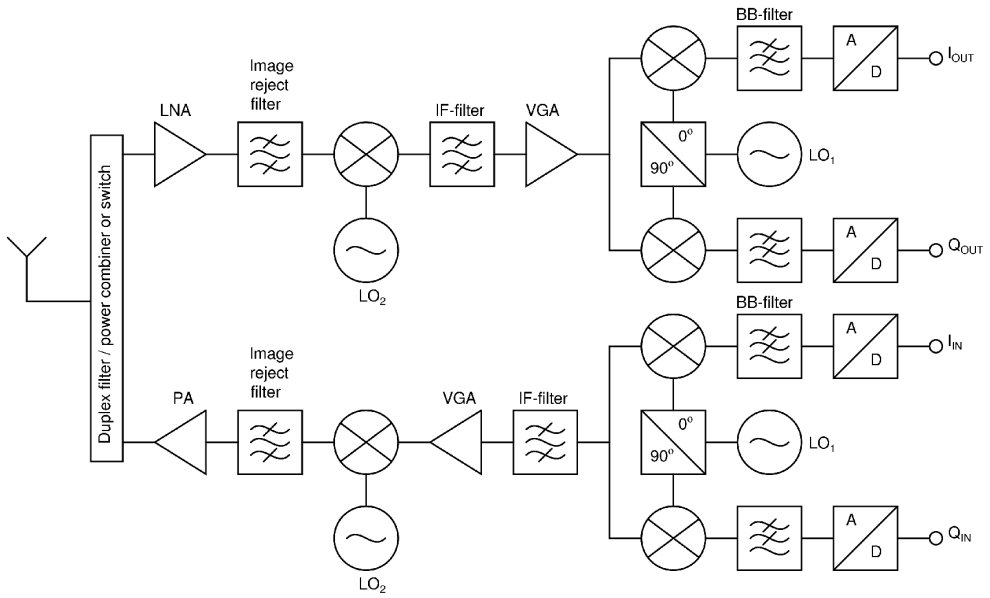

Fig. 31. Superheterodyne transceiver.

In the case of frequency domain duplexing (FDD), a duplex filter is used before the antenna. If time-domain duplexing (TDD) is used, a switch or a power combiner can be used. In the receiver, a low-noise amplifier is followed by an image rejection filter to suppress the unwanted signals and noise at the image frequencies. The channel select filter after the first downconversion is typically at a fixed frequency and the IF is set by the voltage-controlled oscillator (VCO). Therefore, the frequency of the VCO is adjustable in order to cover the whole reception band. The channel select filter is followed by a variable gain amplifier and demodulator, which divides the signals into the I and Q channels.

The image rejection filter for both the receiver and transmitter can be replaced by an image rejection mixer topology [137]. For millimeter wave frequencies the image rejection mixer configuration seems to be an appealing topology since, generally, the filter response determines the available local oscillator tuning range and prevents the overlapping of the desired RF and

image bands. In addition, if the intermediate frequency is low, the image band is close to the RF band, which makes the filter design more problematic. One way to realize a broadband image rejection transmitter utilizing an image rejection mixer is shown in Fig. 32. The topology is also applicable for direct conversion by connecting the baseband channels directly to IF ports.

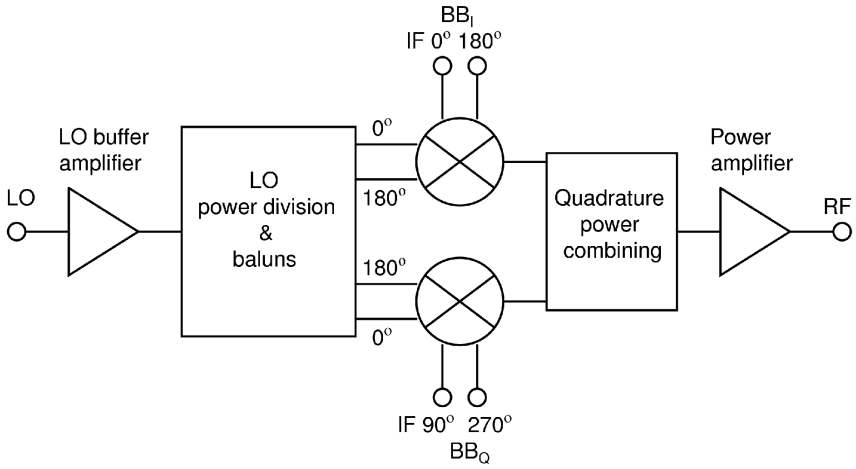

Fig. 32. Block diagram of a W-band image-rejection transmitter (© 2010 IEEE, with permission from [P5]). The topology is also applicable for direct conversion by connecting the baseband I (BB_I) and baseband Q (BB_Q) channels to IF ports.

5.1.2 Direct conversion architecture

The direct conversion topology was published in 1924 by F. M. Colebrook [138]. It is also called the zero-IF or homodyne architecture [139]. A block diagram of a typical direct conversion transceiver is shown in Fig. 33. In the transmitter the modulation and upconversion to RF occur in the same circuit. In the receiver the RF is converted directly to the zero IF frequency. Although the direct conversion architecture eliminates the image reject problem there are challenges that do not appear in the superheterodyne architecture [139], [140]. The direct conversion receiver is sensitive to flicker noise. In the transmitter, the high output power of the power amplifier may couple back to the VCO and modulate it and pull it out of lock. In the receiver, LO leakage can cause DC offsets because of self-mixing. The LO pulling and DC offsets can be alleviated if the power amplifier output spectrum or the frequency of the signal received is sufficiently higher or lower than the oscillator frequency. The LO can be offset by adding or subtracting the output of another frequency [141] or using a divider and an oscillator

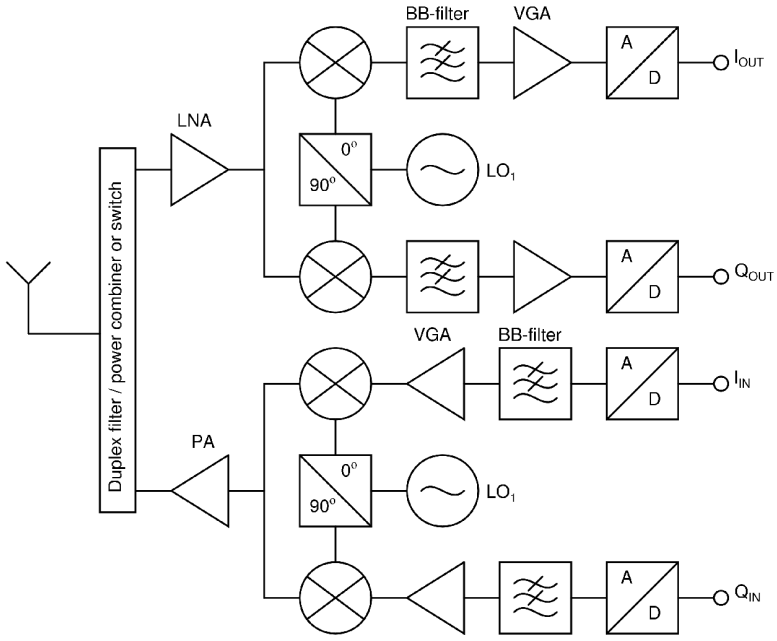

Fig. 33. Direct conversion transceiver.

frequency that is two times higher than the LO. At millimeter-wave frequencies one may employ a lower-frequency LO and a multiplier [11]. Generally, the use of a frequency multiplier allows the phase-locked loop (PLL) to operate at a lower frequency, where the quality of the tuned circuit components is higher and parasitic capacitances have less impact, making it easier to achieve low phase noise and a wide tuning range in the VCO [133].

5.2 Experimental results

5.2.1 A 60-GHz CMOS receiver with an on-chip ADC

A broadband receiver was designed and fabricated for 60-GHz reception in a 65-nm baseline CMOS technology [P7]. To the best of the author's knowledge, this receiver is the first implementation that includes a 60-GHz millimeter-wave front-end, an IF-stage, and an analog baseband circuit with an ADC on a single chip. A block diagram of the single-chip 60-GHz receiver is shown in Fig. 34. The superheterodyne architecture was chosen in order to minimize the number of blocks operating at millimeter-wave frequencies and to take advantage of our previous work in the area of ultra wideband receivers (UWB) at RF frequencies [142].

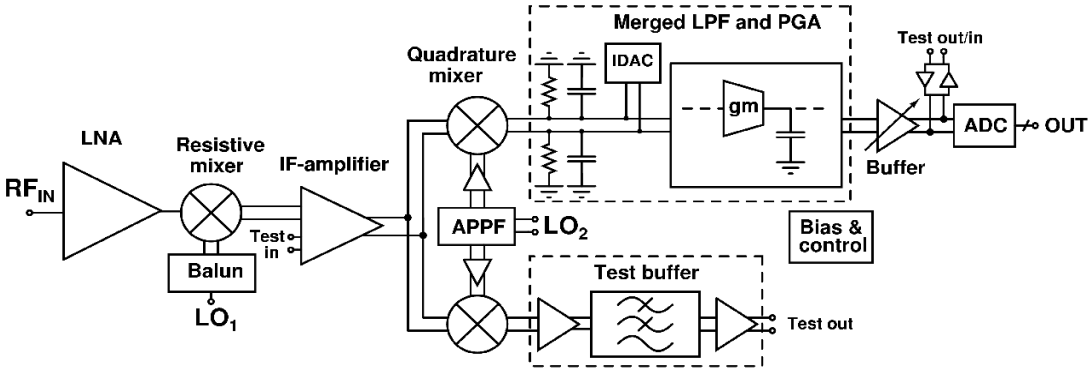

Fig. 34. Block diagram of the 60-GHz receiver (© 2009 IEEE, with permission from [P7]).

To minimize the noise contribution of the resistive mixer and the following stages, a gain of around 20 dB is needed from the 60-GHz low noise amplifier. Therefore, a 4-stage common source amplifier is used before the mixer. The balanced resistive mixer, described in Chapter 4, provides a broadband conversion from the single-ended 60-GHz input to the differential IF. A differential two-stage cascode amplifier follows the resistive mixer before the separation of the IF signal into I/Q baseband signals with a quadrature mixer. The balanced quadrature signals for the mixer are generated on-chip with an active poly-phase filter (APPF) in which the resistors are replaced with transconductors [143]. The baseband circuit contains a merged 275-MHz low-pass filter (LPF) and a programmable gain amplifier (PGA) and is followed by a 6-bit 600-MS/s flash-ADC. The baseband circuit and the ADC support wireless MB-OFDM ultra-wideband system data reception [144]. Both local oscillator signals LO_1 and LO_2 are external. The LO_2 can be swept from 2 to 6 GHz. In the measurements the LO_1 was swept from 59 to 64 GHz. One complete baseband chain with the ADC is integrated on-chip. The other baseband channel includes a wideband buffer for testing purposes.

The measured performance is compared to recently published 60-GHz receiver front-ends fabricated in CMOS and SiGe technologies in Table 8. The experimental results demonstrate the feasibility of a broadband single-chip 60-GHz receiver with an ADC in deep submicron CMOS. Despite the high level of integration, this receiver compares favorably to existing state-of-the-art millimeter-wave front-ends.

Table 8. Comparison to published 60-GHz silicon receiver front-ends.

Gain [dB]	NF [dB]	ICP_{1dB} [dBm]	S_{11} [dB]	V_{DD} [V]	P_{DC} [mW]	Area [mm^2]	Integrated blocks	Technology	Ref
40	5-6.7	-36	< -15	2.7	527	5.78	LNA, mixer, IF amplifier, IF mixer, PLL, frequency tripler	0.13 µm SiGe BiMCOS	[133]
22.5*	8.4**	-	< -6.3	1.2	144	2.64	Antenna, LNA, mixer, TIA, VCO, synthesizer	90-nm CMOS	[145]
22	5.7-8.8	-27.5	-	1.2	36	0.185***	LNA, polyphase filter, mixer, IF mixer, LO	90-nm CMOS	[146]
55.5*	6.1-6.4**	-26	< -10	1.0	24	1.55	LNA, mixer, VGA, buffer amplifier	90-nm CMOS	[147]
51	9	-30	< -15	-	189	3.83	LNA, mixer, IF amplifier, IQ demodulator + buffer, VCO/PLL	90-nm CMOS	[148]
62	-	-	-	1	206	1.9	LNA, VGA, IQ demodulator, LO buffer	90-nm CMOS	[66]
-	-	-	< -15	-	138	-	LNA, IQ-demodulator, VGA, DFE, VCO+PLL	90-nm CMOS	[149]
25****	7****	-26****	< -30	1.5	103	0.68	LNA, mixer, OOK demodulator, limiting amplifier, VCO	90-nm CMOS	[150]
14.7	5.6	-22	-	1.2	151	0.5	LNA, mixer, LO tree,frequency divider	65-nm CMOS	[134]
79	7.0	-38.5	< -12	1.2	198	2.8	LNA, mixer, IF amplifier, IF mixer, IF IQ-generation, BB LPF+PGA, ADC	65-nm CMOS	[P7]

* Power gain instead of voltage gain
** DSB NF
*** Active area without pads
**** LNA and mixer only

5.2.2 A 60-GHz transmitter front-end in CMOS

In the transmitter, the local oscillator signal has to be adequately suppressed. Otherwise, a high LO may compress the power amplifier. Furthermore, the 1-dB output compression point of the mixer should be high in order to reduce the gain requirements of the power amplifier. Therefore, the balanced resistive mixer presented in Chapter 4 seems to be an appealing topology. Nevertheless, enough gain is needed to drive the output stage of the amplifier into compression. The measured OCP_{1dB} of the mixer was -19 dBm and the amplifier presented in [P1] achieved 1.5 dBm OCP_{1dB}. This means that the amplifier should provide a gain of more than 20 dB. Therefore, a five-stage amplifier was chosen for the transmitter front-end circuit as shown in Fig. 35.

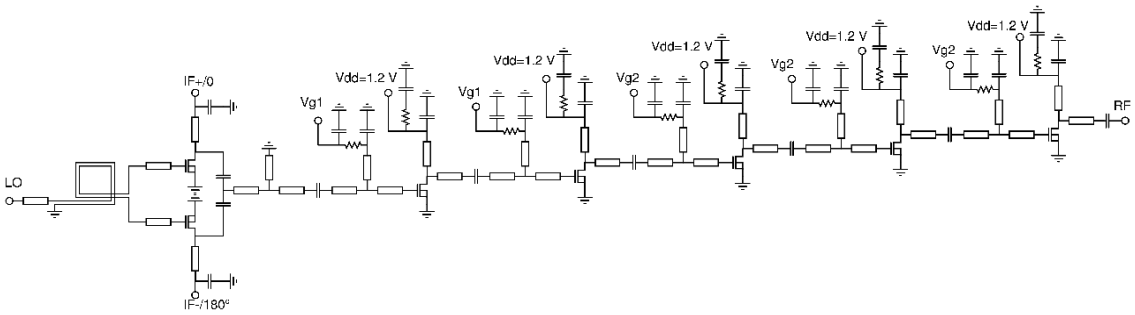

Fig. 35. Simplified schematic of the transmitter front-end (© 2009 IEEE, with permission from [P8]).

The transmitter front-end was fabricated in 65-nm CMOS. The transmitter chip was assembled on a PCB substrate and DC bias pads were bonded to the PCB. The millimeter-wave signals were fed to the chip via RF-probes. The measurements showed a very wideband IF, RF, and LO performance. The performance of the transmitter front-end is compared to recently published transmitter front-ends in Table 9. The transmitter front-end shows good performance and demonstrates the millimeter-wave capability of the 65-nm baseline CMOS technology.

Table 9. Performance comparison of 60-GHz transmitter front-ends.

Conversion gain [dB]	**OCP_{1dB} [dBm]**	**P_{sat} [dBm]**	**P_{DC} [mW]**	**Area [mm^2]**	**Technology**	**Ref.**
0.6	-1.6	5.6	420*	12*	0.15-µm GaAs mHEMT	[151]
3.6-8.1	1-5.5	-	345	4.5	0.15-µm GaAs pHEMT	[152]
34-37	10-12	15-17	800**	6.4**	0.13-µm SiGe BiMCOS	[133]
-	2	4	-	8.4	0.13-µm CMOS	[153]
5	-	-5	92.2	0.366	0.13-µm CMOS	[154]
-	-	6	133	1.5	90-nm CMOS	[66]
15	0	6	-	-	90-nm CMOS	[155]
11.3	-	2.4	374***	1	65-nm CMOS	[134]
12	-3	2	132****	1	65-nm CMOS	[P8]

* including 8 times multiplier and LO amplifier
** including IF amplifier, PLL, frequency tripler
*** including RX, LO tree, divider
**** LO power 8 dBm

5.2.3 A W-band transmitter front-end in CMOS

The transmitter front-end presented in Fig. 32 uses two balanced resistive mixers and quadrature IF-signals, or baseband in-phase and quadrature signals, and in-phase balanced LO drive signals. The image rejection or direct conversion is achieved when the RF signals are summed 90 degrees out of phase. Since a Lange coupler provides both power combining and phasing, quadrature summation in the RF path instead of the LO path was chosen. Furthermore, as the LO power needed is relatively high compared to the RF power after mixing, it is more power-efficient to use the Lange coupler in the RF chain, where a small transistor can be used for compensating the loss of the coupler. The on-chip spiral transmission line baluns fed from a slow-wave coplanar waveguide input are used to perform both the even-to-odd mode transformation, which is required for the balanced mixing operation, and the power division for the LO signal [P6]. A single-stage common-source LO buffer was added before the baluns to lower the required LO power at the input and to compensate the losses of the baluns. Six common-source stages are used in the power amplifier. The transmitter front-end was measured on-wafer. The measured performance of the transmitter front-end and a comparison to a previously published CMOS W-band transmitter are shown in Table 10. The measured results show wideband RF, IF, and LO performances with good output power and image rejection (IR).

Table 10. Measured performance of the W-band transmitter front-end.

P_{sat} [dBm]	OCP_{1dB} [dBm]	RF-bandwidth [GHz]	IF-bandwidth [GHz]	IR-ratio [dB]	Peak gain [dB]	P_{DC} [mW]	Ref.
+6.6	+2.2	75-95	1-8*	15-20	8.5	120	[P5]
+3	NA	80-94	NA	NA	3.8	142	[156]

* Limited by the measurement setup

6 Conclusions

In this thesis, the design of active and passive MMIC components and the circuit design of millimeter-wave integrated low noise amplifiers, power amplifiers, resistive mixers, transmitter front-ends, and receivers have been studied.

Millimeter-wave integrated circuits have traditionally been implemented using technologies which are based on compound semiconductors such as gallium arsenide or indium phosphide. Recently, there has been enormous development in the field of silicon integrated circuits operating at millimeter-wave frequencies. However, the high electron mobility transistor technology provides the best high-frequency noise, gain, and output power performance. The best gain and noise performance have been achieved using InP HEMT technologies. Compared to a GaAs HEMT technology, the InP HEMT technology has higher manufacturing cost, lower breakdown voltage, and more fragile structure. In a metamorphic HEMT technology, a metamorphic buffer layer is grown on the GaAs substrate, which enables the growth of a channel layer with a high indium content. Therefore, comparable noise and gain performance to InP HEMTs can be achieved on a lower cost and higher quality GaAs wafer. Silicon-based technologies have the potential to enable front-end, baseband, analog-to-digital and digital-to-analog converters, and digital signal processing circuitry to be integrated on a single chip. SiGe BiCMOS heterojunction bipolar transistors have better gain, noise and output power performance compared to CMOS transistors. However, when targeting high-volume commercial applications, for example, in the 60-GHz band, the CMOS technology can provide the highest integration level at low cost when produced in large volumes.

As the device scaling of CMOS technologies results in a higher unity gain frequency and maximum frequency of oscillation of the transistor, improved performance at millimeter-wave frequencies is expected. However, the continuing scaling of bulk CMOS process typically produces some challenges for the designer, such as a lower supply voltage, stringent metal density requirements, and thinner dielectric layers above the substrate leading to higher substrate losses of passives. Furthermore, at millimeter-wave frequencies the distributed effects have to be taken into account in the design process and the transistor layout has a significant impact on the performance. In this thesis, millimeter-wave active and passive components in nanoscale CMOS and test structures for measuring and analyzing these components have been

studied and developed. Furthermore, circuit design techniques for pushing CMOS circuits beyond 100 GHz have been presented. Topologies for a coplanar waveguide, microstrip line, and slow-wave coplanar waveguide that are suitable for implementing transmission lines in nanoscale CMOS have been presented. It has been demonstrated that the proposed slow-wave coplanar waveguide improves the performance of the transistor-matching networks when compared to a conventional coplanar waveguide and the floating slow-wave shield reduces losses and simplifies modeling when extended below other passives, such as DC decoupling and RF short-circuiting capacitors. Furthermore, wideband spiral transmission line baluns in CMOS at millimeter-wave frequencies have been demonstrated. The design of amplifiers utilizing the developed components in 65-nm CMOS has been shown. The 40-GHz amplifier achieved a +6-dBm 1-dB output compression point and a saturated output power of 9.6 dBm with a miniature chip size of 0.286 mm^2. The measured noise figure and gain of the 60-GHz amplifier were 5.6 dB and 11.5 dB, respectively. Furthermore, using the active and passive components and circuit design methods presented here, we have been able to design 100-GHz CMOS amplifiers that achieve state-of-the-art results. A wideband balanced resistive mixer utilizing the spiral transmission line balun was demonstrated in CMOS. The proposed V-band mixer achieved a 13.5-dB upconversion loss and 34-dB LO-to-RF isolation with a chip area of 0.47 mm^2. In downconversion, the measured conversion loss and 1-dB input compression point were 12.5 dB and +5 dBm, respectively.

The low-noise amplifier is one of the key components in a millimeter-wave receiver and the power amplifier is perhaps one of the most challenging blocks to design for a millimeter-wave transmitter. At millimeter-wave frequencies the gain of a single transistor is relatively low. Therefore, there is little margin, with power amplifiers, for trade-off between linearity, output power, gain, and efficiency. Because of the low gain, the noise contribution of the following stages becomes significant, which means that several stages have to be cascaded in order to make the noise produced in the following blocks low enough when the total receiver noise figure is calculated. Two low-noise amplifiers for the W-band and D-band were designed and fabricated in a 100-nm GaAs-based metamorphic HEMT technology. Both amplifiers were designed for wideband performance and flat gain response. The measured results demonstrate excellent noise and gain performance. The amplifiers achieved a 22.5-dB gain and a 3.3-dB noise figure at 94 GHz and an 18-19 dB gain and a 5.5-7.0 dB noise figure from 130 to 154 GHz. In the 60-GHz three-stage power amplifier the output stage was divided into two devices in order to achieve adequate gain. The matching circuitry of the output stage performs both the

combining and dividing of the power and also the matching of the output cells. By realizing the output match in two parts, i.e. by first converting the 50-Ω load impedance to a lower impedance level and then matching the impedance at the power-combining point to the desired impedance for the output transistors, a broadband output match was achieved. Instead of using quarter-wave length transformers or Wilkinson power combiners, the matching circuitry was realized using series transmission lines and open shunt stubs. At least in our case, this gave more freedom to choose the impedance levels during the design and resulted in a smaller chip area. The amplifier was implemented in a 150-nm pseudomorphic HEMT technology and exhibited a +17-dBm 1-dB output compression point with a 13.4 dB linear gain.

The wide unlicensed band available around 60 GHz makes possible multi-gigabit per second data transmission using a variety of modulation formats, which means that several architectures can be considered for high data rate transfer. Single-carrier systems with simple modulation schemes are tempting solutions, since analog-to-digital (ADC) and digital-to-analog (DAC) converters (both can consume large amounts of DC power when several Gb/s are desired) can be avoided. However, if the delay spread of the underlying propagation channel is high, then an OFDM is an obvious choice of modulation. For the 60-GHz systems and applications up to and beyond 100 GHz, different transceiver architectures and circuit topologies have to be studied and experimental results are needed to provide an understanding of the trade-offs between different implementations. We demonstrated a 60-GHz CMOS receiver that includes a 60-GHz millimeter-wave front-end, an IF stage, and an analog baseband circuit with an ADC on a single chip. The millimeter-wave front-end consists of a four-stage low-noise amplifier and a balanced resistive mixer. The balanced resistive mixer configuration establishes a broadband conversion from the single-ended 60-GHz input to the differential IF. As a result of the accurate modeling of the millimeter-wave circuit blocks and careful system-level design, a wideband performance and a noise figure as low as 7 dB were achieved. For the 60-GHz range a wideband transmitter front-end in 65-nm CMOS was designed. By utilizing the balanced resistive mixer that was developed in this work and a five-stage amplifier, wideband IF, RF, and LO performances with a +2-dBm output power were achieved. For the W-band applications, a transmitter front-end suitable for both image-rejecting superheterodyne and direct conversion transmission was demonstrated in 65-nm CMOS. It achieved wideband RF, IF, and LO-performances with a +6.6-dBm output power and a 15-to-25-dB image rejection ratio. The obtained results demonstrate that high-performance millimeter-wave radio front-ends are feasible in deep submicron CMOS.

The research for developing millimeter-wave integrated circuits in both CMOS and GaAs technologies is continuing at the Electronic Circuit Design Laboratory. Currently we are designing low-noise amplifiers for frequencies of 165 GHz and 183 GHz in 100-nm and 50-nm GaAs-based metamorphic HEMT technologies. Some of the designs are expected to have more than 20 dB gain above 200 GHz. Because of the low breakdown voltage of a scaled CMOS transistor the design of a millimeter-wave CMOS power amplifier is a challenging task. The ongoing research aims at developing CMOS power amplifiers for 90 to 100 GHz frequency range. Specific design and power combining techniques are utilized for achieving high output power and ensuring reliable operation. We are also building systems for the 60-GHz wireless telecommunication and W-band applications in an ongoing Tekes project (BRAWE). The realized CMOS circuits are packaged using a low temperature co-fired ceramic (LTCC) technology. The work also concentrates on the development of CMOS phased-array front-ends. Our future aim is to push nanoscale CMOS circuits even higher frequencies. In this task, the research work presented in this thesis can be exploited and directly continued.

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