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A 3 μW, 2 MHz CMOS Frequency Reference for Capacitive Sensor Applications

Matti Paavola, Mika Laiho, Mikko Saukoski and Kari Halonen
Electronic Circuit Design Laboratory, Helsinki University of Technology, Espoo, Finland
Email: mhpaavol@ecdl.hut.fi

***Abstract*— In this paper, measurement results for a micropower 2 MHz CMOS frequency reference circuit fabricated with a 0.13 μm CMOS process are presented. This frequency reference circuit, based on source-coupled CMOS multivibrator, provides the clock signal for a read-out circuit of a capacitive sensor. In addition to a low power consumption, a good frequency stability is required. Supply independent biasing and symmetrical loads are used to optimize the frequency stability. The typical power consumption is 3.0 μW at room temperature with 1.8 V supply voltage. When properly calibrated, the frequency stays within $\pm 2.5\,\%$ of the nominal oscillation frequency in the operating voltage range of $1.8 - 2.5$ V (with $\pm 10\,\%$ variation) over a temperature range from -35 to $+85\,^{\circ}$C. The measured phase noise and jitter agree well with the simulations.**

I. INTRODUCTION

When realizing small, inexpensive and low-power microsensors, the sensor interface with signal processing must be integrated as near the sensing element as possible. New applications of different kinds of microsensors have emerged, as advances in the microfabrication technologies have made them increasingly affordable. The use of microsensors in battery-powered equipment requires a low power consumption.

The frequency reference circuit considered in this paper is a part of a low-power interface for a micromechanical capacitive sensor. The interface consists of a front-end circuit that converts the capacitive signal to voltage, an A/D converter that converts the analog signal to digital domain, a clock generator that provides all the required clock signals, and a voltage reference. The voltage reference circuit provides also temperature information for the system. The front-end circuit [1] is able to read a three-axis accelerometer composed of four proof masses. Both the sensor front-end and the A/D converter have to be time-multiplexed between four channels, one for each mass. In addition, the system includes a DSP part that performs signal processing in the digital domain and also controls the function of all other parts of the system. The system has various operating modes that enable a low power consumption.

Since the frequency reference circuit, which is a part of the clock generator, is always active, the minimization of power consumption is a primary goal. The effects of process variations on the oscillation frequency can be eliminated by calibration. After the calibration, the oscillation frequency is not allowed to differ more than $\pm 15\,\%$ from the nominal value of $2\,MHz$, though the operating voltage can change between $1.8 - 2.5\,V$, with an additional $\pm 10\,\%$ variation, and the temperature can change from -40 to $+85\,^{\circ}C$. RMS jitter, which is set by the sampling accuracy requirements, must be smaller than $100\,ns$.

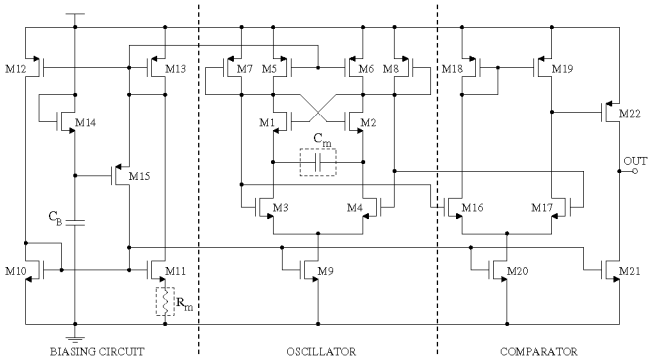

Fig. 1. Presented frequency reference circuit.

In this paper, we present the measurement results for a low-power frequency reference circuit based on the source-coupled CMOS multivibrator presented in [2]. Before showing the measurement results, the circuit is briefly described and the theory related to the optimization of the frequency stability and the phase noise, partially presented in [3], is described more extensively.

II. CIRCUIT DESCRIPTION

Fig. 1 shows the frequency reference circuit that consists of a source-coupled CMOS multivibrator (oscillator), a supply independent biasing circuit and a two-stage comparator. All these three circuit blocks are needed here to form an independent frequency reference circuit. The relaxation-type implementation makes low power consumption possible. Supply independent biasing circuit is necessary due to the large supply voltage range. Symmetrical loads [4] are used in the oscillator to limit the variation of the equivalent load resistance during a clock cycle. Capacitor matrix C_m in the oscillator and resistor matrix R_m in the biasing circuit enable calibration. The voltage swings in the oscillator outputs exhibit significant variations, depending primarily on the tail current and temperature. Because a rail-to-rail clock signal is required, a two-stage comparator is used. The supply independent biasing circuit is equipped with a start-up circuit, formed by transistors M14 and M15, together with capacitor C_B.

A. Optimization of the frequency stability

The oscillation frequency is of the form [2]

$$f_0 \sim \frac{I_9}{C_m V_C}, \tag{1}$$

where I_9 is the tail current, C_m the capacitance of the capacitor matrix, and V_C the amplitude of voltage across the capacitor matrix. Further, V_C can be approximated as

$$V_C = RI_9, \tag{2}$$

where R is the equivalent load resistance. Now, (1) can be written as

$$f_0 \sim \frac{1}{RC_m}. \tag{3}$$

From this equation, it can be seen that the temperature stability of the oscillation frequency can be optimized by minimizing the temperature dependency of the equivalent load resistance R. If the equivalent load resistance remains approximately constant, the tail current affects only the total current consumption. This enables the minimization of the current consumption of the oscillator.

The biasing circuit used here acts as a PTAT (proportional to absolute temperature) current generator, if the MOS transistors M10–M13 operate in the subthreshold region. In this case, the output current is [5]

$$I_{OUT} = \frac{V_T}{R_m} ln\left[\frac{K\,(W/L)}{(W/L)}\right] = \frac{kT}{q}\frac{1}{R_m} ln\,(K)\,, \tag{4}$$

where V_T $(= kT/q)$ is the thermal voltage, R_m the resistance formed by the resistor matrix, (W/L) the W/L-ratio of transistor M10, K the ratio $(W/L)_{11}/(W/L)_{10}$, k the Boltzmann's constant $(1.38 \times 10^{-23}\,J/K)$, T the absolute temperature, and q the elementary charge $(1.602 \times 10^{-19}\,C)$. The reference current is independent of the operating voltage, but it depends on the resistance value and temperature. The current consumption of the whole frequency reference circuit can be optimized simply by adjusting R_m.

Eq. (4) describes the biasing circuit of our design better than the equation previously presented in [3] that holds when transistors operate in strong inversion. If it is assumed that the resistance value R_m in Eq. (4) is independent of temperature, the output current deviates at maximum $-22/+19\,\%$ from the value calculated at the room temperature. From Fig. 2, where the temperature dependency of the resistance value R_m has been taken into account, the simulated temperature dependencies of the tail current I_9, the capacitor voltage V_C, and the equivalent load resistance R can be seen. Note that both the current $(I\,(\mu A))$ and the voltage $(V\,(V))$ are on the left vertical axis and resistance $(R\,(M\Omega))$ is on the right vertical axis. According to the curve of I_9, the deviations in the tail current are about $-38/+36\,\%$ over the temperature range. This means that the temperature dependency is further increased by the negative first order temperature coefficient of the resistance value R_m.

Despite the poor temperature stability of the tail current, the temperature stability of the oscillation frequency is not poor

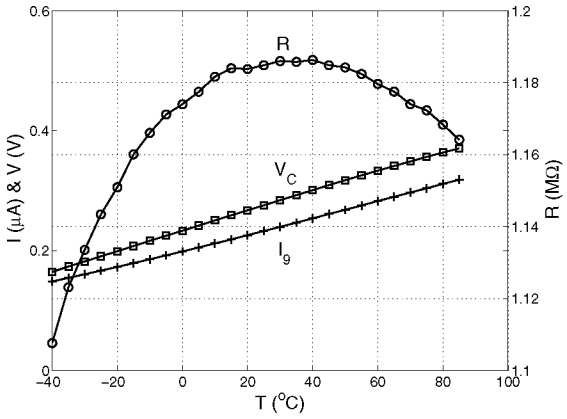

Fig. 2. Simulated temperature dependencies in the oscillator, showing the good temperature stability of the equivalent load resistance R.

in the case of the oscillator topology used here. The curve of the equivalent load resistance in Fig. 2 resembles a parabola. It has the maximum close to the room temperature, which means that the variation of the equivalent load resistance over the temperature range is minimized with good accuracy. In our case, this optimization has been carried out using symmetrical loads that are more linear than pure current source loads [3]. Simulations predict that the oscillation frequency varies about $\pm 5\,\%$ over the temperature range. The maximum simulated deviations from the calibrated oscillation frequency, when the effects of both the temperature and the supply voltage are taken into account, are $+5/-7\,\%$ [3].

B. Phase noise

The phase noise of the frequency reference circuit was studied with transient noise simulations and the current impulse method [3], [6]. The use of transient noise simulations is very time consuming, especially if the effect of individual noise sources on the phase noise must be characterized and optimized. In the current impulse method, the effect of an injected current impulse in parallel to each transistor in different phases of a clock cycle is considered. This way, the phase shift functions for all transistors of the oscillator can be evaluated. The equation for the phase shift per charge can be written as [3]

$$\phi(x) = \frac{1}{q_{inj}} \int_0^{2\pi} \Gamma\,(x)\,\alpha\,(x)\,i\,(x)\,dx, \tag{5}$$

where q_{inj} is the injected charge, $\Gamma\,(x)$ the impulse sensitivity function (ISF), $\alpha\,(x)$ a function that takes cyclostationarity into account, and $i\,(x)$ the injected current impulse.

The RMS- and DC-values of (5) give some insight on how sensitive the oscillator is to a current impulse in parallel to each transistor. A high RMS-value corresponds to a high sensitivity to white noise, while a high DC-value corresponds to a high sensitivity to 1/f-noise. The phase noise due to a single transistor in the $1/f^2$- and $1/f^3$-region can be

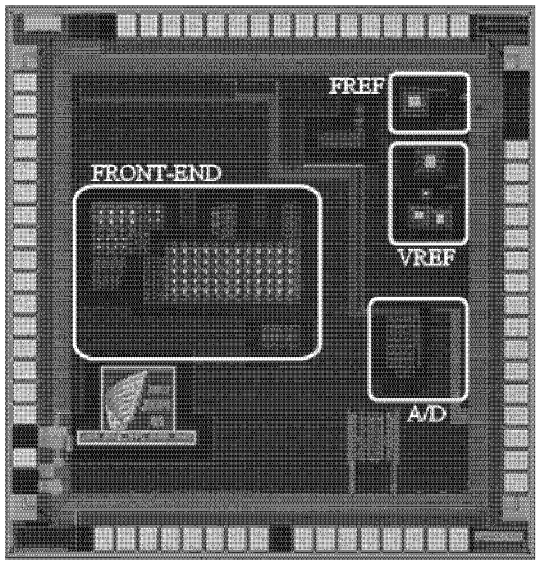

Fig. 3. Microphotograph of the chip.

calculated using the equations

$$L\{\Delta f\} = 10 \cdot log\left[\phi_{rms}^2 \cdot \frac{\overline{i_n^2}/\Delta f}{8\pi^2 (\Delta f)^2}\right] \quad (6)$$

and

$$L\{\Delta f\} = 10 \cdot log\left[\phi_{dc}^2 \cdot \frac{\overline{i_n^2}/\Delta f}{16\pi^3 (\Delta f)^2} \cdot \frac{f_{1/f}}{\Delta f}\right], \quad (7)$$

where ϕ_{rms} and ϕ_{dc} are the RMS- and DC-value of (5), respectively, $\overline{i_n^2}/\Delta f$ is the white noise spectral density, Δf the offset frequency from the carrier and $f_{1/f}$ the corner frequency of 1/f-noise. In the case of uncorrelated noise sources, the phase noise caused by individual noise sources can be summed up directly. The effect of the comparator on the phase noise spectrum can be taken into account by recording the phase shifts at the output of the comparator.

III. MEASUREMENT RESULTS

Fig. 3 shows the microphotograph of the implemented chip. Four separate blocks have been marked: the sensor front-end (FRONT-END), an A/D converter (A/D), a frequency reference circuit presented in this paper (FREF), and a voltage reference (VREF). The area of the chip is $1.67\,mm \times 1.74\,mm$ and the area of the frequency reference circuit is $175\,\mu m \times 85\,\mu m$ ($0.015\,mm^2$).

The functionality of the frequency reference circuit was measured over a temperature range of -35 to $+85\,^{\circ}C$. Nominal values for R_m and C_m are used in this section, because the real process-dependent resistance and capacitance values on the chip can not be accurately known.

A. Power consumption

The average values of the current and power consumption in the case of $R_m = 90\,k\Omega$, $C_m = 0.145\,pF$ at temperatures of -35, $+27$ and $+85\,^{\circ}C$ with supply voltages of 1.8 and $2.5\,V$ are shown in Table I. At room temperature, the average total current consumption with $1.8\,V$ supply voltage is $1.67\,\mu A$, corresponding to an average total power consumption of $3.0\,\mu W$. The current consumption changes about $20\,\%$ when the temperature changes from the room temperature to $+85$ or $-35\,^{\circ}C$. The effect of the operating voltage on the current consumption increases when temperature increases. The measurements show that the current consumption is $7.5\,\%$ greater with $2.5\,V$ operating voltage compared to the case of $1.8\,V$ operating voltage when the temperature is $+85\,^{\circ}C$.

TABLE I
AVERAGE CURRENT AND POWER CONSUMPTIONS.

$V_{DD}\,[V]$	$T\,[^{\circ}C]$	$I\,[\mu A]$	$P\,[\mu W]$
1.8	+85	1.99	3.6
1.8	+27	1.67	3.0
1.8	-35	1.35	2.4
2.5	+85	2.14	5.4
2.5	+27	1.78	4.5
2.5	-35	1.39	3.5

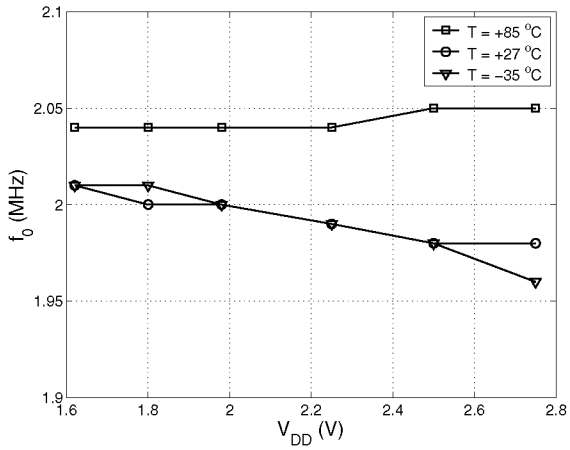

Fig. 4. Measured frequency stability of the circuit, showing the small dependency of the oscillation frequency on both the supply voltage and the temperature.

B. Frequency stability and calibration

The temperature dependency of the oscillation frequency depends on the process corner. It also varies when the values of R_m and C_m are changed, which corresponds to the situation during calibration. The measurements prove that the circuit can provide an oscillation frequency with very small dependency on both the supply voltage and the temperature. The oscillation frequency was calibrated to $2.00\,MHz$ at room temperature with $1.8\,V$ operating voltage by setting $R_m = 71\,k\Omega$ and $C_m = 0.18\,pF$. The average total current consumption is then $2.32\,\mu A$. The measured oscillation frequencies at different temperatures with different supply voltages are shown in Fig. 4. The maximum deviations from the calibrated value are $+2.5/-2\,\%$.

The frequency reference circuit presented here has a large tuning range, since both the oscillator and the biasing circuit can be adjusted. This can be seen in Fig. 5, where a few

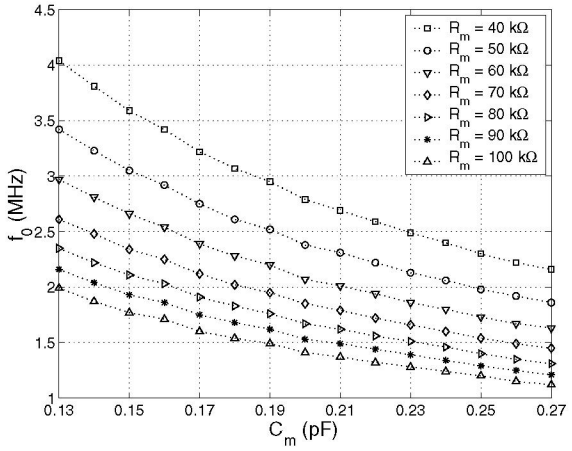

Fig. 5. A few calibration curves, showing the large tuning range of the oscillation frequency.

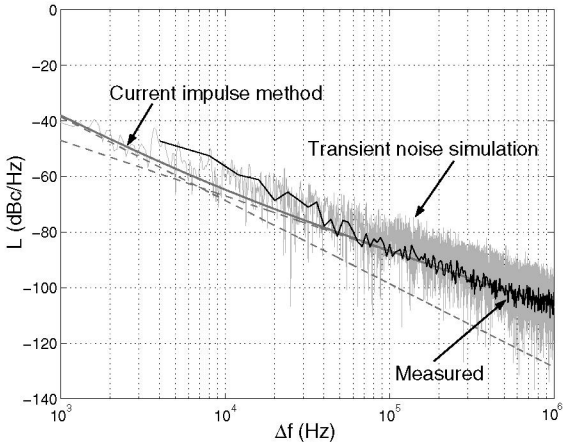

Fig. 6. Measured and simulated phase noise spectra, illustrating the good correspondence between the theory, the simulations and the measurements.

measured calibration curves are shown. Calibration can be done precisely, since C_m and R_m have been designed so that C_m can be tuned at intervals of $5\,fF$ and R_m at intervals of $1\,k\Omega$. Thus, Fig. 5 shows only a fraction of the total calibration points.

C. Phase noise and jitter

Fig. 6 shows the measured and two simulated phase noise spectra at room temperature with $1.8\,V$ supply voltage. Before the phase noise measurement, the circuit was calibrated by setting $R_m = 90\,k\Omega$ and $C_m = 0.145\,pF$. It can be seen that the measured spectrum agrees well with both the spectrum obtained with the current impulse method and the spectrum obtained with the transient noise simulation. In [3], there was some incoherence with the scaling of the phase noise curves formed using the current impulse method that is corrected here. The measured phase noise at $1\,MHz$ offset from the carrier is $-105\,dBc/Hz$. In addition, the effects of white noise and 1/f-noise on the phase noise are plotted separately for the current impulse method. These curves predict that $\Delta f_{1/f^3}$ corner frequency is about at $7\,kHz$. This corner frequency is impossible to predict from the spectra of the measured and the transient noise simulation due to low frequency resolution.

The cycle jitter can be approximated from the $1/f^2$-region of the phase noise spectrum with the equation [7]

$$\Delta t_c = \frac{\Delta f}{f_0^{3/2}} \sqrt{L\{\Delta f\}}, \tag{8}$$

where Δf is the offset frequency from the carrier, f_0 the oscillation frequency or the frequency of the carrier, and $L\{\Delta f\}$ the phase noise at certain offset frequency from the carrier. From the measured spectrum, it can be evaluated that the cycle jitter is $2.0\,ns$. Cycle-to-cycle jitter Δt_{cc} is then $\sqrt{2}$ times the cycle jitter, or $2.8\,ns$. Jitter increases in this circuit when temperature decreases. For example, in the case mentioned above, the cycle jitter is about $1.5\,ns$ at $+85\,^\circ C$ and about $5\,ns$ at $-35\,^\circ C$. The maximum cycle-to-cycle jitter value at $-40\,^\circ C$ can be extrapolated to be below $8\,ns$. Jitter also increases slightly when the supply voltage increases.

IV. CONCLUSIONS

In this paper, measurement results of a micropower $2\,MHz$ CMOS frequency reference fabricated with a $0.13\,\mu m$ CMOS process for capacitive sensor applications were presented. The frequency stability is optimized with symmetrical loads and supply independent biasing. The calibration can be performed accurately, since both the oscillator and the biasing circuit can be adjusted. The measured power consumption, frequency stability, phase noise and jitter agree well with the simulations.

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