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A Micropower Voltage, Current, and Temperature Reference for a Low-Power Capacitive Sensor Interface

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***Abstract*— In this paper, a micropower CMOS voltage, current, and temperature reference fabricated in a $0.13\,\mu\mathrm{m}$ CMOS process is presented. This bandgap-based circuit provides all reference voltages and currents, and temperature information for a low-power interface of a three-axis capacitive microaccelerometer. The total measured current consumption including all required reference voltage buffers, current mirrors, and scaling circuitry is $23.1\,\mu\mathrm{A}$. The simulated current consumption of the core circuit is $5.5\,\mu\mathrm{A}$. According to system measurements, the required resolutions, 10 bits for the reference voltages and 9 bits for the temperature reference, are achieved. The measured TC for the voltage reference is $9.9\,\mathrm{ppm}/^{\circ}\mathrm{C}$, and the analog output of the temperature reference is linear with a $4.9\,\mathrm{mV}/^{\circ}\mathrm{C}$ slope.**

I. Introduction

New applications of different kinds of microsensors have emerged, as advances in microfabrication technologies have made them increasingly affordable. The use of microsensors in battery-powered equipment requires the sensor interface to exhibit low power dissipation and a small die area required by low cost. These requirements can be met by integrating the whole sensor interface into one chip. The low power dissipation requirement makes designing the on-chip voltage, current, and temperature reference circuits challenging. The scaling of a bandgap-based voltage can be done easily with resistor trees, but the extra noise caused by the buffering is the problem. The noise level can be decreased only by increasing the current level, which is not desirable in the low-power application. Since the readout of the sensor takes place in a low frequency (typically a few kHz or less), duty cycles can be decreased aggressively in the interface circuits to lower power dissipation. This makes also possible the use of decreased duty cycles in certain parts of the reference circuits.

In this paper, a low-power voltage (VREF), current (IREF), and temperature (TREF) reference for a sensor interface that obtains a low power dissipation by exploiting time-multiplexing and decreased duty cycles is presented. A primary goal is to minimize the power dissipation of the continuously operating circuit blocks, such as the V/I/TREF core circuit, from which all the required references are generated.

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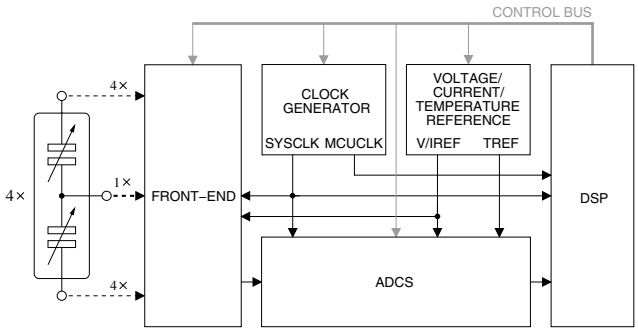

Fig. 1. Block diagram of a low-power interface for a three-axis capacitive microaccelerometer.

This reference circuit has to operate in the supply voltage range from 1.62 to $2.75\,V$ and in the temperature range from -40 to $+85\,^{\circ}C$. Section II describes both the sensor interface and the designed reference circuit. The measurement results are presented in Section III, and finally conclusions are made in Section IV.

II. Circuit Description

In this Section, first the sensor interface is described, and then the bandgap-based V/I/TREF core circuit, the required reference voltage buffers, and scaling circuitry for the TREF are presented.

A. Sensor Interface

The block diagram of a low-power interface for a three-axis capacitive microaccelerometer, composed of four proof masses, is shown in Fig. 1. Time-multiplexed sampling and duty cycles as low as $0.3\,\%$ are used to optimize the die area and power dissipation. The front-end [1] converts the capacitive acceleration information to a voltage. Two ADCs convert the acceleration and temperature information to the digital domain. These ADCs are powered down between their conversion cycles. The clock generator provides a $2\,MHz$ system clock (SYSCLK) [2], and a 1-$50\,MHz$ microcontroller unit clock (MCUCLK). The latter enables the use of a more computationally intensive DSP if required. The DSP performs signal processing in the digital domain and controls the

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functioning of all the other parts of the system. The bandgap-based voltage, current, and temperature reference considered in this paper is needed to provide all reference voltages and currents, and to generate the temperature information.

Mismatch in the reference voltages causes DC offset to the output of the front-end. This offset can be compensated by using DSP. The two ADCs using the capacitance ratio-independent algorithmic approach [3] are insensitive to capacitance ratio, amplifier offset voltage, and flicker noise. Therefore, the accuracy of the system is limited by the thermal noise. The maximum acceleration resolution of the system is 10 bits. The largest deviation allowed in the reference voltage caused by the RMS noise is $V_{REF}/2^{N+1}$, where V_{REF} is the designed reference voltage and N is the required resolution in bits. Temperature information enables the compensation of the temperature-dependent nonidealities. The system has to be able to compensate the temperature offset of 2LSB, meaning that the required accuracy for the TREF is 9 bits, or $125\,^{\circ}C/2^9 = 0.24\,^{\circ}C$.

The front-end and both ADCs need three reference voltages each; a positive reference (REFP), a negative reference (REFN), and an analog ground (AGND) voltage. These voltages are generated by using three buffers, because the duty cycles of the front-end and both ADCs differ from each other. The system has a common AGND of $0.9\,V$. The REFP and REFN voltages are designed to be adjustable at $50\,mV$ steps enabling the interface to be suited for sensors with different sensitivities.

The designed reference circuit, consisting of the V/I/TREF core, the required reference voltage buffers, and scaling circuitry for the TREF, is shown in Fig. 2. The REFBUF1 is the reference voltage buffer for the front-end, and REFBUF2 and REFBUF3 are the reference voltage buffers for the two ADCs. An off-chip resistor R7 is used to provide a more accurate and stable reference current. In the Fig. 2 all resistors at the outputs of the operational amplifiers, except R10, are used as the loads of the second stages of the corresponding operational amplifiers.

B. V/I/TREF Core

The V/I/TREF core is based on Brokaw's bandgap reference [4]. The reference voltage of $1.2\,V$ is of the form

$$V_{REF1V2} = V_{BE2} + 2\frac{R1}{R2}\frac{kT}{q} ln\left(\frac{A_{E1}}{A_{E2}}\right), \qquad (1)$$

where V_{BE2} is the base-emitter voltage of Q2, k the Boltzmann's constant ($1.38 \times 10^{-23}\,J/K$), T the absolute temperature, q the elementary charge ($1.602 \times 10^{-19}\,C$), and A_{E1} and A_{E2} are the emitter areas of Q1 and Q2. The reference voltage of $0.9\,V$ (V_{REF0V9}) is generated using two load resistors, R5 and R6, in series at the second stage of OPA1.

The resolution of the core circuit has to be better than 10 bits, to be on the safe side 12 bits, because extra operational amplifiers are required to buffer the aforementioned voltages. The resolution of 12 bits means that the maximum RMS noise voltage of the V_{REF1V2} can be $146.5\,\mu V$. It is practical

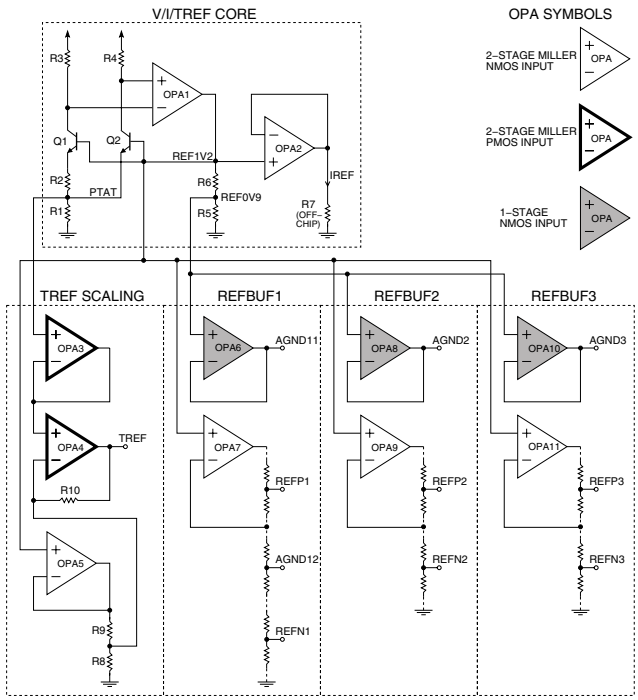

Fig. 2. The presented reference circuit.

to design OPA1 as narrow-band as possible to minimize the noise bandwidth. OPA1 is a two-stage Miller amplifier with NMOS input pair. Its bandwidth is limited by using a large compensation capacitor and a small bias current in the first stage. To minimize noise, large input and load transistors are used.

The proportional-to-absolute temperature voltage (V_{PTAT}) over resistor R1 is exploited in the temperature reference. It varies about from 0.42 to $0.65\,V$ over the temperature range from -40 to $+85\,^{\circ}C$. Because the voltage swing of $0.23\,V$ is not sufficient for the A/D conversion, the PTAT voltage must be buffered, amplified, and shifted to a proper voltage level.

The reference current of $1.0\,\mu A$ is generated by using an off-chip resistor R7 at the second stage of OPA2. All bias currents of the system, excluding the currents needed in the clock generator, are primarily mirrored from the second stage of the OPA2. A number of current mirrors and power down switches are also needed. The switches are used to turn off the circuit blocks according to their duty cycles. Cascode transistors are used to improve current mirroring ratios. The ADCs have different duty cycles and that is why their bias currents must be mirrored separately. The current mirrored directly from OPA2 must flow continuously, because the changing load of OPA2 would cause disturbances.

C. Reference Voltage Buffers

The accuracy requirements for the AGND voltages are not equally tight in all parts of the system. In the ADCs and in certain parts of the front-end the common-mode noise is not critical enabling the separate buffering of AGND and

REFP/REFN voltages. Therefore, one-stage operational amplifiers OPA6, OPA8, and OPA10 are used to buffer these AGND voltages with lower total current consumption. This separate AGND buffering relieves the loading of OPA7, OPA9, and OPA11 that are used to buffer the REFP and REFN voltages. The second stages of these operational amplifiers include resistor trees. OPA7 buffers also the AGND voltage for the parts of the front-end where the common-mode noise is critical.

The voltage difference between two adjacent taps in all three resistor trees is $50\,mV$. Each resistor tree has its own 4 to 16 decoder and the CMOS switches that enable choosing the desired voltage levels for the REFP and REFN. The resistor tree of OPA7 consists of 34 resistors while the resistor trees of OPA9 and OPA11 consist of 28 resistors, respectively. Both the front-end and the ADCs use SC technique, so the loading of the resistor trees changes depending on the clock phase. The resistance values of the unit resistors in the trees have been optimized to fulfill the settling requirements for the accuracy of 10 bits at the worst case with the maximum capacitive load. Settling requirements are tighter for the OPA9 and OPA11 due to higher clock frequencies in the ADCs meaning larger currents.

The REFBUF1 is always active in contrast to the REFBUF2 and REFBUF3 that go to the power down mode when they are not needed. Average current consumptions of the REFBUF2 and REFBUF3 are dropped remarkably as a consequence of decreased duty cycles. In power down mode all unnecessary bias currents are turned off by connecting the gates of the current source transistors to the ground or to the supply, depending on the transistor type.

D. TREF Scaling

Because the load of the V/I/TREF core is not allowed to change, OPA3 is needed to buffer the PTAT voltage. The current consumption of OPA3 has to be minimized, because its bias currents must flow continuously. At the same time, it is not allowed to add very much to the noise level of the PTAT voltage.

OPA5 and the resistors R8 and R9 are used to generate the voltage of $0.55\,V$ from the reference voltage of $1.2\,V$. The parallel connection of the resistors R8 and R9 forms the input resistor for the amplifier circuit formed by OPA4 and the resistor R10. The gain of the TREF amplifier is designed to be 2.68. Thus, the TREF voltage at the analog output changes about from 0.2 to $0.8\,V$, being proper for the A/D conversion.

The combined current consumption of OPA4 and OPA5 is not critical, because a small duty cycle, for example $0.3\,\%$ when the sampling rate of $100\,S/s$ is used, scales the current to a negligible value with respect to the total current of the system.

III. Experimental Results

Fig. 3 shows a microphotograph of the implemented reference circuit. Different circuit blocks are also marked. In this Section the IREF core along with the current mirrors and power down switches are included in the IREF. The largest circuit block is the V/TREF core. Resistors and capacitors require a remarkable part from the total area of the reference circuit that is $0.13\,mm^2$. The functionality of this reference circuit was measured over a temperature range of -35 to $+85\,^{\circ}C$, because of the limited temperature range of the temperature chamber.

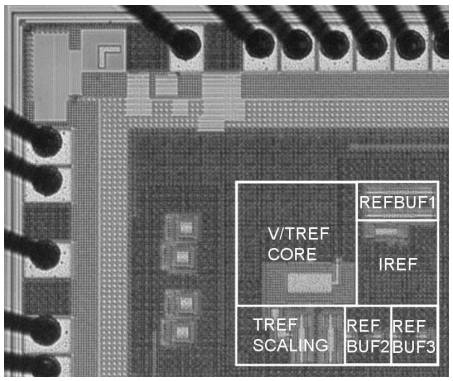

Fig. 3. Microphotograph of the presented reference circuit.

TABLE I
SIMULATED CURRENT CONSUMPTIONS.

	$I\,(\mu A)$	Duty cycle (%)	$I_{tot}\,(\mu A)$
V/TREF core	3.8	100	3.8 (14.3 %)
IREF	$6.7 + 1.5 + 1.5$	$100 + 10 + 0.3$	6.86 (25.8 %)
REFBUF1	8.3	100	8.3 (31.2 %)
REFBUF2	44	10	4.4 (16.5 %)
REFBUF3	44	0.3	0.13 (0.5 %)
TREF scaling	$3 + 31$	$100 + 0.3$	3.1 (11.7 %)
Total			26.6

The simulated current consumptions of different circuit blocks at room temperature, when all four proof masses are read at the sampling frequency of $1\,kS/s$, and the temperature reference at the sampling frequency of $100\,S/s$, are shown in Table I. The total current consumption of the reference circuit is $26.6\,\mu A$. The V/I/TREF core consumes $5.5\,\mu A$ that is about $20\,\%$ from the total current consumption. The IREF and REFBUF1 consume most current, $57.0\,\%$ in total. The current consumptions of the IREF and TREF scaling circuitry consist of more than one part with different duty cycles. The total measured current consumption of the reference circuit is $23.1\,\mu A$ at room temperature.

The temperature coefficient of the voltage reference in units of $ppm/^{\circ}C$ can be calculated using the equation [5]

$$TC = \frac{1}{V_{REF}} \frac{\Delta V_{REF}}{\Delta T} 10^6, \tag{2}$$

where V_{REF} is the reference voltage at room temperature, and ΔV_{REF} is the change of the reference voltage over the temperature range of ΔT. The simulated TC is about $6.7\,ppm/^{\circ}C$. When the ratio of the resistors R1 and R2 remains unchanged, but the absolute values change $20\,\%$, the TC of about $16\,ppm/^{\circ}C$ is achieved. In addition, for example, the effect of the resistor mismatch makes the TC even

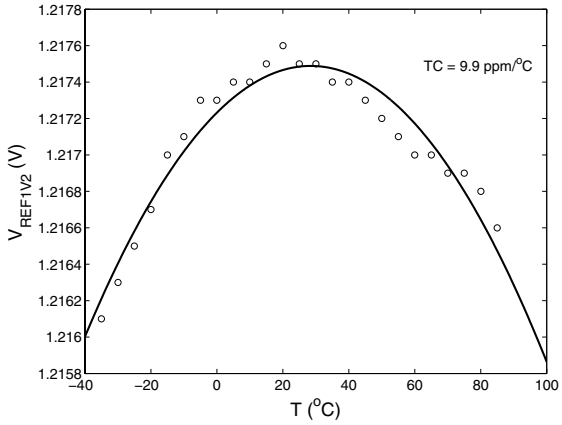

Fig. 4. Measured temperature dependency of the voltage reference.

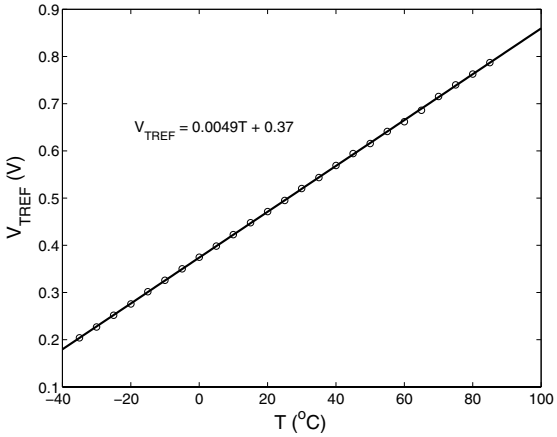

Fig. 5. Measured temperature dependency of the temperature reference.

worse. Fig. 4 shows the measured temperature dependency of the VREF. A temperature coefficient of $9.9\,ppm/\,^{\circ}C$ can be calculated according to the second order fitting curve. Fig. 5 shows the measured temperature dependency of the TREF. All the measured points fall near to the linear fitting curve with the slope of $4.9\,mV/\,^{\circ}C$.

The RMS noise voltage integrated over the bandwidth of $1\,Hz \ldots 1\,MHz$ was evaluated from the measured spectrum. The RMS noise voltage at the temperature of $+85\,^{\circ}C$ is about $150\,\mu V$ for the V_{REF1V2}, and about $340\,\mu V$ for the V_{TREF}, respectively. The resolution of the V_{REF1V2} in the V/I/TREF core is then about 12 bits resulting some margin for the noise caused by the extra buffering. The system measurements of the sensor interface show that the performance of the reference circuit presented here does not limit the overall performance of the system.

The measured REFP1 and REFN1 voltages for the front-end are shown in Fig. 6. The linear fitting curves with their equations are also shown. The order number of the bit combination n is shown on the horizontal axis. One of these 16 discrete voltage pairs of REFP1 and REFN1 is chosen using four control bits.

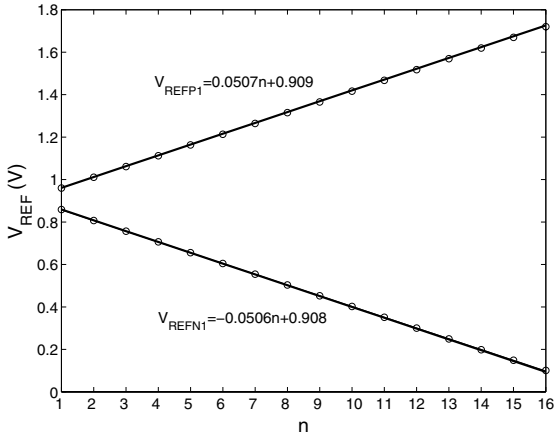

Fig. 6. Measured positive and negative reference voltage for the front-end.

TABLE II
PERFORMANCE SUMMARY.

Technology	$0.13\,\mu m$ CMOS
Supply voltage range	$1.62 \ldots 2.75\,V$
Temperature range	$-40 \ldots +85\,^{\circ}C$
Total current consumption	$23.1\,\mu A$ @ $1.8\,V$
TC of V_{REF1V2}	$9.9\,ppm/^{\circ}C$
TC of V_{TREF}	$4.9\,mV/^{\circ}C$
RMS noise of V_{REF1V2}	$150\,\mu V @ 1\,Hz \ldots 1\,MHz @ +85\,^{\circ}C$
RMS noise of V_{TREF}	$340\,\mu V @ 1\,Hz \ldots 1\,MHz @ +85\,^{\circ}C$

The summary of the measured performance is shown in Table II.

IV. CONCLUSION

In this paper, a micropower CMOS voltage, current, and temperature reference fabricated in a $0.13\,\mu m$ CMOS process for capacitive sensor applications was presented. The reference core consumes about $5.5\,\mu A$ and the whole reference circuit, including all needed reference voltage buffers, current mirrors, and scaling circuitry, consumes $23.1\,\mu A$. According to the system measurements, the accuracy of the VREF is sufficient for 10 bits and the accuracy of TREF is sufficient for 9 bits, respectively. The TC of $9.9\,ppm/\,^{\circ}C$ is achieved for the VREF, and the response of the TREF is linear with the slope of $4.9\,mV/\,^{\circ}C$.

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