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A Micropower Interface ASIC for a Capacitive 3-Axis Micro-Accelerometer

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***Abstract*—In this paper, a micropower interface IC for a capacitive 3-axis micro-accelerometer implemented in a 0.13-μm BiCMOS process is presented. The sensor interface consists of a front-end that converts the acceleration signal to voltage, two algorithmic ADCs, two frequency references, and a voltage, current, and temperature reference circuit. Die area and power dissipation are reduced by using time-multiplexed sampling and varying duty cycles down to 0.3%. The chip with a 0.51 mm^2 active area draws 62 μA from a 1.8 V supply while sampling temperature at 100 Hz, and four proof masses, each at 1.04 kHz. With a $\pm$4-g capacitive 3-axis accelerometer, the measured noise floors in the x-, y-, and z-directions are 482 $\mu g/\sqrt{Hz}$, 639 $\mu g/\sqrt{Hz}$, and 662 $\mu g/\sqrt{Hz}$, respectively.**

***Index Terms*—Capacitive sensor interface circuit, low-power circuit, microelectromechanical system (MEMS), switched-capacitor circuit, three-axis accelerometer, time multiplexing.**

I. Introduction

MICRO-ACCELEROMETERS are micromachined acceleration sensors with dimensions ranging from 1 μm to 1 mm. They find a wide range of applications, including automotive safety and stability control systems, various navigation and guidance systems, vibration monitoring in industrial environments, movement detection in hand-held mobile terminals and control devices such as game controllers, and different biomedical applications, for example.

The readout mechanism of a micro-accelerometer can be, for instance, piezoelectric, piezoresistive or capacitive [1]. Capacitive accelerometers have advantages such as zero static biasing current, the capability of high sensitivity, and excellent thermal stability, making their use in low-power applications attractive. By using a single capacitive accelerometer with a proper configuration, accelerations along all three axes can be measured simultaneously [2], [3]. The structural element of these devices, together with eight fixed electrodes, forms four differential capacitor pairs. All three vector components of linear acceleration, x-, y-, and z-directional, can be evaluated by first measuring these capacitances, and then taking their proper linear combinations. Additionally, the configuration provides redundancy so that fault conditions can be detected.

The use of microsensors in battery-powered equipment requires the sensor interface to exhibit low power dissipation. An inexpensive, yet reliable, highly-sensitive and low-power 3-axis accelerometer with digital output would have a wide range of applications. In order to realize this kind of a sensor, the readout electronics has to be integrated together with the sensor element at chip or module level, forming a microelectromechanical system (MEMS).

In this paper, a micropower interface IC [4] designed for a capacitive 3-axis micro-accelerometer [2] is presented. A majority of the recently published micro-accelerometers have been based on the electromechanical force-balancing $\Sigma\Delta$ loop. This idea has been first reported in 1990 in [5], and since many implementations have been published [6]–[9]. The implementation presented in this paper, in contrast, operates in open-loop configuration [10]. The reasons for this are simple implementation that reduces both silicon area and power dissipation, and a limited voltage range available for electrostatic feedback.

To achieve a wide and linear acceleration range in open-loop configuration, the major linearity-limiting factors have to be carefully taken into account. The most significant ones are the nonsymmetrical and nonlinear electrostatic forces, and the nonlinear displacement-to-capacitance conversion. Both of these factors have been addressed in the front-end design.

The paper is organized as follows. The system is first briefly described in Section II. Different circuit blocks used in the implementation are presented in Section III. In Section IV, the measurement results of the implemented prototype are presented. Finally, conclusions are drawn in Section V.

II. System Description

The block diagram of the sensor interface is shown in Fig. 1. The system is otherwise fully integrated, apart from the off-chip digital signal processing (DSP) and a single resistor which provides a more accurate and stable reference current. The front-end [11] converts the capacitive acceleration information to voltage. Two algorithmic A/D converters (ADCs) [12] convert the acceleration and temperature information to the digital domain. These ADCs are powered down between their conversion cycles. The A/D conversions could have been performed also with a single ADC. However, because the

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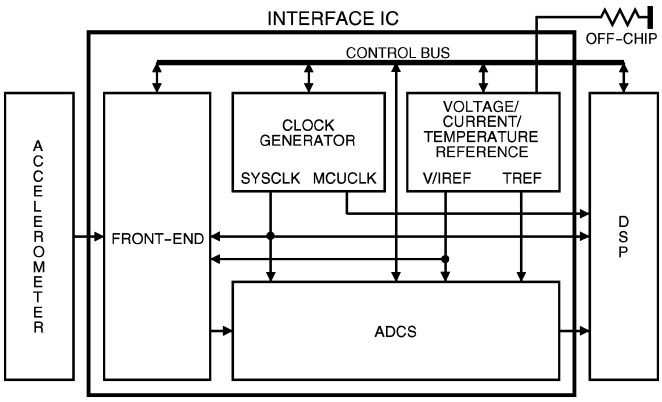

Fig. 1. Block diagram of the implemented interface IC for a 3-axis capacitive micro-accelerometer.

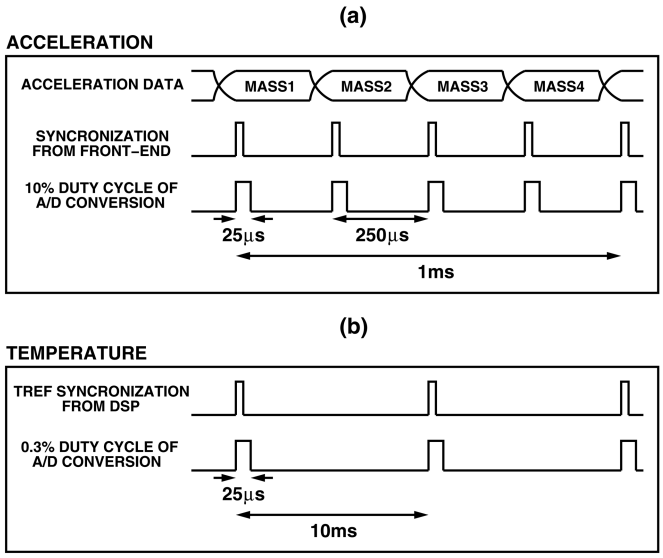

Fig. 2. Use of varying duty cycles in the A/D conversion of (a) acceleration and (b) temperature.

impact of two ADCs on current and silicon area consumption is not significant, the ADCs were decided to be kept independent to keep the implementation more straightforward. The clock generator comprises a 2 MHz system clock generator (SYSCLK) [13], and a 1–50 MHz microcontroller unit clock generator (MCUCLK). The latter enables the use of a more computationally-intensive DSP, if required. The bandgap-based voltage, current, and temperature reference (V/I/TREF) [14] provides all reference voltages and currents, and also the temperature information. The off-chip DSP that is used to control the functioning of the system is currently implemented with computer software.

The main specifications for the sensor interface are low current consumption ($< 100\ \mu$A) and a 10-bit resolution with a $\pm$4-g full-scale input signal ($\mathrm{g} = 9.81\ \mathrm{m/s^2}$) at 100 Hz bandwidth. The system requires two supply voltages, a 1.2 V supply for the MCUCLK, and a 1.8 V supply for all the other circuit blocks. The SYSCLK and the V/I/TREF are designed to work properly up to 2.75 V, without extra calibration. The required operating temperature range is from -40 to $+85\,^{\circ}$C.

The chosen approach to use the front-end with a charge-balancing behavior requires time-multiplexed sampling of the four proof masses of the 3-axis capacitive micro-accelerometer, because the masses have a common middle electrode. Time-multiplexed sampling enables the reading of one, two, or four masses (1-, 2-, or 3-axis operation). Since the readout of the sensor takes place in a low frequency, typically a few kilohertz or less, duty cycles can be decreased aggressively in the interface circuits to lower power dissipation. Nominally, the front-end, which is always-active, samples each proof mass at 1 kHz. The maximum possible sampling frequency per mass is 10 kHz. Fig. 2 describes the duty cycles relating to the A/D conversion of acceleration and temperature. In the case of acceleration, a synchronization pulse created by the front-end is used to trigger the A/D conversion of time-multiplexed data to start. The conversion time of the ADCs is fixed to approximately 25 μs (24 μs plus a start-up period), after which they power down. Because the temperature changes slowly, a 100 Hz synchronization pulse from the DSP is used in the case of the TREF. The ADCs generate the required power-down signals for the V/I/TREF.

Mismatch between the static parts of the sensor capacitors causes dc offset to the output of the front-end. This offset can be compensated for by using DSP. In order to accommodate for the offset voltages at the output of the front-end, the ADCs are designed to have a 12-bit resolution. The required reference voltages for the ADCs must also have a resolution of 12 bits. From the voltage reference point of view, the accuracy requirement means that the largest deviation allowed in the reference voltage, caused by the rms noise, is $V_{\mathrm{REF}}/2^{N+1}$, where V_{REF} is the designed reference voltage and N the required resolution in bits. Jitter performance requirement for the system clock can be approximated with the equation

$$\Delta t_{\max} = \frac{1}{2\pi f 10^{\mathrm{SNR[dB]}/20}} \tag{1}$$

where f is the frequency of a sinusoidal input signal, and $\mathrm{SNR[dB]}$ the required signal-to-noise ratio in decibels. The maximum frequency of the acceleration signal is 5 kHz. Thus, the maximum jitter value for 10-bit resolution is 31 ns. Equation (1) assumes that jitter has a white noise spectrum.

Temperature information makes possible the compensation of the temperature-dependent nonidealities, such as offset. By using the designed 9-bit temperature reference, a $\pm FS/4$ offset variation over temperature can be compensated in a 10-bit interface, without degrading the SNR.

III. Circuit Design

In this section, first the structure and operation of the capacitive 3-axis accelerometer is presented. After that the designed building blocks, namely the front-end, the algorithmic ADC, operational amplifiers used in the front-end and the ADCs, the clock generator, and the voltage, current, and temperature reference, are presented.

A. Accelerometer

A capacitive 3-axis accelerometer and its operation are illustrated in Fig. 3. As discussed earlier, the sensor element con-

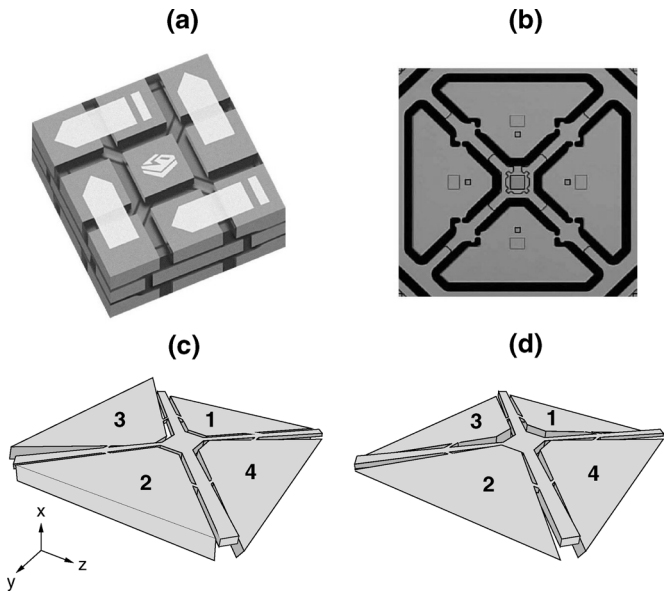

Fig. 3. (a) Encapsulated accelerometer [2], (b) top view of the structural element of the accelerometer (Images courtesy of VTI Technologies, Vantaa, Finland), the sensor element under (c) z-directional and (d) x-directional acceleration.

sists of four differential capacitor pairs, which have a common middle electrode, but top and bottom electrodes of their own. Acceleration causes torque, which tilts the proof masses. This causes the capacitance to change. For example, in Fig. 3(c), the sensor element is under z-directional acceleration. In this case, only masses 3 and 4 react by tilting to opposite directions. In Fig. 3(d), the sensor element has acceleration to x-direction. In that case, all four masses tilt to the same direction. By reading the capacitances with a sensor interface, the accelerations in all three directions can be found as

$$\begin{bmatrix} a_x \\ a_y \\ a_z \end{bmatrix} = \frac{\sqrt{2}}{A_{C/a}} \begin{bmatrix} 1 & 1 & 1 & 1 \\ -1 & 1 & 0 & 0 \\ 0 & 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} \Delta C_{D1} \\ \Delta C_{D2} \\ \Delta C_{D3} \\ \Delta C_{D4} \end{bmatrix} \quad (2)$$

where a_x, a_y, and a_z are the three linear acceleration components, $A_{C/a}$ is the gain from the acceleration in the direction of the sensitive axis of each mass to the capacitance, and ΔC_{Dn} with $n = 1$, 2, 3, or 4 are capacitance differences of the sensor capacitors ($\Delta C_{Dn} = C_{\mathrm{DP}(n)} - C_{\mathrm{DN}(n)}$). Equation (2) assumes that the conversion gain from the acceleration to the capacitance is equal for all four masses. The used subindexing corresponds to the numbering of the proof masses in Fig. 3. The $\sqrt{2}$ coefficient in (2) is caused by the 45° angle between any acceleration vector (x, y, or z) and the sensitive axes of the masses that respond to the acceleration [2].

B. Front-End

To reduce the distorting effects of the electrostatic forces, the single-ended self-balancing bridge [15] was chosen as the starting point in the design of the front-end. Power dissipation and die area of the designed front-end shown in Fig. 4 are optimized by using time-multiplexing. It makes also possible the reading of one, two, or four proof masses of the 3-axis accelerometer. The clock frequency and biasing currents of the front-end are programmable. Performance of the front-end was further improved by adding the following options: correlated double sampling (CDS) to reduce noise, chopper stabilization to reduce offset voltage and noise, and from single-ended to differential conversion to make possible a more effective use of signal range in the ADC.

The attractive electrostatic force between the electrodes of a parallel-plate capacitor is

$$F = \frac{Q^2}{2\varepsilon_r \varepsilon_0 A} \quad (3)$$

where Q is the charge in the capacitor, ε_r the relative permittivity of the insulator, ε_0 the permittivity of a vacuum, and A the plate area. Under acceleration, the capacitances $C_{\mathrm{DP}(n)}$ and $C_{\mathrm{DN}(n)}$ are not equal. Thus, the electrostatic forces are not equal, if these capacitors are biased by a constant voltage. This inequality of the electrostatic forces causes distortion [16]. Thus, to retain the wide linear region of the accelerometer, these forces have to be balanced.

The self-balancing bridge changes the voltage of the middle electrode $\mathrm{D_{MID}}$ such that the charges in the sensor capacitors $\mathrm{C_{DP(n)}}$ and $\mathrm{C_{DN(n)}}$ are equal, and thus the electrostatic forces are also equal. In basic operation mode, when CDS and chopper stabilization are not used, this balance is achieved by repeating the two main clock phases, reset phase ϕ_2 and measurement phase ϕ_1, as shown in Fig. 4. At the beginning of the clock phase ϕ_2, the mass being read is changed and the output voltage of the previous cycle is loaded into the capacitors $\mathrm{C_{4P}}$ and $\mathrm{C_{4N}}$. This voltage was stored in the capacitors $\mathrm{C_{3Pn}}$ and $\mathrm{C_{3Nn}}$ of the latter integrator. Now, the voltage of $\mathrm{D_{MID}}$ is equal to V_{OUTP}. During the clock phase ϕ_2, the output is in hold mode, and thus it can be sampled by the ADC. The loading of the front-end is relieved by first sampling the output to the ADC during a 0.5 μs sampling period, and only thereafter connecting the output of the front-end to feedback. In the clock phase ϕ_1, the mass being read is connected to the reference voltages and the difference of the charges flowing into $\mathrm{C_{DP(n)}}$ and $\mathrm{C_{DN(n)}}$ is integrated. This same cycle is repeated after the other three masses are read each in turn. The output voltage V_{OUT} and thus the voltage of $\mathrm{D_{MID}}$ changes until charge balance is achieved.

To be able to solve this balance voltage, the transfer function for the front-end has to be derived. The transfer function is

$$H(z) = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{REF}}} = \frac{2\left(C_{\mathrm{DP}(n)} - C_{\mathrm{DN}(n)}\right)}{\frac{C_1 C_3}{C_2}(1 - z^{-1}) + \left(C_{\mathrm{DP}(n)} + C_{\mathrm{DN}(n)}\right) z^{-1}} \quad (4)$$

for each $n \in [1 \ldots 4]$. In Fig. 4, the upper and lower branches are identical, and therefore only the first characters of the subindexes of the capacitors in (4) are used.

At dc, the transfer function simplifies to

$$H(1) = \frac{2\left(C_{\mathrm{DP}(n)} - C_{\mathrm{DN}(n)}\right)}{C_{\mathrm{DP}(n)} + C_{\mathrm{DN}(n)}}. \quad (5)$$

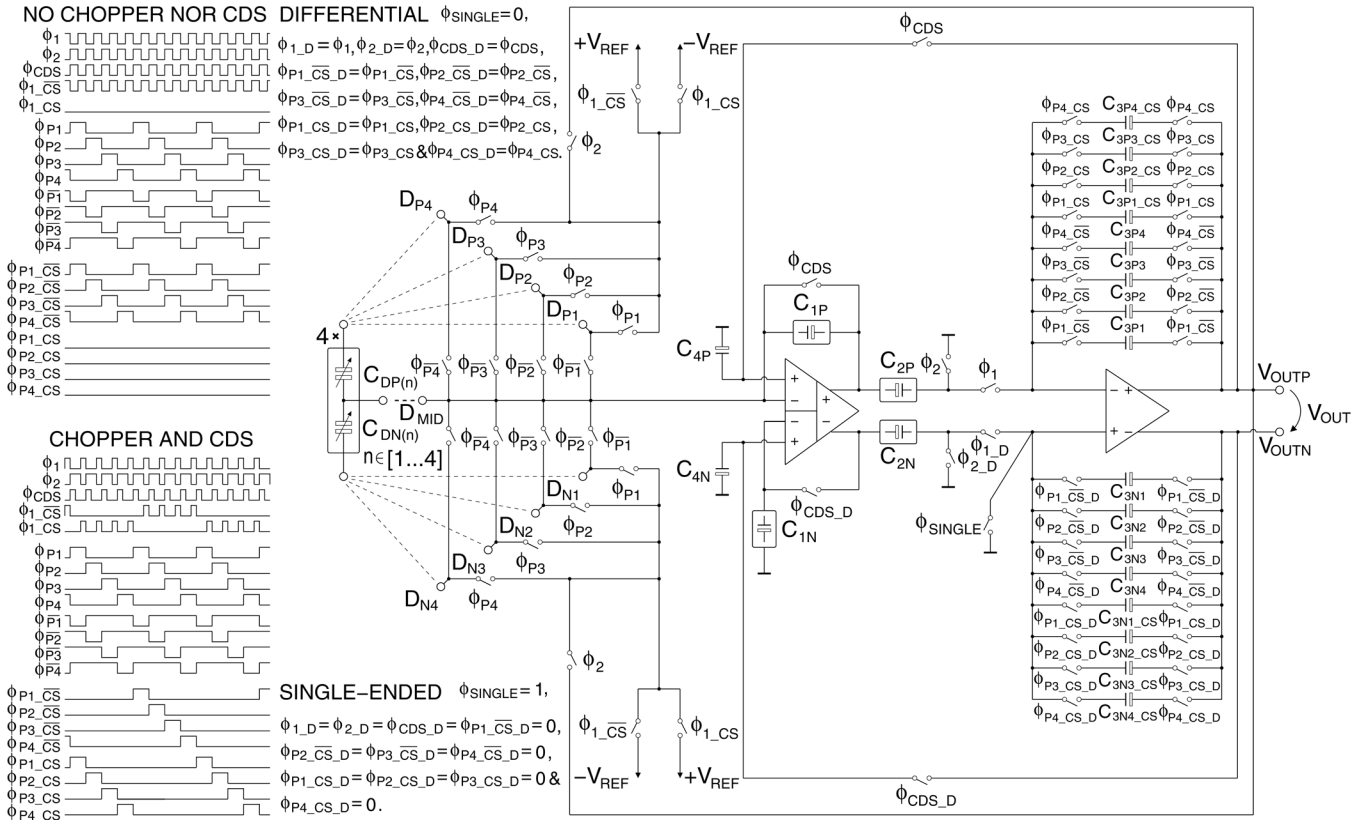

Fig. 4. Schematic of the front-end.

If the capacitors $C_{DP(n)}$ and $C_{DN(n)}$ are again modeled as simple parallel-plate capacitors, their capacitances under acceleration can be written as

$$C_{DP} = \frac{A\varepsilon_r\varepsilon_0}{d-\Delta d} = C_0\left(\frac{d}{d-\Delta d}\right),$$
$$C_{DN} = \frac{A\varepsilon_r\varepsilon_0}{d+\Delta d} = C_0\left(\frac{d}{d+\Delta d}\right). \quad (6)$$

Here, d is the initial distance between the capacitor plates, Δd the change in plate distance induced by acceleration, and C_0 the capacitance with $\Delta d = 0$. By substituting (6) into the dc transfer function (5), we obtain

$$H(1) = \frac{2\Delta d}{d}. \quad (7)$$

This equation shows that the output voltage of the front-end is ratiometric, in other words, the output is linearly proportional to Δd, and hence to the acceleration.

The cancellation of the distorting effects of the electrostatic forces, and the ratiometricity are valid only if the capacitors $C_{DP(n)}$ and $C_{DN(n)}$ can be modeled as parallel-plate capacitors. When the tilting of the masses is taken into account, the effectiveness of both of these linearization properties is reduced.

When CDS is used, an extra clock phase ϕ_{CDS} is required. In the case of chopper stabilization, the masses are read with inverted and non-inverted reference voltages, and both output voltages are stored in their own integrator capacitors. Thus, four extra capacitors and clock phases are required to implement chopper stabilization. When the single-ended to differential conversion is used, the first amplifier operates as a differential difference amplifier (DDA). Making the signal path after the first amplifier differential results in larger dynamic range at the cost of higher power dissipation and larger die area. Capacitors C_{1P}, C_{1N}, C_{2P} and C_{2N} are implemented as matrices to enable the adjustment of the -3 dB point of the front-end according to (4).

C. Algorithmic ADC

The algorithmic ADC uses the same hardware to do the A/D conversion in successive cycles. Hence, it requires very little silicon area, and is a suitable candidate for sensor applications. Furthermore, the algorithmic architecture makes it possible to use a variable sampling rate and resolution together with time-multiplexed sampling, and causes low loading for the front-end and voltage reference. The programmable duty cycles of the ADCs and the respective references allow more flexible control of the current consumption.

The algorithmic ADC is based on a binary search algorithm, which determines the closest digital word to match an input signal. On every cycle, the signal is doubled and a positive or negative reference voltage is added according to

$$V(i) = 2V(i-1) + (-1)^{\mathrm{BIT}(i-1)}V_{\mathrm{REF}} \quad (8)$$

where the number of cycle $i \in [2\ldots N]$, N is the resolution of the A/D conversion, $V(i)$ the signal on the ith cycle, $V(1) = V_{\mathrm{IN}}$, $\mathrm{BIT}(i-1)$ the bit resolved on the previous cycle, and V_{REF} the reference voltage. The minimum conversion time, or number of cycles, for an algorithmic ADC corresponds to the resolution

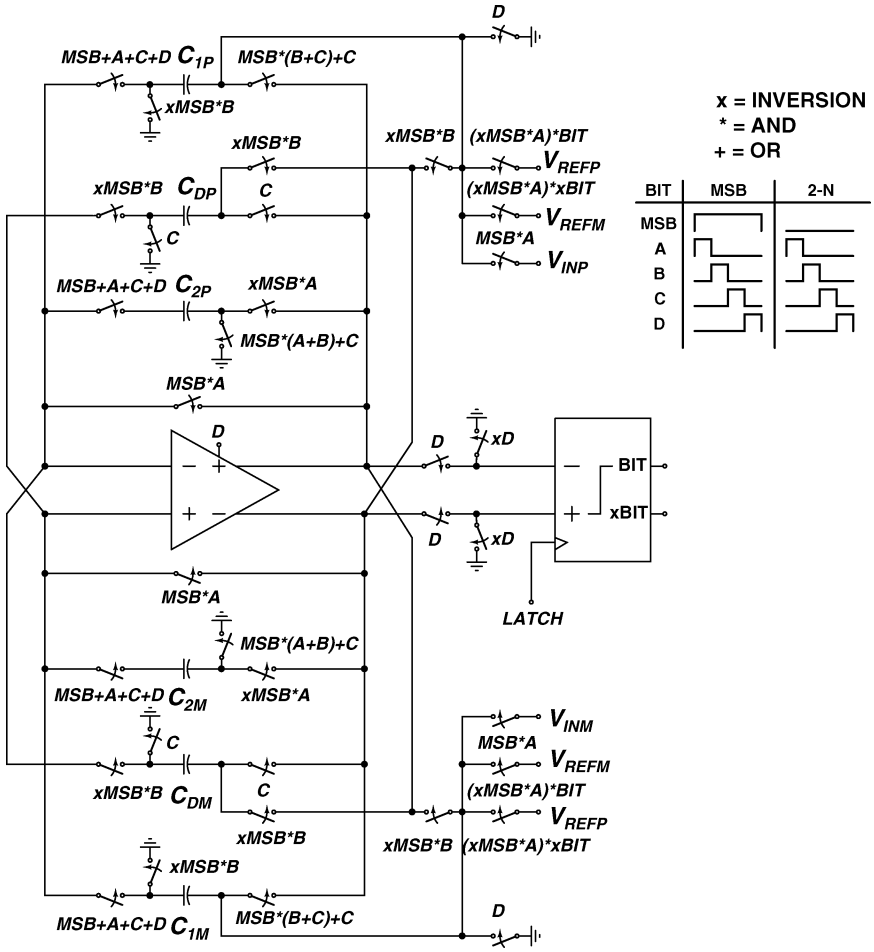

Fig. 5. Schematic of the ADC.

of the A/D conversion in bits. Typically more than one clock step is required to resolve one bit.

The system clock and the maximum sampling rate set the upper limit for the algorithmic ADC operation steps per bit and limit the available topologies. The proper generation of nonoverlapping clock phases requires a duty cycle of 50%. Thus, the system clock must be divided by two before the clock is fed to the clock generator. Hence, the maximum number of operation steps per bit N_{steps} is limited to

$$N_{\text{steps}} \leq \frac{f_{\text{clk}}/2}{N(f_s/2)} \tag{9}$$

where f_{clk} is the frequency of the system clock, N the number of bits, and f_s the sampling rate. The system parameters for A/D conversion with maximum speed and accuracy are $f_{\text{clk}} = 2$ MHz, $N = 12$, and $f_s = 40$ kHz. The resulting number of steps $N_{\text{steps}} \leq 4.1667$. Therefore, the maximum number of steps per bit in the system is four.

The most important factors limiting the switched capacitor (SC) algorithmic ADC accuracy are noise, operational amplifier gain and bandwidth, and capacitor matching. In a straightforward implementation of an SC algorithmic ADC [17], the multiply-by-two operation depends on the capacitor ratios. Hence, the achievable accuracy is limited by the capacitor matching to 10 bits [18]. However, it is possible to implement algorithmic ADC using a capacitance ratio-independent technique [19]. This technique makes the algorithmic A/D conversion independent of the capacitance ratios, which reduces silicon area and makes it possible to implement an over-10-bit ADC without digital calibration.

The presented ADC, shown in Fig. 5, fulfills the system speed requirements by using four clock steps to resolve one bit polarity. The ADC is insensitive to capacitance ratio, amplifier offset voltage, input parasitics, and flicker noise. It requires only one differential amplifier, a dynamic latch, six 2 pF capacitors, 36 switches, and some digital logic. Thus, the active die area for a single ADC is only 0.04 mm^2. The dynamic latch is well suited to low-power applications, since it does not consume static power. The switches are minimum length switches to minimize charge injection. Furthermore, the bottom plate sampling is used to cancel the charge injection. All the switches connected to the amplifier inputs or to ground are implemented as N-channel MOS switches and switches connected to amplifier outputs are implemented as CMOS-switches.

The operating phases of the implemented ADCs are shown in Fig. 6. The total conversion time is $4 \cdot N = 48$ clock steps, where the number of bits $N = 12$. Phases 1–4 constitute the cycle to solve the most significant bit (MSB), and phases 5–8 are recycled to resolve the rest of the bits.

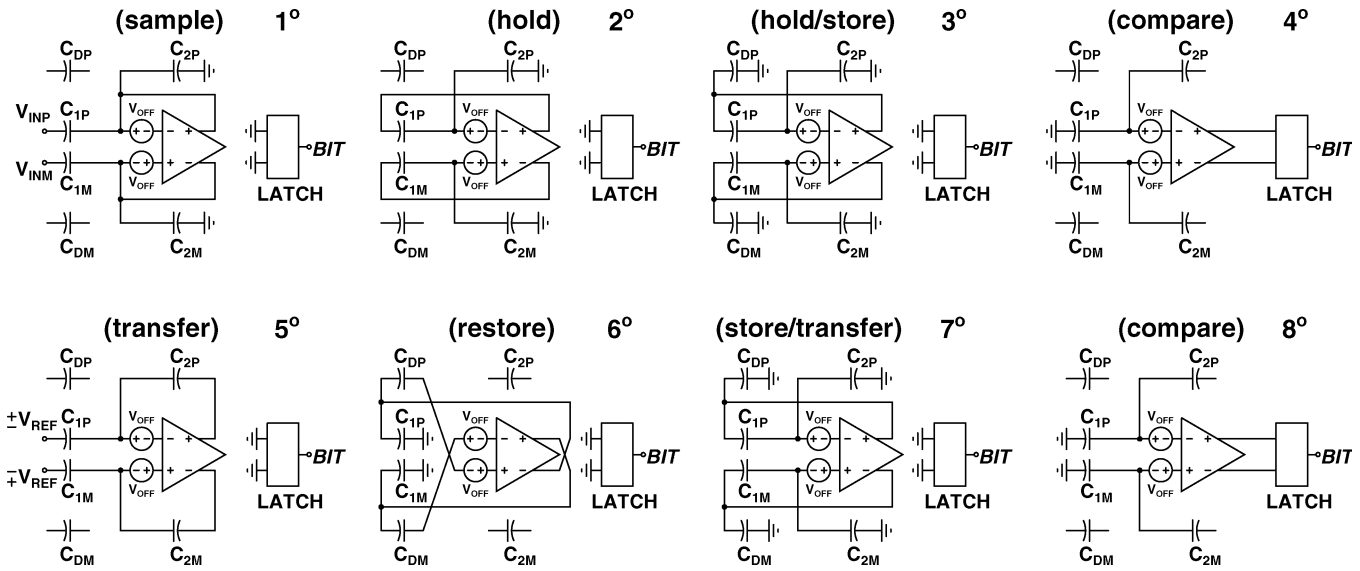

Fig. 6. Operating phases of the ADC.

In phase 1, the input signal $V_{\rm IN}$ is sampled and concurrently the amplifier offset voltage $V_{\rm OFF}$ is stored in capacitors $\rm C_1$ and $\rm C_2$. In the second phase, the amplifier is in hold-mode, and the amplifier offset voltage is cancelled. In phase 3, the amplifier output voltage is stored in capacitor $\rm C_D$ for the next cycle. The accurate output voltage in phase 3, taking into account the finite operational amplifier gain A, is

$$V(1)=\frac{1}{1+\frac{1}{A}+\frac{1}{kA}}V_{\rm IN}+\frac{\frac{k+1}{A+1}}{\frac{A+1}{A}k+\frac{1}{A}}V_{\rm OFF} \qquad (10)$$

where $k = C_1/C_2$ is the capacitor ratio. When $A \to \infty$, the output voltage $V(1) = V_{\rm IN}$. In phase 4, the amplifier is in open-loop configuration. The bottom plate of capacitor $\rm C_2$ is floating, so that the capacitor does not load the amplifier input. The capacitor $\rm C_D$ floats, and thus holds the sampled input signal. In phase 4, the polarity of the sampled input voltage is resolved. If there is parasitic capacitance $\rm C_P$ at the amplifier input, some of the charge stored in capacitor $\rm C_1$ is transferred to this parasitic capacitance, reducing the input voltage at the amplifier input by a factor of $C_1/(C_1+C_P)$. The amplifier offset voltage is cancelled since it is stored in capacitors $\rm C_1$ and $\rm C_P$ in previous phases. The reduction of the input voltage is not a problem, if the amplifier is capable of resolving the input voltage difference correctly, since in the following phase, the charge transferred to capacitor $\rm C_2$ remains independent of the amplifier input parasitic capacitance. In phase 4, the dynamic latch is connected to the amplifier output and the amplifier magnifies the differential input voltage to be larger than the offset voltage of the dynamic latch.

Next, the operating phases 5–8 are described. These phases are recycled $(N-1)$ times for N-bit resolution. First, in phase 5, the bottom plate of capacitor $\rm C_1$ is connected to a positive or negative reference voltage according to (8), and the charge in capacitor $\rm C_1$ is transferred to capacitor $\rm C_2$. Charge stored in amplifier input parasitic capacitances is also transferred to capacitor $\rm C_2$. In phase 6, the same charge that was sampled in the first phase to capacitor $\rm C_1$ is now restored in capacitor $\rm C_1$. This is accomplished using offset polarity reversing [20], [21]. The polarity of the offset voltage is changed by cross-connecting the differential amplifier inputs and outputs during this phase. Phase 7 is identical to phase 3. In phase 7, the charge transferred to capacitor $\rm C_2$ in phase 5 is now transferred back to capacitor $\rm C_1$. As a result, the capacitance mismatch between capacitors $\rm C_1$ and $\rm C_2$ is cancelled. Neglecting higher order terms $(1/A)^2$, the resulting output voltage in phase 7 and also in the following cycles can be expressed as

$$V(i)\approx\frac{\left(2k+\frac{k^2}{A}+\frac{4k}{A}+\frac{1}{A}\right)V(i-1)}{k+\frac{k^2}{A}+\frac{3k}{A}+\frac{1}{A}} +\frac{\left(k+\frac{2k}{A}\right)(-1)^{\mathrm{BIT}(i-1)}V_{\rm REF}+\frac{k}{A}V_{\rm OFF}}{k+\frac{k^2}{A}+\frac{3k}{A}+\frac{1}{A}}. \qquad (11)$$

When $A \to \infty$, the output voltage is equal to ideal output shown in (8). Finally, the output voltage $V(i)$ is stored in capacitor $\rm C_D$ for the next cycle. Phase 8 is identical to phase 4. In phase 8, the polarity of the output voltage $V(i)$ is resolved for the next cycle. Phases 5–8 are then recycled to resolve the desired number of bits.

Since the algorithmic ADC operates in consecutive cycles, where the output depends on the output of the previous cycle, the conversion errors caused by finite operational amplifier gain and incomplete settling cumulate in the algorithmic A/D conversion, and determine the achievable conversion accuracy. When finite gain, offset voltage, and capacitor mismatches are taken into account, the gain requirements for the operational amplifier can be calculated using (11). Assuming that the operational amplifier bandwidth does not limit the performance, to keep the calculated INL and DNL below $\pm$1/2 LSB, the resulting gains for 10- and 12-bit accuracies are 68 dB and 80 dB, respectively. With these gains, the error remains within $\pm$1/2 LSB up to capacitor mismatch of $k = 2$ and amplifier offset voltage $V_{\rm OFF}$ of hundreds of millivolts. The gain requirement does not decrease significantly even with smaller values of k or $V_{\rm OFF}$.

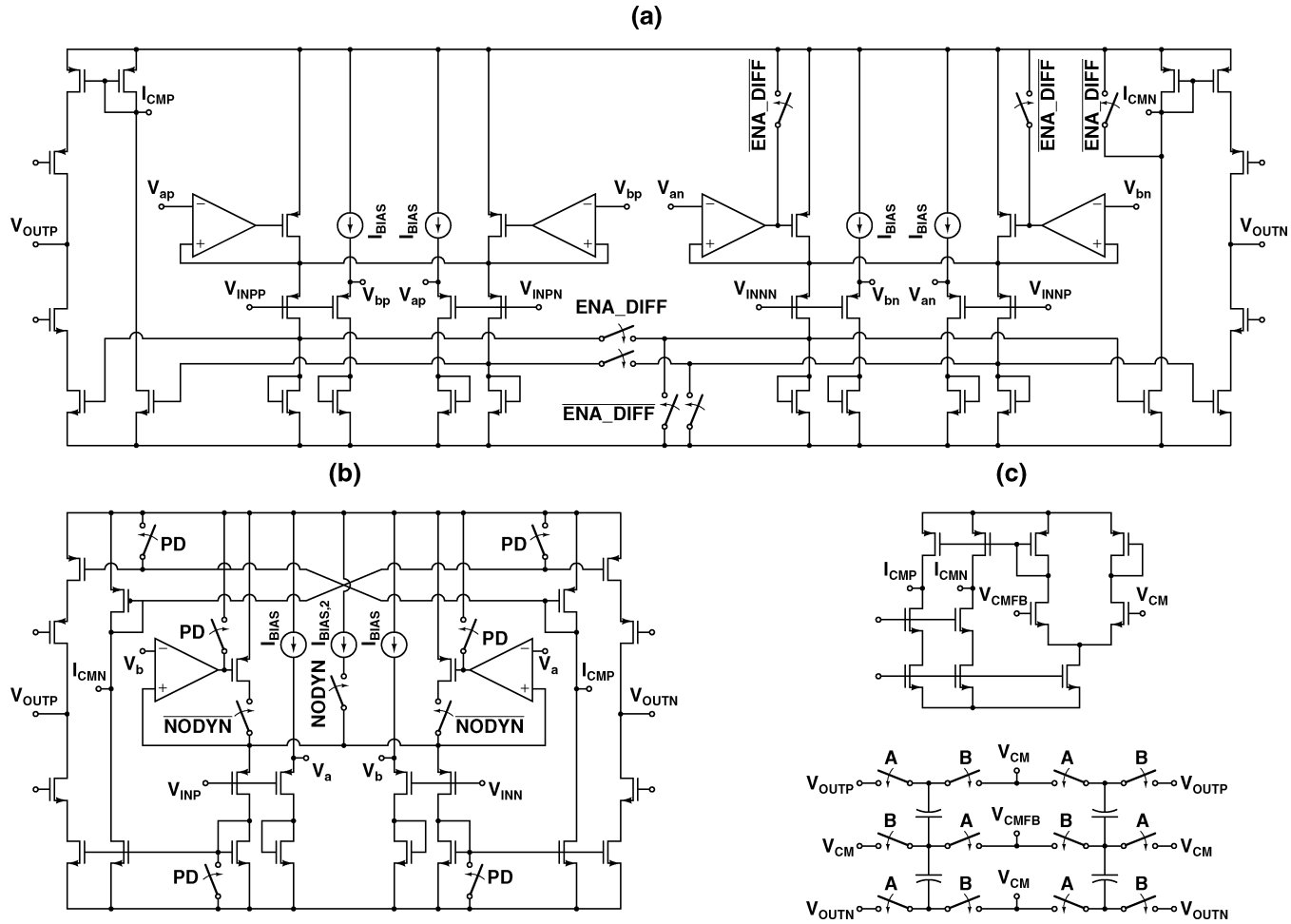

Fig. 7. (a) Schematic of the DDA used in the front-end. (b) Schematic of the operational amplifier used in the ADCs. (c) Schematic of the double-sampling CMFB circuit used in the amplifiers in the front-end and the ADCs.

Even though the operation is insensitive to capacitance mismatches, large mismatches between differential branches give rise to harmonic distortion. However, drawing the layout for the differential capacitors in common-centroid ensures that the harmonic distortion due to the mismatches is negligible.

D. Operational Amplifiers

The operational amplifiers account for a major part of the current consumption in the front-end and in the two ADCs. To minimize power dissipation while driving a capacitive load, a tail-current-boosted Class AB operational amplifier [22] is utilized. In such an amplifier, the bias current increases quadratically proportional to the differential input voltage. The input pair is designed to operate in weak inversion under quiescent conditions, that is, when the differential input voltage is zero. This is to maximize the current efficiency g_m/I_D, where g_m is the transconductance of the device and I_D the biasing current.

The DDA used in the front-end is shown in Fig. 7(a). The original implementation of [22] has been converted into a DDA by adding another tail-current-boosted input pair and summing the currents. The mode between the single-ended and the DDA operation can be chosen with the enable signal ENA_DIFF. Other differences compared to the original implementation are the differential outputs and the additional diodes where the biasing currents I_{BIAS} are steered instead of mirroring them to the output, thus slightly saving in current consumption.

The amplifier used in the ADCs is shown in Fig. 7(b). When this amplifier is used as a comparator in phases 4 and 8, tail-current boosting is disabled with the signal NODYN, replacing the dynamically controlled current sources with the static current source $I_{\mathrm{BIAS},2}$. When the ADC is powered down, the signal PD is used to power down the amplifier. Similar modifications compared to the original implementation as in the DDA were also made to this amplifier.

The second amplifier in the front-end is similar to the one in Fig. 7(b), without the PD and NODYN signals, and their respective switches. Instead, signal ENA_DIFF is implemented to choose between the single-ended and differential operation. In single-ended mode, the negative output is disabled and current-mirroring ratios are changed, in order to keep the gain-bandwidth product (GBW) constant. Additionally, this amplifier employs the method described in [23] to increase the dc gain.

All the three amplifiers use the same kind of double-sampling common-mode feedback (CMFB) topology shown in Fig. 7(c). In the DDA, asymmetrical loading of the differential outputs due to the front-end configuration was taken into account when

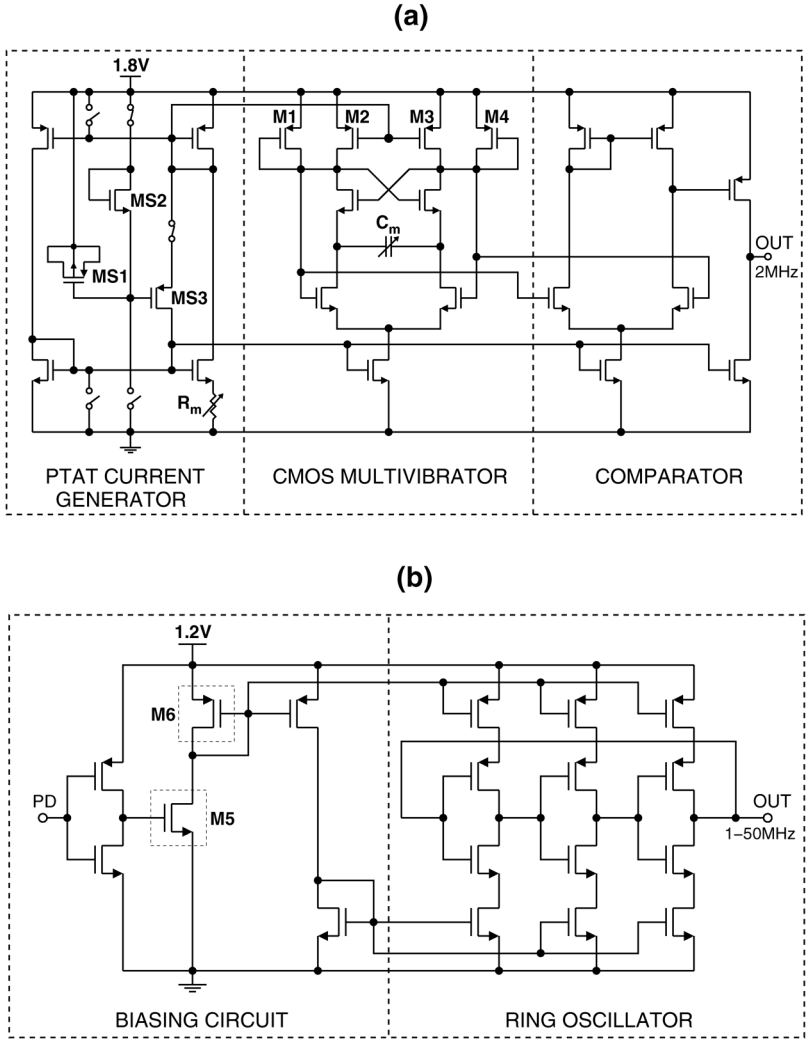

Fig. 8. Schematic of the clock generator: (a) system clock; (b) microcontroller unit clock.

designing the CMFB circuit. The CMFB of the DDA is dynamically biased by mirroring the currents from the outputs of the operational amplifier. When the amplifiers of the front-end are operated in the single-ended mode or when the ADC is in the power-down mode, the CMFB circuit is disabled.

E. Clock Generator

The clock generator shown in Fig. 8 consists of two separate frequency references. The system clock, whose oscillation frequency is fixed to 2 MHz, is always active. The microcontroller unit clock is included to provide a clock signal for the DSP, if more intensive computation is required. Its tuning range extends from 1 to 50 MHz. The required buffers are not shown in Fig. 8. Next, the implementations of these two frequency references are briefly presented.

1) SYSCLK: Since the SYSCLK is always active, the minimization of its current consumption is important. The designed clock generator is based on a source-coupled CMOS multivibrator [24], which makes low current consumption possible. The poor phase noise performance of relaxation oscillators is not a problem in this application as the jitter requirement is not very stringent. Bias currents and voltages are generated by a proportional-to-absolute temperature (PTAT) current generator, while a rail-to-rail clock signal is generated by a two-stage differential comparator. The output buffer drives an on-chip capacitive load of approximately 1.2 pF consisting of wirings and logic gates. Transistors MS1–MS3 form a start-up circuit. MS1 operates as a start-up capacitor that must be discharged before the next start-up. During the start-up MS3 pulls the gates of the NMOS current sources high ensuring a reliable start-up. After the gate of MS1 has charged through MS2, the gate-source voltage of MS3 falls low enough to cut it off.

The buffer dominates the current consumption of the SYSCLK. Typically, the buffer accounts for two thirds of the total current consumption of approximately 6 μA. The frequency stability of the output signal is optimized by using symmetrical loads (M1/M2 and M3/M4) [25] and supply-independent biasing. It is necessary to use the supply-independent biasing because the SYSCLK is designed to operate over the supply voltage range from 1.62 to 2.75 V without extra calibration. The effects of process variations on the oscillation frequency can be eliminated by programming the on-chip resistor $(\mathrm{R_m})$ and capacitor $(\mathrm{C_m})$ matrices. The combination

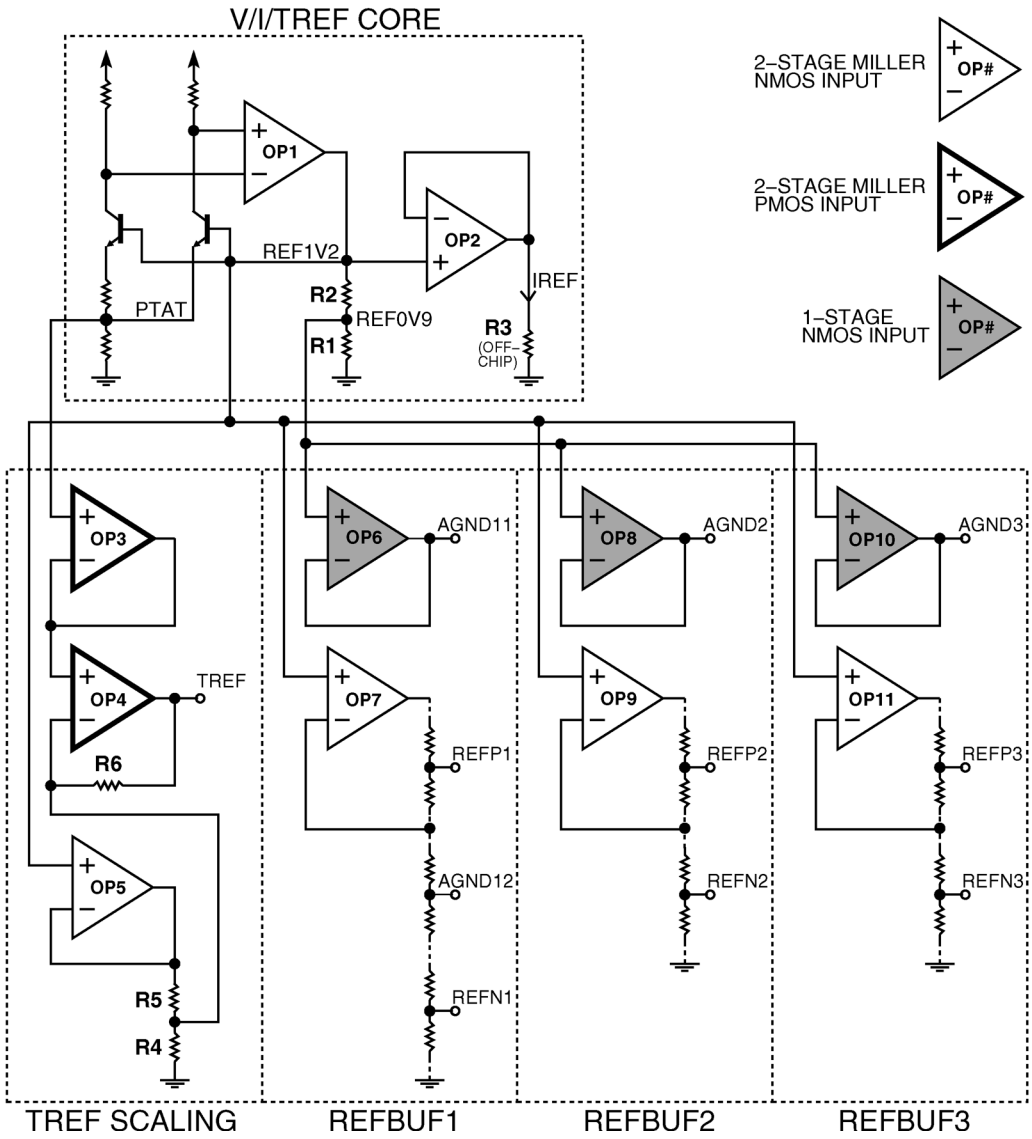

Fig. 9. Schematic of the voltage, current, and temperature reference.

of $\mathrm{R_m}$ and $\mathrm{C_m}$ is a trade-off between current consumption and frequency stability. The SYSCLK does not provide a 50% duty cycle, which means that this must be taken into account at the interface with the sensor front-end and the ADCs.

2) MCUCLK: The MCUCLK is based on a three-stage single-ended current-starved ring oscillator. It uses a 1.2 V supply. The biasing circuit is equipped with frequency tuning and power-down options. M5 and M6 are transistor matrices that enable the frequency tuning from 1 to 50 MHz. Matrix M5 is used for fine tuning and matrix M6 for coarse tuning. The output buffer drives the clock signal to the digital output pad.

The most important requirement for the MCUCLK is that it can provide the whole tuning range in spite of the process, temperature and $\pm 10\%$ supply variation. Low current consumption is also required. Frequency stability over the temperature and supply voltage range is not optimized as it is in the case of the SYSCLK. Thus, the largest deviation from the nominal oscillation frequency due to the temperature and supply is over 50%. Phase noise performance is not critical for this frequency reference.

F. Voltage, Current, and Temperature Reference

The voltage, current, and temperature reference based on the structure of Brokaw's bandgap reference [26] is shown in Fig. 9. The designed reference circuit consists of the core circuit, the required reference voltage buffers, the scaling circuitry for the temperature reference, and the current mirrors and power-down switches (not shown in Fig. 9) required for bias current generation. The current consumption of the continuously operating circuit blocks, such as the core circuit, must be optimized. The use of decreased duty cycles is possible in certain parts of this reference circuit, such as in the reference voltage buffers for the ADCs. The required power-down switches and signals are not indicated in Fig. 9. The front-end and both ADCs require three independent reference voltages each; a positive reference (REFP), a negative reference (REFN), and an analog ground (AGND) voltage. All these circuit blocks have different duty cycles. The REFBUF1 is the reference voltage buffer for the front-end, and REFBUF2 and REFBUF3 are the reference voltage buffers for the two ADCs. The system has a common AGND

of 0.9 V. The REFP and REFN voltages are designed to be adjustable at 50 mV steps, enabling the interface to be suited for sensors with different sensitivities.

1) V/I/TREF Core: The reference voltages of 1.2 V and 0.9 V are generated using two load resistors (R1 and R2) in series at the output stage of the feedback amplifier (OP1). The current reference of 1 μA is generated by using the 1.2 V reference voltage and a 1.2 MΩ off-chip resistor (R3) driven by an on-chip voltage buffer (OP2). The inherent PTAT voltage of the bandgap reference is exploited by the temperature reference. Because the PTAT voltage varies only 0.23 V over the temperature range, it must be buffered, amplified, and shifted to a proper voltage level before A/D conversion. The operational amplifiers required to buffer the aforementioned voltages from the core circuit add to the noise level. In order not to limit the performance of the sensor interface, the core circuit must have the resolution of the order of 12 bits.

An off-chip resistor is included to provide a more accurate and stable reference current. All bias currents of the system, excluding the currents needed in the clock generator, are primarily mirrored from the output stage of the OP2. A number of current mirrors and power-down switches are also needed. The switches are used to turn off the circuit blocks according to their duty cycles. To keep the load of the OP2 unchanged, and thus to avoid disturbances in the core circuit, the currents mirrored directly from OP2 are designed to flow continuously.

2) Reference Voltage Buffers: The REFBUF1 is always active, in contrast to the REFBUF2 and REFBUF3 that go into a power-down mode according to the duty cycles of the corresponding ADCs. In power-down mode, all unnecessary bias currents are turned off, thus dropping remarkably the average current consumptions of these reference voltage buffers.

Because noise in the AGND is not critical in the ADCs and in certain parts of the front-end, a separate buffering of AGND and REFP/REFN voltages is used to relieve the loadings of the operational amplifiers with resistor trees. One-stage operational amplifiers OP6, OP8, and OP10 buffer these AGND voltages, thus lowering the total current consumption. The unit resistors of the trees have been optimized to fulfill the settling requirements in the worst case with the maximum capacitive load.

3) TREF Scaling: Because altering the load of the core circuit causes disturbances, OP3 is needed to buffer the PTAT voltage. The current consumption of OP3 has to be optimized, because its bias currents must flow continuously. At the same time, it is not allowed to add to the noise level of the PTAT voltage too much. The TREF voltage at the analog output changes approximately from 0.2 to 0.8 V, being proper for the A/D conversion. The combined current consumption of OP4 and OP5 is not critical, because a small duty cycle, for example 0.3% when the sampling frequency of 100 Hz is used, scales it to negligibly small values.

IV. Measurement Results

The prototype was fabricated in a 0.13-μm BiCMOS technology, using 2.5 V tolerant high-voltage transistors, metal–insulator–metal (MIM) capacitors and high-resistivity polysilicon resistors. When the core circuit is considered, only in the case of the MCUCLK were the low-voltage transistors used, while the bipolar transistors were used only in the V/I/TREF core circuit. The active core area of the implemented chip shown in Fig. 10 is 0.51 mm^2, while the total die area including pads is 2.76 mm^2. For the measurements, the chip was encapsulated into a plastic quad flat package (QFP) with 80 pins and soldered onto a printed circuit board (PCB). The chip was combined with an external $\pm$4-g capacitive 3-axis accelerometer on the PCB. Next, the most essential measurement results are presented, first for the individual building blocks, and then for the whole system.

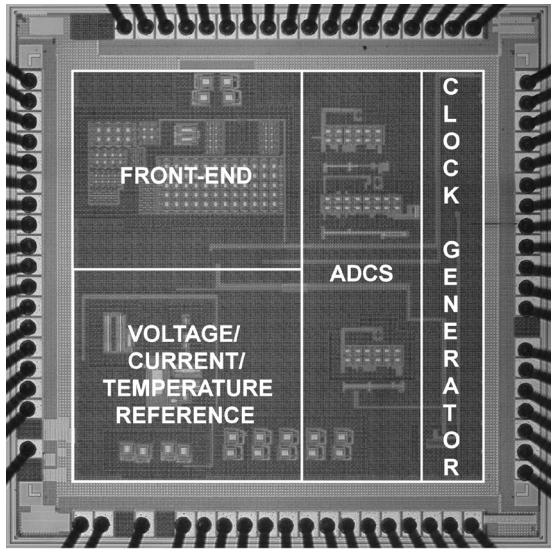

Fig. 10. Microphotograph of the implemented chip.

A. Front-End

The 10 700-point FFT plots for one mass measured from the ADC output in different configurations are shown in Fig. 11. A moving average of 21 points was used to smooth these spectra. Each proof mass was sampled at 1.04 kHz in the differential mode. By comparing these spectra, it can be seen that CDS reduces the noise level approximately 6 dB compared to the case, in which both CDS and chopper stabilization are disabled. Furthermore, chopper stabilization modulates the offset and flicker noise of the front-end to the vicinity of half of the sampling frequency.

The noises of the individual masses can be converted to the noises of the three linear acceleration components by using (2). As mentioned earlier, this equation assumes that all masses have equal sensitivities. The $\sqrt{2}$ coefficient causes an increase of 3 dB in the noise levels of all three directions. In the y- and z-directions, the subtraction of the two signals with opposite signs causes a reduction of 3 dB in the noise levels. These two directions have the same noise levels as the individual masses, but the subtraction removes the flicker noise and offset. In the x-direction, the summation of four signals causes a 3 dB reduction on the noise level compared to the noise level of the individual masses. This summation does not remove either the flicker noise or offset. However, these can be removed by using chopper stabilization without increasing the power dissipation.

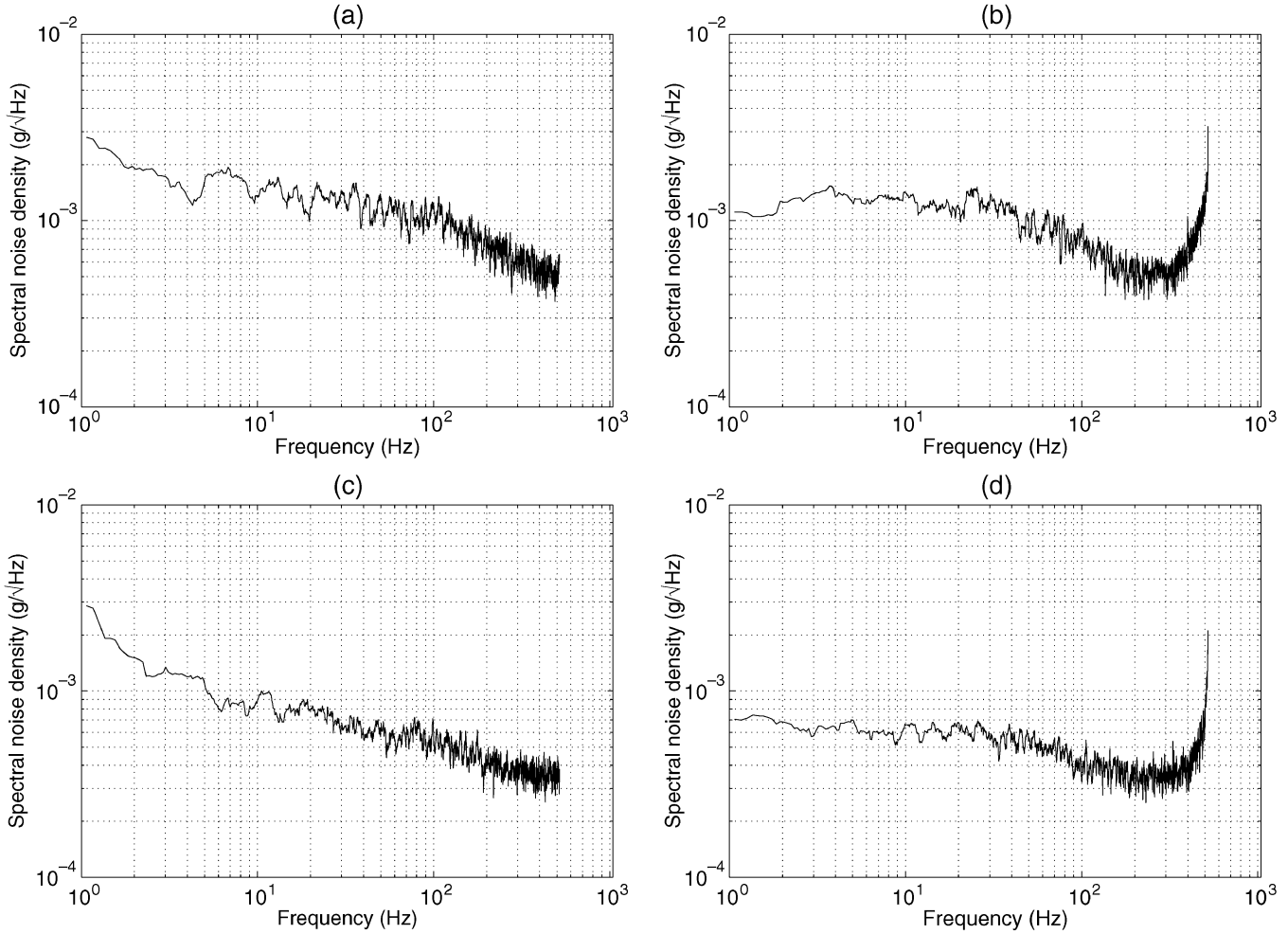

Fig. 11. Measured noise spectra for one mass (a) without CDS and chopper stabilization, (b) with chopper stabilization only, (c) with CDS only, and (d) with CDS and chopper stabilization. 10 700-point FFT, no windowing, moving average of 21 points, sampling frequency 1.04 kHz.

B. ADC

The ADC was measured with the on-chip references. Fig. 12 shows the measured 10 695-point FFT plot for a full-scale 400 Hz sinusoidal input signal. The nominal sampling frequency of 1 kHz was used. The measured SNDR at 100 Hz bandwidth is 57.9 dB, and the measured SFDR 71.8 dB. The measured INL and DNL are shown in Fig. 13. The maximum INL is $+2.94/-3.42$, and the maximum DNL $+1.67/-1.00$, respectively. The measured ADC performance is adequate for the 10-bit accuracy of the sensor interface. The performance of the ADC can be improved by optimizing the biasing current and reference voltages [12].

C. Reference Circuitry

The frequency stability of $\pm 2.5\%$ was measured for the SYSCLK output over the temperature and supply voltage range (1.62–2.75 V) [13]. The measured phase noise at 1 MHz offset frequency is approximately -105 dBc/Hz, which corresponds to the cycle jitter of 2.0 ns [13]. This value is smaller than the maximum jitter for 10-bit resolution approximated with (1). The output of the MCUCLK is driven directly to a bonding pad. When running at 50 MHz, the MCUCLK consumes 27 μA without the buffer.

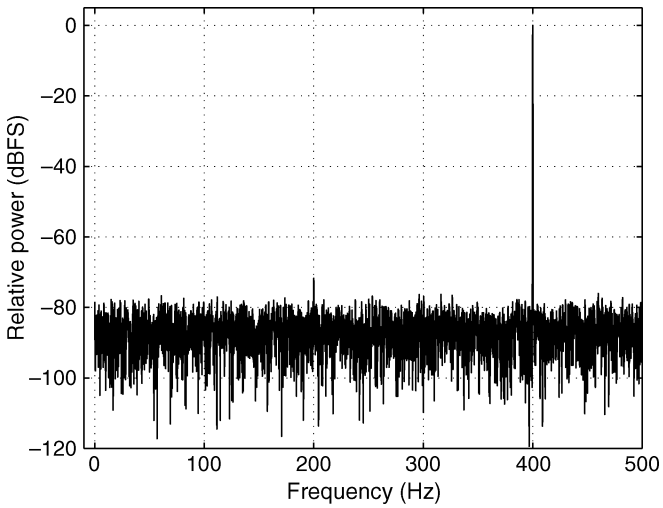

Fig. 12. Measured ADC output spectrum with a full-scale 400 Hz sinusoidal input signal. 10 695-point FFT, Kaiser window with $\beta = 13$, sampling frequency 1 kHz.

According to the measurements, the accuracy of the VREF is sufficient for the 10-bit operation of the sensor interface, and the accuracy of TREF is sufficient for 9 bits. The measured temperature dependencies for both the voltage and temperature ref-

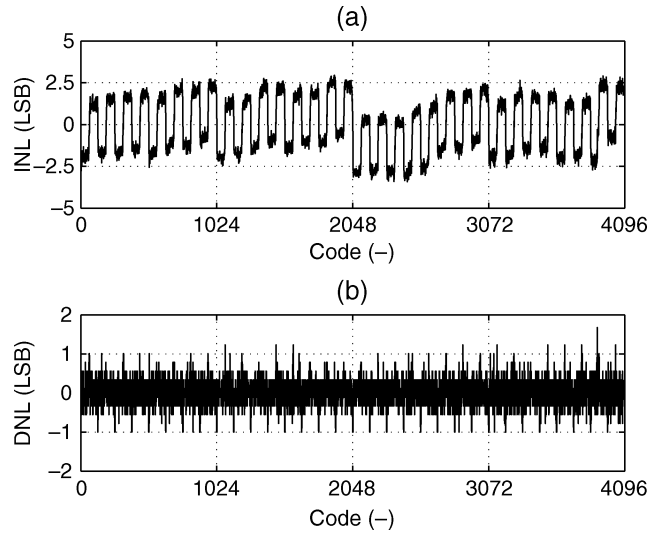

Fig. 13. (a) Measured INL and (b) DNL of the ADC.

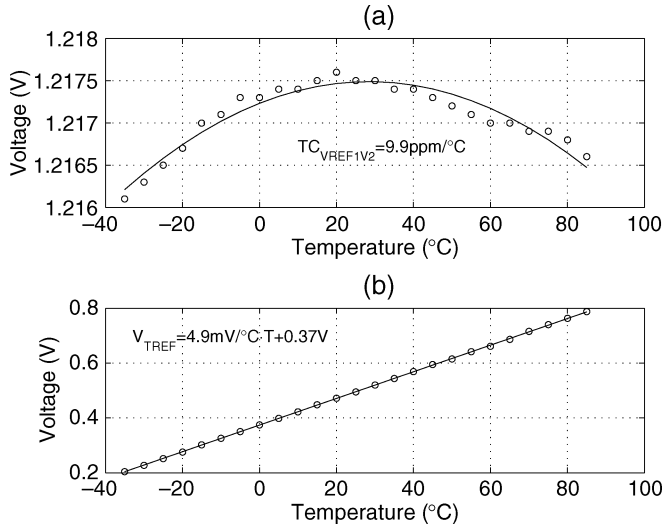

Fig. 14. Measured temperature dependencies of (a) voltage and (b) temperature reference.

erence are shown in Fig. 14. The second order fitting curve for the measured reference voltage predicts a temperature coefficient (TC) of 9.9 ppm/ °C, while all the measured points for the analog output of the temperature reference fall near to the linear fitting curve with a slope of 4.9 $\mathrm{mV/\,^{\circ}C}$ [14]. The noise floor of the A/D converted temperature data is 0.18 °C.

D. System Measurements

The distribution of the measured current consumption while sampling temperature at 100 Hz, and four proof masses, each at 1.04 kHz, is shown in Table I. The active silicon areas of the building blocks are also included in Table I. The voltage, current, and temperature reference consumes almost half of the total current of 62.9 μA consumed by the core circuit. According to a simulation, the two most dominant sub-blocks of the V/I/TREF, namely the REFBUF1 and the IREF including the current mirrors for generating all bias currents, account

TABLE I
DISTRIBUTION OF THE CURRENT CONSUMPTION AND SILICON AREA

Block	Duty cycle	Current		Silicon area	
	(%)	(μA)	(%)	(mm^2)	(%)
Front-end	100	18.3	29.1	0.2983	58.8
ADC	10	5.5	8.7	0.0401	7.9
TREF ADC	0.3	1.7	2.7	0.0401	7.9
SYSCLK	100	6.2	9.9	0.0085	1.7
MCUCLK	5	1.9	3.0	0.0021	0.4
V/I/TREF	100/10/3	29.3	46.6	0.1180	23.3
Total		62.9	100.0	0.5071	100.0

together for approximately 55% of the 29.3 μA consumed by the whole V/I/TREF. The used duty cycles reduce the current consumptions of the ADCs remarkably. The current consumption of the SYSCLK is increased by the buffer that must drive over 1 pF capacitive load. The MCUCLK was not needed in the system measurements. However, its current consumption at 50 MHz is included in Table I. The assumed duty cycle is 5%.

The 10 700-point FFT plots measured for x- and z-directional accelerations with CDS and with and without chopper stabilization in the differential mode are shown in Fig. 15. A moving average of 21 points was again used to smooth the spectra. Each proof mass was sampled at 1.04 kHz. As was discussed in the context of the front-end measurements, the flicker noise is removed in the y- and z-directions without using chopper stabilization in contrast to the case of the x-direction. The measured low-frequency noise floors in the x-, y-, and z-directions when using both CDS and chopper stabilization are 482 $\mu\mathrm{g}/\sqrt{\mathrm{Hz}}$, 639 $\mu\mathrm{g}/\sqrt{\mathrm{Hz}}$, and 662 $\mu\mathrm{g}/\sqrt{\mathrm{Hz}}$, respectively. These results yield a sufficient dynamic range for 10-bit operation at 100 Hz bandwidth.

The functionality of the sensor interface was verified by exciting the system with -4-g $\ldots +4$-g dc accelerations. Accelerations were generated on a rotating rate table. The used measurement setup is shown in Fig. 16. Centrifugal acceleration $a = r\omega^2$, where r is the distance of the sensor element from the centre of the rate table and ω the angular velocity, was used to excite the sensor in all three sensitive directions, one at the time. These measurements were performed in the differential mode with CDS by sampling each mass at 1.04 kHz. The measured ± 4-g dc ramps with a linear fitting curve are shown in Fig. 17. Offsets and gain errors were removed by calibration. The maximum nonlinearities evaluated from the measured data by using the best fit method at ± 2-g range are $+1.5/-1.0\%$ for x-axis, $+0.5/-0.8\%$ for y-axis, and $+0.3/-0.4\%$ for z-axis. The lower linearity in the x-direction can be explained by the structure of the sensor. According to (2), the even order nonlinearity is cancelled in the cases of y- and z-directions. The increased nonlinearity at higher accelerations due to the measurement setup can be seen in Fig. 17.

The rate table was used to generate an acceleration pulse of $+1$-g to z-direction. The measured response is shown in Fig. 18. The resultant of the accelerations to x- and y-directions corresponds to the earth's gravity, because the sensor is slightly slanted on the PCB. The angular acceleration and deceleration of the rate table cause a tangential acceleration component that can clearly be seen in the y-directional acceleration curve. The

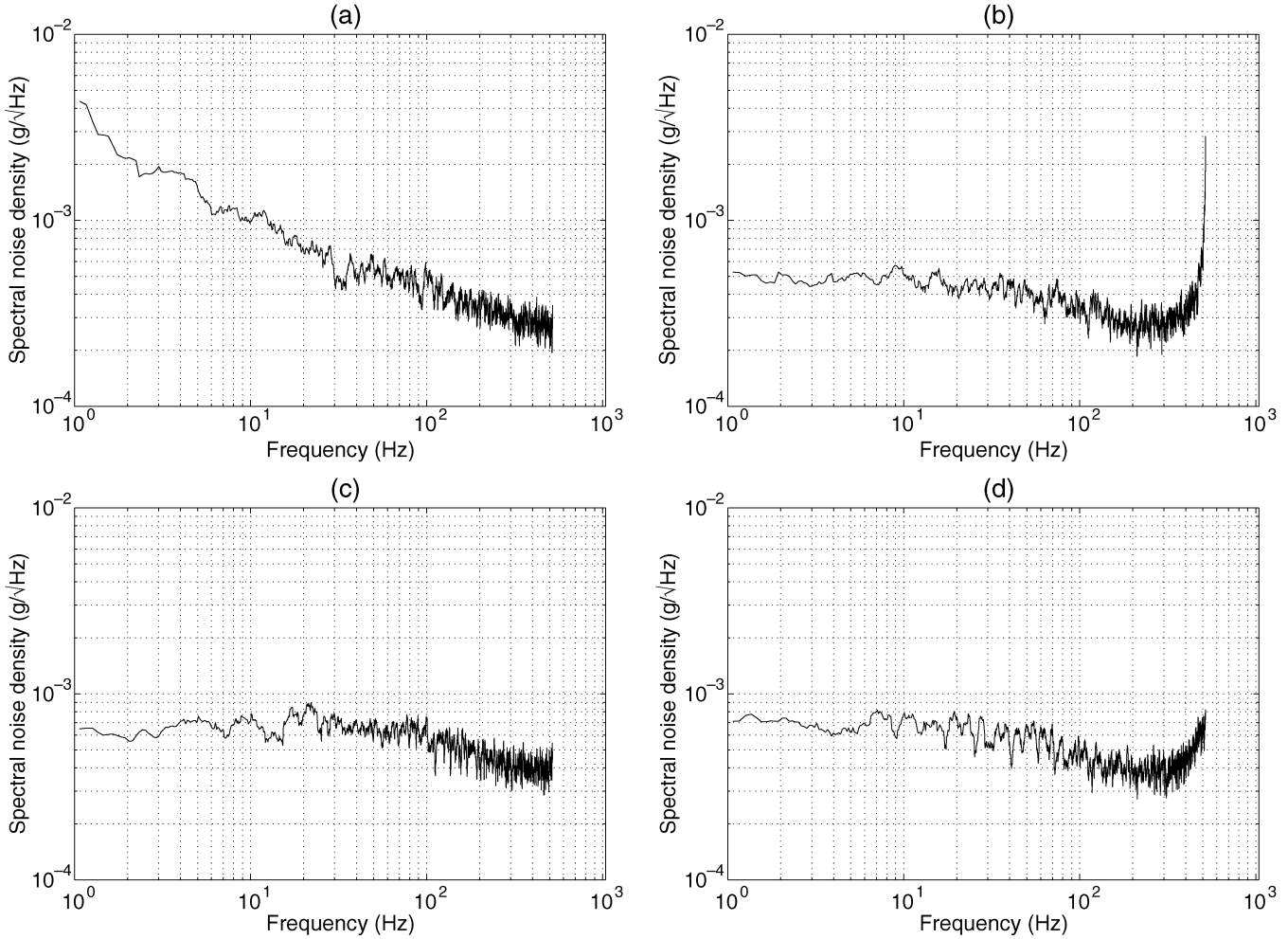

Fig. 15. Measured noise spectra for (a) x-direction with CDS, (b) x-direction with CDS and chopper stabilization, (c) z-direction with CDS, and (d) z-direction with CDS and chopper stabilization. 10 700-point FFT, no windowing, moving average of 21 points, sampling frequency 1.04 kHz.

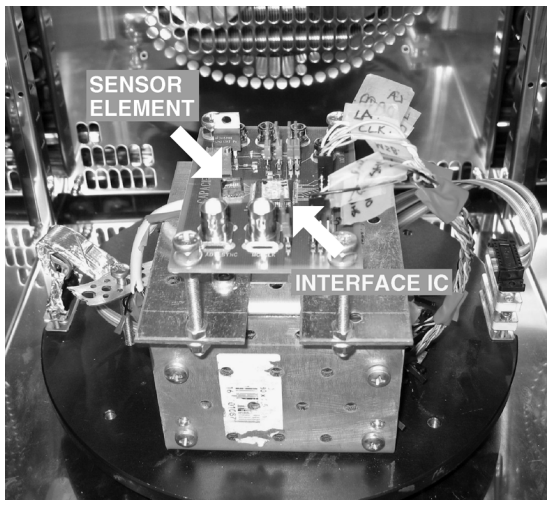

Fig. 16. PCB mounted on the rate table.

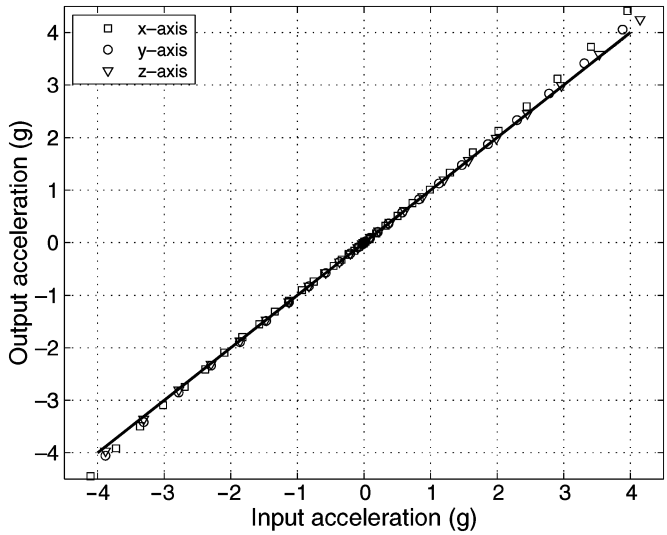

Fig. 17. Measured dc acceleration ramps in x-, y-, and z-directions.

varying acceleration in y-direction is caused by the cogging torque of the rate table.

The overall performance is summarized in Table II. The measured total average current consumptions without the MCUCLK, and the noise floors in the x-, y-, and z-directions, are declared for both single-ended and differential mode when sampling temperature at 100 Hz, and each mass at 1.04 kHz.

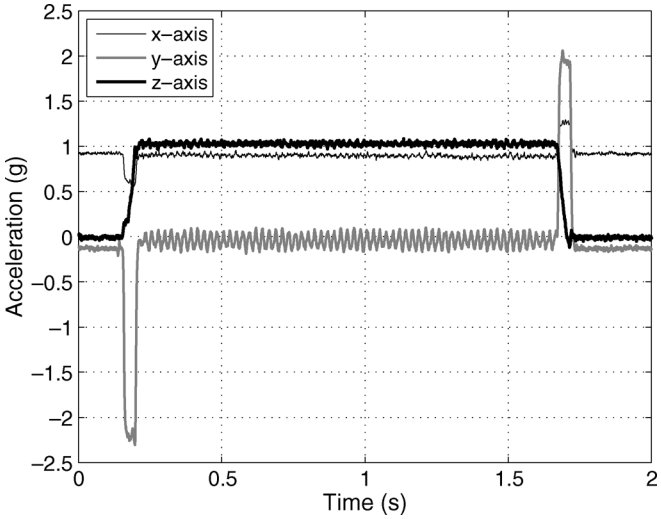

Fig. 18. Acceleration pulse of +1-g in z-direction.

TABLE II
PERFORMANCE SUMMARY

Process	0.13-μm BiCMOS with high-voltage transistors, MIM capacitors, and high-resistivity polysilicon resistors		
Supply	$1.2\,V$ MCUCLK and $1.8\,V$ other circuit blocks		
Active area	$0.51\,mm^2$		
Mode	Single-ended	Differential	
f_s/mass	1.04	1.04	(kHz)
I_{avg} (core)	54	62	(μA)
Noise floor			
x-axis	576	482	$(\mu g/\sqrt{Hz})$
y-axis	868	639	$(\mu g/\sqrt{Hz})$
z-axis	845	662	$(\mu g/\sqrt{Hz})$
TREF	0.18		$(^\circ C)$
Linearity		$(\pm 2\,g)$	
x-axis		$+1.5/-1.0$	(%)
y-axis		$+0.5/-0.8$	(%)
z-axis		$+0.3/-0.4$	(%)

The slight difference in current consumption compared to Table I is explained by the fact that another IC sample was used when the results of Table I were measured. All the results presented in Table II, except the linearity results, were measured by using both CDS and chopper stabilization.

V. CONCLUSION

In this paper, a micropower interface IC for a capacitive 3-axis micro-accelerometer implemented in a 0.13-μm BiCMOS process was presented. Die area and power dissipation were reduced by using time-multiplexed sampling and varying duty cycles as low as 0.3%. The chip with a 0.51 mm^2 active area draws 62 μA from a 1.8 V supply while sampling temperature at 100 Hz, and four proof masses, each at 1.04 kHz. With a $\pm$4-g capacitive 3-axis accelerometer, the measured noise floors in the x-, y-, and z-directions are 482 $\mu g/\sqrt{\text{Hz}}$, 639 $\mu g/\sqrt{\text{Hz}}$, and 662 $\mu g/\sqrt{\text{Hz}}$, respectively. The presented measurement results prove that the use of an open-loop configuration for sensor readout is feasible for low-power applications.

ACKNOWLEDGMENT

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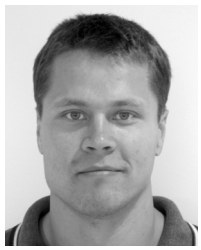

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