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32.2 A 1.5μW 1V 2nd-Order ΔΣ Sensor Front-End with Signal Boosting and Offset Compensation for a Capacitive 3-Axis Micro-Accelerometer

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The advantages of capacitive accelerometers [1], such as zero static bias current and the capability of achieving high sensitivity, are emphasized in ultra-low-power applications. In [1], representing the current state-of-the-art in low-power 3-axis micro-accelerometers, capacitance-to-voltage and A/D conversions were performed separately. In this paper, an ultra-low-power 2nd-order ΔΣ sensor front-end with inherent capacitance-to-digital conversion [2] for a capacitive 3-axis micro-accelerometer is presented. The front-end is designed for 1V operation and 12b accuracy with a 1Hz BW using a 0.25μm CMOS technology.

The schematic of the ΔΣ sensor front-end with the sensor element is shown in Fig. 32.2.1. The capacitive acceleration information from each proof mass is first converted to a charge and then to a bit stream. In order to achieve sufficient (>20dB) mechanical attenuation of folding out-of-band interferers, a minimum f_s of 2kHz per mass was chosen. Chopper stabilization (CS) and CDS are implemented in order to reduce the offset voltage and noise of the front-end. The 1st integrator stage has to use time-multiplexing because of the common middle electrode of the proof masses. The use of six parallel integrators (one for each mass and chop phase) in the 2nd stage makes possible the use of longer settling times, thus reducing power dissipation. To keep the implementation simpler, one comparator is multiplexed between the outputs of the 2nd integrators.

The ΔΣ front-end balances charge (i.e., ensures an equal average charge in both positive and negative detection capacitances) and thus reduces the distorting effects of the nonlinear electrostatic forces. Additionally, the transfer function is of the form $(C_{DP} - C_{DN})/(C_{DP} + C_{DN})$, which cancels the nonlinearity of the displacement-to-capacitance conversion to the first order. The front-end uses two main clock phases, A and B, and three main mass selection phases, M*n*, *n* being the index of the proof mass. In phase A, the mass being read is charged to a proper reference voltage and the 1st integrator samples the offset and flicker noise of the operational amplifier. Simultaneously, the 2nd integrator feeds the sampling capacitor of the comparator. In phase B, the charge of the mass being read is integrated in the 1st integrator and the 2nd integrator samples the new output voltage of the 1st integrator. Additionally, the comparator resolves a new output bit and the DAC capacitor of the 2nd integrator is charged to either reference voltage as determined by the new output bit. The 2nd integrator performs the charge transfer while the other masses are read.

The positive and negative reference voltages (REFP/N) are equal to the supply and ground. Because of the low supply voltage of 1V, the input and output common-mode levels (CM_IN/OUT) of the operational amplifiers are separated to 0.1 and 0.5V, respectively. The capacitor sizes in the 1st integrator are programmed to yield a gain of 0.5. To minimize power dissipation, a tail-current-boosted Class-AB operational amplifier (Fig. 32.2.2(a)) [3] is used in the 1st integrator. The DC gain is increased by using the current sources I_L [4]. The required feedback amplifiers are one-stage amplifiers with NMOS input pairs. The operational amplifier used in the 2nd integrators is a basic current mirror OTA, whose DC gain is increased with the same technique. The amplifiers were designed so that their biasing currents can be increased to enable a maximum f_s of 51.2kS/s per mass. The simulated DC gains of the amplifiers of the 1st and 2nd integrators are approximately 50dB and 45dB, respectively. The dynamic latch with zero static power dissipation (Fig. 32.2.2(b)) [5] is used as a comparator.

A method to boost the available signal and to compensate for the offsets of the sensor capacitors was developed. The operating principle is shown in Fig. 32.2.3. The programmable capacitor matrix C_{CB} can be used to either source or sink charge from the sensor middle electrode DMID. A single matrix is used for all three masses, with different programming. If charge is removed from both sides of the differential sensor capacitor pair, the denominator of the ratiometric transfer function is reduced and the signal is boosted. At the same time, the signal swing at the output of the 1st integrator is reduced, making low-voltage operation easier to achieve. If charge is sourced or sunk from only one side, the system compensates for any offset in the sensor capacitors. The signal boosting and offset compensation can also be used simultaneously.

Because of the low supply voltage, the use of floating switches is not possible without boosting the gate voltages. Therefore, the gate voltage of an NMOS device in a floating transmission gate is increased to $2 \cdot V_{DD}$ using charge pumps (Fig. 32.2.2(c)) [6]. To minimize the silicon area, the number of gate-voltage-boosted floating switches was kept as low as possible. Other switches were implemented as single N- or P-MOS devices. The symbol 2× is used to indicate the gate-voltage-boosted switches in Fig. 32.2.1. The area required by the charge pumps is minimized by driving all the switches operating on the same clock phase with a single pump, and by sizing $C_1 << C_2$ in each pump.

As the sampling frequency is low, the leakage currents of off-state switches must be minimized in order to prevent signal distortion and temperature-dependent offset. The primary source of leakage is the subthreshold current, which was minimized by using a non-minimum channel length to increase the threshold voltage whenever there is a voltage drop over an off-state switch. Additionally, the sensor middle electrode DMID was identified as being especially sensitive to leakage currents. To minimize the leakage into this node, a special ultra-low-leakage switch (Fig. 32.2.2(d), denoted by ULL in Fig. 32.2.1) similar to that in [7] was developed. When CLK=0, then in the case of an NMOS switch, MN1 and MN2 are off, while MP3 pulls the middle node to the positive supply rail. The bulk effect increases the threshold voltage of MN1, significantly reducing the leakage current.

The prototype was fabricated with a 0.25μm CMOS technology with MIM capacitors. The silicon area of the front-end (Fig. 32.2.6) is 0.49mm². The chip was combined with an external ±2g capacitive 3-axis accelerometer on a PCB. The measurements were performed with off-chip references. An FFT of the measured z-directional data is shown in Fig. 32.2.4(a). The measured noise in the x, y and z directions with f_s = 2.048kS/s per mass and chop phase is 917μg/√Hz, 791μg/√Hz and 704μg/√Hz, respectively. These results yield a DR of 72dB at a 1Hz BW. Figure 32.2.4(b) shows the ±2g acceleration ramps, and Fig. 32.2.4(c) an x-direction acceleration pulse, both measured using a rotating rate table. Because of smaller parasitic capacitances, the results are expected to improve when the front-end is bonded directly to the sensor.

This ΔΣ sensor front-end IC draws 1.5μA from a 1V supply while sampling three proof masses, each at 4.096kS/s. The overall performance is summarized in Fig. 32.2.5.

Acknowledgments:
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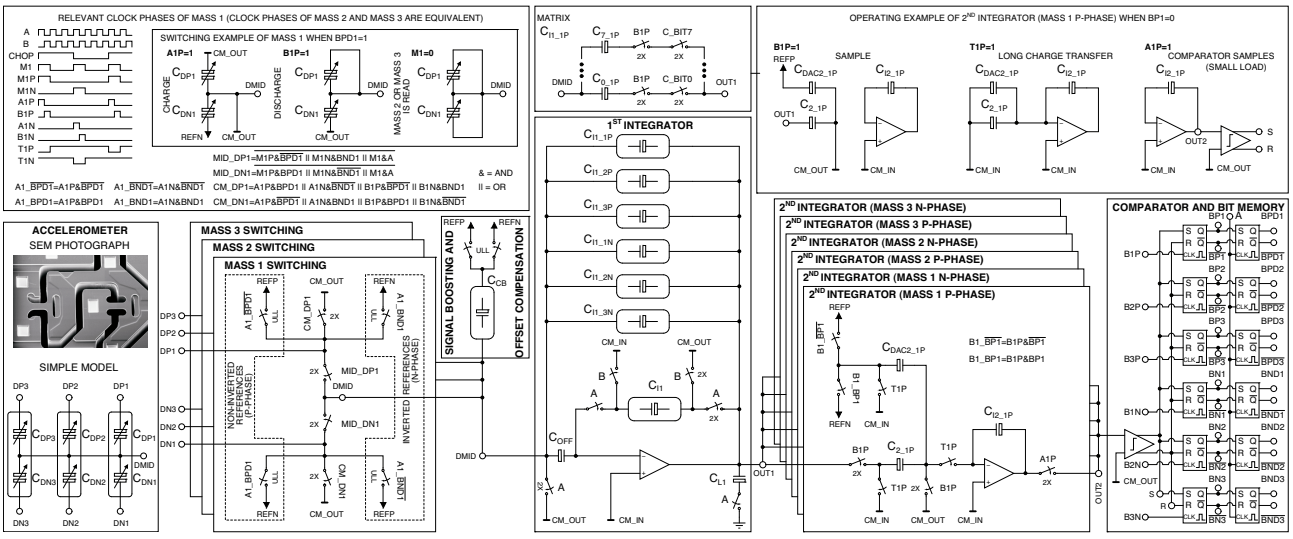

Figure 32.2.1: Schematic of the ΔΣ sensor front-end with an SEM photograph of a 3-axis capacitive micro-accelerometer. (SEM image courtesy of VTI Technologies, Vantaa, Finland)

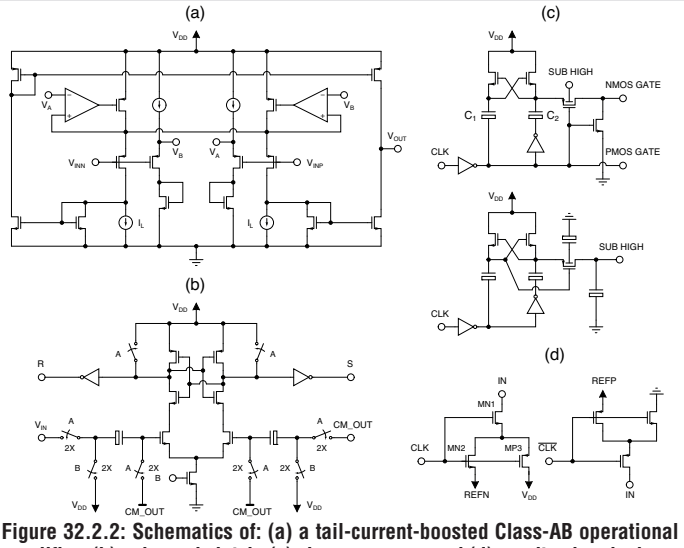

Figure 32.2.2: Schematics of: (a) a tail-current-boosted Class-AB operational amplifier; (b) a dynamic latch; (c) charge pumps, and (d) an ultra-low-leakage NMOS (left) / PMOS (right) switch.

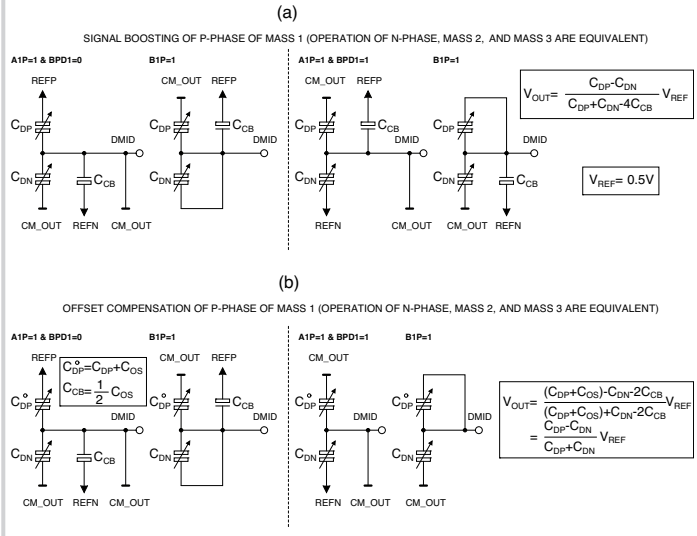

Figure 32.2.3: Operating principle of (a) signal boosting and (b) offset compensation.

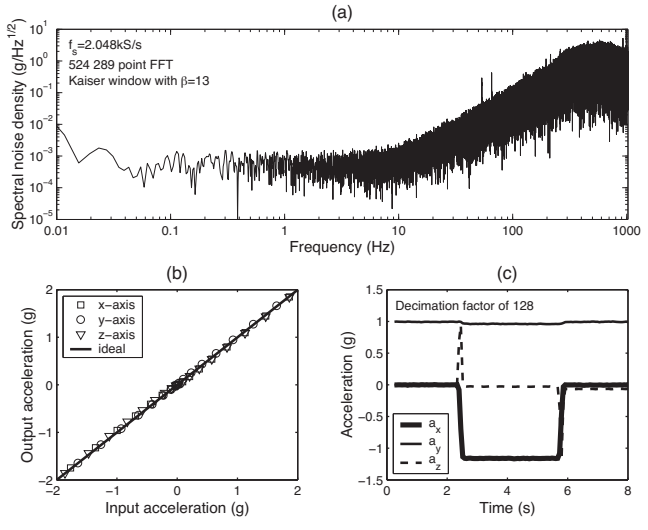

Figure 32.2.4: (a) FFT of measured z-directional data, (b) ±2g acceleration ramps, and (c) an x-directional acceleration pulse.

Process	0.25μm CMOS with MIM capacitors		
Operating mode	With CS and CDS, no signal boosting		
Supply voltage	1V		
Power dissipation	1.5μW		
Sampling frequency per mass	4.096kS/s		
	x-axis	y-axis	z-axis
Noise floor (μg/√Hz)	917	791	704
Current consumption / silicon area	(μA)		(mm^2)
• Opamps	1.4μA		0.0358
• Comparator			0.0006
• Charge pumps			0.0727
• Switches			0.0378
• Clock generator	0.1μA		0.0552
• Capacitors			0.1181
• Wirings			0.1705
Total	1.5μA		0.4907

Figure 32.2.5: Summary of measured performance.

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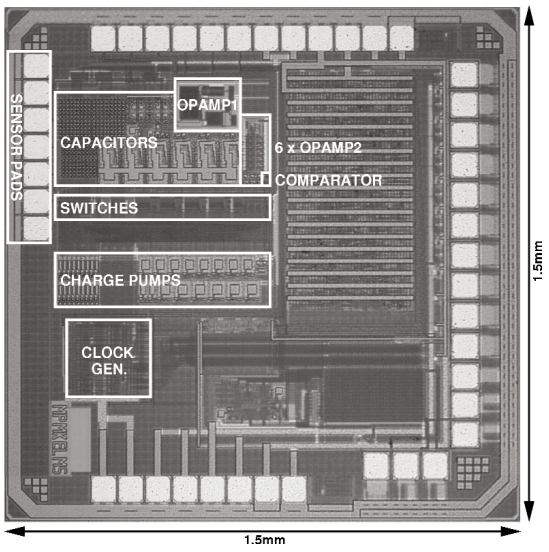

Figure 32.2.6: Chip micrograph.