

Publication P6

Matti Paavola, Mika Kämäräinen, Mikko Saukoski, and Kari Halonen. 2008. A micropower low-dropout regulator with a programmable on-chip load capacitor for a low-power capacitive sensor interface. In: Proceedings of the 15th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2008). St. Julian's, Malta. 31 August - 3 September 2008. Pages 450-453. ISBN 978-1-4244-2182-4.

© 2008 Institute of Electrical and Electronics Engineers (IEEE)

Reprinted, with permission, from IEEE.

This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of the Aalto University School of Science and Technology's products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee.org.

By choosing to view this document, you agree to all provisions of the copyright laws protecting it.

A Micropower Low-Dropout Regulator with a Programmable On-Chip Load Capacitor for a Low-Power Capacitive Sensor Interface

Matti Paavola¹, Mika Kämäräinen¹, Mikko Saukoski^{1,2}, and Kari Halonen¹

¹SMARAD-2/Electronic Circuit Design Laboratory, Helsinki University of Technology, Espoo, Finland

Email: mhpaavol@ecd.tkk.fi

Abstract—In this paper, a micropower low-dropout regulator (LDO) for a low-power capacitive sensor interface fabricated in a $0.25\ \mu\text{m}$ BiCMOS process is presented. The LDO with on-chip voltage and current references, and an on-chip programmable load capacitor, occupies an active silicon area of $0.18\ \text{mm}^2$. It is stable with zero load current over the load capacitance range from 0 to $1\ \text{nF}$. The input voltage range extends from 1.2 to 2.75 V, while the designed output voltage is 1.0 V. The measured quiescent current of the LDO including the on-chip references is $7.6\ \mu\text{A}$. According to the measurements, the regulated output has a temperature coefficient (TC) of $57.2\ \text{ppm}/^\circ\text{C}$, a line regulation of $2.71\ \text{mV}/\text{V}$, and a load regulation of $1.64\ \text{mV}/\text{mA}$. The rms output noise integrated over the bandwidth ranging from 1 Hz to 100 kHz is $1.365\ \text{mV}$.

I. INTRODUCTION

On-chip voltage regulators are required for system-on-chip (SoC) power management. Individual sub-blocks have different requirements for their supply voltages including voltage level, load current, maximum voltage drop, and noise, for example. Low-dropout regulator (LDO) is regarded as a suitable choice for local on-chip voltage regulation due to its fast transient response, low-noise characteristic, low complexity, and no need for inductors. There has been a growing interest to develop capacitor-free LDOs to avoid the use of an impractical off-chip load capacitor [1], [2]. In practice, when designing LDOs for applications, in which the average load currents are order of microamperes or even less, the LDOs must be stable with zero load currents. It is obvious that the efficiency of an LDO designed for such an application becomes low.

In this paper, a micropower LDO with on-chip references and an on-chip programmable load capacitor is presented. The LDO provides a 1.0 V supply for a low-power sensor interface that reads a three-axis capacitive micro-accelerometer. The block diagram of the sensor interface with different supply regions is shown in Fig. 1. The primary supply voltage for the interface IC ranges from 1.2 to 2.75 V. The 2nd-order $\Delta\Sigma$ sensor front-end [3] converts the capacitive acceleration information from each proof mass first to a charge and further to a bit stream. The decimator [4] is required because of the oversampling behaviour of the $\Delta\Sigma$ sensor front-end. The frequency reference (FREF) [5] provides the master clock

The authors wish to thank VTI Technologies, and the Finnish Funding Agency for Technology and Innovation (TEKES) for financial support.

²Starting from the year 2008, M. Saukoski has been with ELMOS Semiconductor AG, Dortmund, Germany.

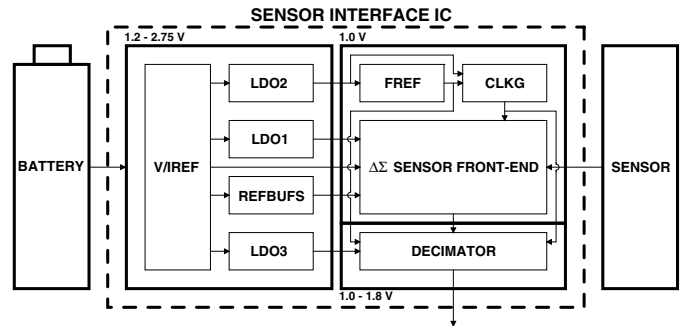


Fig. 1. The presented LDO provides a 1.0 V supply for a low-power sensor interface that reads a three-axis capacitive micro-accelerometer.

signal for both the clock generator of the front-end (CLKG) and the decimator, while the CLKG generates all the clock signals required by the sensor front-end together with the synchronization signal between the front-end and the decimator. The reference voltage buffers (REFBUFS) generate the required reference voltages, a positive reference and common-mode input and output voltages, for the sensor front-end.

The sensor interface has two 12-bit operating modes, namely 1 Hz and 25 Hz modes, according to their signal bandwidths. The sampling frequencies per mass are $4.096\ \text{kHz}$ and $51.2\ \text{kHz}$, respectively. Low power dissipation is required especially in the 1 Hz mode. The sensor interface requires two 1.0 V supplies, one for the $\Delta\Sigma$ sensor front-end, and one for the FREF and CLKG. Additionally, the decimator requires a programmable 1.0–1.8 V supply because the required supply voltage level of the used standard digital cells increases as a function of clock frequency. The LDOs share the voltage and current references in the system level.

A tail-current-boosted Class AB operational amplifier is used in the $\Delta\Sigma$ sensor front-end. From the LDO point of view the used dynamical biasing means that the LDO must be able to respond large current peaks with quite slow settling times. The 25 Hz mode causes larger current peaks being more difficult for the LDO. Fig. 2 (a) shows one of the largest simulated current peaks of the $\Delta\Sigma$ sensor front-end. The required charge is approximated with a triangle resulting in a charge of $50\ \text{pC}$ ($\Delta Q = I_{\text{AVG}} \cdot \Delta t$). The LDO has to feed this charge, which causes a voltage drop at the LDO output. This voltage drop depends on the capacitance in the same node as illustrated in Fig. 2 (b) ($\Delta V = \Delta Q/C$), when assuming the

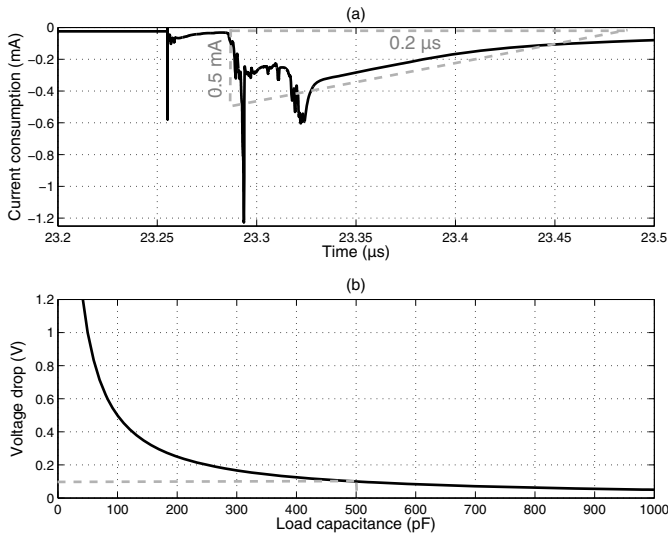


Fig. 2. (a) One of the largest simulated current peaks of the $\Delta\Sigma$ sensor front-end, and (b) a voltage drop as a function of the load capacitance when $\Delta Q = 50 \text{ pC}$.

current peak with a charge of 50 pC . The maximum tolerable voltage drop at the LDO output has been specified to be 0.1 V . Thus, according to Fig. 2 (b), the required load capacitance is 500 pF . The use of dynamic biasing increases the required on-chip load capacitance, and thus the required silicon area, to achieve the maximum tolerable voltage drop.

The rest of the paper is organized as follows. Next, in Section II, the building blocks of the designed LDO are described. The experimental results are presented in Section III, and finally conclusions are made in Section IV.

II. CIRCUIT DESCRIPTION

A. Regulator Core

The regulator core shown in Fig. 3 (a) is based on the LDO presented in [2]. It uses a Q-reduction technique to minimize both the required on-chip capacitance and the minimum output current.

The regulator core consists of the first gain stage (M1-M5), the second noninverting gain stage (M6-M9), the pass transistor (M10) that forms the third gain stage, the required compensation capacitors (C_{m1} and C_{cf}), the feedback resistive network (R_{f1} and R_{f2}), and the equivalent load capacitor and resistor (C_L and R_L). The transistors M2, M4, and M9 form a feedforward transconductance stage.

The compensation capacitor C_{m1} is used to split the poles. At low output current, the nondominant complex poles have a large Q and are located near unity-gain frequency (UGF). The minimum output current level can be reduced by increasing C_{m1} for lowering the UGF. The Q-reduction circuit is formed by C_{cf} and a current buffer formed by M4 and M5. The stability considerations at different loading conditions can be found from [2].

In [2], the minimum output current is reported to be $100 \mu\text{A}$. The LDO presented in this paper is able to operate with zero load current ($R_L \rightarrow \infty$). In this design, the passive

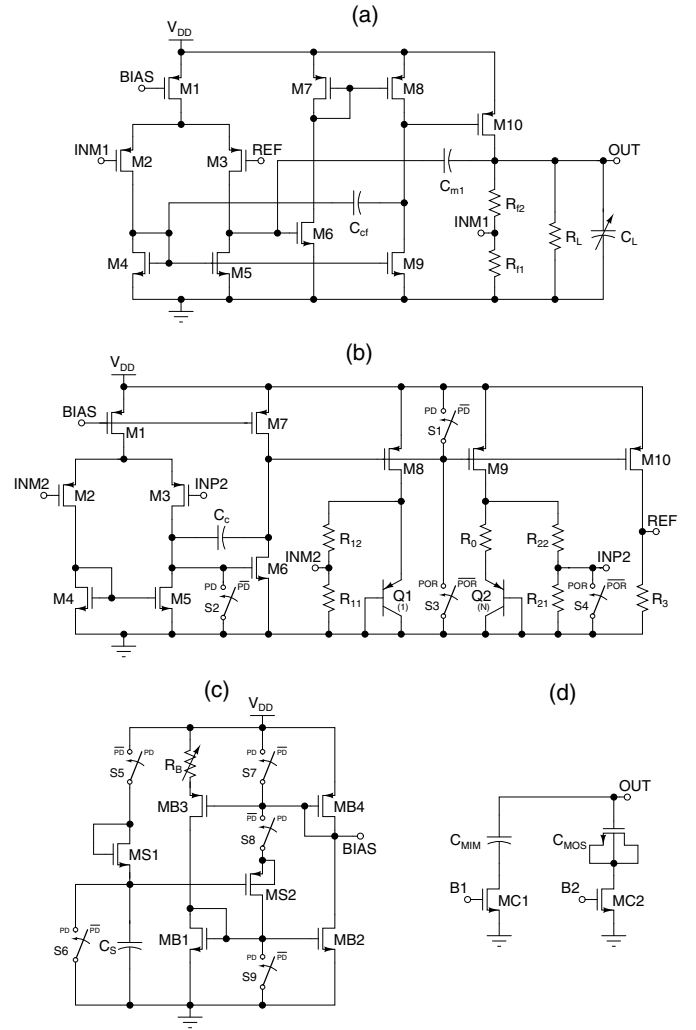


Fig. 3. Schematics of: (a) a regulator core; (b) a bandgap reference; (c) a PTAT current generator, and (d) a load capacitor unit.

components C_{m1} , C_{cf} , R_{f1} , and R_{f2} get the following values: 6.5 pF , 1.5 pF , $150 \text{ k}\Omega$, and $350 \text{ k}\Omega$, respectively. Thus, nominally the current of $2 \mu\text{A}$ flows through the feedback resistive network. The requirement for stability at zero load current results in a small bandwidth of 25 kHz for the loop response, being still sufficient for this application. To cover process variations this prototype LDO was equipped with a programmable on-chip load capacitor of 1 nF .

B. Bandgap Reference

The bandgap reference shown in Fig. 3 (b) is based on the topology presented in [6]. This circuit can also be implemented with a standard CMOS process. A Miller-compensated operational amplifier with a PMOS input pair is used as the feedback amplifier (M1-M7). Its output controls the gates of M8-M10. The drain currents of these three transistors are

$$I_{M8, M9, M10} = \frac{V_{EB1}}{R_1} + \frac{\ln(N)}{R_0} \cdot V_T, \quad (1)$$

where $R_1 = R_{11} + R_{12} = R_{21} + R_{22} = R_2$ and R_0 are resistances of the corresponding resistors, N is the emitter

area ratio, V_T the thermal voltage, and V_{EB1} the emitter-base voltage of the bipolar transistor Q1. To make possible the use of supply voltages down to 1.2 V, the input voltage levels of the operational amplifier are reduced with voltage divisions (resistive networks of R_1 and R_2). The output voltage of the bandgap reference, or the reference voltage, is defined as

$$V_{REF} = \frac{R_3}{R_1} \cdot \left[V_{EB1} + \frac{R_1 \cdot \ln(N)}{R_0} \cdot V_T \right], \quad (2)$$

where R_3 is the resistance of the output stage.

The resistance values were chosen such that the temperature coefficient (TC) of the 0.3 V reference voltage was minimized under typical conditions. The used resistance values are $R_0 = 163 \text{ k}\Omega$, $R_{11} = R_{21} = 500 \text{ k}\Omega$, $R_{21} = R_{22} = 1000 \text{ k}\Omega$, and $R_3 = 375 \text{ k}\Omega$. At the same time, the current consumption was traded off with the silicon area. The typical V_{EB} of the used PNP transistors is about 0.725 V. The bandwidth of the bandgap reference is reduced using the compensation capacitor C_c of 20 pF. As a result, the bandwidths of the negative feedback loop and the closed loop are 6.1 kHz and 37.6 kHz, respectively.

The PMOS switch S1 and the NMOS switch S2 were included to provide a power-down (PD) mode. The NMOS switches S3 and S4 were included to provide a power-on-reset (POR) that can be used to force the bandgap reference to the right operating point, if needed.

C. PTAT Current Generator

The proportional-to-absolute temperature (PTAT) current generator shown in Fig. 3 (c) is used to generate a reference current. The transistors MB1-MB4 together with the resistor matrix R_B form the current generator. The nominal reference current is 75 nA ($R_B = 100 \text{ k}\Omega$). The transistors MS1 and MS2, and the capacitor C_S (5 pF) form a start-up circuit. The switches S5-S9 are required to power down the circuit. The capacitor C_S must be discharged before the next start-up.

D. Load Capacitor Unit

A load capacitor unit is shown in Fig. 3 (d). It consists of one metal-insulator-metal (MIM) capacitor of 70 pF and one NMOS capacitor of approximately 55 pF. The NMOS devices MC1 and MC2 with the W/L ratios of 100 $\mu\text{m}/0.25 \mu\text{m}$ are used for programming (control bits B1 and B2). There are eight load capacitor units on the chip. Thus, the load capacitance can nominally be adjusted at 55 pF or 70 pF steps over the whole capacitance range from 0 to 1 nF using 16 control bits. The used technology provides the stacking of the MIM capacitors above the MOS capacitors. This advantage was used to minimize the silicon area.

III. EXPERIMENTAL RESULTS

The microphotograph of the implemented LDO is shown in Fig. 4. The active silicon area of the LDO is approximately 0.18 mm². The programmable load capacitor occupies 64 % from that despite the capacitor stacking. The size of the chip with bonding pads is 0.975 mm $\times$ 0.984 mm. The experimental results presented in this Section were obtained at room

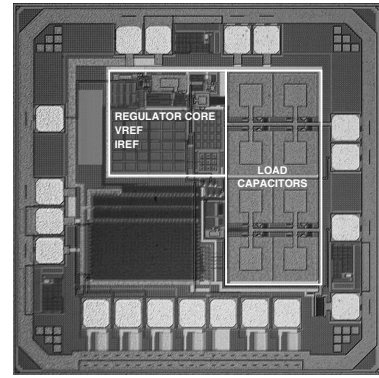


Fig. 4. Microphotograph of the presented LDO.

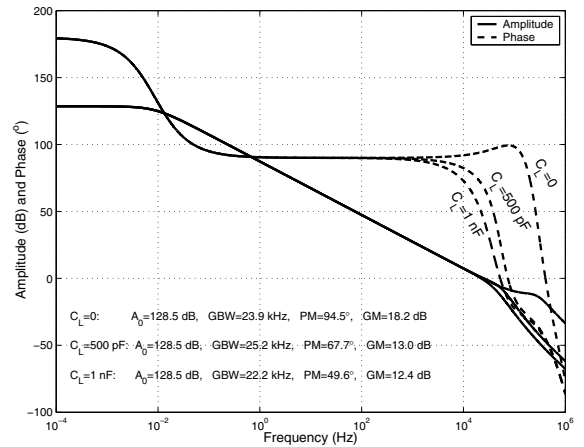


Fig. 5. Loop responses of the regulator core at zero load current with different load capacitances.

temperature with a 2.0 V supply, a 500 pF load capacitor, and zero load current, unless otherwise mentioned.

Three simulated loop responses of the regulator core, corresponding the load capacitances of zero, 500 pF, and 1 nF, are shown in Fig. 5. The worst case condition for stability occurs when $C_L = 1 \text{ nF}$. Typically at zero load current the regulator core has a dc gain (A_0) of 128.5 dB, a gain-bandwidth product (GBW) of 25.2 kHz, a phase margin (PM) of 67.7°, and a gain margin (GM) of 13.0 dB. The phase and gain margins are improved when the load current is increased.

The typical quiescent current of the whole LDO circuit is 7.6 μA . The current generator consumes 150 nA (2.0 %), and the rest of the current is distributed quite equally between the regulator core and the voltage reference, being 3.935 μA (51.5 %) and 3.555 μA (46.5 %), respectively.

The measured temperature dependencies of both the voltage reference and the LDO output are shown in Fig. 6. The TC of the whole LDO is determined mainly by the voltage reference, because the measured TC of the LDO output is only 1.7 ppm/°C worse than the TC of the voltage reference, that is 55.5 ppm/°C. The TCs are calculated according to the fitting curves shown in Fig. 6. The corresponding simulated best case TCs are below 10 ppm/°C. The measured line and load regulation are shown in Fig. 7. The line regulation over the

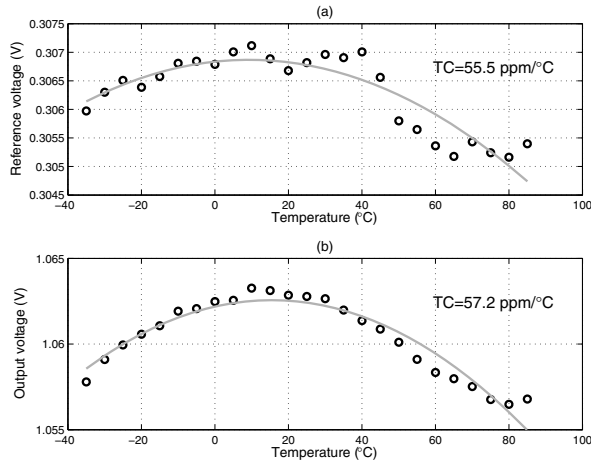


Fig. 6. Measured temperature dependency of (a) the voltage reference, and (b) the LDO output.

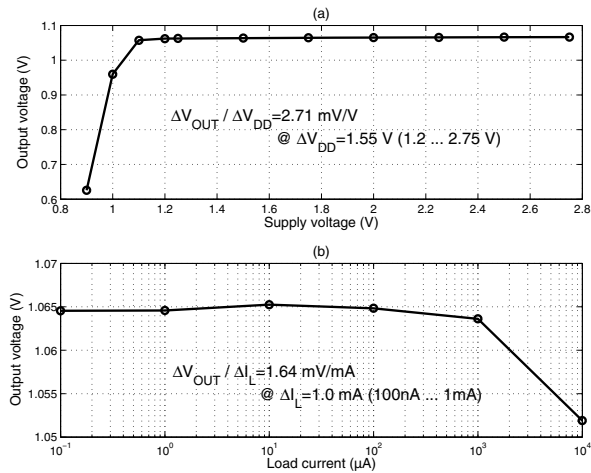


Fig. 7. Measured (a) line and (b) load regulation.

supply voltage range of 1.55 V (1.2 ... 2.75 V) is 2.71 mV/V. The designed bandgap reference limits the minimum input voltage to 1.2 V at -40°C . The load regulation over the load current range of 1 mA (100 nA ... 1 mA) is 1.64 mV/mA.

The measured rms noises integrated over the bandwidth ranging from 1 Hz to 100 kHz at the outputs of the voltage reference and the LDO are 425 μV and 1.365 mV, respectively. The transient responses with rectangular current pulses having the charges of 100 pC (500 $\mu\text{A} \cdot 200\text{ ns}$) measured with different load capacitances are shown in Fig. 8. The hyperbola fitted to the obtained voltage drops is shown in the subfigure. It predicts that the total load capacitance, including all the parasitics arising from wirings, bonding, printed circuit board, and measurement probes, is about 220 pF larger than the nominal capacitance C_L . The summary of the measured performance is shown in Table I.

IV. CONCLUSION

In this paper, a micropower LDO with a programmable on-chip load capacitor fabricated in a 0.25 μm BiCMOS process for a capacitive low-power sensor interface was presented. The input voltage range extends from 1.2 to 2.75 V, while

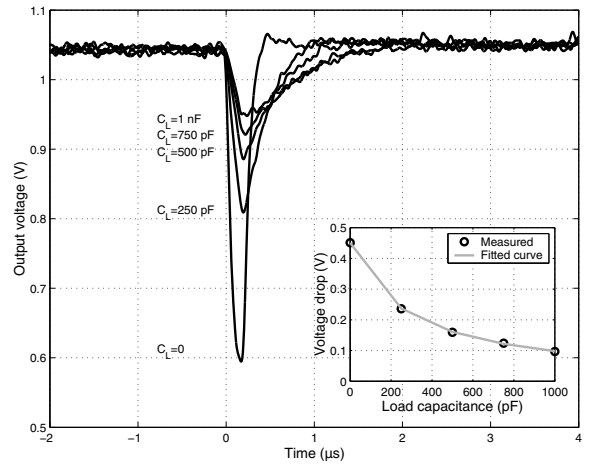


Fig. 8. Measured transient responses with rectangular current pulses having the charges of 100 pC, and the corresponding voltage drops (subfigure) as a function of the load capacitance C_L .

TABLE I
PERFORMANCE SUMMARY.

Technology	0.25 μm BiCMOS
Temperature range	$-40 \dots +85^{\circ}\text{C}$
Input voltage range	1.2 ... 2.75 V
Output voltage	1.0 V
Dropout voltage	0.2 V
Quiescent current	7.6 μA
Output current	0 to 1 mA
Temperature coefficient	57.2 mV/ $^{\circ}\text{C}$
Line regulation	2.71 mV/V
Load regulation	1.64 mV/mA
Rms noise	1.365 mV @ 1 Hz ... 100 kHz @ $+25^{\circ}\text{C}$
On-chip load capacitance	0 ... 1 nF
Active silicon area	0.18 mm ²

the designed output voltage is 1.0 V. The measured quiescent current of the LDO including the voltage and current reference is 7.6 μA . The LDO is stable with zero load current over the load capacitance range from 0 to 1 nF. The regulated output was measured to have a TC of 57.2 ppm/ $^{\circ}\text{C}$, a line regulation of 2.71 mV/V, and a load regulation of 1.64 mV/mA.

REFERENCES

- [1] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003.
- [2] S. K. Lau, P. K. T. Mok, and K. N. Leung, "A low-dropout regulator for SoC with Q-reduction," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 658–664, Mar. 2007.
- [3] M. Kämäräinen, M. Paavola, E. Laulainen, M. Saukoski, L. Koskinen, M. Kosunen, and K. Halonen, "A 1.5 μW 1V 2nd-order $\Delta\Sigma$ sensor front-end with signal boosting and offset compensation for a capacitive 3-axis micro-accelerometer," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2008, pp. 578–579.
- [4] E. Laulainen, M. Kosunen, L. Koskinen, M. Paavola, and K. Halonen, "Decimation filter for a low-power sensor-interface system," in *Proc. IEEE Norchip Conf.*, Aalborg, Denmark, Nov. 2007.
- [5] M. Paavola, M. Saukoski, M. Laiho, and K. Halonen, "A nanopower double-mode 1-V frequency reference for an ultra-low-power capacitive sensor interface," in *Proc. IEEE Eur. Conf. Circuit Theory and Design*, Sevilla, Spain, Aug. 2007, pp. 104–107.
- [6] K. N. Leung and P. K. T. Mok, "A sub-1-V 15-ppm/ $^{\circ}\text{C}$ CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE J. Solid-State Circuits*, vol. 37, no. 4, pp. 526–530, Apr. 2002.