

Publication P9

M. Paavola, M. Laiho, M. Saukoski, M. Kämäräinen, and K. A. I. Halonen. 2010. Impulse sensitivity function-based phase noise study for low-power source-coupled CMOS multivibrators. *Analog Integrated Circuits and Signal Processing*, volume 62, number 1, pages 29-41.

© 2009 Springer Science+Business Media

Reprinted with kind permission of Springer Science and Business Media.

Impulse sensitivity function-based phase noise study for low-power source-coupled CMOS multivibrators

M. Paavola · M. Laiho · M. Saukoski ·
M. Kämäräinen · K. A. I. Halonen

Received: 2 January 2009 / Revised: 6 March 2009 / Accepted: 14 May 2009 / Published online: 3 June 2009
© Springer Science+Business Media, LLC 2009

Abstract In this paper, two micropower frequency references implemented with a 0.13- and a 0.25- μm CMOS process for low-power sensor applications are presented. Both circuits are based on a power-optimized source-coupled CMOS multivibrator. The 2.0-MHz frequency reference uses a nominal 1.8–2.5-V supply voltage. The 24.6/307.2-kHz frequency reference is an evolution of the 2.0-MHz reference and operates with a lower supply of 1.0 V and provides two active operating modes. With 1-pF load capacitances, the 2.0-MHz and 24.6/307.2-kHz frequency references typically consume 6.7 μA and 230/750 nA, respectively. After presenting experimental results relating to frequency trimming and frequency stability, this paper concentrates on the phase noise study of the proposed frequency references. The procedure used to apply the impulse

sensitivity function-based (ISF) phase noise method to CMOS oscillators is described in detail. The phase noise results of both the implemented references obtained with this method agree well with the measurements.

Keywords Impulse sensitivity function · Low-power circuit · Low-voltage circuit · Multivibrator · Oscillator · Phase noise

1 Introduction

Emitter- [1–4] and source-coupled [4–7] multivibrators with a floating timing capacitor are well-known circuits and are commonly used as voltage- and current-controlled oscillators. These circuits are simple, are easily integrated, and provide symmetric output waveforms. The main difference between the bipolar and CMOS implementations relates to the square law characteristics of the CMOS devices and the body effect of the NMOS devices. Two recently published theoretical articles, [4, 7], deepen the understanding of both emitter- and source-coupled multivibrators. In [4], the classical discontinuity theory is used to analyze both types of multivibrators, and accurate formulae for predicting their oscillations are presented. The existence of sinusoidal oscillation with small timing capacitors is proved for the first time. It is also shown that these multivibrators can be represented by a series resonant circuit (RLC). In [7], in contrast to [4], the same differential equation is used to consider both relaxation and sinusoidal oscillations in the CMOS implementation. According to the limit cycles plotted on the phase-plane with differently sized timing capacitors, it can be clearly seen that there is a continuum between sinusoidal and relaxation oscillations.

M. Paavola (✉) · M. Laiho · M. Saukoski · M. Kämäräinen ·
K. A. I. Halonen
SMARAD-2/Electronic Circuit Design Laboratory, Helsinki
University of Technology, 02150 Espoo, Finland
e-mail: mhpaavol@ecd.tkk.fi

M. Laiho
e-mail: mlaiho@ecd.tkk.fi

M. Saukoski
e-mail: mikko.saukoski@elmos.eu

M. Kämäräinen
e-mail: mpkamara@ecd.tkk.fi

K. A. I. Halonen
e-mail: karih@ecd.tkk.fi

M. Laiho
Microelectronics Laboratory, University of Turku, 20520 Turku,
Finland

M. Saukoski
ELMOS Semiconductor AG, 44227 Dortmund, Germany

Figure 1(a) and (b) show the schematics of a conventional and a power-optimized [6] source-coupled CMOS multivibrator, respectively. The power reduction scheme is based on additional switching devices (M3–M4) between the timing capacitor C and the tail current sources. This makes it possible to merge the two tail current sources of the conventional circuit. As a result, the charging current $i = C(\Delta v/\Delta t)$, and thus the oscillation frequency $f_0 = 1/\Delta t = i/(C\Delta v)$, is almost doubled with the same power dissipation of the multivibrator $P = V_{DD}I$, where I is the total tail current of the multivibrator. Alternatively, the power dissipation of the multivibrator can be almost halved while the operating speed is kept constant. Together with I , the resistive load R determines the output voltage swing $V_{swing} = RI$, and hence it affects the oscillation frequency through the proportionality of $f_0 \propto I/(CV_{swing}) = 1/(RC)$ [6]. Compared to the conventional multivibrator the power-optimized structure includes one additional noise source, but as will be seen later in this paper, the devices M3 and M4 make only a minor contribution to the total phase noise. The two frequency reference circuits proposed in this paper are based on the power-optimized multivibrator topology, and they provide master clock signals for two complete, fully integrated, low-power, discrete-time analog sensor interfaces [8, 9].

The general theory of phase noise in electrical oscillators, based on the linear time-variant (LTV) system, is presented in [10]. In this theory, the impulse sensitivity functions (ISFs) of the devices are used to derive their phase noise contributions. The effectiveness of the theory has already been shown, e.g. as presented by the authors in [11]. In this paper, an illustrative 10-step procedure for applying the ISF-based phase noise study to CMOS oscillators is described, after which it is used for the two implemented frequency references. In comparison to the prior publications [11–13], the presentation is extended by providing new simulation

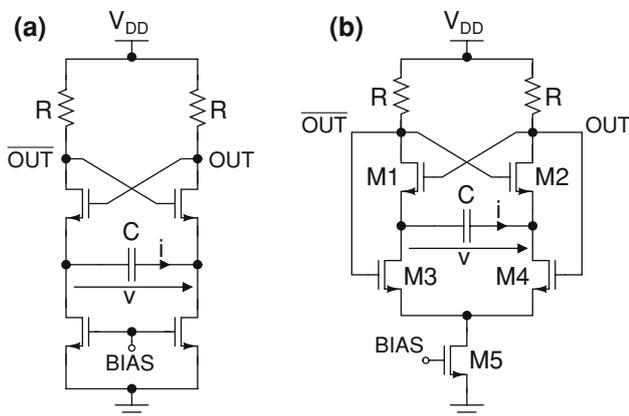


Fig. 1 Schematics of **a** a conventional and **b** a power-optimized source-coupled CMOS multivibrator

and measurement results, together with a more detailed phase noise study. The rest of the paper is organized as follows: Sects. 2 and 3 describe the application-specific requirements and the designed frequency references, respectively. The experimental results are presented in Sect. 4, while the detailed phase noise study and a brief comparative discussion about different phase noise estimation methods are presented in Sects. 5 and 6, respectively. Finally, conclusions are drawn in Sect. 7.

2 Specifications

Low signal and clock frequencies are typical for sensor applications, and this helps to meet often stringent power dissipation requirements. In [8], the input bandwidth BW_{in} of the acceleration signal is specified as being 100 Hz. The input bandwidth in [9] is either 1 or 25 Hz, depending on the operating mode. The master clock frequencies required by the sensor interfaces are 2.0 MHz and 24.6/307.2 kHz, respectively. The instantaneous error in the sampling, caused by rms jitter $\Delta\tau$ in the clock signal, results in a signal-to-noise ratio of

$$SNR = -20 \cdot \log(2\pi f \Delta\tau), \quad (1)$$

where f is the frequency of a sinusoidal input signal [14]. According to (1) the SNR is independent of signal amplitude. The maximum allowed jitter of the master clock signal can be approximated by solving $\Delta\tau$ from (1) and using $f = BW_{in}$. Hence, in order to achieve 12-bit resolution in the sensor interface of [8], which utilizes the 2.0-MHz clock signal, the maximum allowed rms jitter is 0.3 μ s. Because of the limited signal available from the accelerometer that is sensed by the other sensor interface [9] using either the 24.6- or 307.2-kHz master clock signal, a higher resolution of 16 bits is required from the reference circuits. For the two operating modes of this sensor interface the maximum allowed rms jitter values are 2.43 μ s and 97 ns, respectively. The parameters used to specify the aforementioned jitter values are summarized in Table 1. The phase noise values, determined from the white noise regions of the phase noise plots with slopes of -20 dB/dec, can be converted to cycle-to-cycle jitters by using the equation

Table 1 Parameters used to specify the maximum allowed jitter values in the cases of different frequency references and their operating modes

References	f_0	BW_{in} (Hz)	SNR (dB)	$\Delta\tau_{max}$
[8]	2.0 MHz	100	72.2	0.3 μ s
[9]	24.6 kHz	1	96.3	2.43 μ s
[9]	307.2 kHz	25	96.3	97 ns

$$\Delta\tau_{cc} = \frac{\Delta f}{f_0^{1.5}} 10^{L\{\Delta f\}/20}, \tag{2}$$

where Δf is the offset frequency from the carrier, f_0 the oscillation or carrier frequency, and $L\{\Delta f\}$ the phase noise at a certain offset frequency from the carrier in decibels [15].

The frequency references used in [8, 9] nominally operate from a 1.8–2.5-V and a 1.0-V supply voltage, respectively. Additionally, $\pm 10\%$ supply margins were taken into account in these designs. The specified temperature range extends from -40 to $+85^\circ\text{C}$. After the frequency trimming, which is provided for both circuits at the expense of a larger silicon area and longer testing time, the oscillation frequency is not allowed to vary by more than $\pm 15\%$ from the nominal value. These limits include the variation resulting from both the temperature and supply voltage.

3 Circuit description

The operating principle of the power-optimized source-coupled CMOS multivibrator shown in Fig. 1(b) is, briefly, as follows. A cross-coupled pair, formed by the devices M1 and M2, operates as a gain stage and it drives equally sized resistor loads R. The devices M1 and M2 switch alternately on and off, and they control the operation of the differential pair formed by M3 and M4, which in turn determines the direction of the charging current i . The device M5 supplies the tail current. The voltage waveform v across the floating timing capacitor C is a triangle, while the output voltage waveforms can resemble either relaxation or sinusoidal oscillations, depending on the timing capacitance. According to the simulations, the oscillation frequency can be estimated with

$$f_0 \approx \frac{0.8I}{4CV_C}, \tag{3}$$

where I is the tail current, C the capacitance of the floating timing capacitor, and V_C the amplitude of the voltage swing over that capacitor. The coefficient 0.8 arises from the non-ideal switching of M3 and M4 operating in the triode region [6].

Next, the implemented 2.0-MHz frequency reference is described, together with its special characteristics. After that the modifications required for the 24.6/307.2-kHz frequency reference as a result of the lower supply voltage are discussed. The schematics of the frequency references are shown in Fig. 2(a) and (b), respectively, while the matrix structures used for frequency trimming are shown in Fig. 2(c).

3.1 2.0-MHz frequency reference

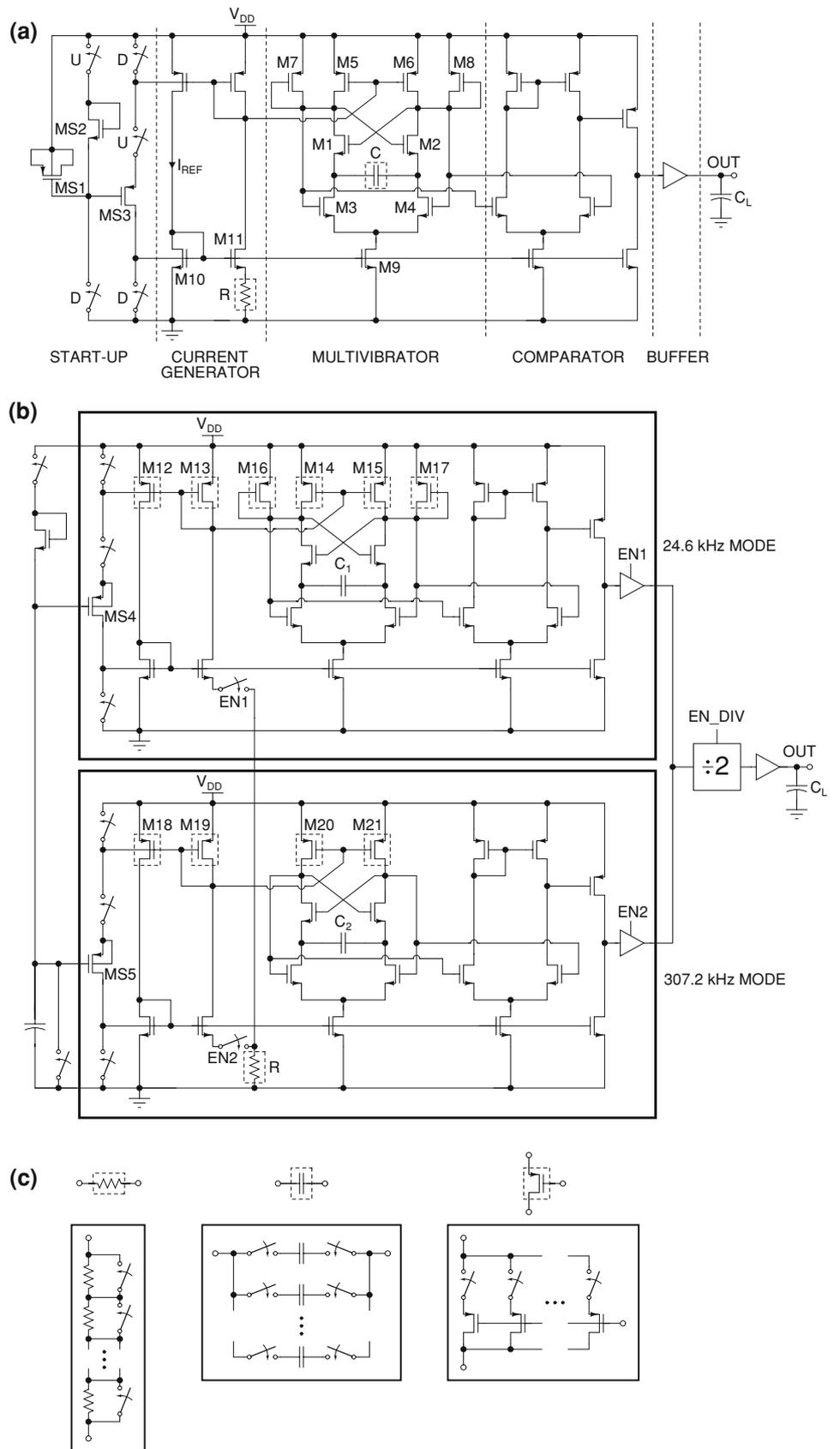
The complete reference circuit consists of a start-up circuit, a current generator, a multivibrator, a comparator, and a buffer. In the multivibrator, the passive loads are replaced with active ones that operate in the linear region. Additionally, based on the simulations the drain clamping with diode-connected PMOS devices (M7–M8) is utilized to improve the overall oscillation frequency stability over the process, voltage, and temperature (PVT) variations. The simulated I–V characteristics of the active load with and without the drain clamping were presented in [12]. With the equally sized devices (M5–M8) used in this implementation the effect of the diode-connected devices can clearly be seen until the larger tail currents. The drain clamping linearizes the equivalent load resistance of the active load by limiting the output voltage swing. The improvement of the overall frequency stability results from the better matching of the PVT dependencies between the numerator and denominator of (3), in other words, mainly from the better stability of the equivalent load resistance [11]. Collector clamping, traditionally used in current-controlled emitter-coupled multivibrators, is considered in detail in [3].

The frequency trimming can be performed by using both a floating timing capacitor matrix C of the multivibrator and a biasing resistor matrix R of the proportional-to-absolute-temperature-type (PTAT) current generator. Supply independent biasing, provided by the PTAT current generator, was chosen because of the large supply voltage range of 1.8–2.5 V. The circuit was designed to operate from 1.62 to 2.75 V without extra calibration. When the devices of the current generator operate in the saturation region and the body effect of M11 is omitted, the reference current can be written as

$$I_{REF} = \frac{2}{\mu_n C_{ox} (W/L)_{10}} \cdot \frac{1}{R^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2, \tag{4}$$

where μ_n is the electron mobility, C_{ox} the gate-oxide capacitance per unit area, $(W/L)_{10}$ the aspect ratio of the device M10, R the biasing resistance, and K the ratio $(W/L)_{11}/(W/L)_{10}$. Thus, I_{REF} is independent of the supply voltage, but it depends on the process corner and temperature. Because the biasing resistance directly affects the tail current, it is better suited for fine-tuning in the case of the low-power fixed-frequency application under consideration. In this implementation, the tail current of the multivibrator ideally equals I_{REF} , and thus (4) can be directly substituted into (3). As a side benefit of trimming, a smaller timing capacitance C , compared to a non-trimmed design, can be used without any need to worry about frequency variation. This makes reduced power dissipation possible.

Fig. 2 Schematics of the presented frequency references: **a** a 2.0-MHz and **b** a 24.6/307.2-kHz frequency reference, and **c** the matrix structures used for frequency trimming



The desired 2.0-MHz oscillation frequency can be achieved with several combinations of R and C . Figure 3 shows the simulated contour plot that illustrates the frequency calibration as a function of both the biasing resistance and the timing capacitance. The contour lines correspond to the oscillation frequencies in megahertz. Another simulated contour plot, shown in Fig. 4, illustrates the temperature and supply voltage dependency of the oscillation frequency. Again, the contour lines correspond to the oscillation frequencies in megahertz. According to the figure, the oscillation frequency typically varies by about $\pm 6\%$ over the specified temperature range and $\pm 1\%$ over the specified supply voltage range. The strong temperature dependency of the tail current is partially eliminated in (3), for V_C also depends on the same current [11]. In contrast to the bipolar version, the oscillation frequency of the CMOS multivibrator also depends on the supply voltage as a result of the nonzero voltage-dependent source-bulk voltages of M1–M4 [5].

A start-up circuit, formed by the devices MS1–MS3 together with some switching devices, is required because $I_{REF} = 0$ also results in a stable operating point. Either the switches marked with U (power-up) or D (power-down) are conducting. MS1 operates as a start-up capacitor, which must be discharged before the next start-up. During the start-up MS3 pulls the gates of the NMOS current sources high ensuring a reliable start-up. After the gate of MS1 has charged through MS2, the gate-source voltage of MS3 falls to a low enough level to cut it off. A rail-to-rail clock signal is generated by using a two-stage differential comparator, while an output buffer drives an on-chip capacitive load of

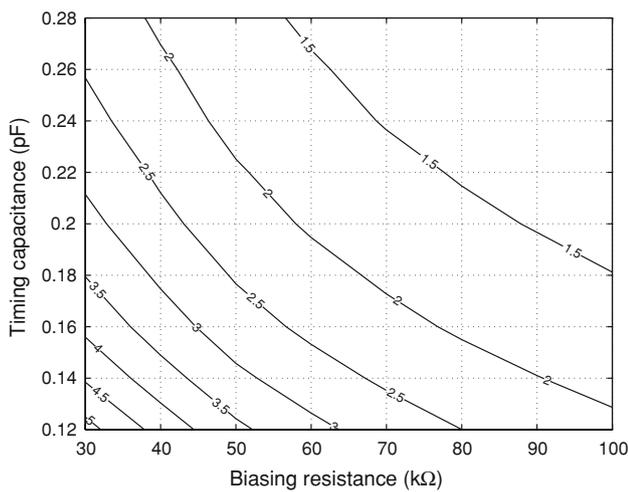


Fig. 3 Simulated contour plot illustrating the frequency calibration of the 2.0-MHz frequency reference by trimming both the floating timing capacitance C and the biasing resistance R . Contour lines correspond to the oscillation frequencies in megahertz

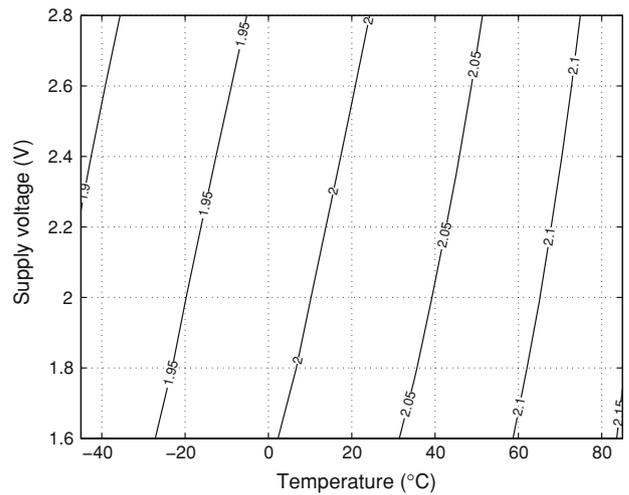


Fig. 4 Simulated contour plot illustrating the temperature and supply voltage dependencies of the 2.0-MHz frequency reference. Contour lines correspond to the oscillation frequencies in megahertz

approximately 1 pF (C_L) consisting of wiring and logic gates.

The simulated voltage waveform across the timing capacitor, and at the outputs of the multivibrator and buffer are shown in Fig. 5(a)–(c), respectively. A timing capacitor of 0.2 pF was used in this simulation. According to Fig. 5(b), the oscillation is neither relaxation nor sinusoidal, but some kind of a mixture of the two. This kind of oscillation waveform could be expected for the required 2.0-MHz signal, because according to (3) the timing capacitance C was minimized to save tail current I , and thus the power dissipation of the multivibrator.

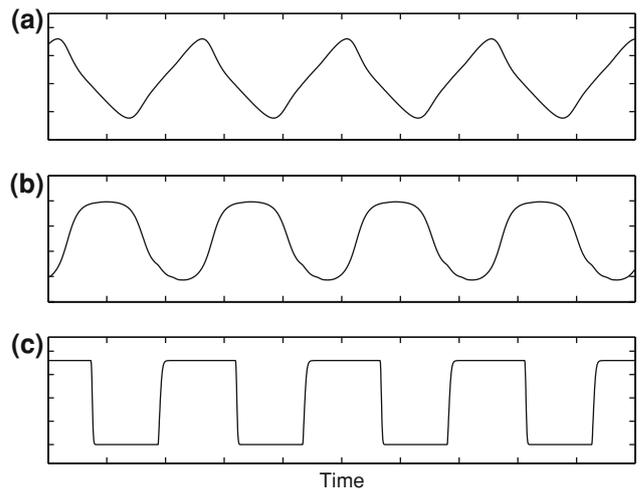


Fig. 5 Simulated voltage waveforms of the 2.0-MHz frequency reference **a** across the timing capacitor, **b** at the multivibrator output, and **c** at the buffer output

3.2 24.6/307.2-kHz frequency reference

Some modifications are required compared to the 2.0-MHz reference circuit because of the lower nominal supply voltage of 1.0 V. The use of a single floating capacitor matrix in the multivibrator, as in the case of the 2.0-MHz frequency reference, is not possible. To solve the floating switch problem, and to provide a large enough frequency tuning range for the calibration of process variations, two parallel frequency references, as shown in Fig. 2(b), were designed, one for each operating mode. The upper and lower branches are active in the 24.6- and 307.2-kHz modes, respectively. The PMOS matrices M12–M21 and a single biasing resistor matrix R, the structures of which are shown in Fig. 2(c), are used for coarse- and fine-tuning, respectively. All the PMOS matrices are trimmed equally and simultaneously using the same control signals. The same resistor matrix and partially the same start-up circuit are used for both operating modes. The timing capacitances C_1 and C_2 are nominally 5.5 and 1.0 pF, respectively.

In the 24.6-kHz mode drain clamping is used in the multivibrator to improve the overall oscillation frequency stability [13], as in the case of the 2.0-MHz reference. In the absence of the drain clamping, the equivalent load resistance of the 307.2-kHz mode varies less than that of the 24.6-kHz mode. In the 307.2-kHz mode, the sufficient frequency stability of $\pm 15\%$ from the nominal value is also achieved without the drain clamping. Therefore, in order to reduce the number of transistor matrices and thus to save silicon area, the drain clamping was excluded from that mode. The bulk electrodes of MS4 and MS5 are connected to their sources to speed up the start-up. Tri-state buffers provide an interface between the parallel frequency references and the customized flip-flop divider [13]. The

enabling of the divide-by-two operation depends on the sensor interface configuration [9].

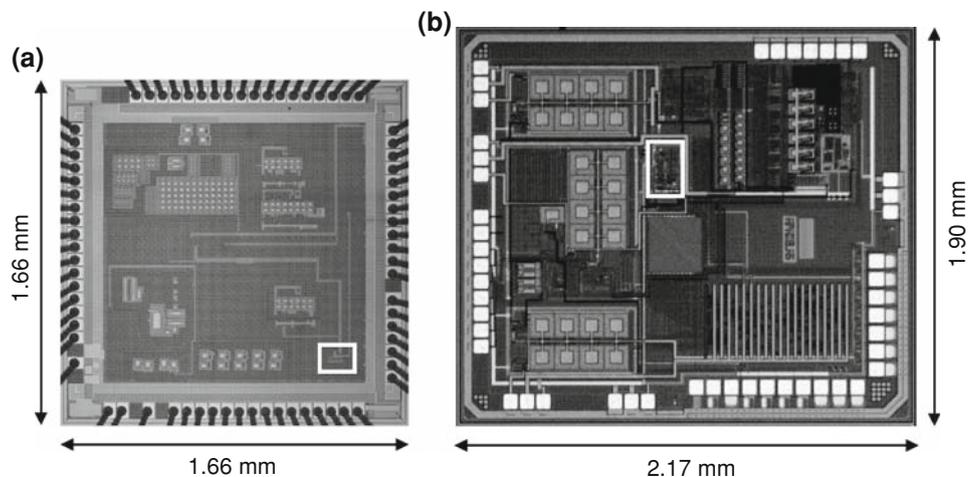
4 Experimental results

Two implemented prototype ICs fabricated in a 0.13- and a 0.25- μm CMOS process are shown on the same scale in Fig. 6(a) and (b), respectively. The active silicon area of the 2.0-MHz frequency reference is 0.0088 mm², while the 24.6/307.2-kHz frequency reference occupies 0.0275 mm². Next, some measurement results of both frequency references are presented.

Figure 7 shows both the measured oscillation frequency and current consumption as a function of temperature for the 2.0-MHz frequency reference. The circuit was calibrated at +25°C by using a 1.8-V supply with $C = 0.2$ pF and $R = 60$ k Ω . Typically, the total current consumption is in the order of 6.7 μA , from which the output buffer accounts for roughly two thirds. When extrapolating the plotted fitting curves down to -40°C , the oscillation frequency changes by +7.5/–8.5%, and the current consumption by $\pm 19.0\%$, both over the specified temperature range. The measured supply voltage sensitivity is of an order of 2.5% over the supply voltage range of 1.62–2.75 V. The linear temperature-frequency characteristics of the proposed frequency reference, shown in Fig. 7, could also be exploited in a temperature reference circuit.

A few calibration curves of the 24.6/307.2-kHz frequency reference measured in the 24.6- and 307.2-kHz operating modes are shown in Fig. 8(a) and (b), respectively. The biasing resistance R was trimmed at 10-k Ω steps. There are three additional fine-tuning steps between all the measured values. Each curve has a total channel width value W of its own, which refers to the transistor matrices [13]. According

Fig. 6 Microphotographs of the implemented prototype ICs. The presented frequency references are marked with white boxes: **a** a 2.0-MHz and **b** a 24.6/307.2-kHz frequency reference



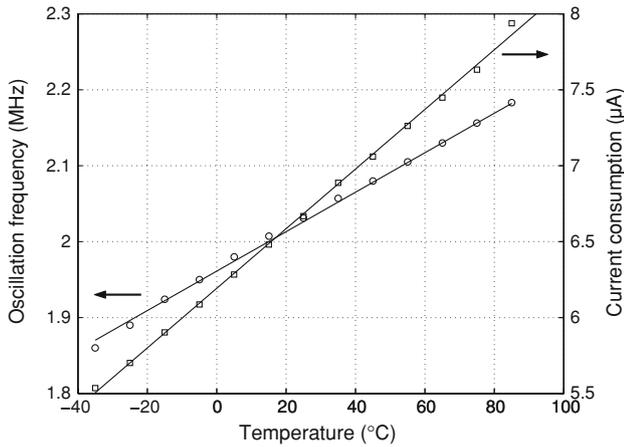
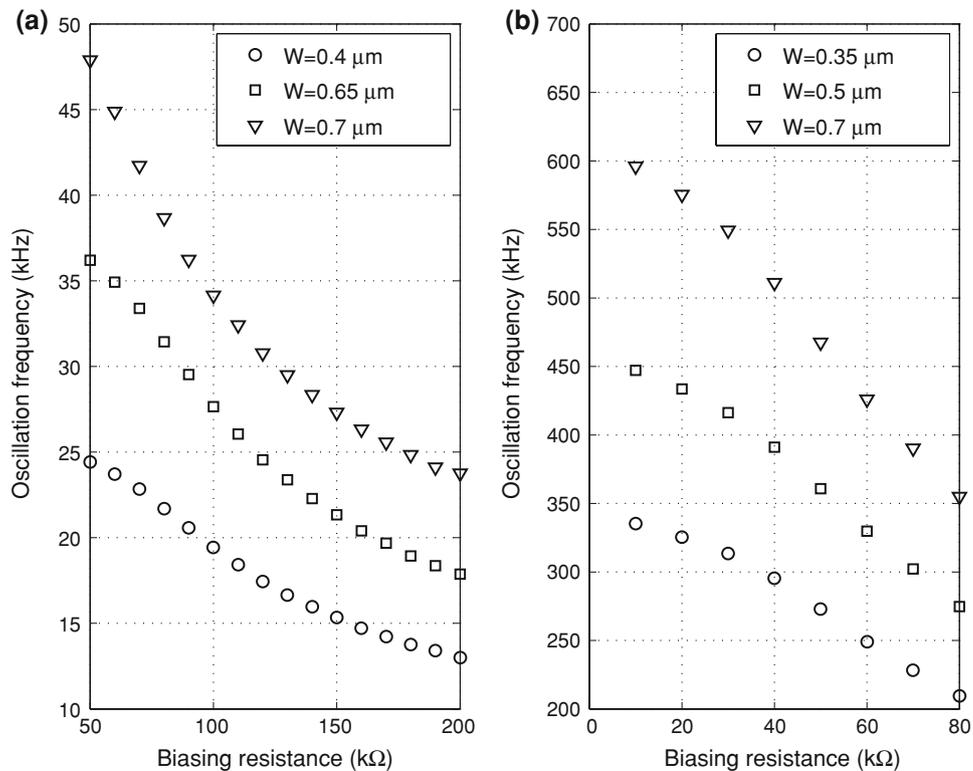


Fig. 7 Oscillation frequency and current consumption of the 2.0-MHz frequency reference measured over the temperature range

to these curves, a large tuning range can be achieved in both operating modes to cover process variations. The typical total current consumptions in the 24.6- and 307.2-kHz operating modes are 230 nA ($W = 0.65 \mu\text{m}$ and $R = 120 \text{ k}\Omega$) and 750 nA ($W = 0.5 \mu\text{m}$ and $R = 67.5 \text{ k}\Omega$), respectively. In the 307.2-kHz mode the output buffer consumes almost one half of the total current, while in the 24.6-kHz mode the share of the buffer is roughly 10%. In the 24.6-kHz mode the measured temperature sensitivity over the specified temperature range is $+7.5/-8.2\%$, while the measured supply voltage sensitivity is 3.8% over the supply range of 0.9–1.1 V.

Fig. 8 Three calibration curves of the 24.6/307.2-kHz frequency reference measured in the **a** 24.6- and **b** 307.2-kHz operating modes, respectively



5 Phase noise study

Next, the procedure used to calculate the ISF-based phase noise spectrum of the CMOS oscillator is described in 10 steps. After that the procedure is applied to the proposed frequency references. Finally, the results are discussed and various phase noise estimation methods are compared.

5.1 Procedure of the ISF method

The ISF-based phase noise can be calculated by using the following algorithm:

1. Simulate a reference clock signal waveform $w_r(t)$ with a stable oscillation from the output of the frequency reference.
2. Similarly, simulate waveforms $w_i(t)$ in the presence of a charge injection by adding a current impulse source $i(t)$ in parallel of each device, one at a time, in different phases of one period T . Therefore, the total number of simulated waveforms with charge injections is $m \times n$, where m and n are the number of devices being considered and the number of injections per period, respectively. A current impulse must be so small that its amplitude affects the phase of the clock signal linearly.
3. Determine the time shifts $\Delta t_i(t)$, caused by the injected current impulses $i(t)$, as a function of time over one period by comparing the waveforms $w_i(t)$

with the reference waveform $w_r(t)$. Depending on the phase when an injection is fed, $\Delta t_i(t)$ can be either positive ($w_i(t)$ ahead) or negative ($w_r(t)$ ahead).

4. Convert the time shifts $\Delta t_i(t)$ to phase shifts by using the equivalence $\Gamma(x) = 2\pi(\Delta t_i(t)/T)$. This dimensionless, frequency- and amplitude-independent function $\Gamma(x)$, with a period of 2π , is called the impulse sensitivity function, or the ISF for short [10]. Note that each device has an individual $\Gamma(x)$.
5. Interpolate more points to the ISFs, if needed.
6. Scale the $\Gamma(x)$ curves by dividing each point by the amount of injected charge q that is the time integral of the injected current impulse $i(t)$. Let this scaled ISF be marked as $\Gamma_q(x)$.
7. Take the cyclostationary behavior of the noise sources into account. First, simulate the periodic current waveform of each device by using the same time interval as that during which the current impulses were injected. Then normalize the current waveforms with their maximum values and let the resulting dimensionless 2π -periodic function be marked as $\alpha(x)$ [10]. The cyclostationarity can now be combined with the ISF by defining the effective ISF as $\Gamma_{q,eff}(x) = \Gamma_q(x)\alpha(x)$. Note that the lengths of $\Gamma_q(x)$ and $\alpha(x)$ must be the same.
8. Calculate a root mean square and a dc value for the $\Gamma_{q,eff}(x)$ of each device. These parameters are marked as Γ_{rms} and Γ_{dc} and they are utilized to determine the white and flicker noise contributions, respectively, of each device to the phase noise.
9. Determine the current white noise spectral density $\overline{i_n^2}/\Delta f$ and the flicker noise corner $f_{1/f}$ for each device. The current white noise spectral density of long-channel CMOS transistors operating in the saturation region is given by

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\frac{2}{3}\mu C_{ox}\frac{W}{L}V_{OD}, \tag{5}$$
 where k is the Boltzmann's constant ($1.38 \cdot 10^{-23}$ J/K), T the absolute temperature, μ the mobility, C_{ox} the gate-oxide capacitance per unit area, W and L the channel width and length of the device, and V_{OD} the gate voltage overdrive [15]. The V_{OD} of a device is defined as the difference of a gate-to-source and a threshold voltage. The flicker noise corner of a device can be determined by using a small-signal noise simulation.
10. The total phase noise $L\{\Delta f\}$ caused by both the white and flicker noise contributions of all the m devices included in the analysis can now be calculated and plotted as a function of Δf in decibels (dBc/Hz) by using (6) [10, 16–18]. All the noise sources are assumed to be uncorrelated. The white and flicker

noise terms, $L_w\{\Delta f\}$ and $L_f\{\Delta f\}$, are pointed out in the equation. The Σ terms take all the devices into account.

$$L\{\Delta f\} = 10 \cdot \log \left[\underbrace{\frac{1}{8\pi^2(\Delta f)^2} \sum^m \left(\Gamma_{rms}^2 \frac{\overline{i_n^2}}{\Delta f} \right)}_{\text{White noise } L_w\{\Delta f\}} + \underbrace{\frac{1}{16\pi^3(\Delta f)^3} \sum^m \left(\Gamma_{dc}^2 \frac{\overline{i_n^2}}{\Delta f} f_{1/f} \right)}_{\text{Flicker noise } L_f\{\Delta f\}} \right] \tag{6}$$

5.2 Applying the ISF method

Next, the above procedure is examined as an illustrative example for the device M1 of the 2.0-MHz frequency reference shown in Fig. 2(a). A current source with a charge of 0.5 fC ($50 \text{ nA} \cdot 10 \text{ ns}$) is added in 11 different phases of a clock period in parallel of M1, and thus an equal number of waveforms $w_i(t)$ is obtained. The resulting time shifts are determined from the comparator output a few periods after the charge injections by comparing the $w_i(t)$ waveforms with the reference waveform $w_r(t)$. By converting the time shifts to phase shifts, an ISF function of M1 can be found. The interpolation is required to smooth out the ISF curve. For example, interpolation from 11 to 502 points with a fifth-order fitting is used here. The ISF of M1 is shown in Fig. 9(a). Next, the ISF is scaled by the injected charge of 0.5 fC, and the new ISF is shown in Fig. 9(b). In order to take the cyclostationarity into account, the proportionality coefficient $\alpha(x)$, shown in Fig. 9(c), is determined from the drain current waveform of M1. When the curves shown in Fig. 9(b) and (c) are multiplied by each other, the effective ISF shown in Fig. 9(d) is found. After that the parameters Γ_{rms} and Γ_{dc} can be calculated. For M1 these parameters are $2.48 \cdot 10^{13}$ and $1.82 \cdot 10^{10}$ rad/C, respectively.

The simulated rms value of V_{OD} was used in (5) to calculate the drain current white noise spectral density of $3.04 \cdot 10^{-25} \text{ A}^2/\text{Hz}$. The flicker noise corner of 3.0 MHz was simulated with a small-signal noise analysis. It was carried out by biasing M1 with its average gate-source voltage between the ground and supply. Now, all the parameters required to calculate the phase noise contribution of M1 are available. Figure 10 shows three spectra for M1, which are the white noise spectrum $L_w\{\Delta f\}$, the flicker noise spectrum $L_f\{\Delta f\}$, and the total phase noise spectrum $L\{\Delta f\}$. The white noise is clearly dominant down to very small offset frequencies ($L\{\Delta f\} \approx L_w\{\Delta f\}$).

Table 2 shows the phase noise parameters for all nine devices (M1–M9) of the multivibrator of the 2.0-MHz

Fig. 9 Simulated ISF-related curves of device M1: **a** a basic ISF function, **b** an ISF scaled with an injected charge, **c** a normalized drain current waveform, **d** an effective ISF

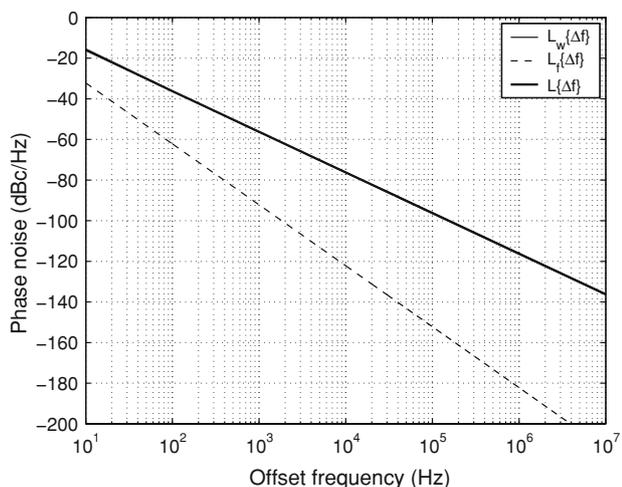
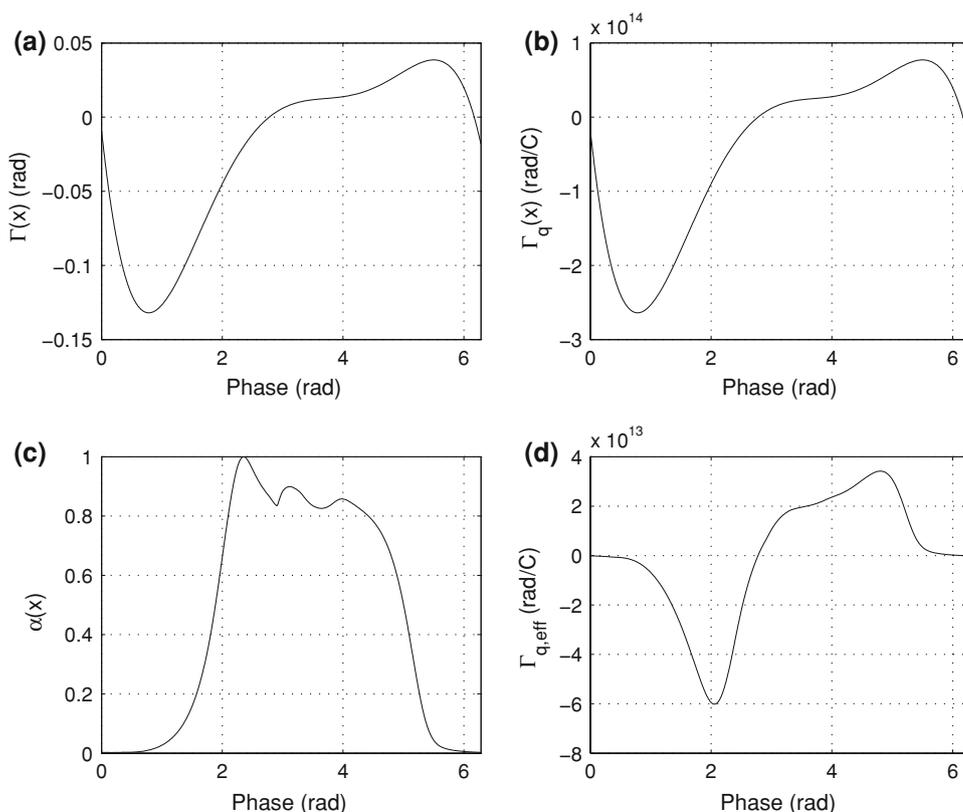


Fig. 10 Phase noise contribution of M1 simulated with the ISF method

frequency reference that were included in the analysis. The values were obtained by repeating the foregoing exemplary procedure of M1 for the other devices. The phase noise levels are reported in decibels at the offset frequency of $\Delta f = 1$ MHz. At that offset the white noise of the tail current source M9 dominates the total phase noise with a share of 31.7%, while the devices M1–M2 and M5–M6 contribute over 10% each. The same kind of phase noise study could be performed at any offset frequency. The different noise

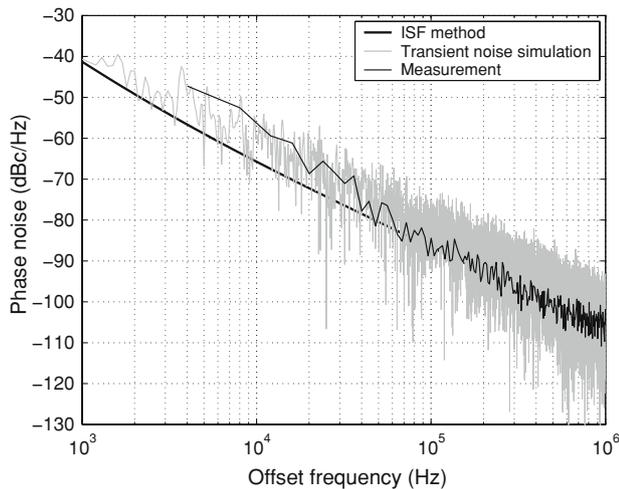
contributions of e.g. M1 and M2 could be caused by the asymmetry resulting from the differential-to-single-ended conversion occurring at the interface of the comparator.

The comparison of different methods used to obtain the total phase noise spectrum of the 2.0-MHz frequency reference is shown in Fig. 11. All three spectra agree well with each other, illustrating the good correspondence between the ISF theory, the transient noise simulation, and the measurement. The measured phase noise at 1 MHz offset frequency is -105 dBc/Hz. The ISF method gives a result that is 1.7 dB better, as shown in Table 2. The rms cycle-to-cycle jitter of 2.0 ns can be evaluated by using (2) for the measured phase noise. It is 150 times smaller than the maximum specified value of 0.3 μ s. The ISF method predicts a flicker noise corner of roughly 2.5 kHz.

Figure 12(a) and (b) show the phase noise spectra of the 24.6/307.2-kHz frequency reference obtained by using the ISF method and the measurement in the 24.6- and 307.2-kHz modes, respectively. In the 24.6-kHz mode, the spectra agree very well with each other. The measured phase noise at the 10-kHz offset frequency is of the order of -68 dBc/Hz, while the prediction of the ISF method is -68.4 dBc/Hz. According to the ISF method, the flicker noise corner is approximately 4 Hz. In the case of the 307.2-kHz mode, the measured phase noise is approximately 5 dB better than that predicted by the ISF method. At an offset frequency of 100 kHz the measured phase

Table 2 Phase noise overview of the 2.0-MHz frequency reference at $\Delta f = 1$ MHz

	Γ_{rms} (rad/C)	Γ_{dc} (rad/C)	$\overline{i_n^2}/\Delta f$ (A ² /Hz)	$f_{1/f}$ (Hz)	$L_w\{\Delta f\}$ (dBc/Hz)	$L_f\{\Delta f\}$ (dBc/Hz)	$L\{\Delta f\}$ (dBc/Hz)
M1	$2.48 \cdot 10^{13}$	$1.82 \cdot 10^{10}$	$3.04 \cdot 10^{-25}$	$3 \cdot 10^6$	-116.2	-182.2	-116.2 (11.0%)
M2	$3.41 \cdot 10^{13}$	$4.60 \cdot 10^{12}$	$2.69 \cdot 10^{-25}$	$3 \cdot 10^6$	-114.0	-134.6	-114.0 (18.7%)
M3	$8.14 \cdot 10^{12}$	$-1.73 \cdot 10^{12}$	$2.57 \cdot 10^{-25}$	$4 \cdot 10^6$	-126.7	-142.1	-126.5 (1.0%)
M4	$7.16 \cdot 10^{12}$	$-4.37 \cdot 10^{11}$	$3.04 \cdot 10^{-25}$	$4 \cdot 10^6$	-127.0	-153.3	-127.0 (0.9%)
M5	$1.40 \cdot 10^{14}$	$-8.46 \cdot 10^{13}$	$1.82 \cdot 10^{-26}$	$13 \cdot 10^3$	-113.4	-144.7	-113.4 (21.1%)
M6	$1.07 \cdot 10^{14}$	$-6.40 \cdot 10^{13}$	$1.82 \cdot 10^{-26}$	$13 \cdot 10^3$	-115.8	-147.1	-115.8 (12.4%)
M7	$5.33 \cdot 10^{13}$	$2.09 \cdot 10^{12}$	$1.36 \cdot 10^{-26}$	$13 \cdot 10^3$	-123.1	-178.1	-123.1 (2.3%)
M8	$3.25 \cdot 10^{13}$	$1.61 \cdot 10^{13}$	$1.37 \cdot 10^{-26}$	$13 \cdot 10^3$	-127.4	-160.3	-127.4 (0.9%)
M9	$1.15 \cdot 10^{14}$	$8.43 \cdot 10^{13}$	$4.08 \cdot 10^{-26}$	$11 \cdot 10^3$	-111.7	-141.9	-111.7 (31.7%)
Σ					-106.7	-132.8	-106.7

**Fig. 11** The phase noise spectra of the 2.0-MHz frequency reference obtained with the ISF method, the transient noise simulation, and the measurement

noise level is -77 dBc/Hz, while the ISF method results in -72.0 dBc/Hz. The reason for this poorer correspondence between the phase noise results obtained with the ISF method and the measurement is unknown to the authors. For this mode the ISF method predicts a flicker noise corner of 53 Hz. By using (2) for the measured phase noises, the rms cycle-to-cycle jitters of 1.03 μ s and 82 ns can be approximated for the 24.6- and 307.2-kHz operating modes, respectively. Thus, this frequency reference closely fulfills the requirements of 2.43 μ s and 97 ns, respectively.

The phase noise was studied in the 24.6-kHz mode more extensively by using the ISF method. Table 3 shows the phase noise results obtained at an offset frequency of 10 kHz, at which the white noise clearly dominates, with different supply voltages and temperatures. According to the table, the phase noise of the 24.6/307.2-kHz frequency reference is relatively insensitive to temperature changes, but it degrades remarkably when the supply voltage deviates from a nominal value of 1.0 V.

6 Discussion

An extensive comparative study of phase noise simulation and estimation methods, presented in [19] and applied to two ring oscillators and one LC oscillator, shows a good 5-dBc/Hz agreement between the methods studied: the ISF method, which is also considered in this paper, the commercial direct phase noise simulators SpectreRF and EldoRF, and measurements. In a similar way to the ISF method, these simulators consider a LTV system to obtain the noise power spectral density. To the best of authors' knowledge, the circuits under consideration in this paper are the first multivibrators for which the ISF-based phase noise results have been published [11–13], and they are further expanded in this paper. At first glance the procedure of the ISF method seems to be time-consuming, but it can be automated to a great extent, for example by using a combination of EldoRF and Matlab, after which it is quite fast and convenient to use. When the procedure is automated, the phase noise spectrum of the CMOS multivibrator circuit can be obtained roughly within 1 or 2 h.

The major advantage of the ISF method is that it provides the white, flicker, and total phase noise spectra for each device taken into account in the analysis. Hence, the dominant noise sources and their types (white or flicker noise) can easily be determined at certain offset frequencies. Though the types of noise sources can be modified in the direct phase noise simulators, three separate simulations must be performed to provide the three corresponding phase noise spectra produced by the ISF method. Transient noise simulation is not an effective method in the case of phase noise considerations, because in order to achieve a sufficient frequency resolution after the Fourier transform, a relatively long transient noise simulation is required. For the CMOS multivibrator circuit a single transient noise simulation may take over 10 h.

Fig. 12 The phase noise spectra of the 24.6/307.2-kHz frequency reference obtained with the ISF method and the measurement in **a** the 24.6- and **b** the 307.2-kHz operating modes, respectively

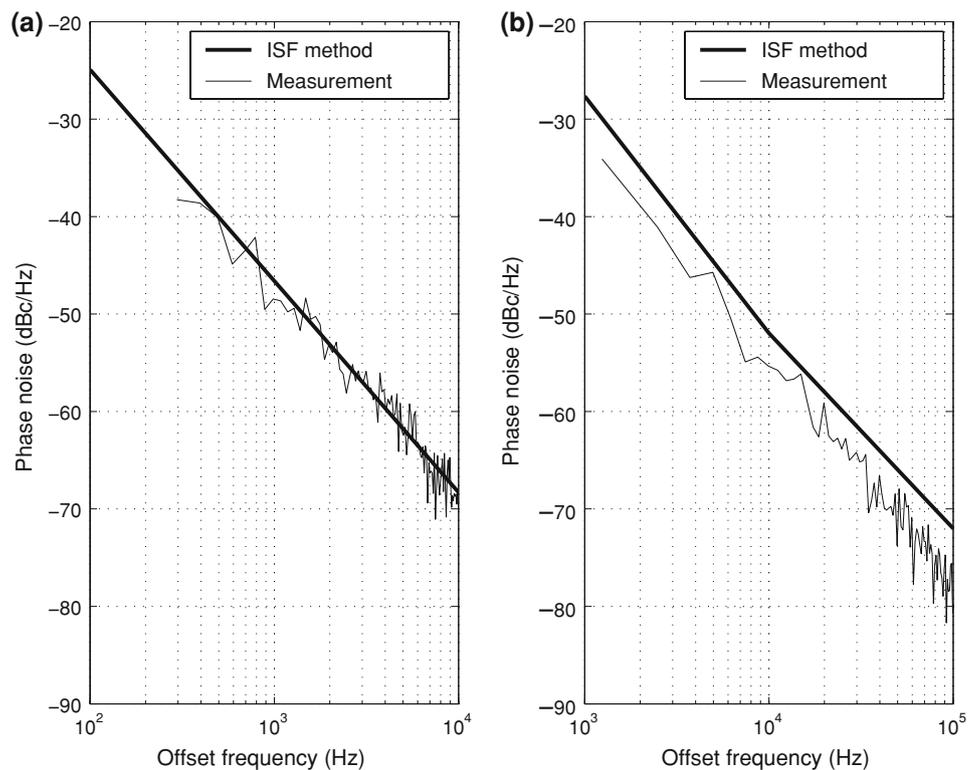


Table 3 The phase noise studied with the ISF method applied to the 24.6/307.2-kHz frequency reference in the 24.6-kHz mode at $\Delta f = 10$ kHz

V_{DD} (V)	T (°C)	$L_w\{\Delta f\}$ (dBc/Hz)	$L_f\{\Delta f\}$ (dBc/Hz)	$L\{\Delta f\}$ (dBc/Hz)
1.0	+85	-68.6	-106.4	-68.6
1.0	+25	-68.4	-103.9	-68.4
1.0	-40	-68.5	-108.4	-68.5
1.1	+25	-61.1	-75.6	-61.0
1.0	+25	-68.4	-103.9	-68.4
0.9	+25	-58.4	-71.5	-58.2

7 Conclusion

In this paper, two micropower, low-voltage frequency references implemented in a 0.13- and a 0.25- μm CMOS process were presented. The CMOS multivibrator-based references provide a 2.0-MHz and a 24.6/307.2-kHz clock signal. The latter operates from a 1.0-V supply and provides two active operating modes. The phase noise of both the frequency references presented was analyzed by using the described procedure for applying the ISF-based phase noise method to CMOS oscillators. The phase noise spectra obtained with the ISF method agreed very well with the measured ones, especially in the cases of the 2.0-MHz reference and the 24.6-kHz mode of the 24.6/307.2-kHz reference, where it was within a couple of decibels.

According to the presented measurement results, by using the chosen circuit techniques, competitive, low-voltage, low-power frequency references practicable for low-frequency applications, such as sensor interfaces, can be implemented.

Acknowledgements The authors wish to thank VTI Technologies, the Nokia Research Center, and the Finnish Funding Agency for Technology and Innovation (TEKES) for financial support.

References

- Gilbert, B. (1976). A versatile monolithic voltage-to-frequency converter. *IEEE Journal of Solid-State Circuits*, *SC-11*(6), 852–864.
- Abidi, A. A., & Meyer, R. G. (1983). Noise in relaxation oscillators. *IEEE Journal of Solid-State Circuits*, *SC-18*(6), 794–802.
- Filanovsky, I. M. (1988). Remarks on design of emitter-coupled multivibrators. *IEEE Transactions on Circuits and Systems*, *35*(6), 751–755.
- Buonomo, A., & Schiavo, A. L. (2006). Analysis of emitter (source)-coupled multivibrators. *IEEE Transactions on Circuits and Systems I*, *53*(6), 1193–1202.
- Finvers, I. G., & Filanovsky, I. M. (1988). Analysis of a source-coupled CMOS multivibrator. *IEEE Transactions on Circuits and Systems*, *35*(9), 1182–1185.
- Song, B., Kim, H., Choi, Y., & Kim, W. (1999). A 50% power reduction scheme for CMOS relaxation oscillator. In *Proceedings of the IEEE Asia Pacific conference on ASICs* (pp. 154–157).
- Filanovsky, I. M., & Verhoeven, C. J. M. (2007). Sinusoidal and relaxation oscillations in source-coupled multivibrators. *IEEE Transactions on Circuits and Systems II*, *54*(11), 1009–1013.

8. Paavola, M., Kämäräinen, M., Järvinen, J., Saukoski, M., Laiho, M., & Halonen, K. (2007). A micropower interface ASIC for a capacitive 3-axis micro-accelerometer. *IEEE Journal of Solid-State Circuits*, 42(12), 2651–2665.
9. Paavola, M., Kämäräinen, M., Laulainen, E., Saukoski, M., Koskinen, L., Kosunen, M., & Halonen, K. (2008). A 21.2 μA $\Delta\Sigma$ -based interface ASIC for a capacitive 3-axis micro-accelerometer. In *Proceedings of the IEEE Asian solid-state circuits conference* (pp. 101–104).
10. Hajimiri, A., & Lee, T. H. (1998). A general theory of phase noise in electrical oscillators. *IEEE Journal of Solid-State Circuits*, 33(2), 179–194.
11. Paavola, M., Laiho, M., Saukoski, M., & Halonen, K. (2006). A 3 μW , 2 MHz CMOS frequency reference for capacitive sensor applications. In *Proceedings of the IEEE international symposium on circuits and systems* (pp. 4391–4394).
12. Paavola, M., Laiho, M., Saukoski, M., & Halonen, K. (2005). A micropower 2 MHz CMOS frequency reference for capacitive sensor applications. In *Proceedings of the IEEE European conference on circuit theory and design* (pp. 425–428).
13. Paavola, M., Saukoski, M., Laiho, M., & Halonen, K. (2007). A nanopower double-mode 1-V frequency reference for an ultra-low-power capacitive sensor interface. In *Proceedings of the IEEE European conference on circuit theory and design* (pp. 104–107).
14. Shinagawa, M., Akazawa, Y., & Wakimoto, T. (1990). Jitter analysis of high-speed sampling systems. *IEEE Journal of Solid-State Circuits*, 25(1), 220–224.
15. Hajimiri, A., Limotyrakis, S., & Lee, T. H. (1999). Jitter and phase noise in ring oscillators. *IEEE Journal of Solid-State Circuits*, 34(6), 790–804.
16. Hajimiri, A., & Lee, T. H. (1998). Corrections to “A general theory of phase noise in electrical oscillators”. *IEEE Journal of Solid-State Circuits*, 33(6), 928.
17. Jannesari, A., & Kamarei, M. (2007). Comments on “A general theory of phase noise in electrical oscillators”. *IEEE Journal of Solid-State Circuits*, 42(10), 2314.
18. Lu, L., Tang, Z., Andreani, P., Mazzanti, A., & Hajimiri, A. (2008). Comments on “A general theory of phase noise in electrical oscillators”. *IEEE Journal of Solid-State Circuits*, 43(9), 2170.
19. Ou, Y., Barton, N., Fetche, R., Seshan, N., Fiez, T., Moon, U-K., & Mayaram, K. (2002). Phase noise simulation and estimation methods: A comparative study. *IEEE Transactions on Circuits and Systems II*, 49(9), 635–638.



M. Paavola was born in Kaustinen, Finland, in 1980. He received the M.Sc. and Lic.Sc. degrees in Electrical Engineering from the Helsinki University of Technology (TKK), Espoo, Finland, in 2005 and 2007, respectively. He is currently pursuing the Ph.D. degree in Electrical Engineering at the Electronic Circuit Design Laboratory, TKK. His research interest is low-voltage, low-power analog circuit design

relating to sensor interfaces, especially to reference circuits and power management.



M. Laiho was born in Parkano, Finland, in 1973. He received the M.Sc., Lic.Sc., and Ph.D. degrees in Electrical Engineering from the Helsinki University of Technology (TKK), Espoo, Finland, in 1999, 2001, and 2003, respectively. He is a postgraduate researcher with the Microelectronics Laboratory, University of Turku, Turku, Finland, and Electronic Circuit Design Laboratory, TKK. His research interests are neuro-morphic vision chips, array

processor realizations and mixed-mode integrated circuits for sensor interfaces.



M. Saukoski was born in Savukoski, Finland in 1978. He received the M.Sc. and D.Sc. degrees in Electrical Engineering from the Helsinki University of Technology (TKK), Espoo, Finland in 2004 and 2008, respectively. During the years 2003–2007 he worked first as a research assistant and then as a research engineer at the Electronic Circuit Design Laboratory, TKK. Starting from the year 2008, he has been with ELMOS Semiconductor AG,

Dortmund, Germany, where he works as a System Design Engineer at ELMOS Microsystems. His main research interests are microelectromechanical sensors and actuators, and low-voltage, low-power, high-accuracy analog circuit design.



M. Kämäräinen was born in Helsinki, Finland, in 1975. He received the M.Sc. and Lic.Sc. degrees in Electrical Engineering from the Helsinki University of Technology (TKK), Espoo, Finland, in 2006 and 2007, respectively. He is currently pursuing the Ph.D. degree in Electrical Engineering at the Electronic Circuit Design Laboratory, TKK. His research interest is low-voltage, low-power analog circuit design relating to sensor front-ends.



K. A. I. Halonen received the M.Sc. degree in Electrical Engineering from the Helsinki University of Technology, Finland, in 1982, and the Ph.D. degree in Electrical Engineering from the Katholieke Universiteit Leuven, Belgium, in 1987. Since 1988 he has been with the Electronic Circuit Design Laboratory, Helsinki University of Technology. From 1993 he has been an Associate Professor, and since 1997 a Full Professor

at the Faculty of Electrical Engineering and Telecommunications. He became the Head of Electronic Circuit Design Laboratory in 1998. He specializes in CMOS and BiCMOS analog integrated circuits, particularly for telecommunication applications. He is the author or co-author of over 200 international and national conference and journal publications on analog integrated circuits. He has been an associate editor of IEEE Transactions on Circuits and Systems I, a guest editor for IEEE Journal of Solid-State Circuits and the Technical Program Committee Chairman for European Solid-State Circuits Conference year 2000. He has been awarded the Beatrice Winner Award in ISSCC'02 Conference in 2002. He is a TPC member of ESSCIRC and ISSCC.