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INTEGRATED REFERENCE CIRCUITS FOR LOW-POWER CAPACITIVE SENSOR INTERFACES

Doctoral Dissertation

Matti Paavola

Aalto University
School of Science and Technology
Faculty of Electronics, Communications and Automation
Department of Micro and Nanosciences

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Abstract

This thesis consists of nine publications and an overview of the research topic, which also summarizes the work. The research described in this thesis concentrates on the design of low-power sensor interfaces for capacitive 3-axis micro-accelerometers. The primary goal throughout the thesis is to optimize power dissipation. Because the author made the main contribution to the design of the reference and power management circuits required, the overview part is dominated by the following research topics: current, voltage, and temperature references, frequency references, and voltage regulators.

After an introduction to capacitive micro-accelerometers, the work describes the typical integrated readout electronics of a capacitive sensor on the functional level. The readout electronics can be divided into four different functional parts, namely the sensor readout itself, signal post-processing, references, and power management. Before the focus is shifted to the references and further to power management, different ways to realize the sensor readout are briefly discussed.

Both current and voltage references are required in most analog and mixed-signal systems. A bandgap voltage reference, which inherently uses at least one current reference, is practical for the generation of an accurate reference voltage. Very similar circuit techniques can be exploited when implementing a temperature reference, the need for which in the sensor readout may be justified by the temperature compensation, for example.

The work introduces non-linear frequency references, namely ring and relaxation oscillators, which are very suitable for the generation of the relatively low-frequency clock signals typically needed in the sensor interfaces. Such oscillators suffer from poor jitter and phase noise performance, the quantities of which also deserve discussion in this thesis.

Finally, the regulation of the supply voltage using linear regulators is considered. In addition to extending the battery life by providing a low quiescent current, the regulator must be able to supply very low load currents and operate without off-chip capacitors.

Keywords capacitive accelerometer, CMOS, power management circuit, reference circuit, sensor interface

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Integroidut referenssipiirit matalan tehonkulutuksen kapasitiivisille anturirajapinnoille

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Työn ohjaaja	

Tiivistelmä

Tämä väitöskirja koostuu yhdeksästä julkaisusta sekä tutkimusaiheen yhteenvedosta. Väitöskirjassa esitetty tutkimus keskittyy matalan tehonkulutuksen anturirajapintojen suunnitteluun kapasitiivisille kolmiakselisille mikromekaanisille kiihtyvyysantureille. Tutkimuksen keskeinen tavoite on tehonkulutuksen optimointi. Koska kirjoittajan pääasiallinen panos keskittyi tarvittavien referenssi- ja tehonhallintapiirien suunnitteluun, yhteenveto-osuutta hallitsee seuraavat tutkimusaiheet: virta-, jännite- ja lämpötilareferenssit, taajuusreferenssit, sekä jänniteregulaattorit.

Kapasitiivisten mikromekaanisten kiihtyvyysanturien johdannon jälkeen työ esittää tyypillisen integroidun kapasitiivisen anturin lukuelektroniikan toiminnallisella tasolla. Anturin lukuelektroniikka voidaan jakaa neljään toiminnalliseen osaan, jotka ovat itse anturin lukeminen, signaalin jälkikäsittely, referenssit, ja tehon hallinta. Ennen referenssi- ja tehonhallintapiireihin siirtymistä käsitellään lyhyesti erilaisia anturin luvun toteutustapoja.

Sekä virta- että jännitereferenssejä tarvitaan useimmissa analogia- ja analogia-digitaalijärjestelmissä. Bandgap-jännitereferenssi, joka itsessään sisältää ainakin yhden virtareferenssin, on käytännöllinen tarkan referenssijännitteen tuottamisessa. Hyvin samanlaisia piiritekniikoita voidaan hyödyntää toteutettaessa lämpötilareferenssi, jonka tarve anturin lukuelektroniikassa voi liittyä esimerkiksi lämpötilakompensointiin.

Työ esittelee epälineaarisia taajuusreferenssejä, eli rengas- ja relaksaatio-oskillaattoreita, jotka sopivat hyvin suhteellisen matalataajuisten kellosignaalien muodostamiseen, joita anturin lukuelektroniikassa tyypillisesti tarvitaan. Kyseiset oskillaattorit kärsivät heikosta jitteri- ja vaihekohinasuorituskyvystä. Näitä suorituskyky-parametreja tullaan myös käsittelemään tässä väitöskirjassa.

Lopuksi tarkastellaan käyttöjännitesäätelyä lineaaristen regulaattorien avulla. Sen lisäksi, että patterin kestoa pidennetään pienellä lepotilan virralla, regulaattorin täytyy pystyä syöttämään hyvin pieniä kuormavirtoja sekä toimimaan ilman ulkoisia kondensaattoreita.

Asiasanat anturirajapinta, CMOS, kapasitiivinen kiihtyvyysanturi, referenssipiiri, tehonhallintapiiri

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Preface

The research work of this thesis was carried out in the Electronic Circuit Design Laboratory, Aalto University School of Science and Technology (formerly Helsinki University of Technology), Espoo, Finland, during the years 2004-2010. The research was divided into two projects, namely "Capacitive Sensor Interface" (CAPACIF) and "Miniaturized Capacitive Sensor Interface" (MINICIF) projects, in both of which a low-power sensor interface for reading a capacitive 3-axis micro-accelerometer was studied. The first one, in the years 2004-2006, was funded by the Nokia Research Center, VTI Technologies, and the Finnish Funding Agency for Technology and Innovation (TEKES), while the second one, in the years 2006-2008, was funded by VTI Technologies and TEKES. During the years 2006-2010 I had the privilege of participating in the doctoral program of the Graduate School in Electronics, Telecommunications and Automation (GETA), which partially funded the research. The Centre of Excellence program (SMARAD2) funded partially the research work during the years 2008-2010. The work was also supported by the Finnish Foundation for Technology Promotion (TES), the Emil Aaltonen Foundation, the Ulla Tuominen Foundation, and the Walter Ahlström Foundation. I gratefully acknowledge all those who provided financial support.

In addition to providing funding, VTI Technologies and the Nokia Research Center are acknowledged for giving their permission to publish the original articles of this thesis. VTI Technologies is further acknowledged for providing the sensor elements and for the assistance and equipment necessary for the rate table measurements. I want to thank my colleagues at VTI Technologies and the Nokia Research Center with whom I co-operated with. Particularly, Mr. Teemu Elo, Dr. Teemu Salo, Mr. Tero Sillanpää, and Mr. Kimmo Törmälehto are acknowledged for many valuable discussions and comments.

I would like to thank my supervisor, Professor Kari Halonen, for giving me the opportunity to work in the laboratory during these years. Professor Halonen provided me with an interesting research topic and a research team with irreplaceable colleagues. I also wish to warmly thank Professor Philip K. T. Mok and Dr. Teemu Salo for reviewing this thesis and for their comments and suggestions.

The staff of the Electronic Circuit Design Laboratory, together with the colleagues who left the laboratory before me, deserve my gratitude for creating a pleasant and encouraging workplace. I warmly thank all the project members I had the pleasure of working with (in alphabetical order): Dr. Jere Järvinen, Dr. Lauri Koskinen, Dr. Marko Kosunen, Mika Kämäräinen, Dr. Mika Laiho, Erkka Laulainen, and Dr. Mikko Saukoski. In particular, I want to thank my great colleague Mika Kämäräinen for our seamless and memorable teamwork, my very talented project manager, Dr. Mikko Saukoski, for his valuable motivation, contribution, and nu-

merous paper reviews, and the instructor of my Master's and Licentiate's thesis, Dr. Mika Laiho, for his important contribution. I would also like to express my special gratitude to Lasse Aaltonen for his significant assistance since I settled at the same laboratory in 2004. I would also like to thank Lasse Aaltonen, Dr. Jere Järvinen, Mika Kämäräinen, Dr. Mika Laiho, and Dr. Mikko Saukoski for all the great free-time activities we have had together. I thank the office colleagues not mentioned above, Antti Kalanti, Pasi Rahikkala, and Timo Speeti, for our countless discussions and for creating a good working atmosphere. Moreover, Antti Kalanti and Mika Kämäräinen deserve special thanks, among others, for all the tight but relaxing badminton games we have played during the current and the last year. I would like to express my gratitude to the secretaries of the laboratory, Anja Meuronen, Lea Söderman, and Helena Yllö, for their kind help with all the practical matters.

My parents, Hilkka and Eero(† 26th May 2009), and my brothers, Jani and Jukka, deserve my warmest gratitude for all the support and love they have given me throughout my life. I also dearly want to thank my parents-in-law, Arja and Juhani Luohio, for their kind support and all the great times we have spent together. I want to thank each and every dear friend not mentioned by name for all the relaxing times we have experienced together.

Finally, and foremost, I want to thank my beloved wife, Laura. You have brought so much love and happiness into my life, and your loving support helps me to get over all my worries.

Espoo, August 2010

Matti Paavola

Contents

List of Publications

This thesis consists of an overview and of the following publications.

[**P1**] M. Paavola, M. Laiho, M. Saukoski, and K. Halonen, "A 3 μW, 2 MHz CMOS frequency reference for capacitive sensor applications," in *Proc. IEEE International Symposium on Circuits and Systems*, Kos, Greece, May 2006, pp. 4391–4394.

[**P2**] M. Paavola, M. Saukoski, M. Laiho, and K. Halonen, "A micropower voltage, current, and temperature reference for a low-power capacitive sensor interface," in *Proc. IEEE International Symposium on Circuits and Systems*, New Orleans, LA, USA, May 2007, pp. 3067–3070.

[**P3**] M. Paavola, M. Kämäräinen, J. Järvinen, M. Saukoski, M. Laiho, and K. Halonen, "A 62μA interface ASIC for a capacitive 3-axis micro-accelerometer," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, USA, Feb. 2007, pp. 318–319.

[**P4**] M. Paavola, M. Kämäräinen, J. A. M. Järvinen, M. Saukoski, M. Laiho, and K. A. I. Halonen, "A micropower interface ASIC for a capacitive 3-axis micro-accelerometer," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, Dec. 2007, pp. 2651–2665.

[**P5**] M. Kämäräinen, M. Paavola, M. Saukoski, E. Laulainen, L. Koskinen, M. Kosunen, and K. Halonen, "A 1.5μW 1V 2$^{\text{nd}}$-order $\Delta\Sigma$ sensor front-end with signal boosting and offset compensation for a capacitive 3-axis micro-accelerometer," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, USA, Feb. 2008, pp. 578–579.

[**P6**] M. Paavola, M. Kämäräinen, M. Saukoski, and K. Halonen, "A micropower low-dropout regulator with a programmable on-chip load capacitor for a low-power capacitive sensor interface," in *Proc. IEEE International Conference on Electronics, Circuits, and Systems*, St. Julian's, Malta, Aug. 2008, pp. 450–453.

[**P7**] M. Paavola, M. Kämäräinen, E. Laulainen, M. Saukoski, L. Koskinen, M. Kosunen, and K. Halonen, "A 21.2 μA $\Delta\Sigma$-based interface ASIC for a capacitive 3-axis micro-accelerometer," in *Proc. IEEE Asian Solid-State Circuits Conference*, Fukuoka, Japan, Nov. 2008, pp. 101–104.

[**P8**] M. Paavola, M. Kämäräinen, E. Laulainen, M. Saukoski, L. Koskinen, M. Kosunen, and K. A. I. Halonen, "A micropower $\Delta\Sigma$-based interface ASIC for a capacitive 3-axis micro-accelerometer," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 11, Nov. 2009, pp. 3193–3210.

[**P9**] M. Paavola, M. Laiho, M. Saukoski, M. Kämäräinen, and K. A. I. Halonen, "Impulse sensitivity function-based phase noise study for low-power source-coupled CMOS multivibrators," *International Journal on Analog Integrated Circuits and Signal Processing*, vol. 62, no. 1, Jan. 2010, pp. 29–41.

Author's Contribution

Prof. K. Halonen was the supervisor during the two projects relating to the research work of this thesis. Dr. M. Saukoski carried the responsibility for the project management during the first project (2004-2006) and also partly (until the end of year 2007) during the second one (2006-2008). The author had the responsibility for the completion of the second project. Dr. M. Laiho was the instructor of the author, mainly during the first project, and L. Aaltonen contributed during both projects through many valuable discussions and with much valuable advice. The first project resulted in the publications [P1]-[P4], whereas the publications [P5]-[P8] were written on the basis of the results of the second project. The last article [P9] covers the results from the frequency reference circuits of both projects. As a general guideline, the first author of each publication had the main responsibility for the manuscript but it was written in co-operation with all the authors.

[P1] A 3 μW, 2 MHz CMOS frequency reference for capacitive sensor applications
The author was responsible for the circuit design, implementation, and measurements of the proposed low-power frequency reference circuit. Dr. M. Laiho instructed the author and Dr. M. Saukoski contributed with much valuable advice.

[P2] A micropower voltage, current, and temperature reference for a low-power capacitive sensor interface
The author was responsible for the circuit design, implementation, and measurements of the proposed low-power voltage, current, and temperature reference circuit. The research was performed by the author under the guidance of Dr. M. Laiho and Dr. M. Saukoski.

[P3] A 62μA interface ASIC for a capacitive 3-axis micro-accelerometer
From the system-level point of view, the responsibility areas were divided in such a way that the author was responsible for the circuit design, implementation, and measurements of the clock generator and the voltage, current, and temperature reference circuit. In addition to the circuits considered in [P1] and [P2], a frequency reference for a micro-controller unit had to be provided. M. Kämäräinen was responsible for the circuit design, implementation, and measurements of the sensor front-end circuit and Dr. J. Järvinen for those of the two algorithmic analog-to-digital converters (ADCs). In addition to the system-level design, Dr. M. Saukoski performed the design of the dynamically-biased operational amplifiers. Mr. P. Rahikkala, Mr. T. Rapinoja, and Mr. O. Viitala assisted in drawing the layout. System measurements were carried out mainly by M. Kämäräinen and the author.

[P4] A micropower interface ASIC for a capacitive 3-axis micro-accelerometer
This publication is an extension of [P3] and thus the responsibilities here were the

same. Additionally, Ms. S. Heikkinen assisted in the ADC measurements.

[P5] A 1.5μW 1V 2$^{\text{nd}}$-order $\Delta\Sigma$ sensor front-end with signal boosting and offset compensation for a capacitive 3-axis micro-accelerometer

The main responsibility for the circuit design, implementation, and measurements of the proposed low-power $\Delta\Sigma$-type sensor front-end was carried out by M. Kämäräinen. The author was responsible for the layout drawing and Dr. M. Saukoski designed the required charge pumps, special switches, and clock generator of the front-end. Meanwhile, in close collaboration, the first prototype of the decimator was designed, implemented, and measured by E. Laulainen under the guidance of Dr. L. Koskinen and Dr. M. Kosunen.

[P6] A micropower low-dropout regulator with a programmable on-chip load capacitor for a low-power capacitive sensor interface

The author was responsible for the circuit design, implementation, and measurements of the proposed low-power low-dropout regulator. M. Kämäräinen contributed to the design through the necessary co-design with the $\Delta\Sigma$ sensor front-end and Dr. M. Saukoski contributed with much valuable advice.

[P7] A 21.2 μA $\Delta\Sigma$-based interface ASIC for a capacitive 3-axis micro-accelerometer

The responsibilities for the building blocks of the sensor interface were divided in such a way that the author had the responsibility for the circuit design, implementation, and measurements of the frequency reference, the voltage and current reference, the reference voltage buffers, and the low-dropout regulators considered in [P6]. The responsibilities relating to the sensor front-end design, implementation, and measurements have already been explained in the context of [P5]. E. Laulainen was responsible for the circuit design, implementation, and measurements of the second prototype of the decimator and he was instructed by Dr. L. Koskinen and Dr. M. Kosunen. The system measurements were carried out by M. Kämäräinen and the author.

[P8] A micropower $\Delta\Sigma$-based interface ASIC for a capacitive 3-axis micro-accelerometer

This publication is an extension of [P7] and thus the responsibilities here were the same. Furthermore, Mr. M. Pulkkinen assisted in automating the rate table measurements.

[P9] Impulse sensitivity function-based phase noise study for low-power source-coupled CMOS multivibrators

The author was responsible for the circuit design, implementation, and measurements of the two low-power frequency references, one of which is considered in [P1]. The instruction of Dr. M. Laiho was significant and Dr. M. Saukoski contributed with much valuable advice. M. Kämäräinen contributed to these designs through the necessary co-design with the sensor front-ends.

Symbols and Abbreviations

$(\overline{a_n^2}/\Delta f)^{1/2}$	Equivalent acceleration spectral density
$\alpha(\omega_0 t)$	Noise modulating function
α	Common-base current gain, $\alpha = I_C/I_E$; gain factor; proportionality coefficient
$\beta(s)$	Transfer function of a feedback network
β	Common-emitter current gain, $\beta = I_C/I_B$
β_F	Feedback factor, $\beta_F = R_{F2}/(R_{F1} + R_{F2})$
$\ddot{x}$	Double time derivative of x, $\ddot{x} = d^2x/dt^2 = a$
$\Delta\omega$	Offset frequency
$\Delta\omega_{1/f^3}$	$1/f^3$ noise corner
$\Delta\phi$	Phase shift
$\Delta\Sigma$	Delta-Sigma
δ	Parameter indicating a fractional part of an integer value
ΔC	Capacitance difference, $\Delta C = C_P - C_N$
Δf	Offset frequency
ΔI_L	Load current variation
Δq	Charge injection
ΔT	Measurement time; temperature range
Δt_1, Δt_2	Response and settling time of a regulator for a sudden increase in the load current
Δt_3, Δt_4	Response and settling time of a regulator for a sudden decrease in the load current
ΔV	Variable actuation voltage; voltage variation
ΔV_{BE}	Base-emitter voltage difference, $\Delta V_{BE} = V_{BE1} - V_{BE2}$
ΔV_C	Voltage change across the output capacitors
ΔV_{ESR}	Voltage change across the equivalent series resistance R_{ESR}

$\Delta V_{G,err}$	Output voltage variation resulting from variations in the closed-loop gain error, $\Delta V_{G,err} = V_{REF} G_{err}$
$\Delta V^*_{G,err}$	Output voltage variation resulting from random errors in the closed-loop gain error
ΔV_{GS}	Gate-source voltage difference, $\Delta V_{GS} = V_{GS1} - V_{GS2}$
ΔV_{LDR}	Output voltage variation resulting from variations in the load current
ΔV_{LNR}	Output voltage variation resulting from variations in the supply voltage
ΔV_{OS}	Variation in the offset voltage
ΔV^*_{OS}	Variation in the offset voltage resulting from random errors
ΔV^*_{random}	Output voltage variation resulting from a random error source
$\Delta V^*_{REF,OS}$	Voltage variation resulting from random errors in the reference voltage and offset voltage
ΔV_{REF}	Variation in the reference voltage
ΔV^*_{REF}	Variation in the reference voltage resulting from random errors
$\Delta V_{systematic}$	Output voltage variation resulting from a systematic error source
ΔV_{TC}	Output voltage variation resulting from variations in the temperature
$\Delta V_{TR,+}$	Output voltage variation resulting from a sudden increase in the load current
$\Delta V_{TR,-}$	Output voltage variation resulting from a sudden decrease in the load current
$\Delta V_{TR,max}$	Maximum output voltage variation resulting from a sudden increase or decrease in the load current
$\dot{x}$	Time derivative of x, $\dot{x} = dx/dt = v$
ϵ_0	Permittivity of the vacuum, $8.85419 \cdot 10^{-12}$ F/m
ϵ_r	Relative permittivity
η	Process-dependent constant; power efficiency, $\eta = P_{OUT}/P_{IN}$
η_I	Current efficiency, $\eta_I = I_{OUT}/I_{IN}$

$\Gamma(\omega_0 t)$	Impulse sensitivity function, i.e., a dimensionless, frequency- and amplitude-independent, 2π-periodic function that describes the phase shift in the oscillation waveform as a result of a charge injection Δq into a certain oscillator node at a phase angle $\omega_0 t$ during the oscillation period.
$\gamma_{1/f}$	Close-in corner frequency for the flicker noise
Γ_{dc}	Dc value of the impulse sensitivity function $\Gamma(\omega_0 t)$
γ_n, γ_p	Coefficients equal to 2/3 for long-channel NMOS and PMOS transistors in the saturation
Γ_{rms}	Rms value of the impulse sensitivity function $\Gamma(\omega_0 t)$
γ_w	Close-in corner frequency for the white noise
κ	White noise proportionality constant determined by the circuit parameters
λ	Slope of the tangent related to the temperature characteristic of the base-emitter voltage; channel-length modulation parameter of the MOS transistor
$\mathcal{L}(f)$	Single-sideband phase noise power spectral density
μ	Digital output in the temperature reference before scaling
μ_n	Electron mobility
μ_p	Hole mobility
ω	Angular frequency, $\omega = 2\pi f$
ω_0	Oscillation frequency
$\omega_{1/f}$	1/f noise corner frequency
ω_r	Resonance frequency, $\omega_r = \sqrt{k/m}$
$\overline{B}$	Bit average
$\overline{T}$	Mean value of period T
$\overline{i^2_{n,1/f}}/\Delta f$	Power spectral density of an input flicker noise current
$\overline{i^2_n}/\Delta f$	Power spectral density of an input white noise current
ϕ_1, ϕ_2	Two non-overlapping clock phases
$\phi_{\Delta V_{BE}}$	Clock phase corresponding the integration of the ΔV_{BE}-dependent current

ϕ_{dc}	Dc value of the excess phase $\phi(t)$ for a periodic oscillation waveform
ϕ_{eval}	Clock phase used to trigger a flip-flop
ϕ_{rms}	Rms value of the excess phase $\phi(t)$ for a periodic oscillation waveform
$\phi_{V_{BE}}$	Clock phase corresponding the integration of the V_{BE}-dependent current
$\phi(t)$	Time-varying signal phase; output excess phase
$\sigma_{abs,1/f}$	Absolute jitter resulting from the flicker noise
$\sigma_{abs,w}$	Absolute jitter resulting from the white noise
σ_{abs}	Absolute or long-term jitter
σ_{cc}	Cycle-to-cycle jitter
σ_c	Cycle jitter
σ_T	Period jitter, standard deviation of period T
τ	Time constant, $\tau = RC$
ζ	Flicker noise proportionality constant determined by the circuit parameters
$A(s)$	Transfer function of an amplifier
$A(t)$	Time-varying signal amplitude
A	Plate electrode area; current gain of a mirror
a	Acceleration
A_0, A_1	Offset term and scaling factor in the linear temperature scaling
A_{CL}	Closed-loop gain
A_{DD}	Supply-output gain
A_{EA}	Gain of the error amplifier
A_E	Base-emitter junction area
$A_{IN,REF}$	Supply gain of the voltage reference
$A_{IN,REG}$	Supply gain of the regulator

A_{IN}	Supply gain, $A_{IN} = \Delta V_{out}/\Delta V_{in}$, defined for the whole frequency spectrum
A_{OL}	Open-loop gain
A_V	Input-output gain
B	Output bit
b_i	i^{th} bit value
B_{out}	Digital output
bs	Bitstream
BW_{CL}	Closed-loop bandwidth
$c(f)$	Frequency-dependent scalar constant that describes oscillator's phase noise
$c(T)$	Curvature of the base-emitter voltage resulting from variations in the temperature
C	Capacitance; unit capacitance; timing capacitance; temperature-independent constant
c	Scalar constant that describes oscillator's phase noise
C_0	Sense capacitance; static part of the detection capacitances
C_B	Bypass capacitance
C_B'	Total bypass capacitance, $C_B' = C_B + C_L$
$c_{cm}(f)$	Frequency-dependent scalar constant that describes the phase noise contribution from the m^{th} colored noise sources
C_{DB}	Drain-bulk capacitance
C_D	Total capacitance at the output of an inverting gain stage
C_F	Feedback capacitance; capacitance in the RC low-pass filter
C_{GD}	Gate-drain capacitance
C_{int}	Integration capacitance
C_L	Load capacitance
C_M	Miller compensation capacitance
C_{node}	Capacitance in a certain node

C_N	Negative side detection capacitance
c_n	Fourier coefficient, $n \geq 0$
C_{OS}	Offset storage capacitance
C_{ox}	Gate-oxide capacitance per unit area
C_O	Output capacitance
C_{par}	Parasitic capacitance
C_P	Positive side detection capacitance
C_S	Sampling capacitance
C_{tot}	Total capacitance
c_w	Scalar constant that describes the phase noise contribution from the white noise sources
D	Damping coefficient
E	Energy stored in the capacitor
E_{tot}	Total energy stored in the system
F	Device excess phase number
f	Frequency
f_{-3dB}	Frequency at which the response is 3 dB below its peak value
f_{0dB}	Unity-gain frequency
f_0	Oscillation frequency
$f_{1/f}$	1/f noise corner frequency
f_{180°	Frequency at which the phase margin of the loop gain reduces to zero
f_B	Input bandwidth
f_c	Carrier frequency; $1/f^3$ corner frequency
$F_{es,eff}$	Effective electrostatic force
F_{es}	Electrostatic force, $F_{es} = -\partial E_{tot}/\partial x$
F_E	External force
F_{fb}	Feedback force

f_N	Nyquist frequency
f_r	Resonance frequency
f_S	Sampling frequency
G_A	Transconductance of the amplifier
G_{err}	Closed-loop gain error
g_{md}	Transconductance of the gain stage in the damping-factor-control circuitry
g_{mf}	Transconductance of the feedforward transconductance stage
g_{mL}	Transconductance of the output stage
g_m	Transconductance
G_P	Transconductance of the pass device
GBW	Gain-bandwidth product
$H(s)$	Transfer function
$H_C(s)$, $H_C(z)$	Transfer function of a CT and a DT compensator
$H_F(s)$, $H_F(z)$	Transfer function of a CT and a DT low-pass filter
$h_\phi(t, \tau)$	Impulse response for the excess phase $\phi(t)$
I	Current; biasing current; unit current; average charging/discharging current
i	Number of cycle
I_A	Current consumed by the error amplifier
I_B	Base current; biasing current
I_{CTAT}	Complementary-to-absolute temperature current
I_C	Collector current
I_D	Drain current
I_E	Emitter current
I_F	Current consumed by the resistive feedback network; pull-down current, $I_F = V_{REF}/R_{F1}$
I_L	Load current

I_{NL}	Non-linear current
I_N	Average discharging current
I_n	Amplitude of the injected sinusoidal noise current
$i_n(t)$	Noise current
I_{PTAT^2}	Proportional-to-square-of-absolute temperature current
I_{PTAT}	Proportional-to-absolute temperature current
I_P	Average charging current; current flowing through the pass device
I_Q	Quiescent current
I_{REF}	Reference current
I_R	Current that flows through the replica biasing branch; current consumed by the voltage reference
I_{sink}	Constant-current sink
I_{SR}	Slew-rate limited current
$I_{start\text{-}up}$	Start-up current
I_S	Saturation current of a bipolar transistor; current sensed from the current flowing through the pass device
I_{TD}	Temperature-dependent current
I_{TI}	Temperature-independent current
I_{trim}	Programmable current
j	Imaginary unit, commonly also denoted by i
K	Oversampling ratio
k	Spring constant; Boltzmann's constant, $1.38066 \cdot 10^{-23}$ J/K
k_B	Boltzmann's constant, $1.38066 \cdot 10^{-23}$ J/K
k_{eff}	Effective spring constant, $k_{eff} = k + k_{es}$
k_{es}	Electrostatic spring constant
K_{fn}	Empirical flicker noise coefficient of an NMOS transistor
K_{fp}	Empirical flicker noise coefficient of a PMOS transistor

K_{VCO}	Gain of a voltage-controlled oscillator
$L(s)$	Loop gain, $L(s) = A(s)\beta(s)$
L	Channel length in a MOS transistor
L_n	Channel length in an NMOS transistor
L_p	Channel length in a PMOS transistor
LDR	Load regulation, $LDR = \Delta V_{OUT}/\Delta I_{OUT}$ at steady-state
LG_{LF}	Low-frequency loop gain
LNR	Line regulation, $LNR = \Delta V_{OUT}/\Delta V_{IN}$ at steady-state
m	Mass; temperature coefficient of the collector current, $I_C \propto T^m$
N	Resolution in bits; number of gain stages in a ring oscillator
n	Arbitrary integer greater than zero
P	Power dissipation
p	Collector current ratio, $p = I_{C1}/I_{C2}$
p_A	Error amplifier pole, $p_A = 1/(2\pi R_A C_A)$
p_B	Bypass pole, $p_B = 1/(2\pi R_{ESR} C_B\text{'})$
P_{IN}	Input power
P_{OUT}	Output power
p_O	Output pole, $p_O = 1/[2\pi R_O\text{"}(C_O + C_B\text{'})]$
PSR	Power supply rejection, $PSR = 1/A_{IN} = V_{in}/V_{out}$, defined for the whole frequency spectrum
Q	Quality factor, $Q = \sqrt{km}/D$; charge
q	Electron charge, $1.602 \cdot 10^{-19}$ C
q_{max}	Maximum charge displacement across the capacitor on the node of interest
R	Resistance
r	Base-emitter junction area ratio, $r = A_{E2}/A_{E1}$; ratio of the aspect ratios of two MOS transistors, $r = (W/L)_2 \,/\, (W/L)_1$
R_A	Output resistance of the amplifier

R_a	Resistance of a one-port active circuit
R_B	Base resistance
r_{ds}	Output resistance of the PMOS pass device
R_{ESR}	Equivalent series resistance
R_F	Resistance in the resistive feedback network; resistance in the RC low-pass filter
R_f	Resistance of a one-port frequency-determining circuit
R_L	Load resistance
R_N	Resistance of the nulling resistor
$R_{O,CL}$	Closed-loop output resistance
$R_{O,OL}$	Open-loop output resistance
R_O"	Resistance in the linear regulator defined as R_O" = R_O'$||(R_{F1} + R_{F2})$
R_O'	Resistance in the linear regulator defined as R_O' = $R_L||r_{ds}$
$R_{type\text{-}1}$, $R_{type\text{-}2}$	Two types of resistors having different temperature dependencies
S	Slope of a voltage waveform
s	Laplace variable, $s = j\omega$ for real frequencies
$S_\phi(f)$	Phase noise power spectral density
$S_V(\omega)$	Output voltage spectrum
S_w	Frequency-domain white noise figure of merit
SNR	Signal-to-noise ratio
T	Absolute temperature
t	Time
T_1, T_2	Charging and discharging time
t_c	1/f transition time
t_{dN}	High-to-low propagation delay
t_{dP}	Low-to-high propagation delay
t_d	Propagation delay

t_{fall}	Time when a sudden decrease in the load current occurs
t_{rise}	Time when a sudden increase in the load current occurs
T_r	Reference temperature
TC	Temperature coefficient
$TNEA$	Total noise equivalent acceleration
V	Voltage
v	Velocity
V_0	Dc bias voltage
V_1, V_2	Upper and lower threshold voltage in a relaxation oscillator
V_{BE0}	Base-emitter voltage at 0 K
V_{BE}	Base-emitter voltage
V_{BIAS}	Biasing voltage
V_B	Biasing voltage
V_{CTRL}	Control voltage
V_C	Amplitude of the voltage waveform across a capacitor
V_c	Voltage waveform across a capacitor
V_{DD}	Supply voltage
V_{DO}	Dropout voltage
$V_{DS,sat}$	Drain-source saturation voltage, $V_{DS,sat} = V_{GS} - V_{TH}$
V_{DS}	Drain-source voltage
$V_{eff,d}$, $V_{eff,t}$	Overdrive voltage of a differential pair and a tail current source, $V_{eff} = V_{GS} - V_{TH}$
V_{g0}	Bandgap voltage of silicon linearly extrapolated down to 0 K, $V_{g0} \approx 1.206$ V
V_{GS}	Gate-source voltage
V_H	Hysteresis voltage, $V_H = V_1 - V_2$
V_{inm}	Negative part of a differential input voltage
V_{inp}	Positive part of a differential input voltage

V_{int}	Voltage at the output of an integrator
V_{IN}	Input voltage
V_{in}	Input voltage
V_{NL}	Non-linear voltage
V_{op}	Amplitude of the differential output waveform
V_{OS}	Offset voltage
V_{outm}	Negative part of a differential output voltage
V_{outp}	Positive part of a differential output voltage
V_{OUT}	Output voltage
V_{out}	Output voltage
V_{PTAT^2}	Proportional-to-square-of-absolute temperature voltage
V_{REF}	Reference voltage
V_R	Voltage that is forced to be approximately V_{REF} in the replica biasing circuit
V_r	Voltage at the reference temperature T_r
V_{swing}	Voltage swing
V_{THn}	Threshold voltage of an NMOS transistor
V_{THp}	Threshold voltage of a PMOS transistor
V_{TH}	Threshold voltage
V_{TR}	Transition voltage
V_T	Thermal voltage, $V_T = kT/q$
W	Channel width in a MOS transistor
x	Displacement in the x-direction; relative displacement between the frame and the proof mass, $x = x_f - x_m$; generally used variable
x_0	Initial distance between the frame and the proof mass
X_a	Reactance of a one-port active circuit
X_f	Reactance of a one-port frequency-determining circuit

x_f	Displacement of the frame
x_m	Displacement of the proof mass
z	Frequency variable in a discrete-time system, $z = e^{j\omega}$ for real frequencies
Z_a	Impedance of a one-port active circuit
z_{ESR}	ESR zero, $z_{ESR} = 1/(2\pi R_{ESR} C_O)$
Z_f	Impedance of a one-port frequency-determining circuit
z_{LHP}	Left-half-plane zero
Z_O	Ground impedance at the output of a linear regulator
Z_P	Output impedance of the PMOS pass device
z_{RHP}	Right-half-plane zero
Z_{shunt}	Shunting impedance resulting from the negative feedback loop of the linear regulator, $Z_{shunt} = (Z_P \| \| Z_O)/(\beta_F A_{OL})$
+FB	Positive feedback
3D	Three-dimensional
A/D	Analog-to-digital
ac	Alternating current; general symbol for time-varying electrical signal such as current or voltage
ADC	Analog-to-digital converter
ASIC	Application-specific integrated circuit
BiCMOS	CMOS technology that includes bipolar transistors
C/D	Capacitance-to-digital
C/f	Capacitance-to-frequency
C/V	Capacitance-to-voltage
CDS	Correlated double-sampling
CHS	Chopper stabilization
CMOS	Complementary metal-oxide-semiconductor
CT	Continuous-time

CTAT	Complementary-to-absolute temperature
D/A	Digital-to-analog
DAC	Digital-to-analog converter
dc	Direct current; general symbol for time-constant electrical signal such as current or voltage
DEM	Dynamic element matching
DFC	Damping-factor-control
DoF	Degree of freedom
DSP	Digital signal processing
DT	Discrete-time
EMI	Electromagnetic interference
ESR	Equivalent series resistance
FOM	Figure of merit
FTS	Feedforward transconductance stage
g	Gravity of the Earth, 9.81 m/s^2
HDO	High-dropout
IC	Integrated circuit
ISF	Impulse sensitivity function
KOH	Potassium hydroxide
LC	Inductor-capacitor
LDO	Low-dropout
LDR	Load regulation
LHP	Left-half-plane
LNR	Line regulation
LPF	Low-pass filter
LTI	Linear time-invariant
LTV	Linear time-variant

MEMS	Microelectromechanical system
MIM	Metal-insulator-metal
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field effect transistor
MSB	Most significant bit
NMOS	N-channel metal-oxide-semiconductor
OTA	Operational transconductance amplifier
OTA-C	OTA-capacitor, oscillator topology comprising OTAs and capacitors
PCB	Printed circuit board
PLL	Phase-locked loop
PM	Phase modulation; phase margin
PMOS	P-channel metal-oxide-semiconductor
ppm	Parts per million
PPV	Perturbation projection vector
PSD	Power spectral density
PSG	Phosphosilicate glass
PSR	Power supply rejection
PSRR	Power supply rejection ratio
PTAT	Proportional-to-absolute temperature
$PTAT^2$	Proportional-to-square-of-absolute temperature
RBVP	Reverse bandgap voltage principle
RC	Resistor-capacitor
RHP	Right-half-plane
rms	Root-mean-square
RTZ	Return-to-zero
S/H	Sample-and-hold

S/s	Samples per second
SAR	Successive approximation register
SBB	Self-balancing bridge
SC	Switched-capacitor
SCS	Single-crystal silicon
Si	Silicon
SiO_2	Silicon dioxide
SNR	Signal-to-noise ratio
SoC	System-on-chip
SOI	Silicon-on-insulator
SR	Slew-rate
SSB	Single-sideband
TC	Temperature coefficient
TI	Temperature-independent
TNEA	Total noise equivalent acceleration
V/F	Voltage-to-force
V/I	Voltage-to-current
VCO	Voltage-controlled oscillator
x/C	Displacement-to-capacitance

1 Introduction

1.1 Background and Motivation

Certainly one of the greatest inventions of the 20$^{\text{th}}$ century, the transistor, was invented at the Bell Telephone Laboratories in 1947 [1]. However, the principle of the metal-oxide-semiconductor field-effect transistor (MOSFET) was patented for the first time by J. E. Lilienfeld in 1925 [2]. MOS technologies with n-type transistors became practical by the early 1960s, and complementary MOS (CMOS) technologies with both n- and p-type transistors in the mid-1960s. The first integrated circuit (IC) was built at Texas Instruments in 1958 [3], and this started the revolution of the semiconductor industry. G. E. Moore, the co-founder of Intel, predicted in 1965 [4] that the number of components per chip would double every year. Ten years later, this well-known Moore's law was redefined by himself in such a way as to state that the number of components per chip would double every two years. To date, IC companies have kept up with that pace for over 40 years. At the same time, the minimum dimensions of a transistor have dropped from about 20 μm to 32 nm [5], resulting in a huge improvement in the speed of ICs. This exponential development in the field of microelectronics has increasingly launched new applications, including, among others, personal computers, laptops, mobile phones, portable music and video players, and handheld game consoles.

Small integrated devices or systems that combine electrical and mechanical components are called microelectromechanical systems (MEMS) [6]. They extend the fabrication techniques developed for the IC industry, for example by adding springs and moving structures to devices. MEMS sensors and actuators, which are devices that convert a non-electrical quantity into an electrical signal and vice versa, respectively, involve additional quantities, such as acceleration, angular velocity, and pressure, that can be sensed. Micromachining enables transducers to be miniaturized by shrinking their size by orders of magnitude, a significant reduction of the costs of fabrication, and integration with the electronics on the same silicon chip. The resonant gate MOS transistor [7], introduced by H. C. Nathanson and R. A. Wickstrom in 1965, is regarded as the first MEMS device. The first high-volume microsensor, the pressure sensor, was marketed by National Semiconductor in 1974. A great effort to fabricate MEMS started in the late 1980s.

One of the most important silicon-based sensors is micromachined inertial sensors [8], comprising accelerometers and gyroscopes. Accelerometers can be used to detect the magnitude and direction of the acceleration, i.e., to sense orientation, vibration and shocks, while gyroscopes can be used to measure the rate of rotation. Since 1990s MEMS accelerometers have been used extensively in airbags as crash sensors, and since then motion sensors have become more and more general as a part of different kinds of systems. The application spectrum of accelerometers is very broad and

includes applications in many different fields [9], such as aerospace, automobiles, biomedicine, the consumer sector, industry, machines, the military, and robotics. Automotive safety and stability control systems, various navigation and guidance systems, biomedical activity monitoring, movement detection in portable terminals and game controllers, vibration monitoring in industrial environments, and safing and arming in missiles are just a few application examples.

For a long time the MEMS market has comprised mature MEMS devices, such as inkjet heads, pressure sensors, and accelerometers. However, there are always several new emerging MEMS devices aiming at commercialization [10], the most promising of which at present are microbolometers, digital compasses, and oscillators. Yole Développement expects that as a result of the economic crisis that began at the end of 2008 the MEMS market will remain flat during the years 2009 and 2010 [11]. The crisis has affected various MEMS markets in different ways. The most dramatic influence has probably been in the automotive area. Nevertheless, Yole Développement has estimated that the MEMS inertial market will increase from 1.8 to 3 B$ during the period 2008-2013 [12]. The MEMS inertial market is dominated by automotive and consumer electronics applications. The consumer area is experiencing the strongest market growth and is expected to overtake the automotive in 2011. The key features of MEMS accelerometers aimed at battery-powered consumer applications, such as mobile phones, include small size, low power dissipation, and 3-axis sensing [13]. The latest consumer applications of 3-axis MEMS accelerometers include Nintendo Wii game controllers and the Apple iPhone.

1.2 Organization of the Thesis

This thesis focuses on the design of low-power electronics for reading a capacitive 3-axis micro-accelerometer. Six integrated circuits were designed, implemented and measured. As a result, two complete micropower sensor interface ICs were demonstrated. The research concentrated mainly on the following building blocks: capacitance-to-voltage (C/V) converters, analog-to-digital (A/D) converters, decimators, current, voltage, and temperature references, frequency references, and supply voltage regulators. The thesis consists of an overview and of the published papers [P1]-[P9]. The overview part is divided into eight chapters. After an introduction, Chapter 2 presents the general structure of accelerometers and discusses MEMS fabrication technologies and micromachined capacitive accelerometers. In Chapter 3, typical integrated readout electronics for a capacitive sensor are described on the functional level. Furthermore, different ways to realize the sensor readout itself, i.e., the C/V and A/D conversions, are briefly discussed. Chapters 4, 5, and 6 introduce fundamental design issues related to the building blocks for which the author was responsible, namely current, voltage, and temperature references, frequency references, and supply voltage regulators, respectively. The publications are summarized in Chapter 7, and finally, before the published papers, conclusions are drawn in Chapter 8.

2 Micromechanical Accelerometers

Most mechanical sensors rely on the deformation of a structure and further on the translation of this deformation into an electrical signal. Micromachined accelerometers are one of the most important types of micromechanical sensors. This chapter first introduces a general accelerometer structure, which corresponds to a second-order mass-damper-spring system. After that the main MEMS fabrication technologies, bulk and surface micromachining, are presented. Bulk-micromachined accelerometers are more applicable for low-noise, high-performance applications, thanks to their larger proof masses, whereas surface-micromachined accelerometers are more attractive for less demanding applications, thanks to their better IC compatibility. Finally, different ways to implement capacitive accelerometers are described.

2.1 General Accelerometer Structure

Linear inertial sensors typically consist of a proof mass (m), a spring (k), and a damper (D), which together form a 1-degree-of-freedom (DoF) mechanical resonator. Figure 2.1 shows a simple lumped element model for such a structure. The proof mass is attached to the frame (f) through the elastic spring, which supports the proof mass mechanically and restores it to the rest position ($x = 0$) after the acceleration is removed. The damper controls the motion of the proof mass. Viscous losses resulting from fluid flow (gas or liquid) dominate often the loss mechanisms in microscale [14]. Therefore, in order to reduce these effects, many MEMS devices are operated in lowered pressure. In parallel plate geometries, in which two surfaces move toward each other, the so-called squeeze film damping occurs. Under slow plate movements the gas is squeezed out, resulting in dissipation losses, whereas under fast plate movements the gas is compressed, thus causing spring forces as

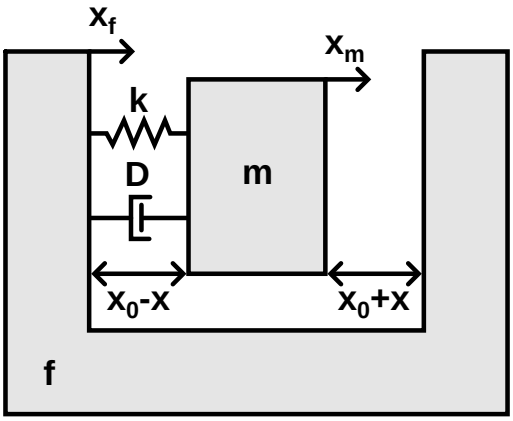


Figure 2.1: General 1-DoF mechanical resonator model for accelerometer structure.

well [14]. Furthermore, a sense methodology is required to convert the mechanical displacement to an electrical output.

It is assumed that the spring is weightless and the proof mass can move only in the x-direction. The movements of the frame and the proof mass are denoted as the absolute displacements x_f and x_m, respectively. In the rest position the relative displacement, $x = x_f - x_m$, is zero and the distance between the proof mass and the frame corresponds to the initial distance x_0. Under accelerated motion x becomes non-zero. In Fig. 2.1, the frame is accelerated to the right, in which case the left- and right-hand gaps between the proof mass and the frame are equal to $x_0 - x$ and $x_0 + x$, respectively. As a result, the acceleration of the system can be determined on the basis of the capacitance changes between the proof mass and fixed conductive electrodes (not shown in Fig. 2.1) attached to the surface of the frame. The equation of motion for the proof mass can be written as [14]

$$\begin{aligned} m\ddot{x}_m - D\dot{x} - kx &= F_E\,, && (2.1)\\ m(\ddot{x}_f - \ddot{x}) - D\dot{x} - kx &= F_E\,, && (2.2)\\ m\ddot{x}_f - F_E &= m\ddot{x} + D\dot{x} + kx\,, && (2.3) \end{aligned}$$

where D is the damping coefficient, k the spring constant, F_E the external force acting on the mass (resulting from actuation, for example), and $\dot{x} = dx/dt = v$ and $\ddot{x} = d^2x/dt^2 = a$. After the Laplace transform has been applied to (2.3), regrouping, and assuming that $F_E = 0$, the transfer function from the acceleration $\ddot{x}_f$ to the displacement x can be written as [9]

$$H(s) = \frac{x(s)}{\ddot{x}_f(s)} = \frac{1}{s^2 + \frac{D}{m}s + \frac{k}{m}} = \frac{1}{s^2 + \frac{\omega_r}{Q}s + \omega_r^2}, \qquad (2.4)$$

where $\omega_r = \sqrt{k/m}$ is the resonance frequency and $Q = \sqrt{km}/D$ the quality factor of the resonator. Since the dc sensitivity of the accelerometer becomes $H(0) = m/k = 1/\omega_r^2$, a low resonance frequency is required for a high dc sensitivity.

Small moving parts, such as the proof mass, are especially susceptible to mechanical-thermal noise caused by, for example, the Brownian motion of the gas molecules surrounding the resonator [15]. Mechanical-thermal noise limits the performance of the accelerometers, especially in applications where the signals are very small. For the resonator the total noise equivalent acceleration (TNEA) $[(\mathrm{m/s^2})/\sqrt{\mathrm{Hz}}]$ can be expressed as [15]

$$TNEA = \sqrt{\frac{\overline{a_n^2}}{\Delta f}} = \frac{\sqrt{4k_BTD}}{m} = \sqrt{\frac{4k_BT\omega_r}{Qm}}, \qquad (2.5)$$

where k_B is the Boltzmann's constant ($1.38066 \cdot 10^{-23}$ J/K) and T the absolute temperature. Accordingly, the mechanical noise can be reduced by increasing Q. Typically, accelerometers are specified by using a number of performance parameters: sensitivity, maximum operating range, frequency response, resolution, full-scale non-linearity, offset, off-axis sensitivity, and shock survival [9].

2.2 MEMS Fabrication Technologies

Silicon is an optimal material for mechanical sensors because of its exceptional mechanical properties, i.e., it always deforms in the same way under an equal load and fails before it is deformed plastically [8]. The latter is advantageous for sensors in overloading conditions, in which case the sensor breaks instead of giving a false signal. Microfabrication has historically been tied to IC fabrication, in which individual devices are photolithographically defined onto a wafer. Bulk micromachining, which has more generally been used in the fabrication of different microstructures [16], emerged in the early 1960s, while microstructures have been fabricated by using surface micromachining since the early 1980s. Batch fabrication makes manufacturing of tens of thousands of micromechanical devices on a single wafer possible. The main challenges of MEMS fabrication include packaging of movable mechanical structures, manufacturing thick structures, and providing good absolute dimensional control [14].

2.2.1 Bulk Micromachining

Bulk micromachining refers directly to its basic principle, according to which three-dimensional (3D) micromechanical structures are implemented by selectively etching the material of a single-crystal silicon (SCS) wafer [16]. As a result, the typical wafer thickness of 500-700 μm [14] makes the fabrication of relatively thick structures possible. Different wet and dry etching techniques with etch-masks and etch-stops are utilized individually or mixed. Wet chemical etching is used for lapping and polishing the wafer surface, delineating patterns and opening windows in insulating materials, as well as dissolving structures in the SCS wafer. Some wet etchants, such as potassium hydroxide (KOH), are anisotropic and they dissolve a certain crystal plane of a semiconductor much faster than the others [16]. However, the type, shape, and size of the SCS structures fabricated with anisotropic wet etching techniques are substantially limited, because the geometry is defined by the internal crystalline structure of the substrate. Early bulk-micromachined devices were made by using wet etching techniques, but advances in plasma processing have made dry etching techniques increasingly popular [14]. In the deep anisotropic dry etching of silicon wafers, reactive gas plasmas can be used to etch narrow channels through the entire wafer while maintaining smooth vertical sidewall profiles. Such etching techniques make possible aspect ratios as high as 50 to 1 or greater, thus potentially providing a significant reduction in device size, when compared to the use of wet etching techniques.

In addition to the need for different etching techniques, wafer bonding techniques are needed to construct complex 3D microstructures by assembling individually micromachined wafers on top of each other [8]. Wafer bonding has also an important role in the final encapsulation, because it provides protection and cavities required for the

free-standing mechanical parts. The spontaneous tendency of clean and flat wafers to adhere to each other can be boosted by using temperature, pressure, electric field, or their combination. Fusion bonding relies on a high-temperature annealing step up to 1200°C for silicon [17], while anodic bonding and thermo-compression bonding, which exploit the use of electrical forces and pressure, respectively, are typically performed at temperatures between 300 and 500°C. In addition to several undesired side-effects, such as doping profile broadening and thermal stresses [16], resulting from the high-temperature annealing, low-temperature fusion bonding techniques are highly required, since most of the common metals used in IC fabrication melt below 450°C. Unfortunately, annealing at temperatures below 800°C may result in inadequate bond strength for subsequent processing steps [16]. The oldest and widely used bonding technique, anodic bonding, which requires the use of additional materials, such as glass, can typically provide a relatively reliable bonding at temperatures below 400°C using dc voltages between 50 and 200 V [16]. Moreover, for example, so-called glass frit wafer bonding [17], which is a thermo-compression bonding technique based on melting of certain glasses under pressure at 500°C, is used in many bulk-micromachined applications, such as pressure sensors.

The silicon-on-insular (SOI) technology makes use of wafers that are manufactured by bonding SCS layers together with a 1-2-μm SiO_2 layer between them [14]. The SiO_2 layer can be considered as a natural etch stop when defining desired structures. Because two silicon wafers are required to form a single SOI wafer, such wafers are more expensive than conventional silicon wafers. However, it may be possible to compensate the increased material costs by the reduced processing costs [14]. Amini et al. have demonstrated high-resolution capacitive accelerometers [18, 19], in which accelerometers were fabricated by using SOI bulk micromachining and interface ICs by using CMOS.

2.2.2 Surface Micromachining

Surface micromachining resembles the traditional IC fabrication, because both of these are based on processing thin films on top of a silicon wafer. As a consequence, the major advantage of surface-micromachined structures is their easy integration with IC circuits [14]. However, their small sizes and masses are often insufficient, especially for capacitive micromechanical transducers, because of the small coupling capacitances available. A typical surface micromachining process, which is illustrated in Fig. 2.2 [14], is based on the deposition and patterning of two thin films on the wafer surface, sacrificial and structural layers, that can be etched selectively. Generally, either SiO_2 or phosphosilicate glass (PSG) is used as the sacrificial material and poly-Si as the structural material [8]. Surface micromachining enables free-standing and freely-moving structures to be implemented that would not be possible with bulk micromachining techniques. Because the residual stress and slow deposition process typically restrict the thickness of each deposited layer to remain below

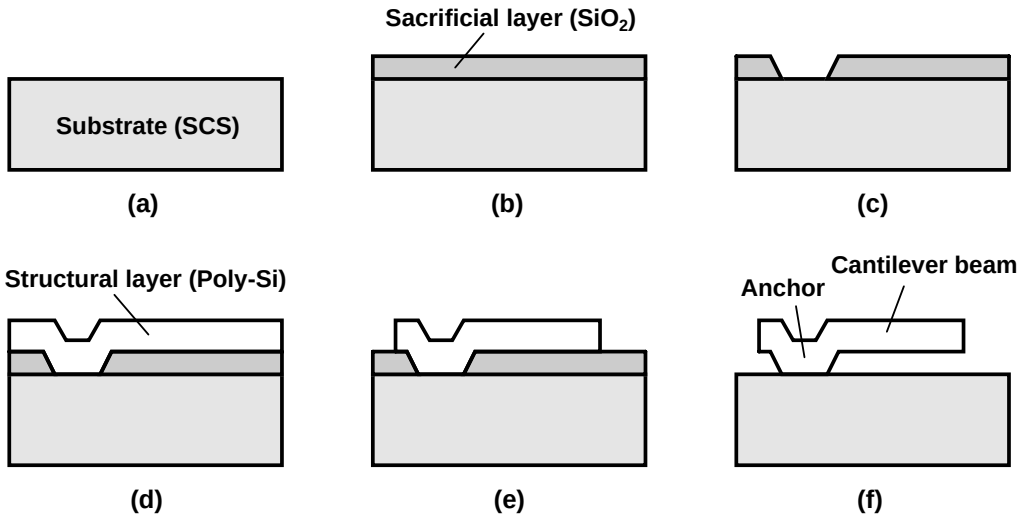


Figure 2.2: Typical surface micromachining process: (a) substrate as a mechanical support; (b) deposition and (c) patterning of a sacrificial layer; (d) deposition and (e) patterning of a structural layer, and (f) release etching.

5 μm [14], the dimensions of surface-micromachined structures, also called semi-3D structures, are substantially smaller than those of bulk-micromachined ones.

2.3 Capacitive Micro-Accelerometers

Accelerometers can be, for example, piezoresistive, capacitive, tunneling-type, resonant, thermal, optical, electromagnetic, or piezoelectric. The first micromachined micro-accelerometer [20] was piezoresistive. The main advantages of such accelerometers are their simple structure and fabrication process, but they suffer from low overall sensitivity, as well as a large temperature dependence. Capacitive micro-accelerometers have a number of advantages: high sensitivity, good dc response and noise performance, low temperature sensitivity, low drift, and low power dissipation [9]. Because of their high-impedance sense node, capacitive accelerometers are susceptible to electromagnetic interference (EMI), and thus their proper shielding and packaging are necessary. Moreover, in order to reduce parasitic capacitance the electronic interface circuitry must be placed in close proximity to the accelerometer. Thanks to their several advantages, capacitive micro-accelerometers have a wide range of different applications, ranging from low-cost automotive and low-power consumer accelerometers to high-precision inertial-grade devices [9].

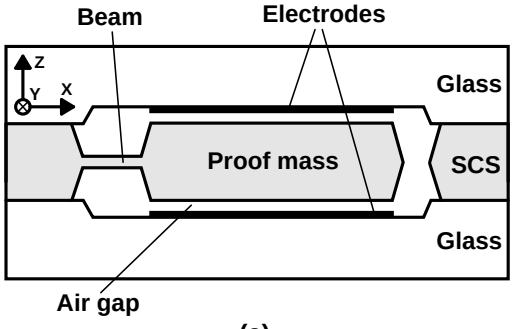
2.3.1 Bulk-Micromachined Capacitive Accelerometers

The first capacitive micro-accelerometers were fabricated by using bulk micromachining and wafer bonding. The main advantage of a bulk-micromachined device

is the large proof mass, while its major drawback is the wafer bonding step needed for the realization of an air gap, which is further required for damping and capacitive sensing [8]. On the other hand, the larger dimensions of a bulk-micromachined accelerometer, compared to its surface-micromachined counterpart, can be seen as a disadvantage as well. There is a trade-off between the capacitance value and damping, since a narrow gap, used to provide large capacitance, results in major damping.

Figure 2.3 (a) shows the basic vertical structure of a bulk-micromachined capacitive accelerometer [8] in which the proof mass is suspended by one cantilever beam. In this structure, the external acceleration perpendicular to the plane of the structure moves the proof mass in the z-direction, resulting in capacitance changes between the proof mass and two fixed conductive electrodes. The parallel-plate sense capacitances can be measured by using electronic readout circuitry. The mass and the largest dimension of a proof mass are typically on the order of 1 mg and 1 mm, respectively. Figure 2.3 (b) shows typical element parameters for a bulk-micromachined accelerometer [14]. Most single-axis bulk-micromachined accelerometers are vertical, because their proof mass can be implemented in a relatively simple way by wet etching [8]. More suspension beams can be used to provide a higher symmetry, and thus lower off-axis sensitivity, the benefit of which lateral bulk-micromachined accelerometers, which have a sensitive axis in the plane of the structure (x or y), typically reap.

The complete 3D acceleration vector can be measured by using a 3-axis accelerometer consisting of a single proof mass [21, 22]. By using such an approach, a remarkable area saving can be achieved compared to an implementation including three single-axis accelerometers. Figure 2.4 (a) shows the top view of the structure for a 3-axis bulk-micromachined capacitive accelerometer [22]. The proof mass is suspended by four beams and it consists of four electrodes. The structure allows relatively long beams and large capacitor plates in a small area. Figures 2.4 (b) and (c) show how the 3-axis accelerometer responds to the z- and x-directional accel-



(a)

Parameter	Value	Unit
Resonance frequency, f_r	1	kHz
Mass, m	1	mg
Spring constant, k	50	N/m
Sense capacitance, C_0	5	pF
Quality factor, Q	0.1	

(b)

Figure 2.3: (a) Basic vertical structure and (b) typical element parameters for a bulk-micromachined capacitive accelerometer.

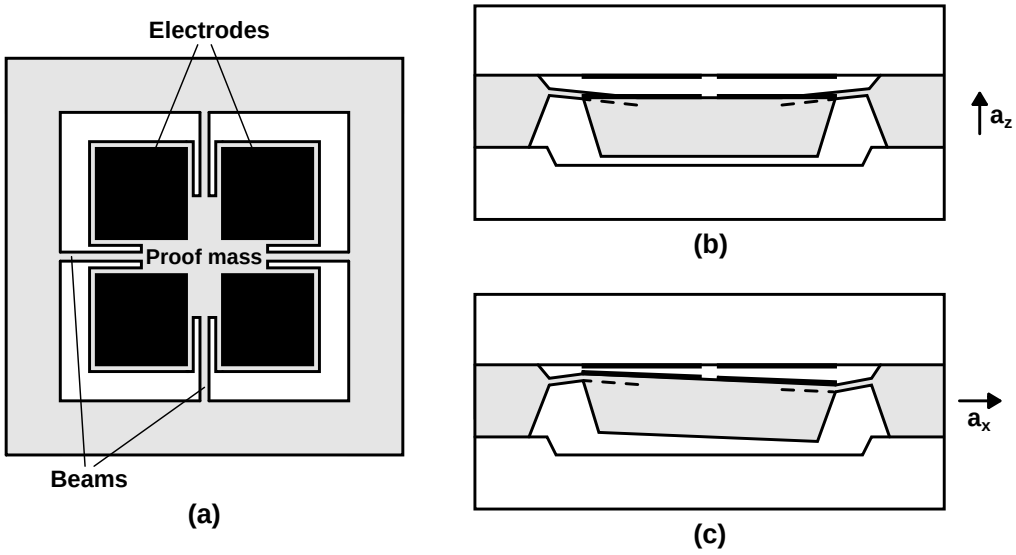


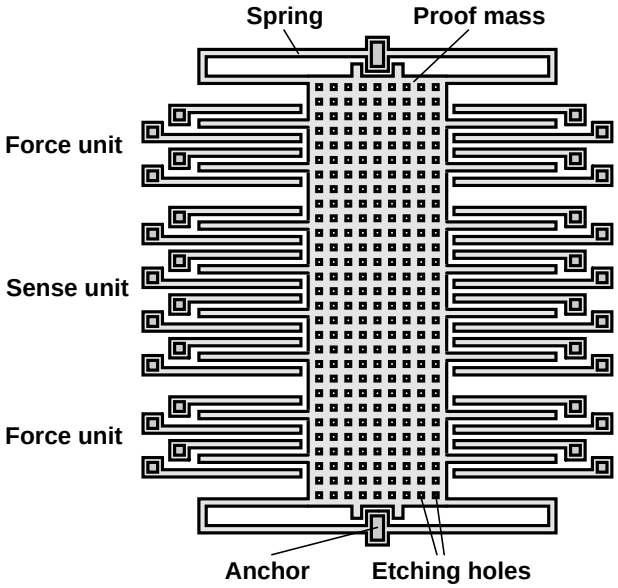
Figure 2.4: 3-axis bulk-micromachined capacitive accelerometer: (a) top view of the structure, and response to (b) vertical and (c) lateral acceleration.

erations, respectively. Vertical acceleration deflects the proof mass in the direction of the acceleration (z-axis), thus resulting in the same capacitance change for all four parallel-plate sense capacitors. Lateral acceleration, on the other hand, causes tilting of the proof mass, which causes the increment and decrement of two capacitances in pairs. As a first-order approximation, an arbitrary input acceleration can be derived from the four capacitance values. The 3-axis bulk-micromachined accelerometer presented in [23] consists of four triangular proof masses suspended asymmetrically with torsion springs. The masses form four differential capacitor pairs with fixed electrodes, make very similar linear responses possible for each of the three axes, and provide larger capacitance levels, as well as higher sensitivity, compared to the structure of Fig. 2.4.

2.3.2 Surface-Micromachined Capacitive Accelerometers

Surface micromachining makes single-wafer implementations and the co-integration of mechanical microstructures with electronic interface circuits easier. The damping can be controlled easily by making arrays of holes through the thin structures. One substantial disadvantage of a surface-micromachined accelerometer is that the noise level calculated with (2.5) becomes more than a hundred times higher than that of a bulk-micromachined accelerometer that can provide high sensitivity with an equivalent noise level of 1 $\mu g/\sqrt{\text{Hz}}$ [8]. However, the noise performance of the surface-micromachined accelerometers is acceptable for many applications, such as in the field of the automotive industry.

Figure 2.5 (a) shows the basic structure of a lateral surface-micromachined accel-



Parameter	Value	Unit
Resonance frequency, f_r	25	kHz
Mass, m	0.2	µg
Spring constant, k	5	N/m
Sense capacitance, C_0	0.1	pF
Quality factor, Q	5	

(b)

Figure 2.5: (a) Basic lateral structure and (b) typical element parameters for a surface-micromachined accelerometer.

erometer [8]. Sense capacitances are formed by using comb structures consisting of a number of moving sense fingers and fixed fingers attached to the proof mass and to the substrate, respectively. Because the thickness of surface-micromachined structures is only on the order of 2 μm, typically 40-100 finger pairs are included to increase the overall capacitance [14]. A proof mass suspended with two folded springs from anchors has a number of etching holes to ensure the complete removal of the sacrificial oxide layer. Because the proof mass moves in the plane of the wafer, the holes do not affect damping in this structure. In addition to sensing the position, the comb structures are used to implement force feedback and self-test functions. In the vertical surface-micromachined accelerometer structure, a proof mass hangs above an electrode attached to the surface of the wafer, and a voltage between the capacitor plates causes an electrostatic force that pulls the proof mass towards the surface of the wafer. The nominal position of the proof mass can be maintained by using a comb structure around the periphery of the proof mass to generate a net pull-up force [24, 25]. The vertical surface-micromachined accelerometer provides a larger capacitance value, up to 1 pF, compared to that of the lateral structure, which remains below 0.2 pF [8]. Typical element parameters for a surface-micromachined accelerometer are shown in Fig. 2.5 (b) [14].

A capacitive 3-axis accelerometer can be implemented by combining one vertical and two lateral surface-micromachined accelerometers. Lemkin et al. were the first to use this kind of approach and integrated a complete 3-axis micro-accelerometer together with the interface electronics [26, 27]. Frequently, bulk and surface micromachining have also been combined. For example, Yazdi et al. presented this kind

of a hybrid fabrication technology [28] for precision micro-accelerometers, which enables a large proof mass, controllable and small damping, and a small air gap to be used. A monolithic hybrid silicon micromachined, high-resolution, 3-axis, capacitive accelerometer consisting of three individual single-axis accelerometers has been demonstrated in [29].

2.4 Discussion

The low-power sensor interface application-specific integrated circuits (ASICs) discussed in this thesis, originally presented in [P4] and [P8], were designed to read a 3-axis bulk-micromachined capacitive accelerometer. For the measurements, the integrated readout electronics were combined with an external encapsulated micro-accelerometer on a printed circuit board (PCB). The results obtained are expected to improve when the interface ASIC is bonded directly to the sensor, as this reduces the parasitic capacitances substantially. The next chapter deals with the electrical interfacing of capacitive micro-accelerometers.

3 Electronic Interfacing of Capacitive Micro-Accelerometers

Capacitive sensing is usually exploited when a high resolution, low power dissipation, and low temperature coefficient are required. The very small low-frequency signals available from micro-accelerometers, together with large parasitics, set strict performance requirements for electronic interfaces. If the capacitive sensing is carelessly designed, the parasitics can reduce the resolution by an order of magnitude or more [30]. In a similar way to resistance changes, capacitance changes can be measured in a bridge configuration, which typically results in a simple circuit. This chapter first describes a typical capacitive micro-accelerometer system and alternative configurations for reading a capacitive sensor. Then the chapter discusses general issues related to C/V conversion. Finally, analog-to-digital converters (ADCs) applicable to sensor applications with low signal frequencies are briefly discussed.

3.1 System Description

A two-chip implementation of a micro-accelerometer system, together with an equivalent electrical model for a capacitive half-bridge and a list of functionalities commonly involved in capacitive interface ASICs, is illustrated in Fig. 3.1. The sensor and interface electronics are implemented separately, but they are mounted in the same package and connected through wire bonding. This kind of a configuration enables the performance of the sensor and electronics to be optimized independently of each other. However, a two-chip implementation suffers from larger parasitics compared to a single-chip implementation as a result of bonding pads and longer interconnections, which must be considered carefully. For example, the series resistances of the interconnection lines from the sensor element to the electronic interface may cause remarkable noise and undesirable time constants [30]. The manufacturing requirements of mechanical elements can be relaxed by shifting requirements such as linearity and matching to the interfacing electronics.

The capacitive half-bridge makes possible the differential capacitive position sensing via the detection capacitances C_P and C_N. These capacitances are formed between the movable middle electrode M, which is connected to the proof mass, and the two stationary electrodes P and N, located at the distances $x_0 - x$ and $x_0 + x$ from the proof mass, respectively. As an analogy with Fig. 2.1, the parameters x_0 and x correspond to the initial distance between the capacitor plates and the change in plate distance induced by acceleration, respectively. In the rest position both C_P and C_N are equal to C_0, i.e., the static part of the detection capacitances. For small displacements $x \ll x_0$ their capacitance changes are approximately the same, corresponding to $\Delta C/2$. Assuming that the transfer function of the sensor readout

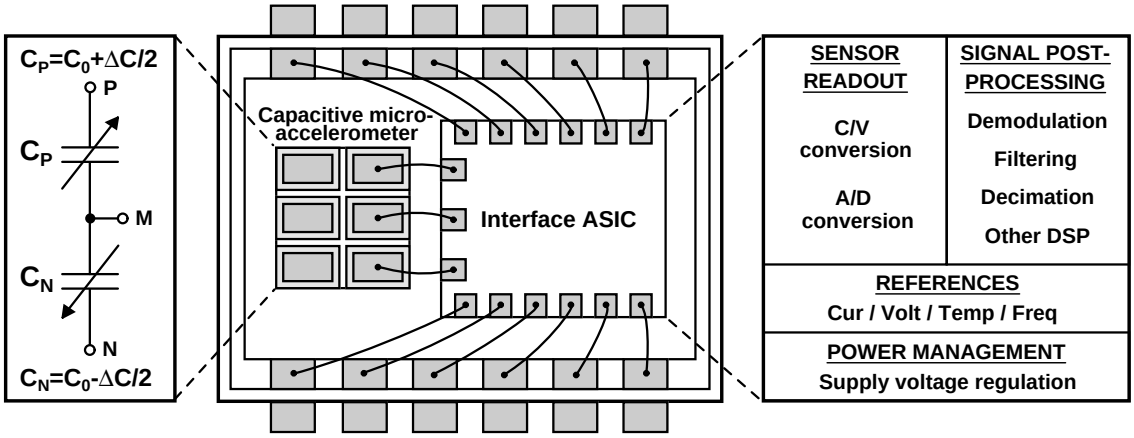


Figure 3.1: Two-chip capacitive micro-accelerometer system, together with a capacitive half-bridge sensor model and a list of functionalities commonly involved in capacitive interface ASICs.

is proportional to $(C_P - C_N)/(C_P + C_N) = \Delta C/(2C_0)$, the sensitivity of a system can be increased by making the signal part ΔC larger with respect to the static part C_0; however, this is at the cost of degraded linearity. For proper operation, the stray capacitances to the substrate and between the fixed electrodes should be kept comparable or smaller than C_0 [30]. By using the parallel-plate assumption the detection capacitances under acceleration can be expressed as

$$C_P = \frac{\varepsilon_r \varepsilon_0 A}{x_0 - x} = C_0 \left(\frac{x_0}{x_0 - x} \right) , \tag{3.1}$$

$$C_N = \frac{\varepsilon_r \varepsilon_0 A}{x_0 + x} = C_0 \left(\frac{x_0}{x_0 + x} \right) , \tag{3.2}$$

where ε_r is the relative permittivity of the insulator between the plates ($\varepsilon_r = 1$ for vacuum or air), ε_0 the permittivity of the vacuum ($8.85419 \cdot 10^{-12}$ F/m), and A the plate area.

The overall system specifications are the main factor determining the implementation of the capacitive interfacing. Regardless of the system configuration, the interface electronics require a front-end circuit that performs the C/V conversion, or, in other words, converts the capacitive information from the mechanical sensor element to a voltage. Furthermore, at least a low-pass filter is needed to limit the bandwidth of the system. In order to make possible some kind of digital signal processing (DSP), which is needed in most modern sensor systems, the ADC is usually included to perform the A/D conversion. Alternatively, a capacitance-to-frequency (C/f) converter can be used to convert the capacitance into a frequency or time delay, which can easily be measured with digital circuits as well [8]. Depending on the application, many other functions, such as demodulation, filtering, decimation, linearization, and temperature compensation may have to be included in the

sensor interface system. In order for a complete fully-integrated sensor interface chip to be implemented, different kinds of reference and power management circuits are usually needed to provide the required current and voltage levels, clock signal frequencies, and, possibly, supply voltage regulation. Moreover, providing the system with a temperature reference enables the temperature-dependent non-idealities, such as offset, to be compensated. Such compensation can be realized in the DSP part, in which case a digital temperature reading is required.

3.1.1 Electrostatic Forces

When a single parallel-plate capacitor with a gap of $x_0 + x$ is biased with a constant voltage V_B, the energy stored in it is

$$E = \frac{1}{2} C V_B^2 = \frac{1}{2} \frac{\varepsilon_r \varepsilon_0 A}{(x_0 + x)} V_B^2. \tag{3.3}$$

The attractive electrostatic force generated between the two electrodes can be solved by using the partial derivative of the total energy E_{tot} stored in the system, which comprises the capacitor and the voltage source, with respect to the displacement [14]. The electrostatic force is thus a non-linear function of both V_B and x. By assuming $x \ll x_0$ and by taking the first two terms of the Taylor expansion, the linear approximation of the electrostatic force becomes [31]

$$F_{es} = -\frac{\partial E_{tot}}{\partial x} = \frac{1}{2} \frac{\partial C}{\partial x} V_B^2 = -\frac{1}{2} \frac{\varepsilon_r \varepsilon_0 A}{(x_0 + x)^2} V_B^2 \approx -\frac{1}{2} \frac{\varepsilon_r \varepsilon_0 A}{x_0^2} V_B^2 + \frac{\varepsilon_r \varepsilon_0 A}{x_0^3} V_B^2 x. \tag{3.4}$$

According to (3.4), the electrostatic force consists of a displacement-independent part and a part with a linear dependence on the displacement. The former, which can be considered as an offset, can be exploited in the electrostatic excitation, whereas the latter reduces the effective spring constant k_{eff}.

The effect of the electrostatic force can be applied to the mass-spring-damper system by adding F_{es} given in (3.4) to the equation of motion stated in (2.3) [31]. As a result, the equation of motion can be rewritten as

$$m\ddot{x}_f - \frac{1}{2} \frac{\varepsilon_r \varepsilon_0 A}{x_0^2} V_B^2 = m\ddot{x} + D\dot{x} + \left(k - \frac{\varepsilon_r \varepsilon_0 A}{x_0^3} V_B^2 \right) x. \tag{3.5}$$

where the factor $k - \varepsilon_r \varepsilon_0 A V_B^2 / x_0^3 = k + k_{es} = k_{eff}$. The reduction of the effective spring constant resulting from the electrostatic spring constant k_{es}, a phenomenon which is known as electrostatic spring softening, results in a lower resonance frequency, and thus a higher dc sensitivity. At the critical V_B, which is often called the pull-in voltage, k_{eff} reduces to zero, and consequently capacitor plates snap together. For capacitive microsensors with nominal gaps in the micron range pull-in occurs within a few volts, often well within the supply voltage range [30]. Consequently, in

order to achieve a wide and linear acceleration range, careful consideration of the electrostatic forces is necessary in the front-end design.

In the case of a differential capacitive sensor structure, such as the capacitive half-bridge shown in Fig. 3.1, there are two opposite electrostatic forces affecting the proof mass, corresponding to the gaps of $x_0 - x$ and $x_0 + x$. The electrostatic force related to the capacitor with the gap of $x_0 - x$ is identical to (3.4), except that the second term of the last expression is also negative. Including the two opposite electrostatic forces, (3.5) can be rewritten as

$$m\ddot{x}_f = m\ddot{x} + D\dot{x} + \left(k - 2\frac{\varepsilon_r \varepsilon_0 A}{x_0^3} V_B^2\right) x. \tag{3.6}$$

Hence, when compared to (3.5) the offset is canceled and the magnitude of the electrostatic spring constant k_{es} is doubled.

3.1.2 Open-Loop Interfaces

Different open-loop configurations for reading a capacitive micro-accelerometer are shown in Fig. 3.2. The configuration (a) is the simplest capacitive interface, consisting of only a continuous-time (CT) front-end and a low-pass filter (LPF). It is

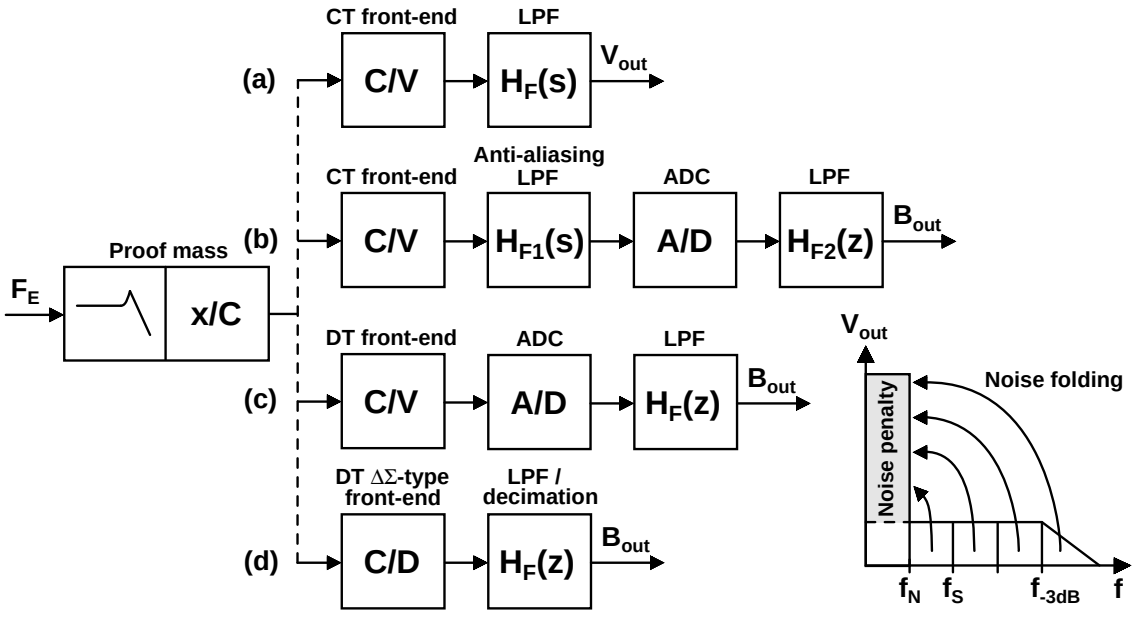


Figure 3.2: Different open-loop configurations for reading a capacitive micro-accelerometer: (a) CT interface with an analog output; (b) partly CT interface with an anti-aliasing LPF and a digital output (noise folding as a result of the sampling of a CT signal, illustrated bottom right); (c) DT interface with a digital output, and (d) DT $\Delta\Sigma$-type interface with direct C/D conversion.

particularly suitable for purely analog systems, which can directly utilize its CT voltage output. Similarly, the configuration (b) has a CT front-end, but it also includes an ADC. In order to avoid the corruption of the low-frequency signal band by aliased components resulting from the sampling of a CT signal, which is also illustrated in Fig. 3.2, a low-pass anti-aliasing filter with a sharp cut-off at f_N must be included before the sampling that occurs in the ADC. The low-pass filter after the ADC can be implemented digitally. In the case of configuration (c), which includes a discrete-time (DT) front-end, the need for a particular anti-aliasing filter is avoided thanks to the bandwidth limitation provided by the mechanical element. If the interface must provide a digital output with low power dissipation, the use of configuration (d), which performs direct capacitance-to-digital (C/D) conversion, can be appropriate. This kind of implementation includes a DT $\Delta\Sigma$-type front-end with an oversampled digital output and a low-pass decimation filter.

There is a fundamental difference between CT and DT interfaces as regards the capacitive loading of amplifiers. In contrast to a CT amplifier, a larger load capacitor results in a lower noise spectral density in a DT amplifier; however, this is at the cost of increased power dissipation for a certain bandwidth. Hence, a CT front-end can achieve a certain resolution with lower power dissipation [30]. It is worth noting that a similar advantage cannot be achieved if a CT front-end is used in a system with a digital output, because of the need for an anti-aliasing filter. Generally, the advantages of open-loop interfaces are their simple implementation, i.e., low power dissipation, and naturally high resolution and stability. Compared to closed-loop interfaces, which will be discussed next, the aforementioned advantages are achieved at the cost of reduced bandwidth and dynamic range, together with greater sensitivity to variations in fabrication and ambient [30].

3.1.3 Closed-Loop Interfaces

One important advantage of capacitive interfaces is that they can potentially be used, in addition to a sensor, as an actuator via an electrostatic force feedback. Figure 3.3 shows two different closed-loop interface configurations that both exploit the electrostatic force as the feedback force F_{fb} to oppose displacements of the proof mass from its initial position. The configuration (a) is a linear force feedback interface with an analog output, while the configuration (b) is a so-called electromechanical $\Delta\Sigma$ modulator interface with an oversampled digital output, first presented in [32]. Thanks to the feedback the mechanical bandwidth can be optimized for sensitivity, regardless of the useful bandwidth of the complete system, which is increased by the loop gain. Additionally, force feedback can be used to improve the dynamic range, linearity, and drift. Accordingly, closed-loop implementations are preferred in high-resolution applications, such as inertial navigation, where a wide dynamic range and low drift over time and temperature are required. In the case of low-damping high-Q accelerometers force feedback is especially important to limit the

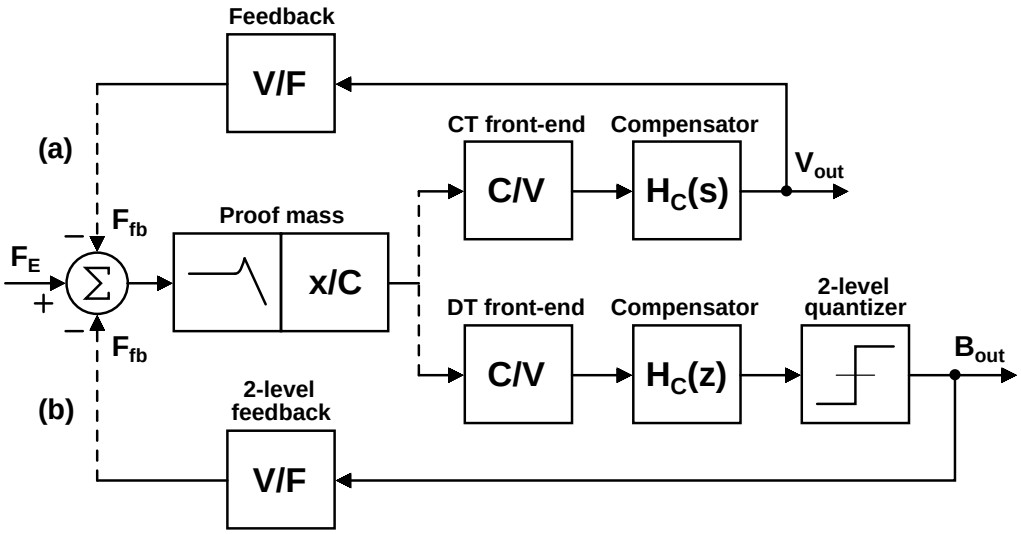


Figure 3.3: Two different closed-loop configurations for reading a capacitive micro-accelerometer: (a) linear force feedback interface with an analog output, and (b) electromechanical $\Delta\Sigma$ modulator interface with an oversampled digital output.

motion of the proof mass at the resonance frequency [8]. Large motions would result in non-linearity.

Electrostatic force feedback with differential actuation can be used to linearize the electrostatic force of symmetric sensors with respect to the biasing voltage V_B. For example, in the case of the structure shown in Fig. 2.5, in which each finger of the proof mass forms capacitors with two fixed electrodes, the linearization can be done by applying the voltages $V_0 + \Delta V$ and $V_0 - \Delta V$ to the fixed electrodes [8]. The voltages V_0 and ΔV correspond to a dc bias and a variable actuation voltage, respectively. Assuming the moving finger is located exactly in the middle between the fixed fingers, in which case $x = 0$ in (3.4), the effective electrostatic force can be written as

$$F_{es,eff} = \frac{1}{2}\frac{\varepsilon_r \varepsilon_0 A}{x_0^2}\left(V_0 + \Delta V\right)^2 - \frac{1}{2}\frac{\varepsilon_r \varepsilon_0 A}{x_0^2}\left(V_0 - \Delta V\right)^2 = 2\frac{\varepsilon_r \varepsilon_0 A}{x_0^2} V_0 \Delta V. \qquad (3.7)$$

Because of the linear relation between $F_{es,eff}$ and ΔV, the differential actuation is particularly suitable for implementing linear CT force feedback.

The closed-loop configuration (b) obtains linearity by utilizing the pulse modulation of the feedback signal, which is a more frequently applied technique [8]. A two-level quantizer included in an oversampled feedback loop determines two feedback force levels. The binary quantizer, together with the intrinsically linear two-level feedback, results in the quadratic relation between the voltage and electrostatic feedback force F_{fb}. The pulse-density of the one-bit digital output tracks the input acceleration, which can be obtained by low-pass filtering and decimating the pulse-density code. Compared to a conventional $\Delta\Sigma$ modulator, which is widely used

in A/D conversion, the electromechanical $\Delta\Sigma$ modulator utilizes the mechanical element as a loop filter. The compensator is required to solve the instability problem caused by the mechanical element, which is often underdamped and has a pair of complex poles at the resonance frequency [30]. The quantization noise, which is a particular feature of the $\Delta\Sigma$ loop, can cause a significant resolution penalty compared to an open-loop implementation. This problem can be alleviated with an optimum transfer function of the compensator and by increasing the order of the loop filter with electronic filters. In the case of a feedback interface with a DT front-end, the sense and feedback phases can be time-multiplexed in such a way that the same capacitors are used for sensing and feedback [30]. In this way the need for dedicated feedback electrodes is avoided in the mechanical element.

3.2 C/V Conversion

The most common approach to measuring the capacitive signal is to apply an ac voltage excitation to the capacitor and detect the resulting current by using a charge integrator or a voltage buffer. Capacitive front-ends typically utilize charge integration because of its better immunity to parasitics. Figures 3.4 (a) and (b) show the commonly-used capacitive half-bridge configured for single-ended and differential sensing [27], respectively. In the single-ended case the capacitance is measured by biasing the stationary electrodes P and N with two opposite ac signals and taking the output from the middle electrode M. A differential output can be achieved with the same sensor element by reversing the roles of the stationary electrodes and the middle electrode. Usually, square wave driving signals are used. However, the high harmonic content of such a signal may excite a parasitic resonance mode of a sensor element. The precise generation of the ac signals over the temperature and supply voltage ranges is required for high output stability [27]. Differential capacitive sensing has several advantages, including improved supply noise immunity and first-order rejection of common-mode errors, such as substrate noise and the charge injection of switches. A single C/V converter can be configured to read a 3-axis capacitive micro-accelerometer, which consists of several capacitive half-bridges, in an area-efficient way by utilizing time-multiplexing [33].

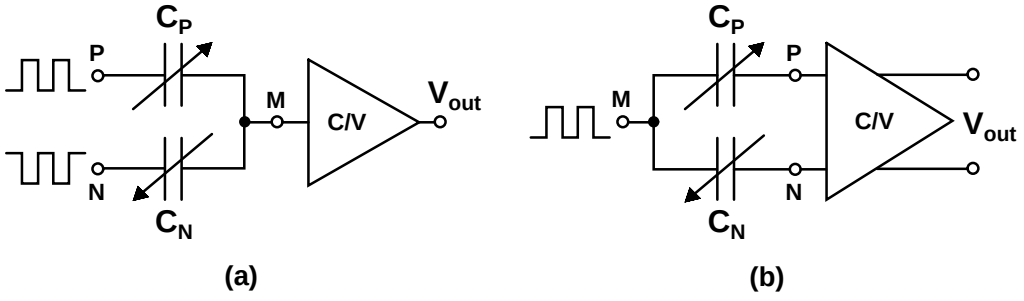


Figure 3.4: (a) Single-ended and (b) differential sensing of a capacitive half-bridge.

The reasons that support the sensor readout mechanically in an open loop are its simple implementation, which reduces both silicon area and power dissipation, and the limited voltage range available for electrostatic feedback. However, according to the earlier discussion in Section 3.1.1, if the electrostatic forces are not taken into account in an open-loop configuration, they cause the reduction of the spring constant, non-linearity, and, in extreme cases, pull-in. The two possible biasing techniques are constant voltage biasing and constant charge biasing, of which the latter can be used to cancel the effect of electrostatic forces. For example, the so-called self-balancing bridge (SBB) circuit [34] changes the middle electrode voltage with a certain delay in such a way that the charges are kept constant, and consequently the electrostatic forces are balanced. One of the major challenges in capacitive sensor interfaces is the low signal level, since noise and interferences are also boosted as a consequence of signal amplification. Because many sensors provide low-frequency signals, this problem is further emphasized by the elevated low-frequency noise floor caused by flicker noise. The flicker noise problem can be relieved by using two alternative circuit techniques with comparable performance, namely chopper stabilization (CHS), which is a CT modulation technique, and correlated double-sampling (CDS), which is a DT sampling technique [35].

3.2.1 Continuous-Time Readout

A CT charge amplifier utilizing the CHS technique, shown in Fig. 3.5 [8], is especially suitable for systems with an analog output. In the same figure, the operating principle of the CHS is illustrated with a progressive signal spectrum [30]. The

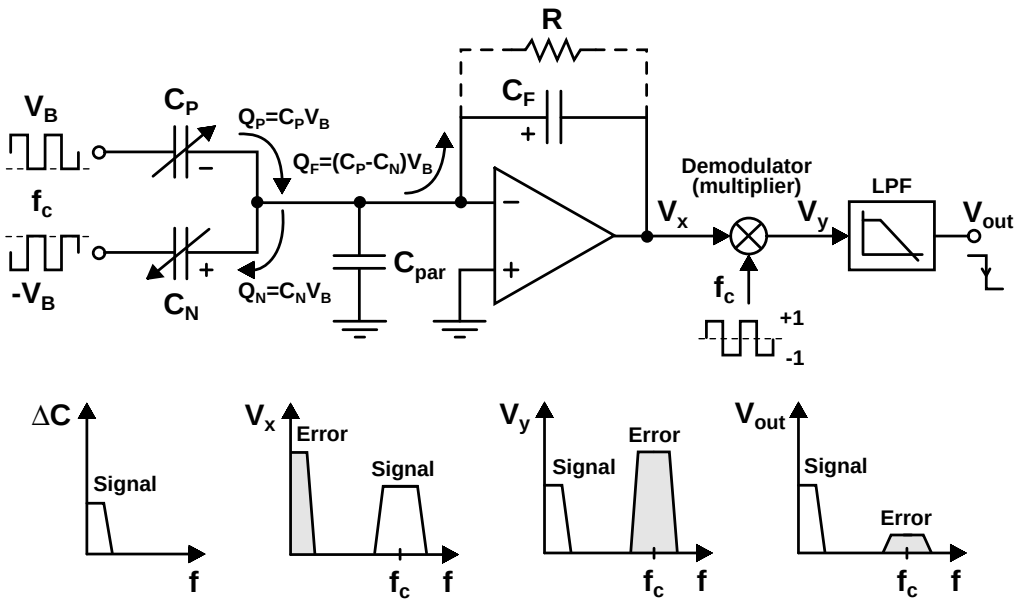


Figure 3.5: Operating principle of a CT charge amplifier using chopper stabilization.

signal is first modulated around a carrier frequency f_c and then the resulting ac signal is amplified and further demodulated back to dc. In contrast to sampling, the signal modulation does not cause noise folding. The demodulation is performed by multiplying the amplifier output by a square wave, which also has the frequency f_c and is in phase with the input signal. As a result, the offset and low-frequency noise of the amplifier are shifted to the vicinity of the carrier, where they can be effectively low-pass filtered from the output signal.

The inverting charge amplifier effectively eliminates the parasitic capacitor because there is virtually zero voltage over C_{par}. The large feedback resistor R is required to define the dc path between the input and output of the amplifier. Since no current can flow into the amplifier input, the amplifier adjusts its output in such a way that the charge is transferred to C_F, thus resulting in an output voltage of the form

$$V_{out} = -\left(\frac{C_P - C_N}{C_F}\right) V_B = -\frac{\Delta C}{C_F} V_B, \tag{3.8}$$

in which the differential change of the detection capacitances, i.e., $C_P = C_0 + \Delta C/2$ and $C_N = C_0 - \Delta C/2$, is assumed. Accordingly, the output voltage is directly proportional to the signal part ΔC and inversely proportional to the feedback capacitance C_F. Note that the CHS technique used in Fig. 3.5 does not affect the transfer function of the structure. It is possible to combine chopper techniques with a DT front-end as well [36].

3.2.2 Discrete-Time Readout

Discrete-time switched-capacitor (SC) circuits are widely used in front-end and ADC implementations. The superior property of SC circuits is that the accuracy of the signal processing function is proportional to the accuracy of the capacitor ratios, instead of their absolute values. The other main advantages of SC circuits are their good voltage linearity and temperature characteristics, while their major disadvantages are clock feedthrough, the need for non-overlapping clock signals, the limited signal bandwidth below the clock frequency, and noise folding [37]. The DT front-end shown in Fig. 3.6 corresponds to the open-loop configuration (d) of Fig. 3.2. This $\Delta\Sigma$-type front-end, which is based on [38], performs the direct C/D conversion mechanically in an open loop. The CDS technique has been applied to this structure by including a so-called offset storage capacitor C_{OS} and a switch that connects the negative input of the operational amplifier to the feedback capacitor in the sampling phase (ϕ_1). During this phase the offset voltage V_{OS} is stored in C_{OS}, while during the integration phase (ϕ_2) C_{OS} is connected in series with the negative input of the operational amplifier. As a result, the effect of offset and low-frequency noise is effectively canceled.

The operating principle of the complete $\Delta\Sigma$-type front-end is simply the following:

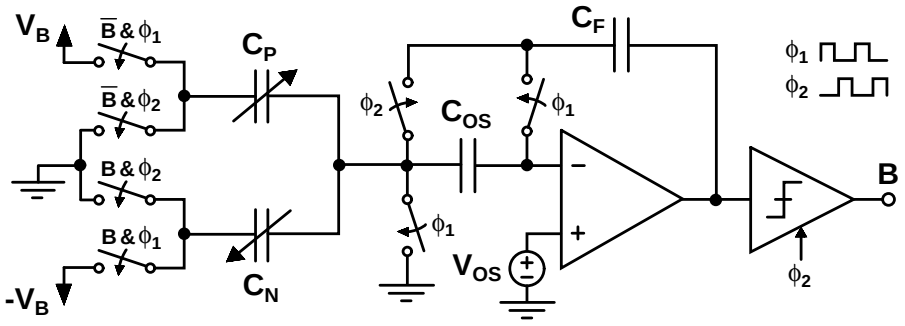


Figure 3.6: $\Delta\Sigma$-type SC front-end utilizing correlated double-sampling and performing direct C/D conversion.

in phase ϕ_1, depending on the previous output bit B, either a positive or negative detection bias voltage, V_B or $-V_B$, is sampled into one of the detection capacitances. In phase ϕ_2, the sampled charge is integrated and the new output bit is evaluated by the comparator. Therefore, the smaller detection capacitance, C_P or C_N, is sampled more often. This structure not only performs the inherent C/D conversion, but also balances charge; in other words, it ensures an equal average charge in the detection capacitors, and thus reduces the distorting effects of the non-linear electrostatic forces. When the parallel-plate capacitor assumptions of (3.1) and (3.2) are used, and it is assumed that the low and high values of B correspond to 0 and 1, the bit average becomes

$$\overline{B} = \frac{C_P - C_N}{2(C_P + C_N)} + \frac{1}{2} = \frac{x}{2x_0} + \frac{1}{2}. \tag{3.9}$$

Accordingly, the output of the structure is ratiometric. It is linearly proportional to the displacement x, and hence also to the acceleration, as becomes evident from (2.4). It is also worth noting that ideally $\overline{B}$ does not depend directly on the biasing voltages.

3.3 A/D Conversion

A general block diagram of an ADC is shown in Fig. 3.7 [37]. It consists of an anti-aliasing low-pass filter, a sample-and-hold (S/H) circuit, a quantizer, and an encoder. The overall transfer function is a discontinuous plot of the input voltage versus the

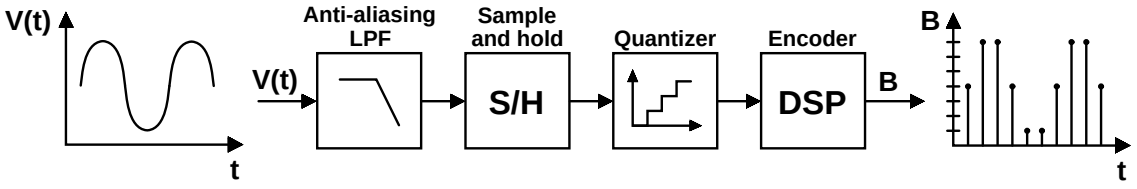


Figure 3.7: General block diagram of an ADC.

2^N output codes, where N is the resolution of the ADC in bits. The data conversion process itself results in quantization error in ADCs. This fundamental error limits the theoretical best signal-to-noise ratio (SNR) in decibels to $6.02N+1.76$, which holds for a sinusoidal input signal. In order to reduce the quantization noise a higher-resolution ADC or oversampling can be utilized. The input bandwidth f_B of Nyquist ADCs is maximized close to one half of the sampling frequency, i.e., $f_S/2$, while in the case of oversampled ADCs it is much less than $f_S/2$. Other mechanisms limiting the achievable SNR are input-referred circuit noise, sampling time uncertainty, also known as aperture jitter, and comparator ambiguity [39].

The choice of a specific ADC architecture depends mainly on the application itself [40]. The ADC architectures are typically classified according to their speed and accuracy, which have a clear relation to each other. For example, the resolution of the fastest ADCs, i.e. flash converters, is restricted to roughly 8 bits, while $\Delta\Sigma$ ADCs are widely used in applications requiring high resolutions of 16-24 bits. However, such high resolutions are achieved at the cost of limited effective sampling rates up to a few tens of kS/s. The ADC architectures that have medium conversion rates up to hundreds of kS/s and medium resolutions of 8-12 bits are attractive candidates for low-power sensor applications. Next, two architectures of this kind utilizing successive approximation and algorithmic approaches are briefly described, after which the concept of $\Delta\Sigma$ modulation, also exploited in the $\Delta\Sigma$-type front-end of Fig. 3.6, is presented.

3.3.1 Successive Approximation ADC

A 2-bit charge-redistribution ADC configured to sampling mode is shown in Fig. 3.8 (a) [41]. This architecture, with a moderate circuit complexity, consists of an S/H circuit, an SC digital-to-analog converter (DAC), a comparator, and a successive approximation register (SAR), together with a control logic. There is no need for any operational amplifier, which is advantageous from the power dissipation point of view. An input S/H is required to keep the signal constant during the conversion

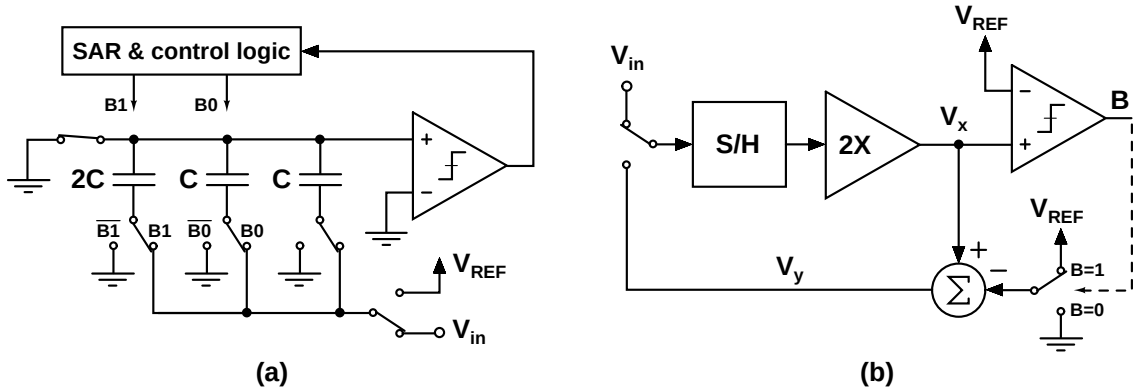


Figure 3.8: (a) 2-bit charge-redistribution SAR ADC and (b) algorithmic ADC.

cycle. The SAR and control logic perform the necessary binary search. At the beginning of the conversion the DAC output is set to midscale and the comparator compares it with the sampled input. The resulting most significant bit (MSB) is stored in the SAR and consequently, depending on the value of the MSB, the DAC output is set to either 1/4 or 3/4 scale, after which the comparator determines the second bit. For the N-bit ADC this procedure continues until all the bit values have been determined.

One bit is determined during each clock cycle, and hence the conversion time of an N-bit SAR ADC is N clock cycles. Because SAR ADCs do not suffer from latency, unlike pipeline or $\Delta\Sigma$ ADCs, they are applicable for single-shot, burst-mode, and multiplexed applications [40]. The power dissipation scales linearly with the sampling frequency. The total capacitance $C_{tot} = 2^N C$, and thus the power dissipation, is increased when the number of bits for better resolution, or the unit capacitor size for better matching, is increased. Typically, the matching of the unit capacitors of the DAC limits the ADC accuracy to 9-11 bits. Two-stage binary-weighted capacitor arrays [42], as well as C-2C ladders, can be used to reduce the total capacitance, area, and power dissipation. In the former case each array resolves $N/2$ bits and C_{tot} is reduced down to $2^{N/2+1}C$, whereas in the latter case C_{tot} increases linearly proportional to N. Regardless of N, a C-2C ladder consists of only two capacitance values, thus facilitating good capacitor matching. The need for the driving force of the reference voltage V_{REF} can be avoided by using the charge-sharing technique [43], in which the signal is processed in the charge domain. Before the conversion the capacitor array is pre-charged to the supply voltage V_{DD} and a binary scaled amount of charge is added or subtracted so that the total charge converges to zero.

3.3.2 Algorithmic ADC

An algorithmic ADC, shown in Fig. 3.8 (b) [44], is an attractive choice to meet the stringent requirements for both power dissipation and silicon area. It is based on a binary search algorithm which determines the closest digital word to match an input signal. The operating principle closely resembles that of the SAR ADC. The same hardware, consisting of an S/H circuit, a multiply-by-two operation, a comparator, and a reference subtraction circuit, is used to perform the A/D conversion in successive cycles. During each cycle, the signal is doubled, the voltage V_x is compared with the reference voltage V_{REF}, and if $V_x > V_{REF}$ then V_{REF} is subtracted from V_x. In this implementation, $-V_{REF}$ has been replaced by ground for simplicity. The voltage V_x of the i^{th} cycle can be written as [37]

$$V_x(i) = \left[2V_x(i-1) - b_i V_{REF}\right] z^{-1}, \tag{3.10}$$

where for the N-bit ADC the number of cycles $i \in [2 \ldots N]$, $V_x(1) = V_{in}$, and b_i is the i^{th} bit value (0 or 1). Accordingly, the minimum conversion time is N cycles.

In a similar way to the SAR ADC, the algorithmic structure enables a variable sampling rate and resolution to be used, together with time-multiplexed sampling. The major advantage of an algorithmic ADC over an SAR ADC is that it causes low capacitive loading for both the front-end and reference circuits [45]. In a conventional SC algorithmic ADC, the multiply-by-two operation depends on the capacitor ratios. The accuracy can be improved by using a capacitance ratio-independent technique [44]. The basic idea is to implement the multiply-by-two operation by sampling the input signal twice using the same capacitor.

3.3.3 $\Delta\Sigma$ ADC

Oversampling ADCs are based on trading off accuracy of amplitude against accuracy of time. A block diagram of the most widely used oversampling ADC, the $\Delta\Sigma$ ADC [46], followed by a digital decimation filter, is shown in Fig. 3.9. The basic first-order single-bit modulator includes a single-bit ADC (comparator), a single-bit feedback DAC (switch), and a first-order loop filter (either a CT or SC integrator). The advantage of the single-bit modulator is its inherently excellent linearity. Ignoring the noise-shaping property of $\Delta\Sigma$ ADCs for a while, within the Nyquist bandwidth the SNR is improved by 3 dB (0.5 bits) for each doubling of $K = f_S/(2f_B)$, which is called the oversampling ratio. The mean value of the output bit stream is a highly accurate representation of the instantaneous value of the relatively slowly-changing input signal. In addition to oversampling, the modulator performs a noise-shaping function by acting as a low-pass filter for the signal and a high-pass filter for the quantization noise. The quantization noise falling outside the signal bandwidth can be removed with a digital low-pass filter, after which the output data rate can be reduced back to the original sampling rate f_S by a downsampler. In the presence of both oversampling and first-order noise shaping, each doubling of K improves the SNR by 9 dB (1.5 bits).

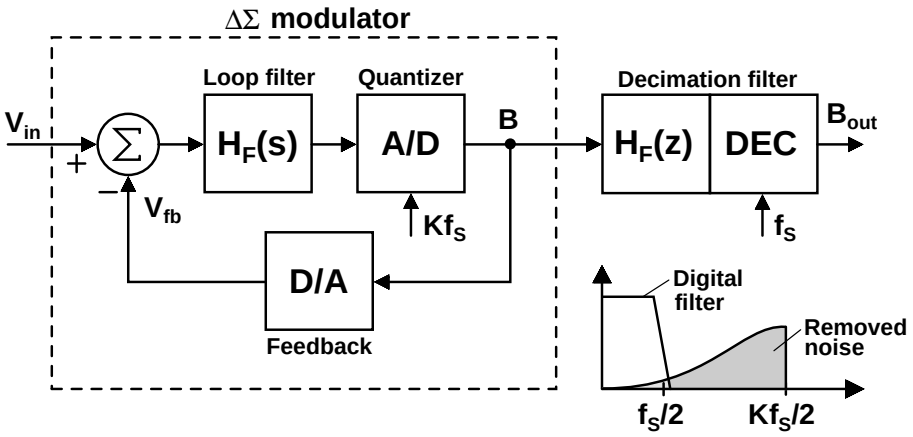


Figure 3.9: Block diagram of a $\Delta\Sigma$ modulator followed by a decimation filter. The effects of oversampling and noise shaping on the noise spectrum are also illustrated.

The $\Delta\Sigma$ architecture is an attractive alternative when very low-level signals must be digitized to high resolution, but then a higher-order structure is usually required to provide sufficient noise shaping. Noise shaping can be improved at the cost of a more complex design by increasing the number of integrators in the modulator, which corresponds to adding poles to a loop filter. In the case of second- and third-order $\Delta\Sigma$ ADCs the SNR improvements corresponding to the doubling of K are 15 dB (2.5 bits) and 21 dB (3.5 bits), respectively [37]. The implementation of higher-than-third-order modulators is challenging because of difficulties with their stabilization. An alternative way to improve the resolution is to use a multibit architecture, where a single-bit quantizer is replaced by a multi-bit counterpart, such as an N-bit flash converter, and the single-bit DAC by a highly linear N-bit DAC. Each additional quantizer bit improves the SNR by 6 dB (1 bit). $\Delta\Sigma$ converters tailored for instrumentation applications characterized by low-frequency or dc input signals are usually referred to as incremental $\Delta\Sigma$ converters. In order to enable the single-shot mode to be used, the loop filter and the decimation filter must be reset at the beginning of a conversion [36]. The decimation filter should, ideally, filter out all the quantization noise from the bitstream. Such a filter can be designed by truncating the impulse response of an ideal filter using a window function, the choice of which is a trade-off between accuracy and complexity [36]. Rectangular (sinc), triangular (sinc^2), and quadratic (sinc^3) windows can be implemented relatively easily by using counters and accumulators.

3.4 Discussion

Two low-power interface ASICs for a capacitive 3-axis micro-accelerometer were designed, implemented, and measured. Both sensor interfaces, which have been reported in detail in the publications [P4] and [P8], operate mechanically in an open loop and provide digital output. The first interface, discussed in [P4], utilizes the basic DT approach (Fig. 3.2 (c)), while the second interface, discussed in [P8], uses the DT $\Delta\Sigma$-type approach (Fig. 3.2 (d)). When using a $\pm$4-g capacitive 3-axis micro-accelerometer, the first ASIC provides 10-bit operation at a 100-Hz signal bandwidth, whereas the second ASIC provides 12-bit operation at 1- and 25-Hz signal bandwidths. The 1-Hz mode is optimized for very low power dissipation.

It is very important to consider electrostatic forces in an open-loop configuration, because they cause the reduction of the spring constant, nonlinearity, and, in extreme cases, pull-in. The effect of electrostatic forces were taken into account in the two sensor interface ASICs by utilizing an SBB-type and a $\Delta\Sigma$-type sensor front-end, respectively, both of which tend to balance the electrostatic forces. The latter front-end performs the direct C/D conversion, thus being especially suitable for low-power applications. Furthermore, the $\Delta\Sigma$ sensor front-end, characterized by both oversampling and noise-shaping functions, is particularly suitable if very small low-frequency signals must be digitized to high resolution. In both sensor interface

designs, a single front-end circuit was configured to read a 3-axis capacitive micro-accelerometer, which consists of several capacitive half-bridges, in an area-efficient way by utilizing time-multiplexing. Additionally, the elevated low-frequency noise floor caused by flicker noise was alleviated by using the CHS and CDS techniques. Both sensor front-ends have very low current consumption. The SBB-type front-end consumes 18.3 μA from a 1.8 V supply when sampling four proof masses, each at 1.04 kHz, whereas the $\Delta\Sigma$-type front-end consumes 1.1 μA or 20.0 μA from a 1.0 V supply (on-chip regulation from a 1.2-2.75-V battery voltage) when sampling three proof masses, each at 4.096 kHz (1-Hz mode) or 51.2 kHz (25-Hz mode), respectively.

ADCs are required in most modern sensor systems to provide digital outputs and to enable some form of DSP, such as filtering and decimation, to be used. The ADC architectures with both medium conversion rates and resolutions, such as SAR and algorithmic ADCs, are particularly suitable candidates for low-power sensor interfaces. The first interface ASIC included two 12-bit ratio-independent algorithmic ADCs [45, 47]. In addition to converting the acceleration information into the digital domain, the same kind of ADC was configured to provide a digital temperature reading. The ADC enables a variable sampling rate and resolution to be adopted, together with time-multiplexed sampling, and causes low loading for the front-end and voltage reference. The ADC is very compact, occupying just 0.04 mm^2, and it consumes only 5.5 μA and 1.7 μA from a 1.8 V supply thanks to reduced duty cycles of 10% and 0.3% that are used here when the acceleration and temperature information are converted into the digital domain, respectively. The second sensor interface ASIC, which performs the direct C/D conversion, avoids the need for an explicit ADC subsequent to the sensor front-end.

Implementing fully-integrated sensor interface ASICs requires different kinds of reference (e.g., current, voltage, temperature, frequency) and power management circuits. To make battery-powered operation possible, in [P8] the system-on-chip (SoC) power management is provided by using low-dropout (LDO) linear regulators. The next three chapters are devoted to the fundamentals and low-power design issues related to current, voltage, and temperature references (Chapter 4), frequency references (Chapter 5), and supply voltage regulators (Chapter 6), respectively.

4 Current, Voltage, and Temperature References

Current and voltage references are an essential part of most electrical systems. Actually, current references are intrinsic components of voltage references as well. Voltage references are required, for example, to define the input and output full-scale range of ADCs and DACs, respectively. Temperature references, or temperature sensors, are very similar circuits compared to voltage references, and they can be used as a part of the interface electronics for the compensation of temperature-dependent non-idealities. This chapter starts by describing the characteristics of a base-emitter voltage of a bipolar transistor, on which the operation of current, voltage, and temperature references relies in most cases. After that the corresponding reference circuits are discussed in more detail in that order.

4.1 Bipolar Transistor Characteristics

Low-cost digital CMOS processes provide two types of parasitic bipolar transistors, namely lateral pnp transistors and substrate (vertical) pnp transistors, which are by-products of the MOS transistors. Usually, these parasitic transistors have worse properties than their counterparts in bipolar processes, such as lower current gain $\beta = I_C/I_B$ and higher base resistance R_B. The main disadvantage of a lateral pnp transistor is an associated parasitic substrate pnp transistor, because of which at least 20-40% [36] of the total emitter current flows vertically into the substrate rather than laterally into the collector, thus causing very non-ideal I_E–V_{BE} characteristics. Thanks to their more ideal behavior and lower sensitivity to stress, substrate pnp transistors are preferred when voltage or temperature references are being implemented in the CMOS technology [48].

4.1.1 Base-Emitter Voltage

The collector current of a pnp transistor in its forward-active region, when the Early effect is neglected, is given by

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right), \tag{4.1}$$

where I_S is the saturation current of a transistor, V_{BE} the base-emitter voltage[1], and V_T the thermal voltage (≈25.8 mV at 300 K). The thermal voltage is given by $V_T = kT/q$, where k is the Boltzmann's constant, T the absolute temperature,

[1]In the literature, the symbols V_{BE} and ΔV_{BE} are often also used for pnp devices, though strictly speaking V_{BE} should be replaced by either $|V_{BE}|$, or V_{EB}. The same sign convention is used in this thesis.

and q the electron charge ($1.602 \cdot 10^{-19}$ C). The strongly temperature-dependent saturation current can be expressed as [49]

$$I_S = CT^{\eta} \exp\left(-\frac{V_{g0}}{V_T}\right), \tag{4.2}$$

where C is a temperature-independent constant, η a process-dependent constant approximately between 3.6 and 4 [50], and V_{g0} the bandgap voltage of silicon linearly extrapolated down to 0 K (≈1.206 V).

Solving (4.1) with respect to V_{BE}, assuming the temperature coefficient of the collector current to be m, i.e., $I_C \propto T^m$, and using the expression (4.2) for I_S, the temperature dependence of V_{BE} can be shown to be of the well-known form [49]

$$V_{BE} = V_{g0} - [V_{g0} - V_{BE}(T_r)]\frac{T}{T_r} - (\eta - m)\, V_T \ln\left(\frac{T}{T_r}\right), \tag{4.3}$$

where T_r is the reference temperature. The temperature dependence of V_{BE}, together with its linear approximation, is illustrated in Fig. 4.1 (a). The typical temperature coefficient (TC) of V_{BE} is in the order of –2 mV/°C. The non-linearity, or curvature, caused by the factor $\ln(T/T_r)$ is roughly parabolic and it amounts to a few millivolts for CMOS substrate pnp transistors when biased at a proportional-to-absolute temperature (PTAT) current [51]. When designing accurate references

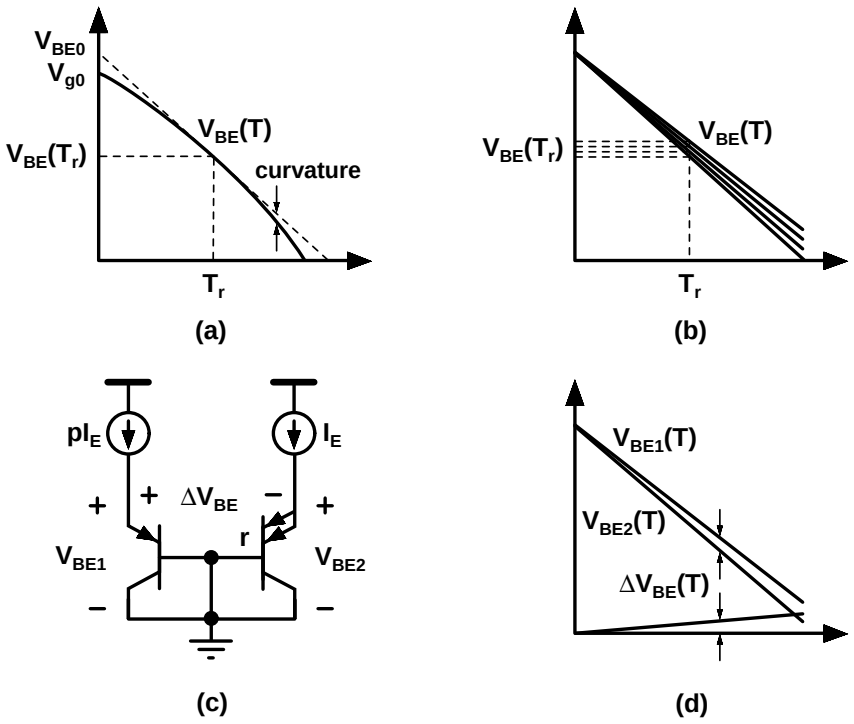


Figure 4.1: (a) Temperature dependence of V_{BE} and its linear approximation; (b) variation of V_{BE} as a result of process spread; (c) generation of ΔV_{BE} using diode-connected substrate pnp devices, and (d) temperature dependence of ΔV_{BE}.

it may be useful to perform the Taylor series expansion about the reference temperature T_r for the logarithmic term of (4.3), which changes both the temperature-independent and linear components. As a result, the base-emitter voltage can be expressed as $V_{BE} = V_{BE0} - \lambda T - c(T)$, where V_{BE0} corresponds to the base-emitter voltage at 0 K, λ is the slope of the tangent, and $c(T)$ the curvature [36].

4.1.2 Base-Emitter Voltage Difference

A single base-emitter voltage, as illustrated in Fig. 4.1 (b), is not so reproducible because the process variations can cause V_{BE} to spread by as much as 10 mV [48] at the reference temperature T_r. The difference between two base-emitter voltages, V_{BE1} and V_{BE2}, generated with two different collector current densities, can be used to largely eliminate that problem. The two diode-connected substrate pnp transistors shown in Fig. 4.1 (c) produce

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln\left(\frac{pI_C}{I_S}\right) - V_T \ln\left(\frac{I_C}{rI_S}\right) = V_T \ln(pr), \tag{4.4}$$

where p and r correspond to the collector current ratio I_{C1}/I_{C2} and the base-emitter junction area ratio A_{E2}/A_{E1} of the two pnp transistors, respectively. The larger pnp device is assumed to be made of a parallel combination of r smaller devices. Provided that p is constant, ΔV_{BE} is independent of process parameters, as well as the absolute values of the collector currents. In other words, ΔV_{BE} is very reproducible and suitable for use for integrated reference circuits. In order to ensure that ΔV_{BE}, shown in Fig. 4.1 (d), is accurately PTAT, the current gains $\alpha = I_C/I_E$ of the diode-connected substrate pnp devices must be independent of the current levels used [36].

4.1.3 Non-idealities in Base-Emitter Voltage

In addition to the curvature in its temperature dependence, the base-emitter voltage suffers from other non-idealities as a result of, among other factors, series resistances, process variations, and mechanical stress. In the case of substrate pnp transistors, which have low current gains and high base resistances, the effective resistance in series with the emitter is typically a few tens of Ohms and it is dominated by the base resistance [36]. Generally, the effect of series resistances can be alleviated by reducing the current levels, by using larger unit devices, or, alternatively, by exploiting one of the compensation techniques presented in [36]. The influences of non-zero base-collector and base-emitter voltages are called the forward and the reverse Early effects, respectively. The modeling of the reverse Early effect is particularly important when accurate voltage references and temperature sensors with an analog output are being designed. In the case of digital temperature sensors utilizing the ratiometric temperature measurement principle, the multiplicative error

resulting from the reverse Early effect is canceled [36].

When a biasing resistor R is used to determine the emitter current of a pnp transistor, the base-emitter voltage can be expected to deviate from its ideal value as a result of process variations in the current gain α, the biasing resistance R, and the saturation current I_S. When the relative errors of these parameters themselves are assumed to be temperature-independent, the resulting error voltages in V_{BE} are then either PTAT or complementary-to-absolute temperature (CTAT) in nature [49]. Such a PTAT spread causes the V_{BE} curve to rotate around the fixed point V_{BE0} at 0 K, as illustrated in Fig. 4.1 (b). Therefore, a calibration at only one temperature is sufficient for a PTAT correction [36]. The voltage-mode PTAT correction can be performed in discrete steps by adjusting a programmable resistor array in series with the emitter, or continuously by using laser trimming. The correction can also be performed in the current domain by trimming the bias current or the emitter area, the latter approach not being as practical, since the voltage drops across the switches in series with the emitters add directly to the base-emitter voltages. Because silicon and packaging materials have different thermal expansion coefficients, packaging exposes the whole die to mechanical stress that depends on both temperature and time [52]. The stress-induced changes in I_S directly affect V_{BE}, while ΔV_{BE} is insensitive to stress at moderate current levels [36], provided that the stress affects both devices equally. In order to provide accurate trimming, first, a wafer-level trimming can be performed to correct the errors resulting from process variations, and then, after packaging, the errors resulting from package-induced stress can be partially trimmed out.

A mismatch in the current density ratio of the two substrate pnp devices, i.e., pr in the case of Fig. 4.1 (c), affects the accuracy of the PTAT voltage given in (4.4). Using precision layout techniques, it is possible to achieve 0.1% matching, which is clearly insufficient for certain applications, such as precision temperature sensors [36]. Fortunately, these mismatches can be reduced to almost zero on average by utilizing the so-called dynamic element matching (DEM) technique [53], in which unit current sources and/or unit bipolar devices are dynamically interchanged. Consequently, the first-order errors are canceled in the average of the base-emitter voltages. In addition to providing a timing scheme for the required switches, a low-pass filter is required to filter out the dynamic error signals superimposed on the average base-emitter voltage as a result of switching. Generally, in order to average out the first-order mismatch of both current sources and bipolar devices, a total of $(p+1)(r+1)$ DEM steps is required.

4.2 Current References

Most voltage and temperature references require one or several current references, which have a well-characterized and controlled temperature behavior. In this sec-

tion, basic current reference circuits with different temperature behaviors will be presented. Furthermore, some start-up circuits required to prevent the zero-current state of current references will be described.

4.2.1 PTAT Current References

The most commonly used current reference is a proportional-to-absolute temperature (PTAT) current reference, which is practical, predictable, and linear over a wide range of currents [49]. In addition to the need for analog circuits, like voltage and temperature references, they are useful for biasing amplifiers with bipolar or subthreshold MOS input pairs, because the temperature dependence of their transconductance ($g_m = I_C/V_T$) can effectively be canceled. As a result, the gain-bandwidth product (GBW) of the amplifier becomes independent of the temperature.

Three basic PTAT current reference topologies are shown in Fig. 4.2. The structure (a) requires the use of npn devices, and therefore it cannot be integrated in a standard CMOS process, unlike the structures (b) and (c). In order to provide an exponential I_D–V_{GS} characteristic in the circuit configuration (b), the n-channel MOS (NMOS) transistors M_1 and M_2 must operate in the subthreshold (i.e., $V_{GS} < V_{TH}$). In the simplest implementation of (c), the operational amplifier can be replaced by a common-gate amplifier. This kind of approach is applicable if the accuracy of a PTAT current does not degrade too much as a result of the channel-length modulation of the NMOS devices that are required. A proportional-to-square-of-absolute temperature ($PTAT^2$) current reference can be useful for the cancelation of the second-order temperature dependence in the precision curvature-corrected voltage references. All-MOS implementations of a PTAT and a $PTAT^2$ current reference

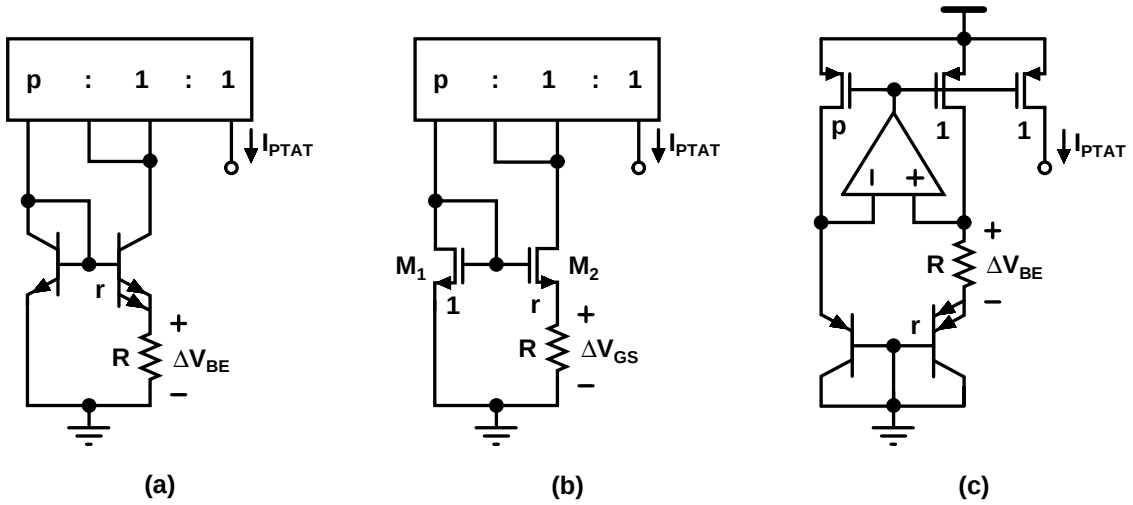


Figure 4.2: PTAT current references based on the use of (a) npn devices; (b) subthreshold NMOS devices, and (c) substrate pnp devices.

with low-voltage capability for sub-1-V operation have been reported in [54] and [55], respectively.

Ideally, all the three topologies shown in Fig. 4.2 output the same reference current. In the structures (a) and (c), the difference in base-emitter voltage given in (4.4) is forced across the resistor, thus resulting in

$$I_{PTAT} = \frac{\Delta V_{BE}}{R} = \frac{V_T}{R} \ln (pr) \,. \tag{4.5}$$

In practice, because of the temperature dependence of the biasing resistor, this current is not accurately PTAT. In the case of the structure (b), ΔV_{GS} is utilized instead of ΔV_{BE}. It must be noted that in subthreshold operation leakage currents may overwhelm the drain current at moderately high temperatures. According to (4.5), the PTAT current references have high immunity against variations in the supply voltage. Assuming that M_1 and M_2 in Fig. 4.2 (b) operate in strong inversion saturation (i.e., $V_{GS} > V_{TH}$ and $V_{DS} \geq V_{DS,sat}$) with equal drain currents ($p = 1$), channel-length modulation is negligible, and the body effect of M_2 is neglected, the output current can be expressed as [56]

$$I_{REF} = \frac{2}{\mu_n C_{ox} (W/L)_1 R^2} \left(1 - \frac{1}{\sqrt{r}}\right)^2 , \tag{4.6}$$

where μ_n is the electron mobility, C_{ox} the gate-oxide capacitance per unit area, and r the ratio $(W/L)_2 / (W/L)_1$. Accordingly, the reference current is still fairly independent of the supply voltage, but it depends more heavily on the process when compared to its PTAT counterpart. In practice, the structure (b) suffers from the body effect as a result of a non-zero bulk-source voltage of M_2, which can be eliminated by converting the structure into its p-channel MOS (PMOS) counterpart and tying the source and bulk terminals of each PMOS device.

Because the nominal values of the current gain decrease with every new process generation, the effect of finite β increases and the resulting errors must be considered carefully, especially in precision references. Figure 4.3 (a) shows a modified PTAT current reference utilizing the resistor R/p in series with the base of Q_1 [57]. As a result, the PTAT current becomes proportional to $(\beta + 1)/\beta$ which cancels the current gain dependence of V_{BE3}. Compared to the compensation technique presented in [58], in which the base current of an auxiliary substrate pnp is added to the emitter current of the primary substrate pnp, the modified PTAT current reference is much more effective, particularly at lower current gains, and is suitable for low-voltage applications [36].

4.2.2 CTAT Current References

A complementary-to-absolute temperature (CTAT) current reference is often needed when implementing a first-order temperature-independent current reference, as well

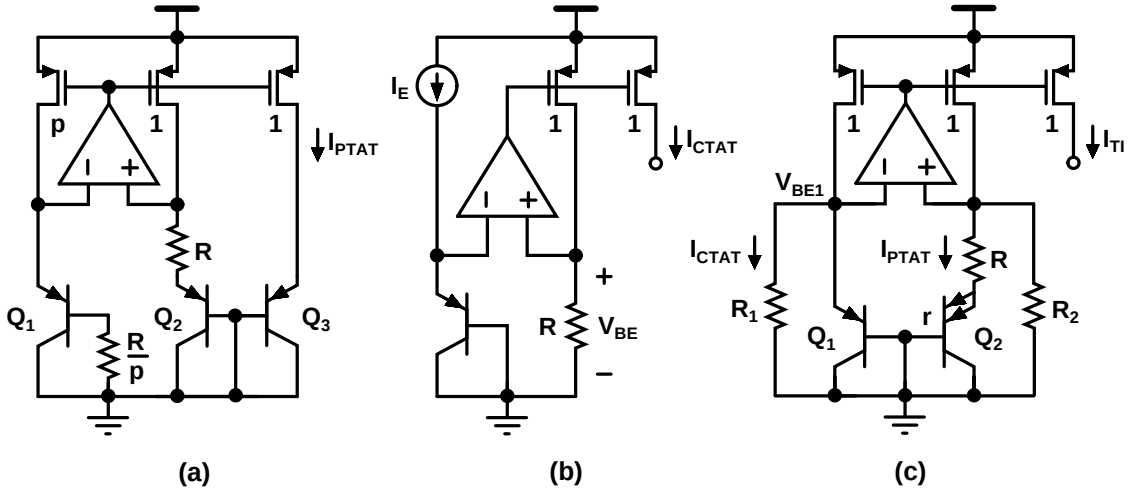


Figure 4.3: (a) Modified PTAT current reference for the compensation of the finite current gain; (b) CTAT current reference, and (c) TI current reference.

as a curvature-corrected voltage reference. Figure 4.3 (b) shows a CTAT current reference based on the use of a single substrate pnp. The base-emitter voltage is forced across the resistor by using an operational amplifier, and the resulting output current is of the form

$$I_{CTAT} = \frac{V_{BE}}{R} = \frac{V_T}{R}\ln\left(\frac{I_C}{I_S}\right). \tag{4.7}$$

In order to guarantee the forward-active region of the pnp device, the current $I_E = I_C/\alpha$ must be greater than I_{CTAT} under all operating conditions. The non-linear effects of V_{BE} can be reduced by choosing I_E to be PTAT in nature [49]. Because of the spread in both I_S and R, a CTAT current is less reproducible than a PTAT current.

4.2.3 TI Current References

A first-order temperature-independent (TI) current reference can be constructed by appropriately summing a CTAT current to a PTAT current. Such a CMOS-compatible current reference is shown in Fig. 4.3 (c) [59]. A PTAT current is generated by forcing ΔV_{BE} across the resistor R, while a CTAT current is generated by forcing V_{BE1} across the resistor R_1, which is nominally equal to R_2. The output current appears as the sum of these two currents. When the effect of finite current gain is neglected, the output current becomes

$$I_{TI} = I_{PTAT} + I_{CTAT} = \frac{\Delta V_{BE}}{R} + \frac{V_{BE1}}{R_{1,2}} = \frac{V_T}{R}\ln(r) + \frac{V_T}{R_{1,2}}\ln\left(\frac{I_{PTAT}}{I_{S1}}\right). \tag{4.8}$$

The resistance values R and $R_{1,2}$ are used to correctly proportion the magnitudes of the PTAT and CTAT currents, respectively. Another approach to generating a TI

current reference is simply to force a temperature-independent voltage, generated by a voltage reference, across a resistor.

4.2.4 Start-Up Circuits

Current references have an additional stable operating point that corresponds to the zero-current state. Therefore, a start-up circuit is required to prevent this undesirable state. Two optional continuous-current start-up circuits, namely a current source M_1 and a current sink M_2, are shown in Fig. 4.4 (a). In order not to significantly degrade the PTAT nature of the main currents, a small amount of start-up current, $I_{start\text{-}up} \ll I_{PTAT}$, is either sourced or sunk into or from a low-impedance node, n1 or n2, respectively.

A discontinuous-current start-up circuit shown in Fig. 4.4 (b) [49] is preferred because it does not disturb the operation of the core circuit and it consumes less quiescent current. This start-up circuit senses the state of the current reference by sinking $I_{start\text{-}up}$ only when the core circuit is approaching the zero-current state. The state of the core circuit is monitored by comparing the constant-current sink I_{sink}, which flows through M_2, with I_{PTAT} mirrored from the core circuit. In order to provide the desired operation, in the steady state I_{sink} must be below I_{PTAT} under all operating conditions. Thus, in the off-state the high-impedance node n3 is pulled low and M_1 starts to sink $I_{start\text{-}up}$ from the node n2, thus setting the core circuit to work. When the core circuit achieves the right operating state, the node n3 is pulled high and $I_{start\text{-}up}$ through M_1 is disabled. The capacitor C is included to slow down voltage transitions on n3, thus filtering transient noise [49].

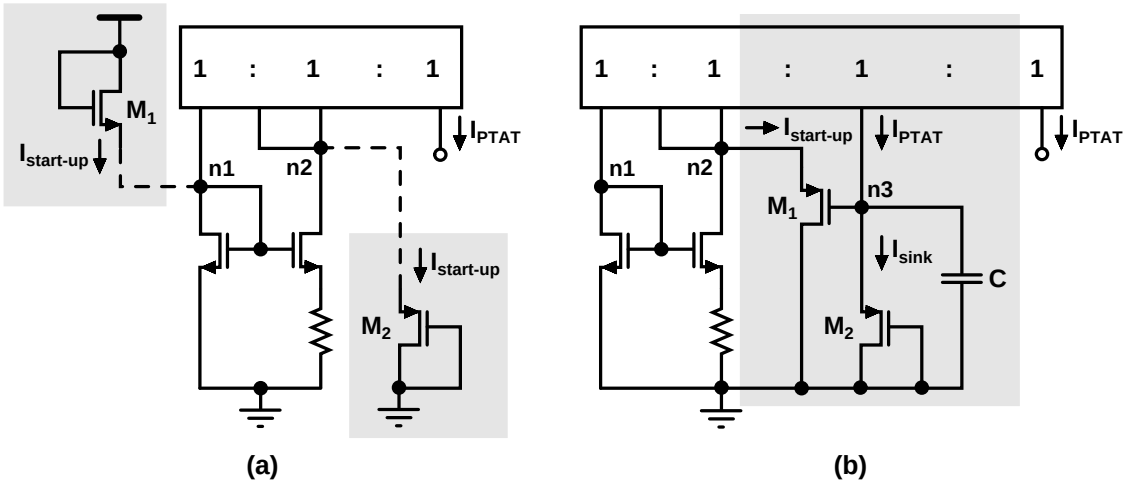


Figure 4.4: (a) Two optional continuous-current start-up circuits: current source M_1 and current sink M_2; and (b) discontinuous-current start-up circuit.

4.3 Voltage References

Voltage references can be categorized on the basis of the temperature compensation attempt they use. Temperature-uncompensated Zener and forward-biased diodes fall into the zero-order category. First-order references compensate for the linear term of the temperature dependence of the base-emitter voltage given in (4.3), while second- and higher-order references, which are called curvature-corrected references, compensate for linear and one or more higher-order temperature components, respectively. The voltage references that are based on forward-biased diodes and utilize temperature compensation are commonly referred to as bandgap references, because their output voltage typically approaches V_{g0}. Hilbiber introduced the first bandgap reference in 1964 [60], and this was followed by Widlar's seminal work in 1971 [61]. Next, the concept of the first-order voltage reference and several such circuit topologies will be presented. After that different curvature correction techniques to compensate for the systematic error of the base-emitter voltage resulting from temperature will be presented. Finally, other non-idealities than temperature dependence related to voltage references will be discussed.

4.3.1 First-Order Voltage References

Generally, first-order temperature compensation can be realized in a voltage reference by summing properly scaled base-emitter and PTAT voltages, i.e.,

$$V_{REF} = \alpha_1 V_{BE} + \alpha_2 V_T \ln(pr), \tag{4.9}$$

where α_1 and α_2 are gain factors, and p and r correspond to the collector-current and emitter-area ratios of two bipolar transistors, respectively. The principle of the traditional first-order bandgap voltage reference with $\alpha_1 = 1$ is illustrated in Fig. 4.5 (a). In order to provide first-order temperature compensation, the second term of (4.9) must cancel the linear term of (4.3), which is denoted here by $-\lambda T$. Hence, the gain factor α_2 must be chosen to be such that

$$\alpha_2 = \frac{\lambda q}{k \ln(pr)}. \tag{4.10}$$

Assuming λ is approximately 2.2 mV/°C, the value of α_2 ranges roughly from 9 to 23 with typical current density ratios between 3 and 16 [36]. Consequently, the first-order temperature-compensated output voltage is close to 1.2 V and the minimum supply voltage of such bandgap structures is limited to roughly 1.4 V ($V_{DD,min} = V_{REF} + V_{DS,sat}$).

Ideally, the resulting reference voltage is dominated by the residual second-order temperature dependence of V_{BE} and its maximum appears at the reference temperature T_r, as illustrated in Fig. 4.5 (b). The effectiveness of the temperature

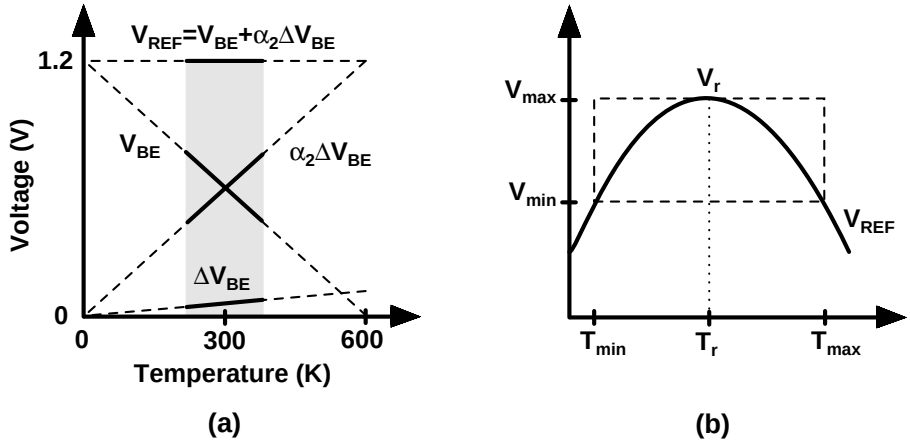


Figure 4.5: (a) Principle of the first-order bandgap voltage reference and (b) the residual second-order temperature dependence of the reference voltage.

compensation method used is typically expressed with the residual TC of the reference voltage in units of ppm/°C. This TC is usually calculated with the so-called box method, i.e.,

$$TC = \frac{V_{max} - V_{min}}{V_r \left(T_{max} - T_{min}\right)} \cdot 10^6, \tag{4.11}$$

where V_r is the output voltage at the reference temperature. The temperature dependence of first-order bandgap references typically ranges from 20 to 100 ppm/°C [49].

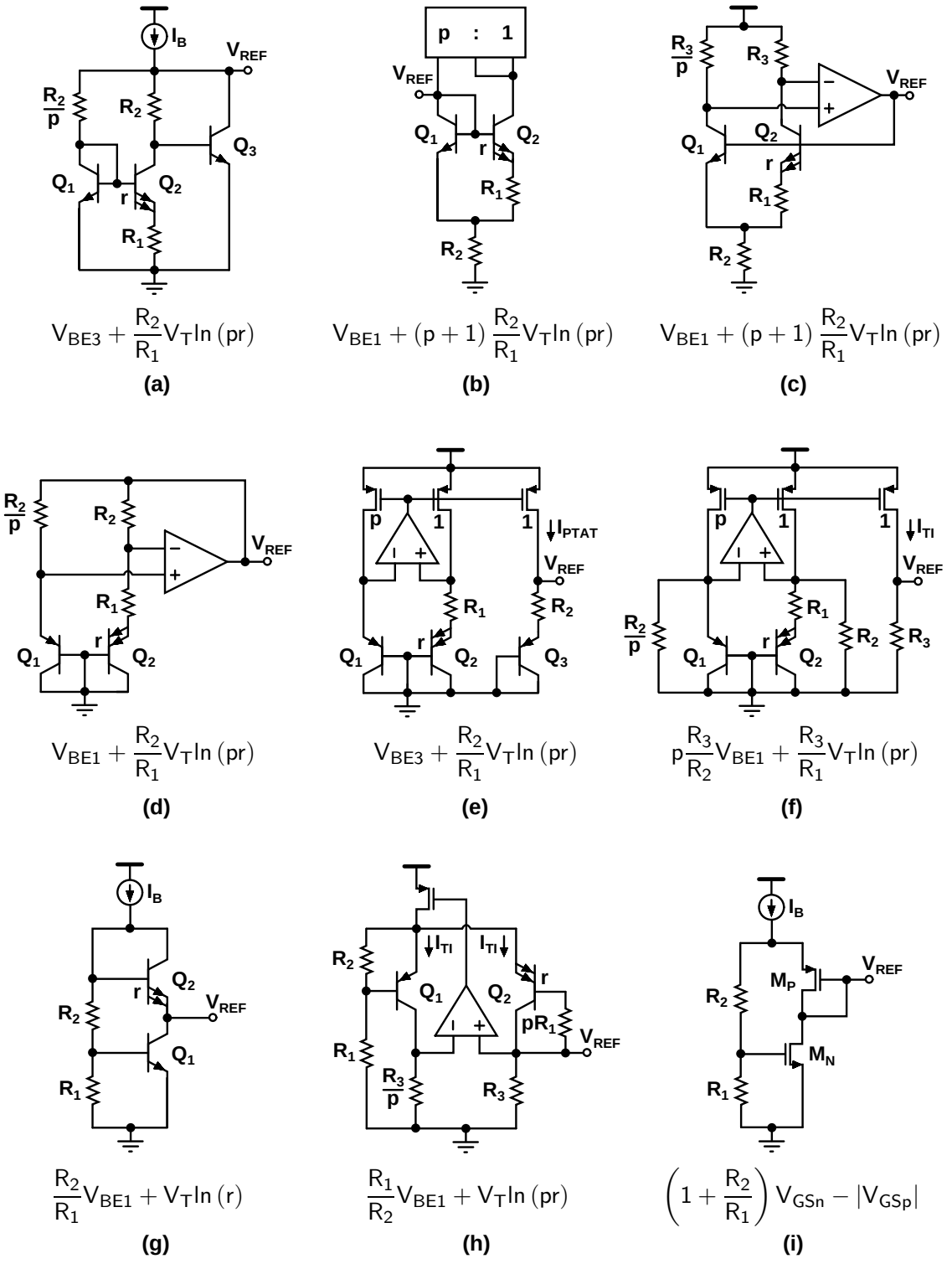
The same kind of temperature behavior can also be achieved by using subthreshold MOS devices, since, when biased with a fixed drain current, their gate-source voltage decreases linearly with temperature [62]. In that case V_{BE} is replaced by V_{GS} in (4.9). Another way to implement voltage references with MOS devices is based on exploiting the different temperature dependencies of the threshold voltages between an NMOS and a PMOS device [63]. Next, different types of first-order voltage references, shown in Fig. 4.6 together with their output voltage expressions, are presented.

A. Bipolar Bandgap References

Three basic first-order bipolar bandgap references proposed by Widlar [61] and Brokaw [64] are shown in Figs. 4.6 (a)-(c). All these topologies require the use of npn bipolar devices, they inherently include a PTAT current reference, their gain factor α_1 equals one, and the optimal TC can be achieved with the gain factor α_2 given in (4.10). Brokaw bandgap cell can be used either without or with an operational amplifier in the feedback loop, as shown in (b) and (c), respectively.

B. CMOS Bandgap References

The first-order bandgap references shown in Figs. 4.6 (d) and (e) can be implemented with substrate pnp devices, and are thus more useful than the structures (a)-(c).



$V_{BE3} + \frac{R_2}{R_1} V_T \ln(pr)$ **(a)**

$V_{BE1} + (p+1)\frac{R_2}{R_1} V_T \ln(pr)$ **(b)**

$V_{BE1} + (p+1)\frac{R_2}{R_1} V_T \ln(pr)$ **(c)**

$V_{BE1} + \frac{R_2}{R_1} V_T \ln(pr)$ **(d)**

$V_{BE3} + \frac{R_2}{R_1} V_T \ln(pr)$ **(e)**

$p\frac{R_3}{R_2} V_{BE1} + \frac{R_3}{R_1} V_T \ln(pr)$ **(f)**

$\frac{R_2}{R_1} V_{BE1} + V_T \ln(r)$ **(g)**

$\frac{R_1}{R_2} V_{BE1} + V_T \ln(pr)$ **(h)**

$\left(1 + \frac{R_2}{R_1}\right) V_{GSn} - |V_{GSp}|$ **(i)**

Figure 4.6: First-order voltage references together with their output voltage expressions. (a)-(c) Bipolar bandgap references [61, 64]; (d)-(e) CMOS-compatible bandgap references [65, 56]; (f) purely current-mode CMOS-compatible sub-1-V bandgap reference [59]; (g) bipolar and (h) CMOS-compatible bandgap reference based on RBVP [66, 67], and (i) CMOS voltage reference based on weighted ΔV_{GS} [63].

Similarly to (a)-(c), the topology (d) proposed by Kuijk [65] is based on the use of an inherent PTAT current reference. In contrast, the bandgap reference (e) uses a separate PTAT current reference and a bandgap output stage consisting of R_2 and Q_3 [56]. The output voltage expressions of the circuit configurations (d) and (e) are of the same general form as those of the circuits (a)-(c).

C. Sub-Bandgap References

As a result of single battery-cell operation, as well as lower breakdown voltages, many structures have been proposed to manage with low supply voltages down to roughly 1 V. These circuits are often called sub-1-V voltage references. The purely current-mode CMOS-compatible sub-1-V bandgap reference proposed by Banba et al. [59], shown in Fig. 4.6 (f), uses a TI current reference and the resistor R_3. The advantage of this topology is that a fraction of the traditional bandgap voltage of 1.2 V can be achieved by scaling both terms of (4.9) by resistor ratios, i.e., $\alpha_1 \neq 1$ and $\alpha_2 \neq 1$. From the operational amplifier design point of view, in order to manage with the low supply voltages, the input common-mode voltage levels can be scaled down by replacing R_2 and R_2/p by resistive voltage dividers [68].

Lin et al. presented the bipolar bandgap reference shown in Fig. 4.6 (g) in [66]. That structure generates a first-order temperature-compensated sub-1-V output. It is based on the reverse bandgap voltage principle (RBVP), realized by using a V_{BE1} multiplier and a subtraction of V_{BE2}. In contrast to the basic bandgap references (a)-(e), in (4.9) V_{BE} is scaled instead of $V_T \ln(pr)$, in which case $\alpha_1 \approx 1/6$ and $\alpha_2 = 1$ [67]. As a result, the output voltage is of the order of 200 mV. The main drawback of this circuit is that the key transistor Q_1 operates in the deep saturation region, in which slight changes in the collector-emitter voltage significantly affect the base current. Sanborn et al. proposed a CMOS-compatible sub-1-V voltage reference [67], shown in Fig. 4.6 (h), which also utilizes the RBVP technique. Though lateral pnp devices must be used instead of substrate pnps, good overall performance has been reported in [67]. As opposed to the structure (g), this circuit does not suffer from the mismatch between the collector currents of Q_1 and Q_2 resulting from the Early effect. The resistor pR_1 is added to cancel the error resulting from the base current of Q_1 through R_1.

D. Other CMOS Voltage References

Figure 4.6 (i) shows a simple CMOS-compatible voltage reference presented by Leung et al. in [63]. Both the MOS devices should operate in the saturation region and their channel-length modulation effect should be minimized. The temperature drifts of V_{THn} and V_{THp}, the magnitudes of which decrease linearly with temperature, are mutually compensated. The linear and non-linear terms of the derivative of the output voltage with respect to temperature can be set to zero by certain resistor and transistor ratios, respectively. Because the temperature dependence of the threshold voltage is not perfectly linear and the temperature dependence of the electron and hole mobility cannot completely be canceled over the entire temperature range, a

non-linear temperature-dependent error voltage appears at the output [63]. Sub-1-V operation can be achieved by using this topology with low-V_{TH} devices. Another way to implement a low-power purely CMOS voltage reference is to use subthreshold MOSFETs, as demonstrated in [62].

4.3.2 Curvature Correction Techniques

The temperature drift of first-order voltage references may become a problem in some high-performance systems, for instance in precision temperature sensors [36]. Additionally, the requirements for battery-powered operation, i.e, a low quiescent current flow and low-voltage operation, increasingly impose stringent specifications on integrated references. Hence there is a growing need for higher-order curvature-corrected references. Various approaches to compensate for [49, 50, 69, 70, 71], or even fully cancel [49, 72, 73], the non-linear term of (4.3) have been proposed. Typically, the TCs of curvature-corrected bandgap references extend from 1 to 20 ppm/°C. Next, different types of curvature correction techniques will be briefly discussed.

A. Second-Order Correction

The non-linear temperature-dependent characteristics of V_{BE} can be compensated for by summing an artificially generated non-linear voltage component to the first-order voltage reference. The idea of the second-order bandgap reference and the third-order residual temperature dependence of the resulting reference voltage are shown in Figs. 4.7 (a) and (b), respectively. One realization example of such a curvature correction is shown in Fig. 4.8 (a) [49]. The basic Brokaw bandgap cell is modified by splitting the resistor R_2 shown in Fig. 4.6 (b) into two parts, R_2 and R_3, and by forcing a $PTAT^2$-type current to flow through R_3. The second-order

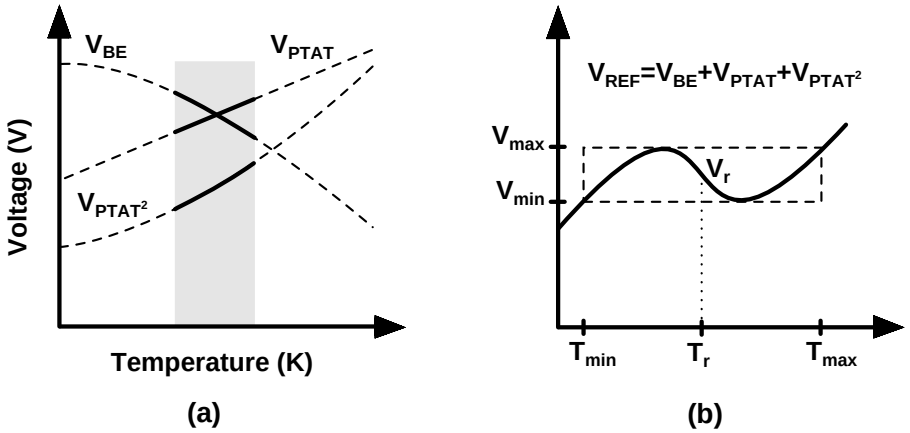


Figure 4.7: (a) Voltage components required for the second-order bandgap voltage reference, and (b) the residual third-order temperature dependence of the resulting reference voltage.

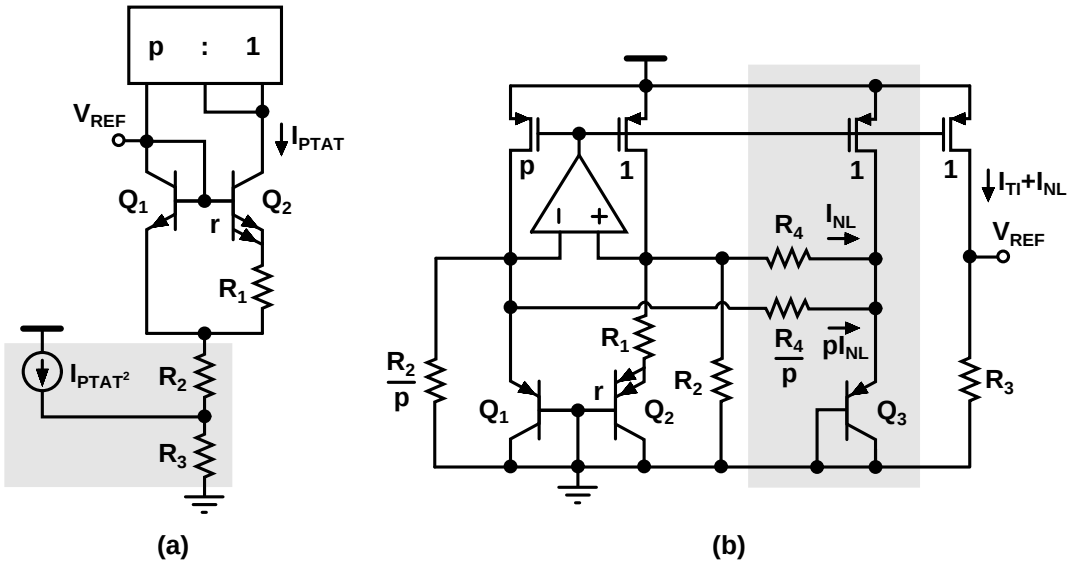


Figure 4.8: (a) Second-order and (b) higher-order curvature-corrected bandgap reference.

curvature-corrected reference voltage thus becomes

$$V_{REF} = V_{BE1} + (p+1)\frac{(R_2+R_3)}{R_1}V_T \ln(pr) + R_3 I_{PTAT^2}. \tag{4.12}$$

The last term partially cancels the negative temperature dependence of the logarithmic term of the base-emitter voltage. Alternatively, a second-order bandgap reference can be implemented by exploiting the temperature-dependent resistor ratio technique [49], in which the ratio of $R_{\text{type-2}}/R_{\text{type-1}}$ should be roughly linearly positive. The disadvantages of this simple technique are the large mismatch between the two types of resistors and a strong dependence on a given process technology.

B. Exponential and Piecewise-Linear Correction

Higher performance can be achieved if the correcting term is designed to match the nonlinearity of the diode (i.e., $T\ln(T)$) better. In [69], the so-called β compensation scheme, which is based on the exponential temperature dependence of the forward-current gain of npn devices, $\beta \propto e^{-1/T}$, is presented. This technique is based on the use of a base current as the curvature correction source, and it does not need any extra circuitry compared to the first-order bandgap reference structure, unlike the second-order bandgap references. A good overall performance can be achieved with low quiescent currents, but the minimum supply voltage is restricted to roughly 1.5 V. Moreover, the process variations in the reference voltage will increase as a result of variations in β [36]. A curvature-corrected bandgap reference based on a piecewise-linear current-mode technique is proposed in [71]. The non-linear current component I_{NL} is practically zero in the lower half of the temperature range, within which the circuit operates like a first-order bandgap reference, while it increases non-linearly in the upper half of the temperature range. The temperature-dependent

currents are summed in the output stage.

C. Higher-Order Correction

The curvature correction is further improved theoretically if the non-linear term itself is derived from a diode voltage. A higher-order bandgap reference, proposed in [73], can provide an accurate reference voltage with a potentially low quiescent current flow; however, this is at the expense of a supply voltage higher than roughly 4 V as a result of stacking multiple base-emitter voltages. Another exact bandgap reference is presented in [49]. In contrast to the implementation of [73], the TC of the reference voltage is exactly canceled for any non-integer value of the process-dependent parameter η. The minimum supply voltage of that structure is only moderate, roughly 1.8 V.

A simple yet effective low-voltage curvature-corrected bandgap reference, which is based on the current-mode topology shown in Fig. 4.6 (f) and the use of a temperature-dependent bias current ratio, is shown in Fig. 4.8 (b) [72]. Compared to the basic temperature-uncompensated version, only one additional current branch, including Q_3, and the resistors R_4 and R_4/p are required. The basic idea behind this curvature correction scheme is to correct the non-linear term by the proper combination of two base-emitter voltages, of which one is defined by using a temperature-independent current ($m = 0$) and the other by using a PTAT current ($m = 1$). As a result, the non-linear voltage V_{NL} proportional to $V_T \ln(T/T_r)$ is forced through the resistors R_4 and R_4/p, thus leading to the non-linear current flow $I_{NL} = V_{NL}/R_4$ between the branches. This circuit configuration results in an output voltage of the form

$$V_{REF} = R_3 \left[p\frac{V_{BE1}}{R_2} + \frac{V_T \ln(pr)}{R_1} + \frac{V_{NL}}{R_4} \right] \tag{4.13}$$

$$= p\frac{R_3}{R_2} \left[V_{BE1} + \frac{1}{p}\frac{R_2}{R_1} V_T \ln(pr) + (\eta - 1) V_T \ln\left(\frac{T}{T_r}\right) \right], \tag{4.14}$$

where the choice of $R_4 = R_2/[p(\eta - 1)]$ cancels the non-linearity of the base-emitter voltage V_{BE1}. Quite a similar curvature correction method based on a diode-voltage loop is presented in [50]. However, that technique is more complex and it consumes more quiescent current.

4.3.3 Non-ideal Effects

A. Parasitic Error Sources

Most voltage reference circuits adopt a voltage-mode output stage, in which the base-emitter voltage is used directly in series with the output. In this simple way, additional errors are not introduced [49]. The parasitic errors, such as the mismatch of the resistors and finite output resistance of the transistors, affect both the absolute value and the TC of the reference voltage. If it is assumed that the error

sources themselves are temperature-independent, they cause PTAT spread. For example, in the case of a typical bandgap cell shown in Fig. 4.6 (b), the tolerance and temperature coefficients of the resistors affect the base-emitter voltage only, and the mismatch of the resistors affects the PTAT voltage only, whereas current mirror mismatch, bipolar mismatch, and the Early effect affect both of them [49]. Depending on the resistor material used, as well as the physical layout properties, the resistor mismatch can extend from 0.1 to 5%, whereas the current mirror mismatch can range from 0.5 to 5%, depending on the current mirror configuration [49]. The mirroring accuracy can be improved by increasing the output resistance of the mirror. On the basis of the discussion in Section 4.1.3, series resistances, process variations in α and I_S, and mechanical stress also affect the achievable accuracy of the reference voltage.

B. Offset and Low-Frequency Noise

The regulated voltage references, i.e., those which utilize an operational amplifier in the feedback loop, suffer from input offset voltages caused by, for example, asymmetries in the physical layout. As an example, in the presence of the input offset voltage V_{OS}, the bandgap reference shown in Fig. 4.6 (d) results in a non-ideal reference voltage of the form

$$V_{REF} = V_{BE1} + \frac{R_2}{R_1}\left[V_T \ln\left(pr\right) - V_{OS}\right] . \tag{4.15}$$

Accordingly, the offset voltage is amplified to the reference output by the same factor of R_2/R_1 as the ΔV_{BE} [56]. Furthermore, the offset voltage varies with temperature, thus degrading the TC of the reference voltage. Offset voltages can be minimized by using several techniques, such as by utilizing precision layout techniques, by exploiting unequal collector currents to further increase ΔV_{BE}, and by using a chopper amplifier, the idea of which was already described in the context of a CT charge amplifier in Section 3.2.1.

The output noise of voltage references may have considerable effects on the performance of low-noise circuits, such as a high-precision A/D converter, because the reference noise is directly added to the input of the subsequent circuit block and even the addition of a large output capacitor may not suppress low-frequency flicker noise components [56]. Fundamentally, noise floors do not decrease proportionately when input supply voltages are lowered, thus leading to an effective reduction in dynamic ranges. The output noise of voltage-mode references tends to be lower than that of current-mode ones with the same power dissipation and die area, because voltage-mode references do not necessarily require a current mirror [67].

C. Load Regulation

Many voltage reference topologies inherently require an operational amplifier in the feedback loop, i.e., a regulating loop, to establish the reference voltage [49]. As a side benefit, the variations in output voltage with respect to changes in loading and

operating conditions are reduced. Load regulation (LDR) performance refers to the steady-state output voltage variations resulting from dc changes in the load current. The need for a regulated low-impedance output depends on the loading demands of the system. The use of an unregulated current-mode output stage may be acceptable if there is a large capacitive load and no need for a steady-state current. Voltage references may affect the speed of the circuits that they feed and cause crosstalk between different circuits through reference lines. In low-power applications, in which high-speed operational amplifiers cannot be used, the external disturbances can be suppressed by bypassing the critical node to ground with a large capacitor. Depending on the environment, however, it may even be preferable to leave the critical node agile so that it can quickly recover from transients [56]. Therefore, in order to mimimize the effects caused by noise injection, most integrated systems utilize a regulated voltage reference.

D. Line Regulation and Power Supply Rejection

As long as the open-loop gain of the operational amplifier used in the regulated voltage reference is sufficiently high, the output voltage is relatively independent of the input supply voltage. Line regulation (LNR) performance refers to the steady-state output voltage variations from dc changes in the input supply voltage. Instantaneous variations in the loading of the input supply itself, particularly resulting from digital circuits, cause transient variations to occur [56]. The power supply rejection (PSR) performance of a regulated voltage reference typically depends on the rejection properties of the operational amplifier, and thus degrades at high frequencies as a result of various capacitive paths. Both the LNR and PSR performance can be improved by increasing the effective impedance from the sensitive node, particularly from the reference voltage node, to the input supply. The effective output resistance of a stand-alone device can be improved by roughly 30 to 50 dB by using a simple unregulated cascode circuit, and at least an order of magnitude more by using a regulated cascode circuit [49]. However, in low-voltage applications the use of cascodes is typically impossible because of the limited voltage headroom available, thus also limiting the LNR and PSR performance. Another way to improve the PSR performance is to isolate the noisy and variable supply from the reference core circuit by using a pre-regulator, which can be essentially either a zero-order or a first-order voltage reference [49].

E. Overall Accuracy

The overall accuracy of a voltage reference is typically determined by the combination of its TC and LNR performance [74], i.e.,

$$\text{Accuracy} = \frac{\Delta V_{TC} + \Delta V_{LNR}}{V_{REF}}\,, \tag{4.16}$$

where ΔV_{TC} and ΔV_{LNR} are output voltage variations resulting from variations in the temperature and supply voltage, and V_{REF} is the nominal reference voltage. The LDR performance is more appropriately taken into account in the overall accuracy in the case of supply voltage regulators, which will be discussed in Chapter 6.

4.4 Temperature References

Most integrated temperature references, generally called temperature sensors or temperature transducers, make use of the characteristics of bipolar transistors. Temperature sensors based on, for example, the temperature dependence of resistors and MOS transistors [75] and thermal delay-lines [76, 77] have also been reported. In a smart temperature sensor, the sensor core circuitry is combined with the interface electronics on a single chip. In order to produce a digital representation of temperature, the so-called ratiometric temperature measurement, in which a temperature-dependent signal is compared to a reference signal, is required. Thanks to the fast development of smart temperature sensors, they can compete with conventional temperature sensors, such as platinum resistors, thermistors, and thermopiles, in terms of both cost and accuracy [36]. However, the operating range of integrated temperature sensors may be too restricted for some applications. Next, after a literature review of temperature sensors, the main characteristics of such circuits compared to voltage references, i.e., the ratiometric temperature measurement principle and the ratiometric curvature correction technique, will be discussed. Finally, the optimized charge balancing readout scheme for smart temperature sensors will be described.

4.4.1 Summary of Literature

The use of a base-emitter voltage of a bipolar transistor as a temperature sensor is straightforward, but, as discussed in Section 4.1, the base-emitter voltage suffers from non-linearity and its sensitivity is process-dependent. The first analog temperature sensor based on ΔV_{BE} was presented by Verster in 1968 [78]. Later, in 1974, Dopkin introduced the first monolithic temperature sensor of that kind [79]. Boomkamp et al. presented the first digital temperature sensor in 1985, the design of which was represented in [80]. That circuit was implemented with bipolar technology and it was based on the sequential feeding of a temperature-dependent current I_{TD} and a first-order temperature-independent current I_{TI} to a current-to-frequency converter.

The input signal in a temperature sensor is essentially a low-frequency or dc signal. Hence, smart temperature sensors can provide the so-called single-shot mode, in which, to save power and to reduce self-heating, at least part of the circuitry is powered down after producing a single temperature reading. A low-power CMOS smart temperature sensor, introduced by Bakker et al. in 1996 [81], uses a first-order CT $\Delta\Sigma$ modulator to generate the output bitstream proportional to I_{TD}/I_{TI}. The circuit consumed 3 μA at a sample rate of 2 S/s and achieved an inaccuracy of $\pm$1°C over the temperature range from –40 to 120°C after calibration at two temperatures. Two years later Tuthill presented an SC temperature sensor [82] with a comparable performance and an average current consumption as low as 0.3 μA at a sample rate of 10 S/s. A low-cost untrimmed temperature sensor utilizing both chopper and DEM techniques in the PTAT current generator was proposed by Bakker et al. in

1999 [83]. That sensor achieved accuracy comparable with that of the one described in [81] over the temperature range from –20 to 100°C.

During the last decade, the steady increase in the heat dissipation of microprocessors has further boosted the development of smart CMOS temperature sensors. Consequently, significant improvements in the accuracy of integrated temperature sensors have been obtained through precision interfacing techniques [36]. Pertijs et al. presented two CT temperature sensor designs with an inaccuracy of ±1.5°C [84] and ±0.5°C [85] from –50 to 120°C, respectively, and an SC design characterized by many more dynamic error correction techniques with an inaccuracy as low as ±0.1°C from –55 to 125°C [57]. In all these sensors, the ratiometric curvature correction technique [36] was applied to minimize the overall curvature in the output resulting from the systematic error of the base-emitter voltage. The sensor with the best performance with respect to both accuracy and power dissipation consumes 75 μA from a 2.5-5.5-V supply, while operating continuously at a sample rate of 10 S/s [57]. Batch calibration was used in [84], while individual calibration after packaging was used in [85] and [57].

A further optimized implementation with respect to cost and power dissipation was presented by Aita et al. [86]. Their smart temperature sensor achieved a batch-calibrated inaccuracy of ±0.25°C from –70 to 130°C with a threefold reduction in current consumption, thus being 25 μA, while using the same sample rate and supply voltage as the one described in [57]. During the present year several implementations with comparable inaccuracies have been proposed. The recent trend has been towards deep-submicron temperature sensors. A temperature sensor with an energy-efficient zoom ADC, which combines a coarse SAR conversion and a fine $\Delta\Sigma$ conversion, realized in a 0.16-μm CMOS process, consumes only 6 μA from a 1.8-V supply [87], while an npn-based temperature sensor implemented with a 65-nm CMOS process draws 8.3 μA from a 1.2-V supply [88]. The latter demonstrates that it is possible to implement accurate low-power low-voltage temperature sensors in deep-submicron CMOS processes. Furthermore, a temperature sensor based on the thermal diffusivity of silicon, namely the use of an electrothermal filter consisting of a heater and a thermopile, was demonstrated to exhibit an untrimmed inaccuracy of ±0.2°C from –55 to 125°C in [77]. Therefore, its untrimmed inaccuracy is comparable to the inaccuracy of the aforementioned state-of-the-art batch-calibrated temperature sensors based on bipolar transistors. As opposed to the temperature sensors proposed in [87] and [88], this approach is not applicable for low-power applications because of the high heater power of 2.5 mW.

4.4.2 Ratiometric Temperature Measurement

The conceptual schematic of a smart temperature sensor based on the use of three substrate pnp devices is shown in Fig. 4.9 [36]. The base-emitter voltage difference ΔV_{BE} is amplified by a factor α and combined with V_{BE} to provide an input and a

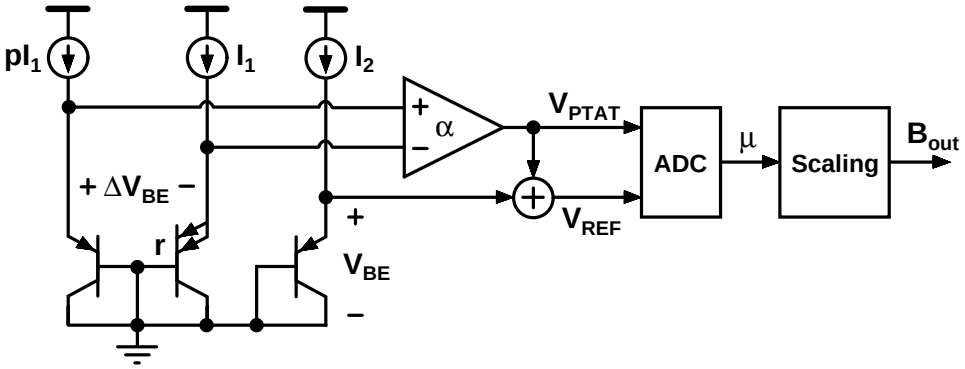


Figure 4.9: Conceptual schematic of a smart temperature sensor.

reference voltage to an ADC. As a result, the output of the ADC becomes[2] [36]

$$\mu = \frac{V_{PTAT}}{V_{REF}} = \frac{\alpha \Delta V_{BE}}{V_{BE} + \alpha \Delta V_{BE}} = \frac{\alpha V_T \ln(pr)}{V_T \ln\left(\frac{I_2}{I_S}\right) + \alpha V_T \ln(pr)}. \tag{4.17}$$

The output μ has to be PTAT, since V_{REF} can be considered as temperature-independent. Linear scaling can be implemented to provide a final digital output $B_{out} = A_0 + A_1\mu$ in degrees Celsius, where $A_0 \approx -273$ K and $A_1 \approx 600$ K. Thus, $\mu = 0.5$ corresponds to 27°C. With the use of that kind of approach only roughly 30% of the ADC input range is used. A more complicated expression of μ can be used to increase the usable input range to 90%, in which case the resolution of the ADC can be scaled down by a factor of three [36].

4.4.3 Ratiometric Curvature Correction

If V_{REF} is designed to be slightly greater than required in a typical voltage reference, its positive linear temperature dependence in (4.17) can be expressed as [36]

$$\mu \propto \frac{1}{V_{REF}} \propto \frac{1}{1+xT} = 1 - xT + \frac{1}{2}(xT)^2 - \ldots \tag{4.18}$$

The resulting non-linearity itself can be used as the curvature correction source to compensate the second-order non-linearity of V_{BE} [84]. The minimum non-linearity is achieved under the condition $[\partial^2\mu/\partial T^2]_{T=T_r} = 0$. This type of curvature correction relies on the ratiometric nature of the temperature sensor. Its realization only alters the circuit parameters, not the structure of the temperature sensor. Moreover, the scaling parameters A_0 and A_1 of the final digital output need to be slightly adjusted.

4.4.4 Optimized Charge Balancing Readout

$\Delta\Sigma$ ADCs are particularly suitable for the narrow-bandwidth signals characteristic of temperature sensors. A staightforward and an optimized charge balancing scheme

[2]Note that, for simplicity, the factors α_1 and α_2 used in (4.9) are replaced here by the factors one and α, respectively.

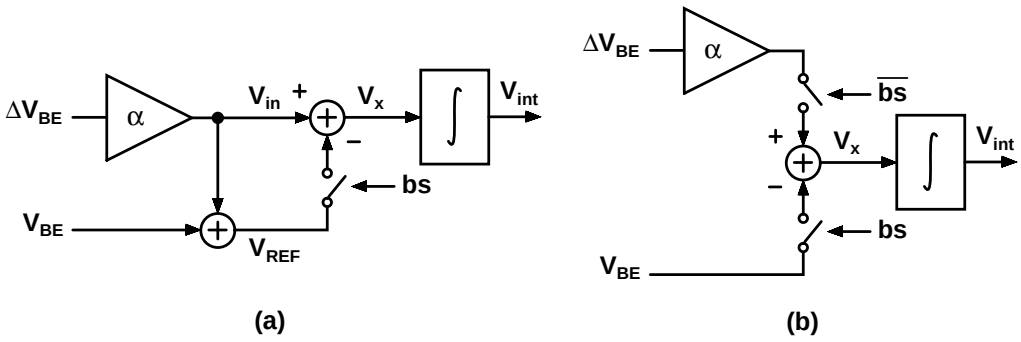


Figure 4.10: (a) Straightforward and (b) optimized charge balancing scheme for implementing a smart temperature sensor.

for producing the transfer function (4.17) are illustrated in Figs. 4.10 (a) and (b), respectively [36]. In the latter case, the integrator's input voltage V_x equals $\alpha\Delta V_{BE}$ if the value of the bitstream bs is zero, and $-V_{BE}$ if its value is one. The main advantage of this particular technique, when compared to its straightforward counterpart, is that there is no need for an explicit reference voltage V_{REF}. Both CT [81, 83, 84, 85] and DT [57, 86] designs based on this optimized charge balancing scheme have been reported.

A. Continuous-Time Approach

Charge balancing can be implemented in a first-order CT $\Delta\Sigma$ implementation, shown in Fig. 4.11, by using two voltage-to-current (V/I) converters that convert V_{BE} and ΔV_{BE} into currents with opposite polarity [81]. The gain α can be realized by using a larger resistor and/or a shorter integration period for V_{BE}, i.e. $R_2 > R_1$ and/or $\phi_{V_{BE}} < \phi_{\Delta V_{BE}}$ by a fraction δ, such that $\alpha = R_2/(\delta R_1)$ [36]. In precision temperature sensors some form of offset cancellation is typically required in the V/I converter of ΔV_{BE}, the offset requirement of which is the most stringent. Moreover, DEM techniques are typically required since the accuracy of α is mainly determined by the matching of R_1 and R_2. Switching the outputs of the V/I converters causes intersymbol interference as a result of the dependence on the bitstream, thus causing extra non-linearity and an increased quantization noise level [36]. This problem

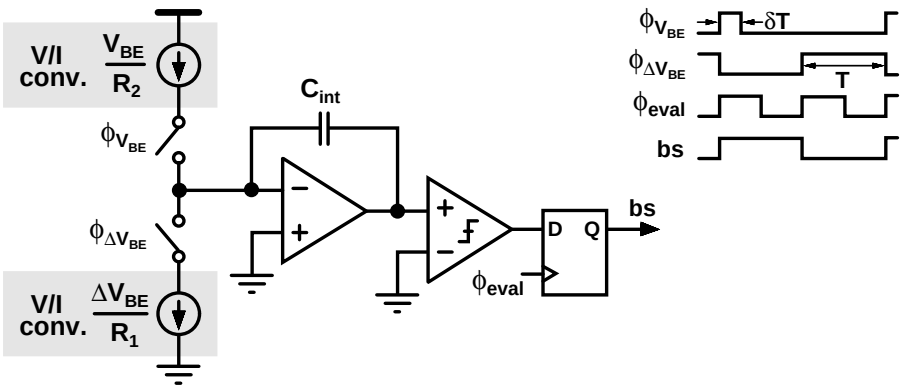


Figure 4.11: First-order CT $\Delta\Sigma$ modulator based on the use of two V/I converters.

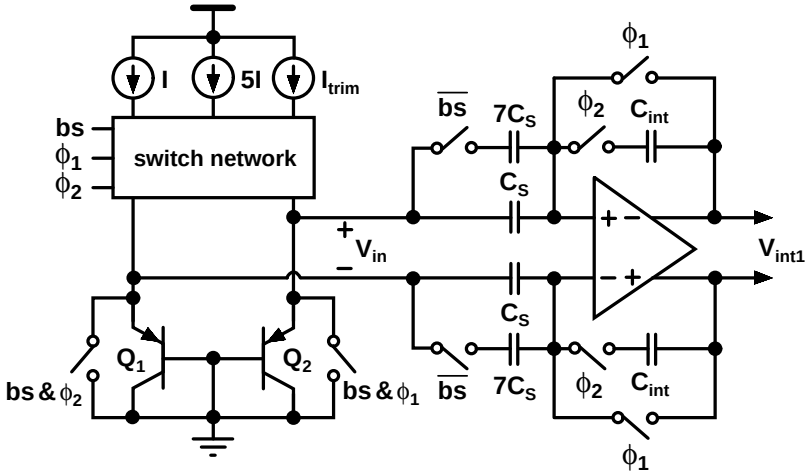


Figure 4.12: Front-end of the fully differential SC $\Delta\Sigma$ modulator.

can be prevented by using the return-to-zero (RTZ) switching technique, in which the outputs of both V/I converters are switched off at the end of every clock cycle. Dynamic error correction techniques cause switching transients as well.

B. Discrete-Time Approach

A simplified schematic of the front-end of the fully differential SC $\Delta\Sigma$ modulator is shown in Fig. 4.12 [57]. CDS is used to eliminate the offset and 1/f noise of the operational amplifier. If $bs = 0$, during ϕ_1 the current I is directed to Q_1 and the current $5I$ to Q_2, while during ϕ_2 the currents are swapped, in such a way that the resulting overall change in the output of the integrator is proportional to $2\Delta V_{BE}$. If $bs = 1$, during ϕ_1 the emitter of Q_2 is shorted to ground, while Q_1 is biased by the programmable current I_{trim}. Again, during ϕ_2 the roles of the bipolar transistors are swapped, in such a way that the overall change in the integrator's output is proportional to $-(V_{BE1} + V_{BE2})$. The gain α can be realized by using a larger sampling capacitor for ΔV_{BE} than for V_{BE}, and/or performing multiple charge transfers in one cycle of the $\Delta\Sigma$ modulator. In order to provide the gain of 16 in [57], a sampling capacitor that is eight times larger, together with a double integration, is used for ΔV_{BE}. Mismatch errors between capacitors can be averaged out by using DEM techniques. In a fully differential implementation the effects of leakage currents are relieved because they appear as common-mode.

The non-ideal noise shaping of a first-order modulator for a dc input signal does not prevent its use for instrumentation purposes. However, the use of a second-order $\Delta\Sigma$ modulator allows a significant reduction in clock frequency and thus also in power dissipation compared to a first-order modulator [57]. The optimized charge balancing scheme can be added to a second-order modulator by introducing a feedforward path over the first integrator [36]. Another advantage is that the peak-to-peak output swing of the first integrator is significantly reduced. The low-pass characteristic of a $\Delta\Sigma$ modulator can be used to suppress disturbances present in its input signal, such as dynamic error signals generated in the sensor core circuitry.

C. CT vs. DT Readout

In a CT implementation, accuracy requirements, rather than noise requirements, typically determine the power dissipation, whereas in a DT implementation the noise and settling requirements are dictated by the minimum sampling capacitor size and minimum bias current, respectively [36]. Power dissipation can be reduced in both cases by powering down the sensor part of the time. The overall average power dissipation may be reduced, even if the output data rate is kept the same, because the average power dissipation of the supporting circuitry, such as the bias circuit, is reduced. SC circuits are much less sensitive to switching transients, because sampling occurs at the end of a clock phase. As a conclusion, CT implementations are preferred for very low-noise or low-power temperature sensors, whereas SC implementations are more suitable when dynamic error correction techniques are widely used [36].

4.5 Discussion

Base-emitter voltages, and especially their differences, are very practical in the design of accurate and predictable current, voltage, and temperature references. In contrast to a single V_{BE} voltage, provided that the collector current ratio is constant, ΔV_{BE} is very reproducible, being independent of process parameters, as well as the absolute values of the collector currents. Most voltage and temperature references require one or several current references which have a well-characterized and controlled temperature behavior. A low-power first-order bandgap reference was designed for both sensor interface ASICs. The first ASIC, which operates from a 1.8-2.5-V supply, utilizes a regulated version of the Brokaw's bandgap reference (Fig. 4.6 (c)) [P2]. Its buffered output voltage is forced across a resistor to generate a current reference, which roughly has a temperature-independent characteristic. The temperature reference part that was also included exploits the PTAT voltage inherently available in the corresponding bandgap topology. In order to provide a digital temperature reading, ratiometric temperature measurement, in which a PTAT voltage is compared to a reference voltage, is required. Before the A/D conversion, the PTAT voltage had to be buffered, amplified, and shifted to a proper voltage level. Because of the low supply voltage requirement of 1.2 V (battery voltage 1.2-2.75 V), a current-mode CMOS-compatible bandgap reference (Fig. 4.6 (f)) [P8], which inherently provides a TI current reference, was implemented for the second interface ASIC.

In addition to the aforementioned reference core parts, several reference voltage buffers with resistor string loads had to be designed for both ASICs to provide the detection bias, reference, and common-mode voltage levels that were required in the sensor front-end and ADC circuits. In the case of the first interface ASIC [P4], a total of three such reference voltage buffers had to be provided, one for the SBB-type sensor front-end and two for the two algorithmic ADCs converting the acceleration and temperature information to the digital domain, because the ADCs

are powered down between their conversion cycles in order to save power. Similarly, the corresponding reference voltage buffers make use of reduced duty cycles. Two reference voltage buffers with resistor string loads, one for each operating mode in order to optimize power dissipation, were designed for the second sensor interface ASIC [P8].

The core circuitry of the current, voltage, and temperature reference that was designed for the first interface ASIC consumes only 5.5 μA from a 1.8-V supply. Including all required reference voltage buffers, current mirrors, and scaling circuitry, the total current consumption is increased to 23.1 μA. In the case of the second interface ASIC, when excluding the reference voltage buffers, the current and voltage reference circuitry consumes only 4.8 and 8.6 μA from a 1.2-2.75 V supply in the 1- and 25-Hz modes, respectively. When the current consumptions of the reference buffers are included, the corresponding values are increased to 8.4 and 60.7 μA, respectively. The reference voltage buffer starts to dominate the total current consumption of the system, particularly in the 25-Hz mode, because the $\Delta\Sigma$-type sensor front-end causes large worst-case load capacitance in the order of 30 pF for the common-mode output voltage; the fact that must carefully be taken into account in the design of the resistor string load of the reference voltage buffer. It is also worth noting that the maximum capacitive signal available from the $\pm$4-g accelerometer did not cover the whole input range of the $\Delta\Sigma$ sensor front-end, but was limited roughly to the level of one twelfth of the full-scale range. In practice, this meant that the 16-bit accuracy was required from both the sensor front-end and the reference voltage generation, which had an adverse effect on the current consumption of the reference voltage buffers.

5 Non-linear Frequency References

The function of frequency references, or oscillators, is to produce stable and periodic time-varying output waveforms that can serve as the information or timing signals for the signal-processing circuits [89]. Oscillators can be divided roughly into tuned (sinusoidal) and non-linear (square wave, or triangular) oscillators [90], though essentially all oscillator circuits can be considered as non-linear because of their non-linear amplitude control mechanism. Thanks to their simple structure, non-linear oscillators, namely ring and relaxation oscillators, are particularly attractive for providing relatively low-frequency timing signals, from hundreds of kHz to tens of MHz, for low-power sensor interfaces, in which neither their poor phase noise performance nor poor spectral purity becomes a problem. This chapter starts by introducing oscillator basics, after which the focus shifts to ring and relaxation oscillators, and finally to jitter and phase noise performance.

5.1 Oscillator Basics

5.1.1 Oscillator Models

Oscillators are typically modeled as linear systems by using either a feedback model or a negative resistance model, as illustrated in Figs. 5.1 (a) and (b) [91], respectively. The preference of one model over the other depends on the oscillator configuration. The feedback model consists of an amplifier $A(s)$ and a frequency-selective feedback network $\beta(s)$ connected in a positive feedback loop. The closed-loop transfer function is given by

$$H(s) = \frac{A(s)}{1 - A(s)\beta(s)}, \tag{5.1}$$

where $A(s)\beta(s) = L(s)$ is the loop gain. The circuit may oscillate at ω_0 if the so-called Barkhausen criteria [89]

$$|L(j\omega_0)| \geq 1 \quad \text{and} \quad \angle L(j\omega_0) = 0^\circ \tag{5.2}$$

are satisfied at that frequency. However, it must be noted that these conditions may provide misleading results if they are met at multiple frequencies [91]. If the circuit is unstable about its operating point (i.e., a complex pole pair in the right-half-plane (RHP)), electronic noise or turn-on transient in the supply voltage may initiate the oscillation and produce a growing waveform. Hence, oscillators are autonomous circuits that are able to produce and sustain an output signal V_{out} without applying any input signal V_{in} [91]. As V_{out} becomes larger, the non-linearity of the active devices starts to limit its growth, eventually causing the loop gain to be reduced to exactly unity (i.e., a complex pole pair on the $j\omega$-axis).

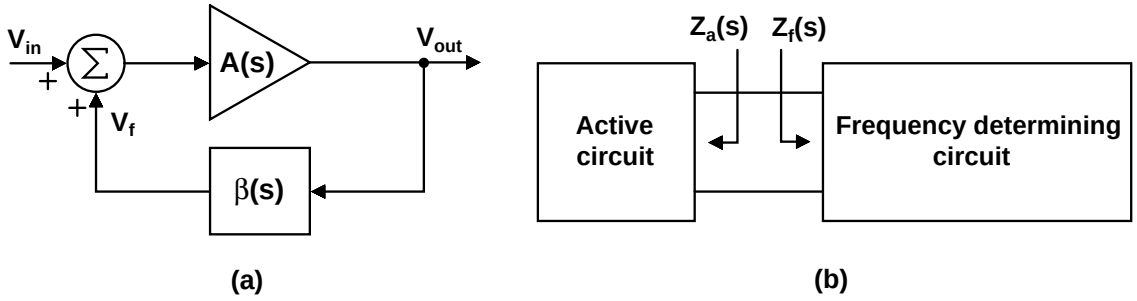


Figure 5.1: Oscillator models: (a) feedback and (b) negative resistance model.

The negative resistance model shown in Fig. 5.1 (b) consists of a one-port active circuit and a one-port frequency-determining circuit, which are characterized by the impedances $Z_a = R_a + jX_a$ and $Z_f = R_f + jX_f$, respectively. The function of the active circuit is to produce a small-signal negative resistance. In the case of this model, the widely-used conditions for the oscillation build-up are [91]

$$R_a(\omega_0) + R_f(\omega_0) < 0 \quad \text{and} \quad X_a(\omega_0) + X_f(\omega_0) = 0. \tag{5.3}$$

Accordingly, the circuit provides oscillation at ω_0 if the total resistive component is negative and the total reactive component becomes zero at that frequency. Again, misleading results may arise if the total reactive component becomes zero at multiple frequencies [91].

5.1.2 Oscillator Categories

There is a wide range of different oscillator architectures reported in the literature [56, 89, 90, 92, 93]. Typically, tuned oscillators make use of some kind of a frequency-selective or tuned circuit (RC/SC/LC/crystal oscillators) in a feedback configuration. The oscillation conditions discussed in the previous section can also be met without using resonators. Ring oscillators, which are cascades of inverting gain stages in a unity-gain feedback, are able to provide oscillation if the open-loop gain remains sufficient when the phase shift around the loop becomes zero. Relaxation oscillators, in turn, are able to oscillate even if the small-signal phase shift is insufficient, since their open-loop input/output characteristics involve hysteresis [93].

LC and crystal oscillators can provide excellent phase noise performance and high spectral purity because they are relatively insensitive to the properties of the active devices and have a frequency-selective feedback network [89]. Because of the large passives needed at lower frequencies, the use of integrated LC oscillators [93] is predominantly restricted to the radio and millimeter-wave frequencies. Oscillators that make use of piezoelectric crystals, such as quartz, can provide oscillation frequencies from a few kHz to several hundred MHz, depending on the design and orientation of

the crystal, with superior stability with respect to time and temperature (e.g., 1-2 ppm/°C) [89]. Unfortunately, such crystals are incompatible with IC technology as they require expensive external components. Silicon micromachined resonators, or MEMS oscillators, can also offer excellent stability and high quality factors over a wide range of frequencies, thus making them suitable for use in reference oscillators [94]. Though the uncompensated temperature stability of such resonators is inferior to that of quartz, typically in the order of 26 ppm/°C [94], these devices have the advantages of being capable of being combined with standard CMOS circuitry at the chip or package level and providing electrostatic tuning capability through the electrostatic spring constant k_{es} discussed in Section 3.1.1.

The use of both RC and SC sinusoidal oscillators is typically restricted by the bandwidth of the operational amplifiers. Furthermore, the frequency tuning of RC oscillators requires the simultaneous adjustment of several component values [89], whereas existing clock signals are required to control the switches in SC oscillators. Sinusoidal oscillators can also be implemented by exploiting operational transconductance amplifiers (OTAs) and capacitors. Because OTAs can provide larger bandwidths than conventional operational amplifiers, OTA-C oscillators can be used for signal generation up to hundreds of MHz [95]. Both types of non-linear oscillators, i.e., ring and relaxation oscillators, are very suitable for IC design, since they are straightforward to design, predictable in performance, do not require external components, thus being compact in size, can provide a linear and wide tuning range that can span orders of magnitude, and have inherent quadrature output capability [89]. However, because of the absence of high-Q frequency-selective elements, non-linear oscillators suffer from poor phase noise performance. Because the period of a ring oscillator is determined only by the sum of a few gate delays, its maximum oscillation frequency, which can be several GHz [96], is always much higher than that of a relaxation oscillator.

5.1.3 Voltage-Controlled Oscillators

Most applications require the output frequency of an oscillator to be a function of a control input, which is typically a voltage. Voltage-controlled oscillators (VCOs) are important building blocks in phase-locked loops (PLLs), which are used extensively in frequency synthesizers and clock recovery circuits. The ideal VCO characteristic, i.e., the oscillation frequency f_0 as a function of the control voltage V_{CTRL}, can be expressed as

$$f_0(V_{CTRL}) = f_0(0) + K_{VCO}V_{CTRL}, \tag{5.4}$$

where K_{VCO} is the constant gain in units of Hz/V. In practice, K_{VCO} is not a constant and it is desirable to minimize the non-linearity of (5.4), for example, in order to achieve better settling behavior in PLL designs [56]. On the other hand, it may be important to minimize K_{VCO} to reduce the effect of noise in V_{CTRL} on the output phase and frequency. The required tuning range depends on the application

demands, as well as process and temperature variations in the VCO center frequency. The center frequency of some CMOS oscillators may vary by as much as a factor of two, whereas frequencies that are tunable over one to two orders of magnitude are required in some applications [56].

5.2 Non-linear Oscillators

5.2.1 Ring Oscillators

A. Single-Ended Ring Oscillators

A ring oscillator consists of a number of inverting gain stages in a loop. To fulfill the Barkhausen criteria of (5.2) at the same frequency and to avoid the positive feedback near zero frequency (i.e., latch-up) resulting from signal inversions, an odd number $N \geq 3$ of inverting gain stages is required, as illustrated in Fig. 5.2 (a) by using basic CMOS inverters. Hence, the total frequency-dependent phase shift required for the loop to oscillate is 180°. One very useful property of ring oscillators is that they can provide multiple clock phases, which are $360°/N$ out of phase with respect to each other. In practice, N is determined by various requirements, such as speed, power dissipation, and noise immunity.

One period of oscillation corresponds to the time it takes for a transition to propagate twice around the ring. Thus, the oscillation frequency can be expressed as [97]

$$f_0 = \frac{1}{N(t_{dN} + t_{dP})} \approx \frac{2}{NCV_{DD}} \left(\frac{1}{I_N} + \frac{1}{I_P} \right)^{-1} \approx \frac{I}{NCV_{DD}}, \tag{5.5}$$

where t_{dN} and t_{dP} are the high-to-low and low-to-high propagation delays, C is the total capacitance at the output of each inverter stage, and I_N and I_P are the average discharging and charging currents. The first approximation assumes that the propagation delays are of the form $t_d = CV_{DD}/(2I)$, where $V_{DD}/2$ corresponds to the inverter's transition point, while the second approximation assumes symmetric operation, i.e., $I_N = I_P = I$. The average dynamic power of an N-stage CMOS inverter-based ring oscillator is given by

$$P = V_{DD} I = NCf_0 V_{DD}^2, \tag{5.6}$$

Additionally, so-called crowbar current is drawn directly from the supply to ground during transitions, which approximately doubles the total power dissipation of a symmetric ring oscillator [96].

The average discharging and charging currents of a basic CMOS inverter delay cell, I_N and I_P, can be limited by using constant current biasing of the inverters, as shown in Fig. 5.2 (b) [98]. If the biasing circuit required is neglected, both the oscillation frequency and the dynamic power dissipation of this type of a ring oscillator,

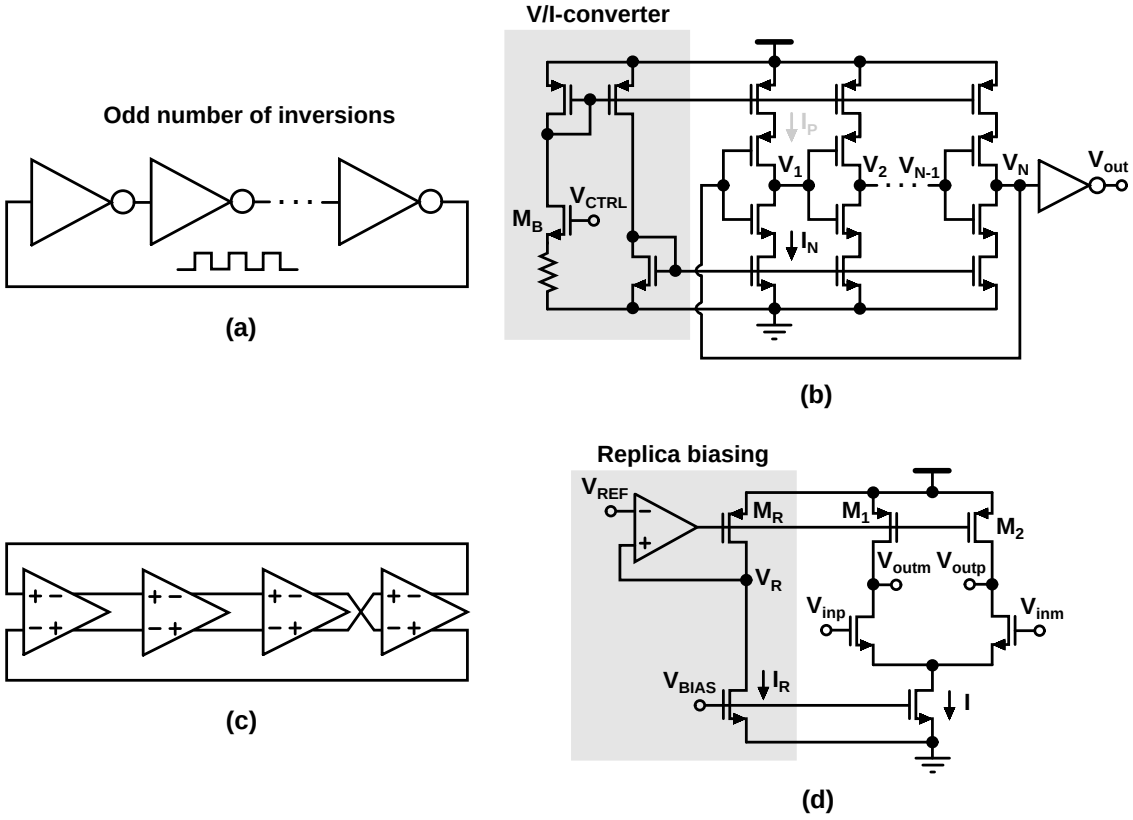


Figure 5.2: N-stage single-ended ring oscillators utilizing (a) basic and (b) current-starved CMOS inverters; (c) a four-stage differential ring oscillator, and (d) a basic differential delay stage with PMOS load transistors operating in the linear region.

also called a current-starved ring oscillator, are those given in (5.5) and (5.6). The proportionality of f_0 to I_N and I_P makes voltage-controlled operation possible. A relatively linear VCO characteristic can be obtained by sizing the resistively degenerated transistor $\mathrm{M_B}$ to be so wide that its V_{GS} is almost V_{THn}, regardless of V_{CTRL} [98]. Because a large load capacitance at the output of a ring oscillator can strongly affect the oscillation frequency, one or two inverters are typically used for buffering.

B. Differential Ring Oscillators

Fully differential gain stages can be used to implement differential ring oscillators, which exhibit better supply insensitivity than their single-ended counterparts. Another advantage of differential ring oscillators is that they can also use an even number of gain stages, as illustrated in Fig. 5.2 (c). This four-stage differential ring oscillator is able to provide quadrature outputs, the property of which is very useful in many communication applications [90]. Figure 5.2 (d) shows a basic differential delay stage with PMOS load transistors operating in the linear region. Assuming equal propagation delays for high-to-low and low-to-high transitions, i.e., $t_{dN} = t_{dP} = t_d$, the oscillation frequency of an N-stage differential ring oscillator

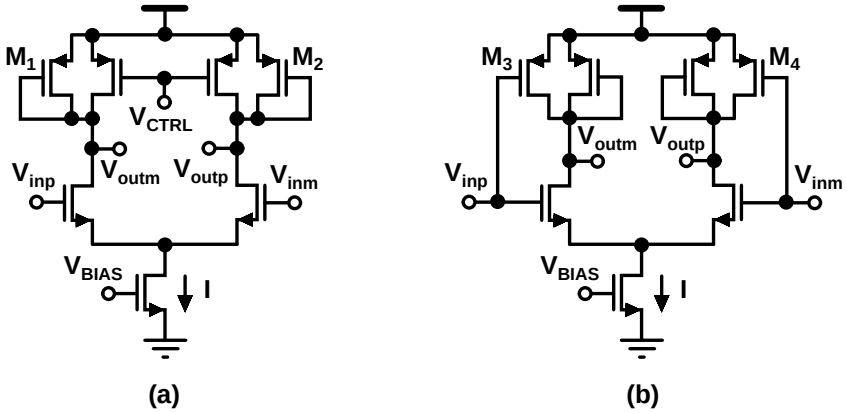


Figure 5.3: (a) Differential delay stage with linearized PMOS transistor loads for greater supply noise immunity, and (b) differential delay stage that makes possible a wide frequency tuning range.

can be expressed as [96]

$$f_0 = \frac{1}{2Nt_d} \approx \frac{I}{2NCV_{swing}}, \tag{5.7}$$

where I is the tail current and C and V_{swing} are the total capacitance and the voltage swing at each output node, respectively. If the biasing circuitry is neglected, the power dissipation of an N-stage differential ring oscillator becomes $P = V_{DD}NI$.

It is worth noting that V_{swing} depends on I as well. This implies that in order to provide practical tunability through the tail current, some kind of amplitude control must be added to the circuit. A replica biasing circuit [99, 100], embedded in the differential delay cell with PMOS loads in Fig. 5.2 (d), is widely used when differential voltage-controlled ring oscillators are being implemented. The amplifier applies negative feedback to the gate of M_R operating in the deep triode region and forces V_R and V_{swing} to be approximately V_{REF} and $V_{DD} - V_{REF}$, respectively. The oscillation frequency can be tuned by simultaneously varying I_R and I through a V/I converter, such as the one included in Fig. 5.2 (b). The advantage of combining the replica biasing technique with a differential delay stage that has a PMOS input pair [100] is that the oscillation frequency becomes inversely proportional to V_{REF}, instead of $V_{DD} - V_{REF}$. As a result, both noise immunity and frequency stability with respect to the supply voltage are improved.

A differential delay stage with linearized PMOS transistor loads, also known as symmetrical loads [101], is shown in Fig. 5.3 (a). This kind of a delay stage with additional diode-connected PMOS load transistors M_1 and M_2 can be used to provide greater immunity to supply noise [101], as well as to the upconversion of flicker noise [96]. A somewhat similar differential stage, shown in Fig. 5.3 (b) [56], is attractive for applications requiring a very wide tuning range. The PMOS transistors M_3 and M_4 are driven by inputs. As a result, relatively constant output swings are achieved even with large variations in the tail current. By exploiting this kind of a differential

stage in a ring oscillator, a tuning range as large as four orders of magnitude or more, and with less than a doubled variation in the output voltage swing, can be achieved. In order to provide higher noise immunity without additional voltage headroom, the differential control of the tail currents on the basis of the use of a current folding topology [56] can be utilized. Different tuning techniques based on the use of a positive feedback circuit and interpolation are presented in [56].

5.2.2 Relaxation Oscillators

A. RC Relaxation Oscillators

A typical RC relaxation oscillator is shown in Fig. 5.4 (a). It consists of an inverting Schmitt trigger placed in an RC feedback loop. Thus, during the first half of the period V_{out1} increases exponentially towards V_{DD} with the time constant $\tau_1 = RC$. When V_{out1} reaches V_1, V_{out2} changes its state and consequently V_{out1} starts to decrease exponentially towards ground by the same time constant $\tau_2 = \tau_1$. When V_{out1} reaches V_2, V_{out2} changes its state again, thus initiating a new cycle. The charging and discharging times T_1 and T_2 become equal if the upper and lower threshold voltages V_1 and V_2 reside symmetrically with respect to $V_{DD}/2$. The oscillation frequency can be expressed as [98]

$$f_0 = \frac{1}{T_1 + T_2} = \frac{1}{RC\left[\ln\left(\frac{V_{DD}-V_2}{V_{DD}-V_1}\right) + \ln\left(\frac{V_1}{V_2}\right)\right]}. \tag{5.8}$$

The accuracy and stability of V_1 and V_2 are critical, because they directly affect the oscillation frequency. A dual-comparator Schmitt trigger [89] can be used to keep V_1 and V_2 stable during the oscillation cycle. In that kind of a structure one of the comparators changes its state when V_{out1} reaches V_1, while the other changes its state when V_{out1} reaches V_2. If the power dissipation of the Schmitt trigger is neglected, the absolute minimum power dissipation of this oscillator is given by [102]

$$P_{min} = C f_0 V_H V_{DD}, \tag{5.9}$$

where $V_H = V_1 - V_2$ is the hysteresis voltage.

B. Constant-Current Charge and Discharge Oscillators

Current sources, rather than resistors, are used in this type of relaxation oscillators to charge and discharge the timing capacitor. A voltage-controlled version of such an oscillator, in which a non-inverting Schmitt trigger drives a current-starved inverter stage, is shown in Fig. 5.4 (b) [98]. The oscillation frequency of this topology is of the form

$$f_0 = \frac{I_{D1} I_{D2}}{C\left(V_1 - V_2\right)\left(I_{D1} + I_{D2}\right)}. \tag{5.10}$$

Assuming $I_{D1} = I_{D2} = I_D$, then $S_1 = |S_2| = I_D/C$ and the oscillation frequency

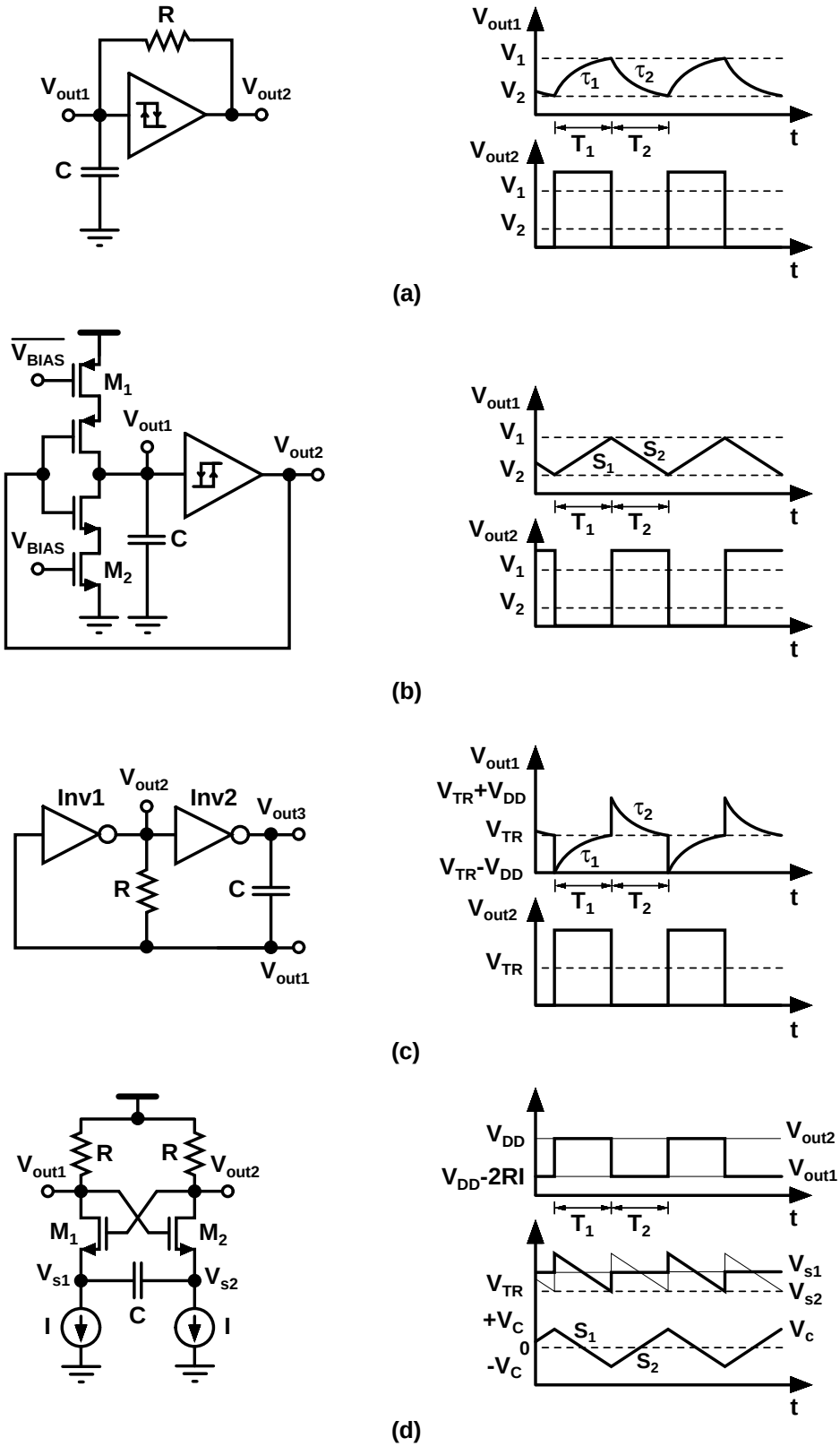


Figure 5.4: (a) RC relaxation oscillator; (b) constant-current charge and discharge oscillator; (c) simple astable multivibrator, and (d) source-coupled multivibrator.

simplifies to $f_0 = I_D/[2C(V_1 - V_2)]$. This condition implies a triangular wave in V_{out1} and a square wave with a 50% duty cycle in V_{out2}. The absolute minimum power dissipation given in (5.9) holds for this type of relaxation oscillator as well.

C. Astable Multivibrators

A simple astable multivibrator circuit including only two CMOS inverters and an RC network is shown in Fig. 5.4 (c) [98]. The two inverter outputs are in opposite states at all times and the capacitor C is alternatively charged and discharged with the same time constant $\tau_1 = \tau_2 = RC$. The inverters change their states when V_{out1} reaches V_{TR}, at which point a voltage equal to V_{DD} is either increased to or reduced from V_{out1}, depending on the direction of the transition in V_{out3}. Assuming $V_{TR} = V_{DD}/2$, the oscillation frequency can be expressed as [98]

$$f_0 = \frac{1}{2RC\ln\left(\frac{V_{TR}+V_{DD}}{V_{TR}}\right)} = \frac{1}{2RC\ln(3)}. \tag{5.11}$$

Frequency drift is caused primarily by variations in V_{TR} induced by temperature and supply voltage. The frequency stability can be improved substantially by replacing the CMOS inverter stages by high-gain comparator stages, where the transition voltage V_{TR} can be derived from a resistor string [89].

Both emitter-coupled [103, 104, 105, 106] and source-coupled [106, 107, 108, 109] multivibrators with a floating timing capacitor are well-known circuits, which can be actually considered as a subclass of the constant-current charge and discharge oscillators [89]. They are typically preferred over the conventional relaxation oscillators utilizing a Schmitt trigger, because they can inherently provide symmetrical output waveforms, as well as higher oscillation frequencies [89]. In the source-coupled multivibrator shown in Fig. 5.4 (d), a cross-coupled pair M_1-M_2 operates as a gain stage driving resistor loads R. The transistors M_1 and M_2 switch alternately on and off, and they determine the charging direction of the timing capacitor C. Assuming M_1 is on and M_2 is off, $V_{out1} = V_{DD} - 2RI$, $V_{out2} = V_{DD}$, and V_{s2} ramps down with a slope of $S_1 = -I/C$ until it reaches V_{TR}, consequently turning M_2 on and M_1 off. Hence, the positive feedback around M_1 and M_2 provides rapid switching at the end of each half-cycle, thus breaking the feedback for most of the period [93]. The second half-cycle is a time-shifted replica of the other half-circuit.

The resulting voltage waveform across C, $V_c = V_{s1} - V_{s2}$, is a triangle (i.e., $S_2 = |S_1|$), while the output voltage waveforms V_{out1} and V_{out2} can resemble either relaxation or sinusoidal oscillations, depending on the size of the capacitance C. Assuming a symmetrical V_c with a peak-to-peak variation of $2V_C$, the oscillation frequency can be written as [107]

$$f_0 = \frac{I}{4CV_C}. \tag{5.12}$$

The oscillation frequency depends on the supply voltage as a result of the body effect of M_1 and M_2, which has an effect through V_C [107]. Moreover, the control

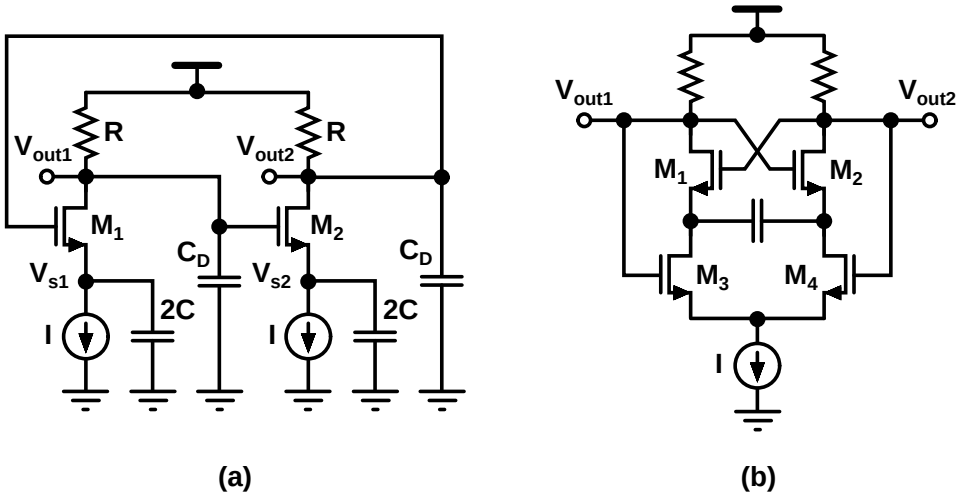


Figure 5.5: (a) Redrawn schematic of a source-coupled multivibrator, and (b) its power-efficient variant.

characteristic is generally a non-linear function of the current. Extensive analyses presented in [106] and [109] prove that there is a continuum between sinusoidal and relaxation oscillations. At high frequencies (i.e., small C), the hysteresis diminishes and the signals at the drain and source of M_1 and M_2 become close to sinusoids. The source-coupled multivibrator can be redrawn as shown in Fig. 5.5 (a) [110], i.e., as a cascade of two inverting gain stages with capacitive degeneration. Assuming equal transconductances g_m for M_1 and M_2 and equal total capacitances C_D for each output node, for the circuit to oscillate at ω_0, the two poles of each stage, i.e., $-g_m/(2C)$ and $-1/(RC_D)$, must contribute 90° phase shift. This implies that ω_0 must be the geometric mean of these two poles, yielding [110]

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_m}{2RCC_D}}, \tag{5.13}$$

which is of the same form as the ones derived in [106] and [109].

A power-efficient variant of the source-coupled multivibrator is shown in Fig. 5.5 (b) [108]. The power reduction scheme is based on combining the two tail current sources into one and adding a differential pair M_3-M_4 to provide current steering. The control of the current steering is derived directly from the outputs, and it works in such a way that M_1 and M_4, and M_2 and M_3, are alternately on in pairs. As a result, all the tail current I is ideally used for charging, and thus a 50% power reduction [108] is achieved with a given oscillation frequency, when compared with the basic configuration. In order to limit the output voltage swings in current-controlled operation, clamping diodes from V_{DD} to both output nodes are traditionally used [107]. When load resistors are replaced with PMOS transistors operating in the triode region, the replica biasing approach shown in Fig. 5.2 (d) can be utilized.

5.3 Jitter and Phase Noise

Like other analog circuits, oscillators are susceptible to noise. In the case of a practical oscillator both the signal amplitude $A(t)$ and phase $\phi(t)$ are functions of time. Disturbances in the amplitude are usually negligible or unimportant, and only the random deviations in phase are considered. Random fluctuations in the oscillator output frequency can be expressed in terms of (timing) jitter and phase noise. Jitter is a time-domain measure of the timing accuracy of the oscillator period, while phase noise is a frequency-domain view of the noise spectrum around the oscillator signal [111].

5.3.1 Summary of Literature

Jitter and the phase noise of oscillators have attracted much attention among IC designers. One of the best-known phase noise models is the Leeson model for tuned tank oscillators [112]. Unfortunately, this model includes two empirical parameters, namely the device excess phase number F and the $1/f^3$ noise corner $\Delta\omega_{1/f^3}$, which are typically used as fitting parameters for measured data. In [104], the jitter of relaxation oscillators is quantified by dividing the noise voltage by the slope of the waveform at the transition point. Since then the same time-domain first-crossing approximation has occasionally been used in the case of ring oscillators [113, 114, 102, 97]. Jitter and phase noise formulas are derived in detail for both single-ended and differential ring oscillators in [97]. These formulas take both white and flicker noise into account and they are suitable for hand calculations. A frequency-domain phase noise study for both ring and relaxation oscillators is presented in [110].

The general theory of phase noise in electrical oscillators proposed in [115] is based on a linear time-variant (LTV) model and gives an important insight into the phase noise generation process through impulse sensitivity functions (ISFs) and the time-varying nature of the noise sources, i.e., cyclostationarity. Both linear time-invariant (LTI) and LTV models erroneously predict infinite noise power density at the carrier frequency, as well as infinite total integrated power [116]. A more complete unifying phase noise theory for white and colored noise sources is presented in [116] and [117], respectively. This theory relies on a non-linear differential equation and predicts a Lorentzian shape of the spectrum, which implies that the noise power density at the carrier is finite and that the total carrier power is preserved despite spectral spreading resulting from noise. Like an ISF in the LTV model of [115], a perturbation projection vector (PPV) serves as a transfer function from a noise source to the scalar c and can be used to identify the sensitivity of a node to noise [118].

5.3.2 Relation between Jitter and Phase Noise

A. Period Jitter

In the presence of phase noise, the period of a free-running oscillator has a Gaus-

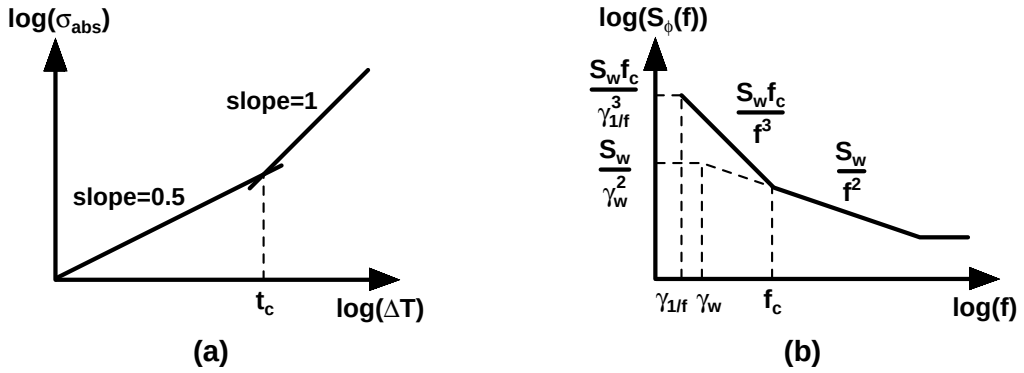


Figure 5.6: (a) Accumulation of absolute jitter with measurement time and (b) phase noise PSD with close-in corner frequencies.

sian distribution with a mean $\overline{T}$ and a standard deviation σ_T, which is here called period jitter. The terms cycle jitter σ_c and cycle-to-cycle jitter σ_{cc} have been used inconsistently in place of 'period jitter' in the literature [111]. According to the definitions of [119], cycle jitter corresponds to the period jitter used here, whereas cycle-to-cycle jitter is defined in such a way that it compares the oscillation period with the preceding period, instead of the mean period, thus describing the short-term dynamics of the period. Assuming white noise sources, two successive periods are uncorrelated and the variance of cycle-to-cycle jitter is twice as large as that of period jitter, yielding $\sigma_{cc} = \sqrt{2}\sigma_T$ [119].

B. Absolute Jitter

Absolute or long-term jitter σ_{abs} is defined as the cumulative sum of timing errors during the measurement time ΔT. Since its variance diverges with time, this type of jitter definition is typically used for PLLs, where an oscillator periodically receives correction pulses. In practice, both uncorrelated and correlated noise sources exist in a circuit, and thus the absolute jitter of a free-running oscillator accumulates over ΔT, as illustrated in Fig. 5.6 (a) [120]. The white noise of the oscillator dominates below the 1/f transition time t_c, resulting in $\sigma_{abs,w} = \kappa\sqrt{\Delta T}$ [114], while flicker noise dominates above t_c, yielding $\sigma_{abs,1/f} = \zeta\Delta T$ [96], where κ and ζ are proportionality constants determined by the circuit parameters.

C. Phase Noise

Phase noise is a continuous stochastic process indicating random accelerations and decelerations in phase, while an oscillator operates at a nominally constant frequency in steady state [97]. The phase noise is specified in the frequency domain by using the power spectral density (PSD) $S_\phi(f)$. In essence, phase noise broadens the spectral peaks while still keeping the total power of the oscillator unchanged. Phase noise has been shown to have a Lorentzian spectrum [121, 116], which has the total power of one and avoids any singularities at $f = 0$. In the absence of flicker noise and if any noise floor is ignored, the single-sideband (SSB) phase noise PSD $\mathcal{L}(f)$ at a frequency offset f in dBc/Hz (dB below the carrier within a unit bandwidth) can

be approximated as [116]

$$\mathcal{L}(f) \approx 10 \log_{10} \left[\frac{1}{\pi} \frac{\pi f_0^2 c}{(\pi f_0^2 c)^2 + f^2} \right], \tag{5.14}$$

where c is a scalar constant that describes the phase noise of the oscillator. The phase noise spectrum goes flat at offset frequencies below the Lorentzian linewidth $\pi f_0^2 c$ [121]. Assuming $\pi f_0^2 c \ll f \ll f_0$, the phase noise can be approximated as $\mathcal{L}(f) \approx 10 \log_{10}[(f_0/f)^2 c]$, which corresponds to the decay of phase noise at a rate of –20 dB/dec.

In the presence of any colored noise, such as flicker noise, the phase noise spectrum no longer displays a Lorentzian spectrum. There is no closed-form expression for the phase noise in the presence of flicker noise [111], but analytical models can be found in [117] and [121]. The model presented in [121] is a convolution of a Lorentzian with a Gaussian spectrum, in which the Lorentzian spectrum describes the white noise sources and the Gaussian spectrum describes the flicker noise sources. On the basis of the model presented in [117], the effect of any colored noise on the phase noise spectrum can be taken into account by replacing c in (5.14) by the frequency-dependent scalar $c(f) = c_w + \sum_{m=1}^{M} |c_{cm}(f)|^2$ [118], where c_w describes the phase noise contribution from the white noise sources and c_{cm} that from the mth-colored noise sources.

D. Equating Phase Noise to Jitter

In [120], a simple model to relate the time-domain absolute jitter and frequency-domain phase noise in the presence of flicker noise sources is presented. Figure 5.6 (b) shows a typical sideband phase noise spectrum $S_\phi(f)$ with close-in corner frequencies $\gamma_{1/f}$ and γ_w, which limit the phase noise power from growing to infinity at $f = 0$. The $1/f^2$ region with a –20 dB/dec slope is due to the white noise, while the $1/f^3$ region with a –30 dB/dec slope is due to the upconversion of the flicker noise. At large frequency offsets the phase noise spectrum eventually flattens out as a result of the noise floor. Though flicker noise is a non-stationary process, in practice it is always modeled as a colored stationary process [120, 117]. Accordingly, the model in [120] exploits the following relationship between absolute jitter and phase noise for both the white and flicker noise

$$\sigma_{abs}^2(\Delta T) = \frac{2}{\pi^2 f_0^2} \int_0^\infty S_\phi(f) \sin^2(\pi f \Delta T)\, df. \tag{5.15}$$

The analysis of [120] proves that the total absolute jitter can be expressed as

$$\sigma_{abs,tot}(\Delta T) = \kappa \sqrt{\Delta T} + \zeta \Delta T = \frac{\sqrt{S_w}}{f_0} \left(\sqrt{\Delta T} + \alpha \sqrt{f_c} \Delta T \right), \tag{5.16}$$

where S_w is the frequency-domain white noise figure of merit and α a coefficient of approximately five. Thus, the relation between t_c and f_c, the latter of which

corresponds to the 1/f^3 corner frequency, becomes $t_c \approx 1/(25f_c)$. The experimental results presented in [120] for a dozen VCOs prove that the model predicts the value of ζ with an error smaller than 10%. Because the phase noise in the 1/f^2 region is of the form $\mathcal{L}(f) = S_w/f^2$, and on the other hand, (5.15) with $\Delta T = 1/f_0$ results in $\sigma_T^2 = S_w/f_0^3$ [97], the relation between the period jitter and phase noise (both resulting from the white noise only) can be written as [96]

$$\sigma_T = \frac{f}{f_0^{1.5}} 10^{\mathcal{L}(f)/20}, \tag{5.17}$$

where $\mathcal{L}(f)$ is given in units of dBc/Hz.

5.3.3 Impulse Sensitivity Function Theory

An impulse sensitivity function (ISF), which is denoted as $\Gamma(\omega_0 t)$, describes the phase shift $\Delta\phi$ in the oscillation waveform as a result of a charge injection Δq into a certain oscillator node at a phase angle $\omega_0 t$ during the oscillation period. This dimensionless, frequency- and amplitude-independent, 2π-periodic function relates to the output excess phase $\phi(t)$ by the equalities [115]

$$\phi(t) = \Gamma(\omega_0 t)\frac{\Delta q}{q_{max}} = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\omega_0 t) i_n(t) dt, \tag{5.18}$$

where $q_{max} = C_{node} V_{swing}$ is the maximum charge displacement across the capacitor at the node of interest and $i_n(t)$ the noise current injected into this node. Any fluctuation in the phase persists indefinitely, whereas the excess amplitude tends to decay with time thanks to the amplitude-restoring mechanism of practical oscillators [115]. Typical ISFs for a harmonic oscillator, a ring oscillator, and an RC relaxation oscillator are illustrated in Figs. 5.7 (a)-(c) [122], respectively.

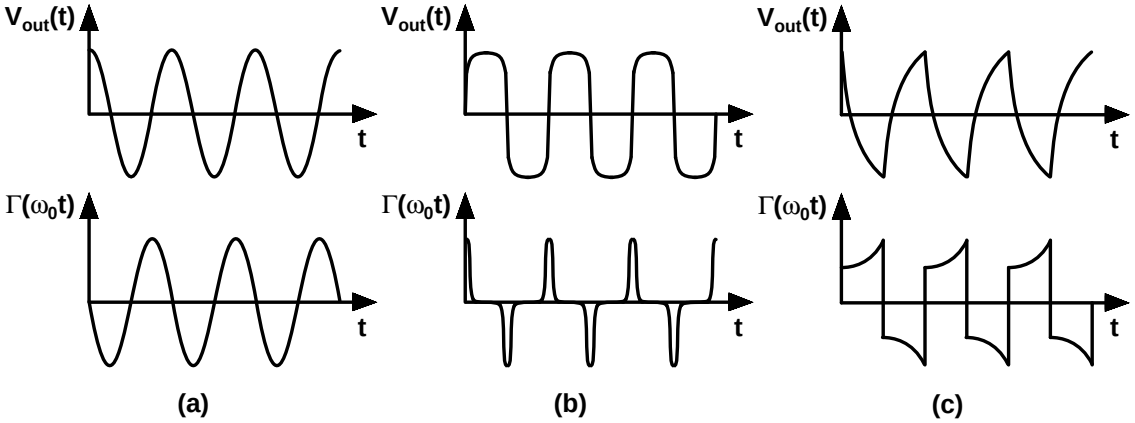


Figure 5.7: Typical ISFs for (a) harmonic oscillator; (b) ring oscillator, and (c) RC relaxation oscillator.

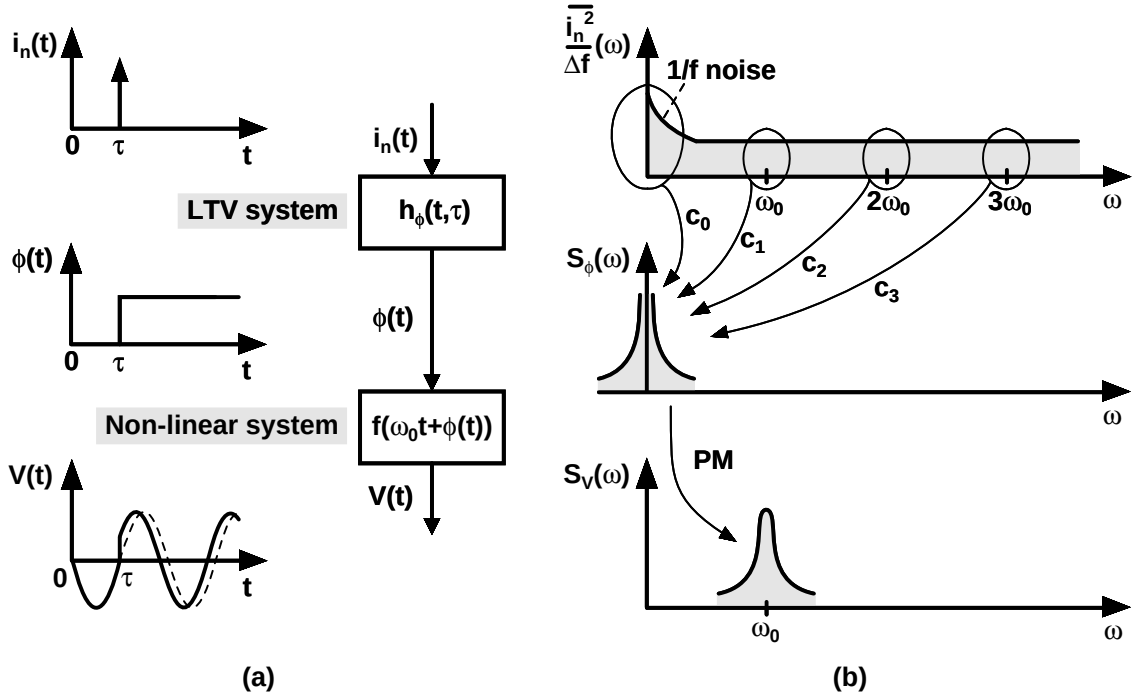


Figure 5.8: (a) Propagation of a current impulse to the phase shift on the output voltage waveform and (b) conversion of a current noise spectrum to phase fluctuations and further to phase noise sidebands around the carrier.

The ISF can be expanded in a Fourier series because of its periodicity. As a consequence, applying a current $i_n(t) = I_n \cos[(n\omega_0 + \Delta\omega)t]$ close to any integer multiple of the oscillation frequency results in two equal sidebands at $\pm\Delta\omega$ in $S_\phi(\omega)$ [115]. This phenomenon is explained in [110] by non-linear mixing, but the LTV theory under consideration proves that non-linearity is not needed to explain frequency translations. As depicted in Fig. 5.8 (a) [115], the conversion of device noise current to output voltage can be considered as a cascade of an LTV current-to-phase converter, which corresponds to the unit impulse response for excess phase $h_\phi(t, \tau)$, and a non-linear phase-to-voltage converter, which represents a phase modulation (PM). The frequency-domain illustration is shown in Fig. 5.8 (b) [115]. The current noise near dc gets upconverted and weighted by c_0, the current noise near the carrier stays there but gets weighted by c_1, and the current noise near the other integer multiples of the carrier gets downconverted and weighted by c_n ($n \geq 2$). These weighting factors correspond to the Fourier coefficients. The phase noise spectrum $S_\phi(\omega)$, as an input to the non-linear phase-to-voltage converter, transforms the phase noise sidebands to the output voltage spectrum $S_V(\omega)$. Interestingly, the ISF theory reduces to the LTI model if c_1 is set to unity while all the other Fourier coefficients are discarded.

The root-mean-square (rms) and dc values of $\Gamma(\omega_0 T)$ describe the phase noise resulting from white and flicker noise, respectively. The SSB phase noise spectrum for

an arbitrary oscillator resulting from a white noise current source can be expressed as [123]

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{\Gamma_{rms}^2}{q_{max}^2}\frac{\overline{i_n^2}/\Delta f}{2\Delta\omega^2}\right), \tag{5.19}$$

where $\overline{i_n^2}/\Delta f$ is the white power spectral density of an input noise current. A flicker noise current source with a power spectral density of $\overline{i_{n,1/f}^2}/\Delta f = \overline{i_n^2}/\Delta f \cdot (\omega_{1/f}/\Delta\omega)$, where $\omega_{1/f}$ is the 1/f noise corner frequency, results in a phase noise spectrum that is of the form[1] [115]

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{\Gamma_{dc}^2}{q_{max}^2}\frac{\overline{i_n^2}/\Delta f}{2\Delta\omega^2}\frac{\omega_{1/f}}{\Delta\omega}\right). \tag{5.20}$$

The ratio between the $1/f^3$ noise corner, i.e., the offset frequency at which (5.19) and (5.20) become equal, and the device 1/f noise corner corresponds to the ratio $\Gamma_{dc}^2/\Gamma_{rms}^2$. Because Γ_{dc} can be reduced significantly by providing symmetry in the oscillation waveform, poor 1/f device noise does not necessarily translate to poor close-in phase noise.

Large signal swing and fast transition improve the noise performance because then signal power is maximized and the period during which the oscillator is sensitive to noise is minimized [124]. Moreover, the devices do not contribute noise while turned off. The cyclostationarity of a noise source, such as the variation of the channel noise of a MOS device during the oscillation period, can be taken into account by multiplying the relating $\Gamma(\omega_0 t)$ with $\alpha(\omega_0 t)$ [115], which is the deterministic 2π-periodic noise modulating function that can be derived from the device noise characteristics and noiseless steady-state waveform. Since the current-to-phase conversion of Fig. 5.8 (a) is linear, the individual contributions of various noise sources can be combined by using superposition. According to a comparative study presented in [125] for two different ring oscillators and an LC oscillator, the results obtained on the basis of the ISF theory were within 3 dBc/Hz compared to the direct phase noise simulations (SpectreRF and EldoRF), and within 5 dBc/Hz compared to the measurements.

5.3.4 Phase Noise of Ring and Relaxation Oscillators

A. Single-Ended Ring Oscillators

Assuming that V_{TR} equals $V_{DD}/2$ and the threshold voltages of both NMOS and PMOS transistors equal V_{TH}, the SSB phase noise resulting from white noise in an

[1] Based on (5.18) the terms Γ_{rms}^2/q_{max}^2 and Γ_{dc}^2/q_{max}^2 in (5.19) and (5.20) can be replaced by $\phi_{rms}^2/\Delta q^2$ and $\phi_{dc}^2/\Delta q^2$, respectively, where ϕ_{rms} and ϕ_{dc} are the rms and dc values for the phase shift resulting from charge injections Δq during the oscillation period.

N-stage CMOS inverter-based oscillator can be expressed as [97]

$$\mathcal{L}(f) = 10\log_{10}\left\{\frac{2kT}{I}\left[\frac{1}{V_{DD}-V_{TH}}(\gamma_n+\gamma_p)+\frac{1}{V_{DD}}\right]\left(\frac{f_0}{f}\right)^2\right\}, \tag{5.21}$$

where k is the Boltzmann's constant, T the absolute temperature, I the average charging/discharging current, and γ_n and γ_p the coefficients equal to 2/3 for long-channel devices in the saturation [96]. The SSB phase noise resulting from flicker noise can be written as [97]

$$\mathcal{L}(f) = 10\log_{10}\left[\frac{C_{ox}}{8NI}\left(\frac{\mu_n K_{fn}}{L_n^2}+\frac{\mu_p K_{fp}}{L_p^2}\right)\left(\frac{f_0^2}{f^3}\right)\right], \tag{5.22}$$

where C_{ox} is the gate-oxide capacitance per unit area, μ_n and μ_p the electron and hole mobilities, K_{fn} and K_{fp} the empirical flicker noise coefficients, and L_n and L_p the channel lengths of the NMOS and PMOS devices, respectively.

Interestingly, the phase noise resulting from white noise sources is independent of N, whereas the phase noise resulting from flicker noise improves with an increasing N. According to (5.21) and (5.22), the phase noise performance can be improved by increasing I, V_{DD}, and N, as well as L_n and L_p. It is worth noting that I does not depend on N, but in reality it depends on V_{DD}. According to the ISF-based analysis of single-ended ring oscillators presented in [96], the peak value of an ISF can be reduced by increasing N, which corresponds to faster transitions, whereas Γ_{dc}, and hence the upconversion of flicker noise, can be reduced by providing symmetric rising and falling edges. Assuming that the symmetry criteria are well satisfied, the net effect of increasing N on the phase noise, however, disappears as a result of the increased number of noise sources, which is in agreement with (5.21).

The fundamental reasons for the poor phase noise performance of ring oscillators are that they dissipate all the stored energy during the same cycle (i.e., low Q-value) and the device noise is at its maximum during the transitions, which is where the sensitivity is the greatest [96], as becomes evident from Fig. 5.7 (b). In the case of mixed-signal ICs, the switching of nearby circuits typically causes perturbations and glitches in the supply voltage that far exceed all thermodynamic noise [97]. One of the characteristics of ring oscillators is that there is a strong correlation at different nodes as a result of substrate and supply noise. Consequently, when identical noise sources at all the nodes of a single-ended ring oscillator are assumed (phase difference in multiples of $2\pi/N$), only noise in the vicinity of integer multiples of $N\omega_0$ affects the phase [96].

B. Differential Ring Oscillators

When an N-stage differential ring oscillator consisting of NMOS differential pair delay stages with resistor loads is being considered, the SSB phase noise resulting

from white noise can be written as [97]

$$\mathcal{L}(f) = 10\log_{10}\left\{\frac{2kT}{I\ln(2)}\left[\gamma_n\left(\frac{\frac{3}{4}}{V_{eff,d}}+\frac{1}{V_{eff,t}}\right)+\frac{1}{V_{op}}\right]\left(\frac{f_0}{f}\right)^2\right\}, \tag{5.23}$$

where $V_{eff,d}$ and $V_{eff,t}$ are the overdrive voltages of the differential pair and tail current devices and V_{op} is the amplitude of the differential output waveform. The propagation delay is determined by decaying exponentials caused by the RC loads, which appears as a coefficient ln(2) in the denominator of (5.23). Interestingly, flicker noise in the differential pair changes the duty cycle of the output without affecting the period which corresponds to the upconversion of the flicker noise to $2f_0$. Instead, the flicker noise of the tail current sources modulates the delay directly. The dominant flicker noise source is typically the diode-connected MOSFET of the tail current mirror, because it causes correlated noise in all delay cells and the current mirroring ratio may be large. Therefore, the resulting SSB phase noise resulting from flicker noise can be approximated with [97]

$$\mathcal{L}(f) = 10\log_{10}\left[\frac{AK_{fn}}{WLC_{ox}}\left(\frac{1}{V_{eff,t}^2}\right)\left(\frac{f_0^2}{f^3}\right)\right], \tag{5.24}$$

where A corresponds to the current gain of the mirror.

Since, in the case of a differential ring oscillator, tail currents and thus also voltage swings must be scaled down with increasing N for a given oscillation frequency and power dissipation, the phase noise degrades proportionally to N. As a result, single-ended ring oscillators may be used in a less noisy environment to achieve better phase noise performance for a given power dissipation [96]. According to [96], the minimum number of differential delay stages should be used for the best performance, despite the fact that power dissipation is not a primary concern. In [126], the optimum N to minimize the phase noise for a given power budget is re-examined with an assumption that the oscillation frequency is too high for the full switching of a differential pair. The analysis takes into account the propagation of white noise around the ring oscillator loop, provides a modified version of (5.23) with dependence on N through the excess phase noise factor ζ, and suggests that the optimum N in a differential ring oscillator is five. For a smaller N, the effect of propagating white noise degrades the signal power and the phase noise [126].

Ideally, the supply noise appears as common-mode in both outputs of a differential delay stage, thus having no effect on the propagation delay. However, because of the poor common-mode rejection of delay stages in an unbalanced state, voltage-dependent diffusion capacitances at the outputs, the body effect of NMOS transistors, and charge injection into the common source of the differential pair through the parasitic capacitance also make differential ring oscillators susceptible to supply and substrate noise [124]. In the case of differential oscillators, only noise in the vicinity of integer multiples of $2N\omega_0$ affects the phase [127]. In order to provide

symmetry in each half-circuit of a differential ring oscillator, and thus to reduce the flicker noise upconversion [96], as well as substrate and supply coupling [101], more linear loads, such as resistors or linearized MOS devices, can be used.

C. Relaxation Oscillators

A minimum achievable phase noise is derived for an RC relaxation oscillator in [102] by taking into account only the white noise caused by the resistor. The resulting minimum phase noise can be approximated by

$$\mathcal{L}_{min}(f) \approx 10 \log_{10} \left[\frac{3.1kT}{P_{min}} \left(\frac{f_0}{f} \right)^2 \right]. \tag{5.25}$$

where $P_{min} \approx 0.52 C f_0 V_{DD}^2$ is the minimum power dissipation when the power dissipated by the comparator is neglected. Similarly to ring oscillators, the phase noise can be improved by increasing the supply voltage and the charging current. In [102], the same kind of study is applied for a single-ended ring oscillator as well. The resulting minimum phase noise is equal to (5.25), except that $P_{min} = NCf_0V_{DD}^2$ and the factor 3.1 becomes 7.33, the result of which is in agreement with (5.21) with substitutions $V_{TH} = V_{DD}/2$ and $\gamma_n = \gamma_p = 2/3$. According to the experimental study in [102], the gap between the measured and the minimum achievable phase noise performance is much larger in the case of a relaxation oscillator than a ring oscillator, being of the order of 20 dB versus 5 dB, respectively, which may result from the continuous current flow of the former. This suggests that a single-ended ring oscillator is more attractive in terms of power-phase noise tradeoff, providing a less noisy environment.

5.4 Discussion

Thanks to their simple structure, ring and relaxation oscillators are particularly suitable for providing relatively low-frequency timing signals for low-power sensor interfaces, in which neither their poor phase noise performance nor poor spectral purity becomes a problem. Because of the high supply sensitivity of single-ended ring oscillators, they are predominantly used to provide timing signals for digital circuits, which have only modest requirements for the stability of the clock signals.

Two low-power frequency references, a fixed 2-MHz power-efficient version of the source-coupled multivibrator [P1, P9] and a tunable 1-50-MHz three-stage current-starved ring oscillator, were designed for the first sensor interface ASIC [P4] to provide timing signals for the SC-type front-end and ADCs, and for the DSP, respectively. The frequency stability of the output signal of the 2-MHz oscillator is optimized by using symmetrical loads and a supply-independent current reference (Fig. 4.2 (b)). It is necessary to use the supply-independent biasing because this circuit was designed to operate over the supply voltage range from 1.62 to

2.75 V without extra calibration. The effects of process variations on the oscillation frequency can be eliminated by programming the on-chip resistor and capacitor matrices. Nominally, the buffer of the 2-MHz oscillator accounts for two thirds of the total current consumption of roughly 6 μA. A power-efficient source-coupled multivibrator was chosen to provide timing signals for the second sensor interface ASIC as well [P8, P9], namely for the $\Delta\Sigma$ sensor front-end and the decimator. The oscillation frequencies required in the two operating modes are 24.6 kHz and 307.2 kHz, respectively. In order to manage with the low supply voltage of 1.0 V (on-chip regulation from a 1.2-2.75-V battery voltage) and the two operating modes with a roughly twelvefold difference in their oscillation frequencies, and still provide a way to calibrate the process variations, each operating mode was provided with its own frequency reference. With 1-pF load capacitance, the frequency reference that was designed nominally consumes only 230 nA and 750 nA while generating 24.6 kHz and 307.2 kHz clock signals, respectively.

The source-coupled multivibrators that were designed for the two sensor interface ASICs typically exhibit no more than $\pm$10% combined variation in oscillation frequency over the specified temperature and supply voltage ranges [P9]. The $\Delta\Sigma$ sensor interface sets tighter jitter requirements [P9], since the need for 16-bit accuracy, which is due to the limited signal available from the accelerometer used, also holds for the timing signals that are generated. In addition to simulations and measurements, the phase noise performance of these source-coupled multivibrators was studied on the basis of the ISF theory (Section 5.3.3) and the details are presented in [P9].

6 Low-Dropout Linear Regulators

The most fundamental functions of an electrical system are supplying and conditioning power. Voltage regulators are especially important in high-performance SoC solutions to convert unpredictable and noisy supplies to accurate and stable output voltages that are insensitive to variations in the input supply, loading environment, and various operating conditions [128]. Linear regulators are suitable for local on-chip voltage regulation because of their low complexity, low noise, and fast transient response. Low-dropout (LDO) linear regulators, or, in short, LDOs, have become increasingly popular in battery-powered systems thanks to their low-power nature. This chapter starts by introducing the basics of linear regulators, after which the focus is on frequency compensation and circuit techniques aimed to enhance the performance of linear regulators.

6.1 Linear Regulator Basics

6.1.1 Basic Structure and Operation

The general structure of a linear regulator, shown in Fig. 6.1 (a), consists of a pass device (M_P), a feedback network (R_{F1} and R_{F2}), an error amplifier (A_{EA}), a voltage reference (V_{REF}), and an output filter (C_O, R_{ESR}, and C_B) [74]. The load circuitry is modeled here by using the combination of a current sink, a resistor, and a capacitor (I_L, R_L, and C_L). The circuit senses the output, compares it with the reference, and uses the difference to modulate the resistance of the pass device, i.e., the amplitude of the load current I_L. The regulation loop cancels the output voltage variations resulting from, for example, the load current, input voltage, and temperature. Large output capacitance C_O (e.g., 1 nF-10 μF) is required to suppress transient variations,

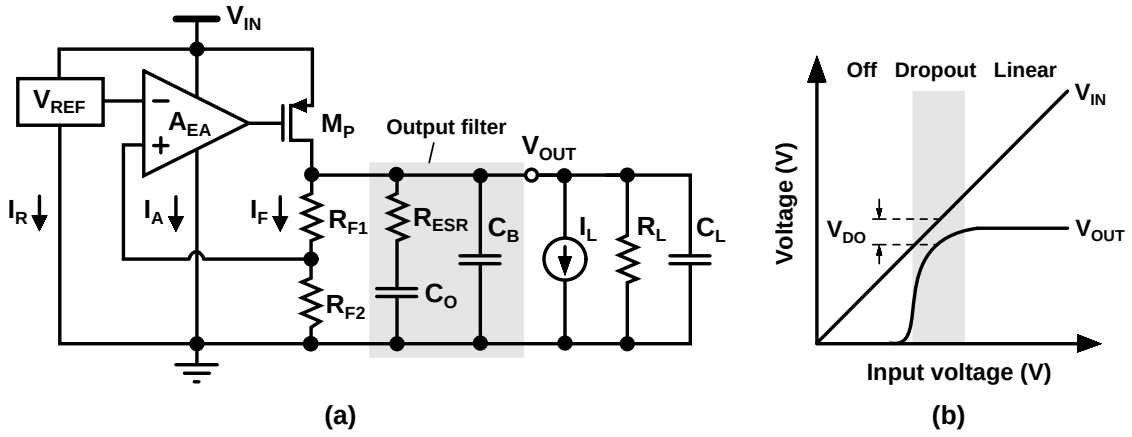


Figure 6.1: (a) Basic linear regulator structure and (b) its typical input-output voltage characteristics.

since the regulator responds to quick load current changes after some finite delay, during which the output capacitor sources or sinks the difference. This capacitor has the parasitic equivalent series resistance (ESR) R_{ESR}, which is highly variable according to the process and temperature (e.g., 1-500 mΩ) [128]. The total output voltage variation is often reduced by adding low-ESR bypass capacitance C_B (in the order of nanofarads), which supplies most of the almost instantaneous load current.

The operation of a linear regulator is illustrated in Fig. 6.1 (b) [128]. In the linear region the regulator operates properly, regulating the output with some finite non-zero loop gain. At the lower end of the linear region ($V_{IN} \approx V_{OUT} + V_{DS,sat}$) one of the transistors in the loop enters the triode region and the output is regulated with a reduced loop gain. When the input voltage decreases further, the regulator enters the dropout region, where the loop gain drops to zero and the pass device supplies all the current it can. The dropout voltage V_{DO} is defined as the input-output voltage difference where the control loop stops regulating [128]. At the edge of the off region the circuit reaches its headroom limit and the output voltage reduces to zero.

The optimum power efficiency $\eta = P_{OUT}/P_{IN}$ of a linear regulator can be achieved if V_{DO} is low and the circuit is biased slightly above its dropout region, in which case [128]

$$\eta = \frac{V_{OUT}}{V_{IN}}\eta_I \leq \frac{V_{IN} - V_{DO}}{V_{IN}} \left(\frac{I_L}{I_L + I_Q} \right) \leq 1 - \frac{V_{DO}}{V_{IN}}. \tag{6.1}$$

where η_I is the current efficiency, and $I_Q = I_F + I_A + I_R$ the total quiescent current or ground current of the regulator. The parameter I_Q is particularly important in portable devices, where load currents may often fall to near to zero, which implies that η_I becomes zero as well. The minimum power dissipation of a linear regulator is given by $P_{min} = V_{IN}I_Q + V_{DO}I_L$, where the first term dominates at very low load currents and the second one at moderate-to-high load currents. The lowest V_{DO} (roughly 0.2-0.4 V) can be achieved by using p-type pass devices, the lowest I_Q by using MOS devices, the highest I_L by using bipolar pass devices, and the lowest R_{DS} (i.e., the fastest response time) by using n-type pass devices [74]. Typically, the best compromise between these performance parameters can be achieved by using the PMOS pass device, whereas n-type pass devices are preferred for those applications where fast response times are required at the expense of lower efficiency. Because an NMOS pass device is connected as a source follower, its use requires the amount of one threshold voltage more headroom (V_{DO} is increased accordingly), compared to its PMOS counterpart.

6.1.2 Linear vs. Switching Regulators

Linear regulators can be categorized according to their power level, compensation scheme, and dropout voltage [128]. If the dominant low-frequency pole of a linear regulator is located at the output, it is said to be externally compensated, whether

the compensation capacitor is on-chip or not, while it is said to be internally compensated if the dominant low-frequency pole is located at some internal node. In [128], the distinction made between low- and high-dropout (LDO/HDO) linear regulators is based on the V_{DO} limit of 0.6 V. The advantages of linear regulators are their low complexity, low output noise/ripple, and fast transient response, while their disadvantages include their limited output range ($V_{OUT} < V_{IN}$), and limited power efficiency [74].

Switching regulators, also called switching converters or dc-dc converters, are able to provide a flexible output range ($V_{OUT} < V_{IN}$ or/and $V_{OUT} > V_{IN}$) and high power efficiencies in the order of 80-95%, the latter of which is due to the low voltage drop across the power switches [128]. Such high-efficiency switching regulators are inherently more complex and costly than their linear counterparts, because they practically require off-chip inductors and capacitors, and they suffer from higher noise content, as well as slower transient response. If a noise-sensitive load must be driven with a high input-output voltage difference, it may be appropriate to first perform downconversion by using a power-efficient switching pre-regulator and then provide the low-noise supply using a cascaded linear post-regulator [74].

6.1.3 Overall Accuracy

The regulator's load regulation (LDR) performance can be improved by increasing the dc open-loop gain, because the LDR corresponds to the regulator's steady-state closed-loop output resistance. It can be written as $LDR = \Delta V_{LDR}/\Delta I_L = R_{O,CL} = R_{O,OL}/(1 + A_{OL}|_{DC}\beta_F)$ [74], where $R_{O,OL}$ and A_{OL} are the open-loop output resistance and gain and $\beta_F = R_{F2}/(R_{F1} + R_{F2})$ is the feedback factor. In practice, because steady-state changes in V_{IN} also manifest themselves indirectly through the supply-induced variations in V_{REF}, the overall line regulation (LNR) of the regulator corresponds to the following superposition: $LNR = A_{IN}|_{DC} = \Delta V_{LNR}/\Delta V_{IN} = A_{IN,REG}|_{DC} + A_{IN,REF}|_{DC}A_{CL}$ [128]. The parameters $A_{IN,REG}$ and $A_{IN,REF}$ are the supply gains of the regulator and voltage reference and A_{CL} is the regulator's closed-loop gain, i.e., V_{OUT}/V_{REF} or $1/\beta_F$. The power supply rejection (PSR) performance of a regulator, in turn, corresponds to the reciprocal of the overall supply gain A_{IN}, and it is defined for the whole frequency spectrum.

Since any temperature-induced variation in the reference voltage (ΔV_{REF}) or input-referred offset voltage of the error amplifier (ΔV_{OS}) propagates to V_{OUT} through the closed-loop gain A_{CL}, the overall TC of the regulator output can be approximated as a sum of the TCs of V_{REF} and V_{OS}, i.e., $TC \approx (\Delta V_{REF} + \Delta V_{OS})/(V_{REF}\Delta T)$ [74]. The closed-loop gain error G_{err}, which results in systematic variation of $\Delta V_{G,err} = V_{REF}G_{err} = -V_{REF}/(1 + A_{OL}\beta_F)$ in V_{OUT}, tends to reduce the output voltage level [128] and it can be reduced by increasing A_{OL}.

The overall accuracy of a regulator is determined by systematic and random errors

together. Load (ΔV_{LDR}), line (ΔV_{LNR}), temperature (ΔV_{TC}), gain ($\Delta V_{G,err}$), and transient ($\Delta V_{TR,max}$) effects are all systematic, monotonic, and mostly linear, while process-induced variations in the reference voltage (ΔV^*_{REF}), the error amplifier's input-referred offset (ΔV^*_{OS}), and the closed-loop gain error ($\Delta V^*_{G,err}$) are random [128]. Because transient variations depend on the rise and fall times of I_L, and thus heavily on the application, the effect of $\Delta V_{TR,max}$ is often excluded from the overall accuracy specification. The random variations typically overwhelm all the systematic variations in V_{REF}, as a result of which the systematic error sources are often absorbed by ΔV^*_{REF}. Moreover, the effects of ΔV^*_{REF} and ΔV^*_{OS} are typically combined into the same parameter $\Delta V^*_{REF,OS}$ and both the systematic and random closed-loop gain errors are neglected. Consequently, the overall accuracy can be approximated by [128]

$$\text{Accuracy} \approx \frac{\sum \Delta V_{systematic} \pm \sqrt{\sum (\Delta V^*_{random})^2}}{V_{OUT}} \tag{6.2}$$

$$\approx \frac{\Delta V_{LDR} + \Delta V_{LNR} + \Delta V_{TC} \pm \sqrt{\left(\Delta V^*_{REF,OS} \frac{V_{OUT}}{V_{REF}}\right)^2}}{V_{OUT}}. \tag{6.3}$$

Though linear regulators typically achieve accuracies between 1 and 3% on the basis of (6.3), depending on the application's loading profile, another 1-7% should be allocated for $\Delta V_{TR,max}$ [128], which will be discussed next.

6.1.4 Transient Variations

Switching loads and supplies often inject substantial noise into modern mixed-signal systems, thus degrading the overall regulating performance and possibly making the effect of inherent electrical noise negligible [128]. In the worst-case situation, I_L suddenly steps from zero to its maximum value $I_{L,max}$, or vice versa, as shown in Fig. 6.2 (a). The linear regulator's transient responses to such sudden increases and decreases in the load current are typically asymmetrical, as illustrated in Fig. 6.2 (b) [74], since a Class A error amplifier's ability to charge and discharge the large parasitic capacitance of the pass device is asymmetrical.

When the load current increases suddenly, the additional load current $\Delta I_{L,max}$ discharges the output capacitors until enough time has elapsed to allow the control loop to respond. Because C_O is typically much greater than the total bypass capacitance C_B', i.e., the sum of C_B, C_L, and the drain-to-bulk capacitance of a PMOS pass device, it supplies most of the additional load current. After the response time Δt_1, the pass device starts to supply $\Delta I_{L,max}$ and some additional current to charge and slew C_O and C_B' back to their targeted voltage, which is the amount of ΔV_{LDR} below the ideal regulated voltage as a result of the load regulation effect. The settling time Δt_2 depends on the time required for the pass device to fully charge C_O and C_B', as well as the phase margin (PM) of the open-loop frequency response [74]. In

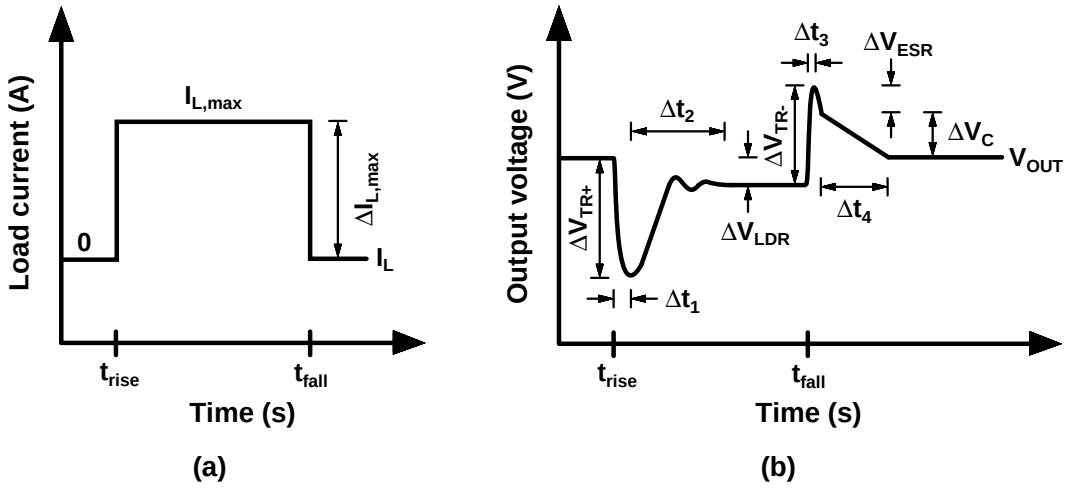


Figure 6.2: (a) Sudden worst-case load current increase and decrease, and (b) the typical transient response of a linear regulator to such load current changes.

the case of a sudden decrease of the load current to zero, the pass device continues to charge C_O and C_B' until the control loop responds after Δt_3 by shutting off the pass device. As a result, the voltage drop across R_{ESR} (ΔV_{ESR}) disappears, after which it takes time Δt_4 to discharge the output capacitors (ΔV_C) through the feedback network by the pull-down current $I_F = V_{REF}/R_{F2}$ (Fig. 6.1 (a)), and thus to achieve the initial output voltage.

Assuming the buffer slews only for a sudden increase in the load current, i.e., $\Delta V_{TR+} > \Delta V_{TR-}$, and subtracting the effect of LDR from ΔV_{TR+}, the transient accuracy can be approximated as [74, 128]

$$\Delta V_{TR,max} \approx \frac{\Delta I_{L,max}}{C_O + C_B}\left(\underbrace{\frac{1}{BW_{CL}} + \frac{C_{par}\Delta V}{I_{SR}}}_{\approx \Delta t_1} + C_O R_{ESR}\right) - R_{O,CL}\Delta I_{L,max}, \qquad (6.4)$$

where BW_{CL} is the closed-loop bandwidth of the circuit, ΔV the voltage variation at the large parasitic capacitor C_{par} at the gate of the pass device, and I_{SR} the slew-rate-limited (SR) current of the buffer that drives the pass device. The control loop requires a bandwidth-limited delay to initiate the slewing condition. However, the response time Δt_1 is typically governed by the internal SR conditions of the feedback loop, which can be relieved by increasing I_{SR} at the expense of an increase in I_Q [74]. The third term of (6.4) results from the presence of the R_{ESR}.

6.2 Frequency Compensation

6.2.1 Uncompensated Response

A loop gain small-signal model of a linear regulator and its uncompensated response are shown in Figs. 6.3 (a) and (b), respectively [128]. The system is potentially

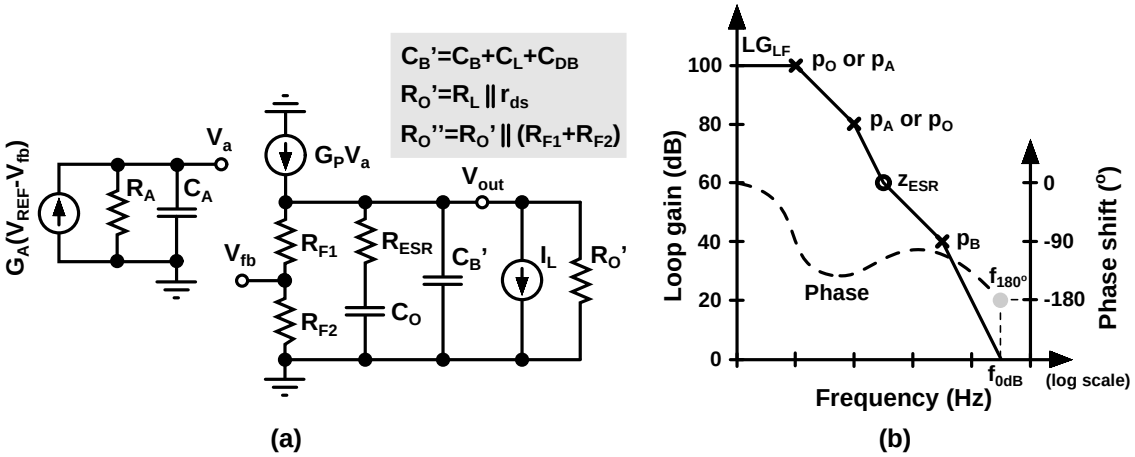


Figure 6.3: (a) Loop gain small-signal model of a linear regulator and (b) its uncompensated response.

unstable because its overall transfer function includes one zero[1] and three poles. The low-frequency loop gain is given by $LG_{LF} = G_A R_A G_P R_O"\beta_F$, the ESR zero by $z_{ESR} = 1/(2\pi R_{ESR} C_O)$, and the output pole, error amplifier pole, and bypass pole by $p_O = 1/[2\pi R_O"(C_O + C_B')]$, $p_A = 1/(2\pi R_A C_A)$, and $p_B = 1/(2\pi R_{ESR} C_B')$, respectively. The definitions for C_B', R_O', and $R_O"$ are denoted in Fig. 6.3 (a), where C_{DB} and r_{ds} correspond to the drain-bulk capacitance and output resistance of the PMOS pass device.

Depending on the regulator architecture, the dominant low-frequency pole can reside either at V_{out} (p_O) or V_a (p_A). The location of the z_{ESR}–p_B zero-pole pair is highly unpredictable [128] because of their dependence on R_{ESR} ($z_{ESR} < p_B$ by a ratio of C_O/C_B'), because of which z_{ESR} may be located either inside or outside the regulator's unity-gain frequency f_{0dB}. Irrespective of the approach used to compensate the regulator's potentially unstable two-pole response, increasing both LG_{LF} and p_A under low I_Q constraints, which also implies difficulties to keep parasitic error amplifier poles at high frequencies, compromises stability. As a result, the nominal LG_{LF} and f_{0dB} are typically restricted to below 50-60 dB and below 0.5-1 MHz, respectively [128]. Generally, it is practical to keep the parasitic poles slightly more than a decade above $f_{0dB,max}$ and introduce an equal number of left-half-plane (LHP) zeros to offset them.

6.2.2 Compensated Responses

A. Externally Compensated Response

In order to keep p_O as the dominant low-frequency pole, it is practical to use a large C_O and a PMOS pass device. Assuming $r_{ds} \approx 1/(\lambda I_L)$, where λ is the channel-length

[1]Additionally, the gate-drain capacitance C_{GD} of the pass device introduces a RHP zero that naturally tends to reside at high frequencies because of the large G_P.

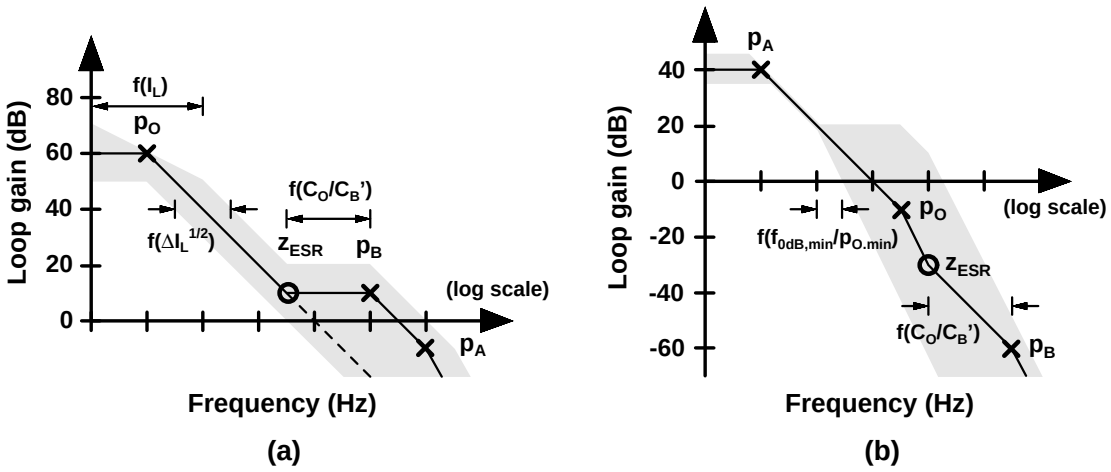


Figure 6.4: Illustration of highly-variable frequency response of (a) externally and (b) internally compensated linear regulator utilizing a PMOS pass device.

modulation parameter, the output pole can be approximated by $p_O \approx \lambda I_L/[2\pi(C_O + C_B')]$ [128]. Hence, the location of p_O increases directly proportional to the highly-variable I_L, whereas $LG_{LF} \propto G_P r_{ds}$ decreases inversely proportional to $\sqrt{I_L}$ as a result of the square-root characteristics of the PMOS pass device. Accordingly, $GBW = LG_{LF}p_O$ increases proportional to $\sqrt{I_L}$.

The highly variable frequency response of an externally compensated linear regulator utilizing a PMOS pass device is illustrated in Fig. 6.4 (a) [128]. Stabilizing a linear regulator is challenging, especially because of the large variations in I_L and R_{ESR}. In order to maintain stability, the pole p_A must reside at or above the highest possible f_{0dB}, which is probably not self-evident because of the large C_{par} at the gate of the pass device (e.g., 50-100 pF). The ratio of the maximum and minimum f_{0dB} can be approximated as $\sqrt{I_{L,max}/I_{L,min}}C_{O,max}/C_{B,min}'$ [128].

B. Internally Compensated Response

In order to keep p_A as the dominant low-frequency pole, it is convenient to use smaller output capacitors and either an NMOS source follower or a Miller-compensated PMOS as a pass device. Such pass devices make the GBW relatively insensitive to variations in I_L, as illustrated for the Miller-compensated PMOS case in Fig. 6.4 (b) [128]. Ultimately, Miller compensation introduces a dominant low-frequency pole p_A and pushes the output pole p_O to higher frequencies. As a result, the GBW becomes independent of I_L, since $GBW \propto LG_{LF}p_A \propto G_P R_O"/(2\pi R_A C_A) \approx 1/(2\pi R_A C_M)$, where C_M is the Miller compensation capacitance.

The output resistance of the pass device, which is roughly $1/g_m$ for both the follower and Miller-compensated pass devices, and thus also p_O, varies substantially over the range of I_L [128]. It is difficult to maintain high bandwidth at very low load currents, because then p_O is pulled to substantially low frequencies. As a result, p_O may nominally precede both z_{ESR} and f_{0dB} in the presence of the relatively large

C_O that may be required for transient performance [128]. Again, the frequency range of f_{0dB} is further expanded by large variations in R_{ESR}. In some low-power applications, the need for C_B, as well as very large C_O, may be avoided, in which case z_{ESR} and p_B can be moved well above the frequencies of interest.

C. External vs. Internal Compensation

The main advantages of externally compensated regulators over their internally compensated counterparts are better transient accuracy and better PSR performance, which are due to greater C_O and p_A, respectively [128]. Internally compensated regulators with restricted C_O and f_{0dB} make total on-chip integration possible and are particularly suitable for low-power applications aimed, for example, at portable battery-powered devices. In the case of internal compensation, the stability constraints become increasingly stringent under light loading conditions, which is due to the migration of p_O to lower frequencies.

6.2.3 Compensation Methods

Multi-stage amplifiers can be stabilized in many ways. Different frequency compensation methods have been discussed, for example in [129] and [130]. Moreover, an extensive analysis and comparison of such methods, among others of those shown in Fig. 6.5, can be found in [131]. Next, these techniques, which are usable in internally compensated regulators, will be discussed briefly.

A. Miller Compensation

A widely-used two-stage Miller-compensated amplifier, shown in Fig. 6.5 (a), suffers from the presence of a RHP zero ($z_{RHP} = -g_{mL}/C_M$), which substantially degrades the amplifier's stability. The RHP zero results from the out-of-phase feedforward small-signal current through the Miller capacitor $\mathrm{C_M}$. This feedforward current can be limited, for example, by adding a so-called nulling resistor $\mathrm{R_N}$ in series with $\mathrm{C_M}$ [132], as denoted in Fig. 6.5 (a). The RHP zero becomes completely eliminated when $R_N = 1/g_{mL}$. However, it is preferable to further improve the PM by making R_N larger than $1/g_{mL}$, and thus to shift the RHP zero to the LHP zero. Alternatively, the RHP zero can be effectively eliminated by adding a feedforward transconductance stage (FTS) between the amplifier input and output [129], instead of using $\mathrm{R_N}$ in series with $\mathrm{C_M}$. This so-called multipath approach is denoted by a dashed line in Fig. 6.5 (a). The FTS feeds a small-signal current, which completely cancels that flowing through $\mathrm{C_M}$ when $g_{mf1} = g_{m1}$. The advantages of this approach are that it does not affect the pole locations, unlike the use of R_N, and the compensation criteria are independent of g_{mL}, i.e., this technique is suitable for use over a large output current range [131].

B. Nested Miller Compensation

An additional buffer stage is often used in the error amplifier of a linear regulator to

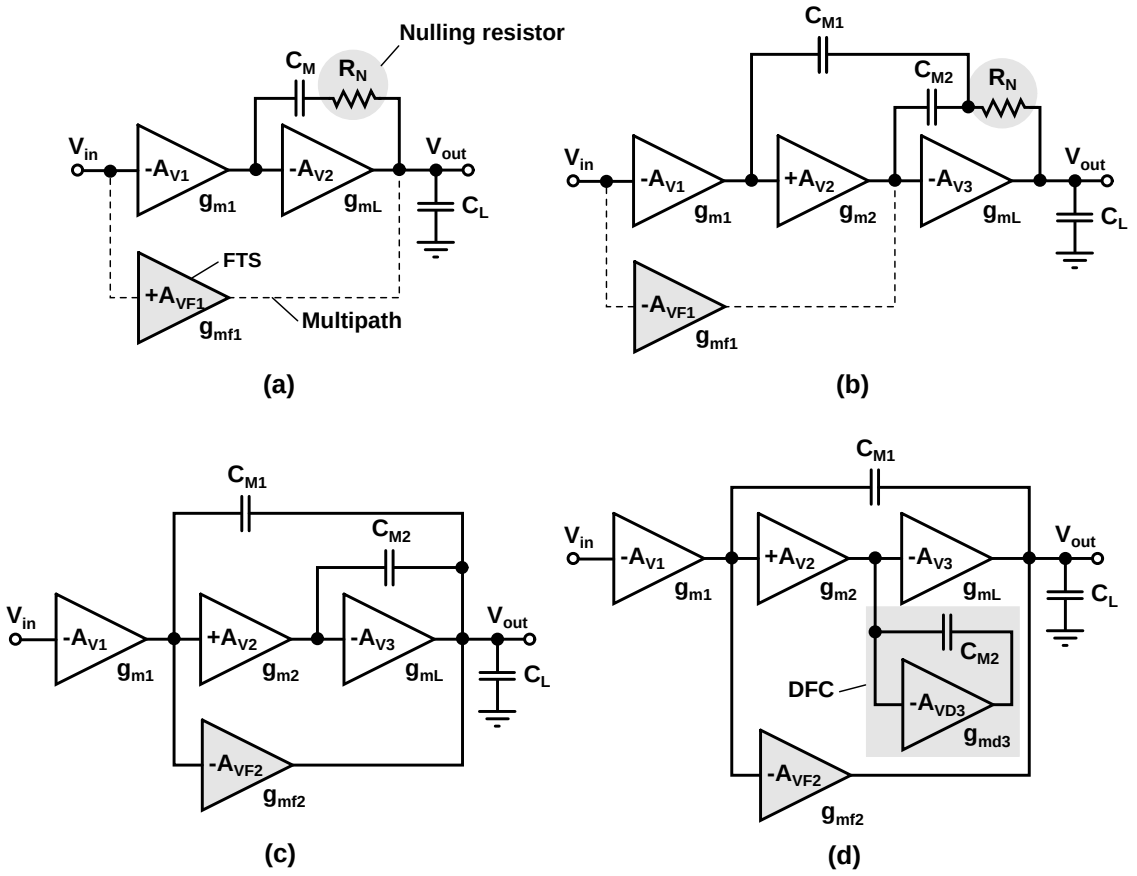


Figure 6.5: Frequency compensation methods suitable for stabilizing multi-stage amplifiers: (a) Miller compensation and (b) nested Miller compensation with nulling resistor and multipath options; (c) nested Miller compensation with feedforward transconductance stage (FTS), and (d) damping-factor-control (DFC) frequency compensation.

drive the highly capacitive gate of the pass device. In that case, the so-called nested Miller compensation technique [129] shown in Fig. 6.5 (b) can be used to maintain stability. A nested Miller-compensated amplifier has two non-dominant poles, which can appear either as two separate poles or as a complex pole pair. It is more useful to create a complex pole pair [131], because then C_{M1} and C_{M2} can be made smaller, and as a side benefit the effect of two zeros on the stability becomes negligible. When compared to the basic Miller compensation, nesting compensation further halves the achievable GBW. The stability of a nested Miller-compensated amplifier can be improved by sizing $g_{mL} \gg g_{m1}$ and g_{m2} [131]. If this condition, which is difficult to guarantee in low-power conditions, is not satisfied, the transfer function includes a RHP and a LHP zero ($z_{RHP} < z_{LHP}$). As illustrated in Fig. 6.5 (b), the RHP zero can again be eliminated either by using a nulling resistor or a multipath.

An LDO reported in [133] extends the use of nested Miller compensation with multipath by a feedforward capacitor, which helps to reduce the large Q (i.e., to increase the small damping factor) of the non-dominant complex poles, and thus to reduce

the minimum I_L that is required to keep the LDO stable. The lower limit of I_L is governed by the minimum g_{mL} that is at least required to avoid a RHP pole making the LDO unstable. This LDO is especially suitable for SoC local voltage regulation as it requires only a 6-pF on-chip capacitance and is able to provide a large output current range from 100 μA to 100 mA [133]. The bandwidth of a nested Miller-compensated amplifier can be further increased by moving the FTS from the amplifier's input to the buffer's input [131], as shown in Fig. 6.5 (c). This compensation scheme requires a smaller C_{M1} and C_{M2} and it is particularly practical for low-power designs, because it does not require the condition $g_{mL} \gg g_{m1}$ and g_{m2} to be satisfied.

C. Damping-Factor-Control Compensation

A three-stage amplifier can also be made stable without using nesting compensation, namely by replacing the feedforward capacitor C_{M2} of Fig. 6.5 (c) by a local so-called damping-factor-control (DFC) circuitry [131] at the input of the third gain stage, as illustrated in Fig. 6.5 (d). The DFC, which consists of a gain stage (A_{VD3}) and a feedback capacitor (C_{M2}), functions like a frequency-dependent capacitor. A local feedback may be needed to control the dc operating point of the DFC's high-impedance node. This technique requires a much smaller C_{M1} than the previous nesting topologies and it is especially suitable for driving large capacitive loads [131]. It is worth noting that other compensation techniques are more appropriate for driving small capacitive loads. A complete LDO circuit based on using this frequency compensation scheme is presented in [134]. The circuit is able to operate with and without a large off-chip capacitor. The transient accuracy and PSR also remain good without the off-chip capacitor, in which case the worst-case settling time is of the order of 2 μs and PSR is –30 dB at 1 MHz ($V_{IN} = 1.5$ V and $I_L = 100$ mA). In order to maintain stability without the off-chip capacitor, however, there is a lower limit of 1 mA for I_L. Depending on the design, this limit can extend roughly from 100 μA to 10 mA [134].

6.3 Circuit Techniques

Circuit designers have put much effort into developing linear regulator techniques that extend the operational life of battery-powered systems and improve regulating performance, transient accuracy, and PSR. It is worth noting that reducing an LDO's quiescent current comes at the cost of lower speed, increased input-referred offset, and degraded ac accuracy, and that both the overall and transient accuracies are trade-offs with LDO stability [128]. In addition to the efficient frequency compensation techniques [131, 133, 134] discussed earlier, other circuit techniques reported to enhance the performance of linear regulators include, among others, a current-efficient voltage buffer [74] to improve the efficiency at low load currents, a PMOS pass device with forward-biased source-bulk pn junction [74] to increase the maximum current capability, a floating reference principle [135] to enhance load

regulation, an output stage replica to guarantee stability independent of the load, as well as to improve transient response [136, 137], and an NMOS cascode device to improve the PSR performance [138, 139, 140, 141]. Next, some of the aforementioned techniques will be briefly discussed.

6.3.1 Current-Efficient Buffer

A positive feedback can be exploited to accelerate the transient response by increasing the current available for SR conditions. Figure 6.6 (a) shows such a current-efficient common-source buffer stage [74], which senses variations in I_L and adjusts the steady-state biasing conditions of the buffer device M_B accordingly . The sensing PMOS device M_S carries a considerably smaller current than the pass device M_P (e.g., $I_P = 1000I_S$). Under zero-to-light loading conditions, in which case I_S is negligibly small, the current source I_{B1} biases M_B. A sensor buffer consisting of the lateral pnp transistors Q_1 and Q_2 ensures that M_P and M_S function in the same operating region with each other [128]. Increasing the aspect ratio of M_S and the gain of the current mirror M_1-M_2 may compromise the stability of the regulator. An RC low-pass filter can be placed between the gates of M_1 and M_2 to ensure that the loop gain of the positive feedback (+FB) remains below the loop gain of the overall regulator across all frequencies of interest. The quiescent current of this kind of dynamically-biased buffer becomes negligible with respect to I_L under both low and high I_L conditions, thus circumventing the performance trade-offs between the SR and I_Q requirements of typical LDOs [142]. According to the simulation results presented in [142], by using this kind of current-efficient buffer the response time required for the regulator to respond to I_L step from zero to 50 mA in 1 ns is reduced from 60 μs to less than 3 μs [128].

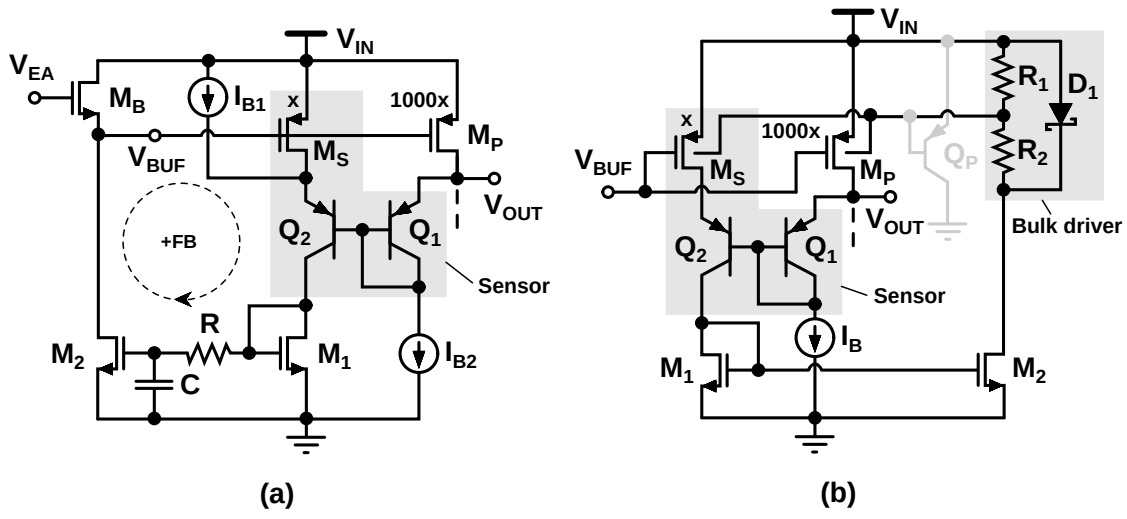


Figure 6.6: (a) Current-efficient buffer and (b) forward-biased pass device.

6.3.2 Current Boosting

It is possible to improve the driving capability of a PMOS pass device without increasing the input voltage or device size, i.e., without slowing the loop, by forward-biasing its source-bulk pn junction [74], which effectively reduces the threshold voltage $|V_{THp}|$ of the pass device. The circuit shown in Fig. 6.6 (b) uses the same kind of output current sensing principle as that in Fig. 6.6 (a) and enables the dynamic adjustment of $|V_{THp}|$ to be performed through a bulk driver [74]. The threshold voltage is reduced at higher load currents only, during which I_S, as well as the current through the bulk driver, becomes remarkable. To prevent considerable current flow into the substrate through the parasitic pnp device Q_P, the reduction in the bulk voltage level must be limited to below one V_{BE}. The limitation is guaranteed here by using a resistive voltage divider comprising R_1 and R_2 across a Schottky diode D_1 [128].

The transient response of a linear regulator can also be improved by utilizing multiple pass devices. In [143], the current through the master pass device is sensed and amplified to flow through the slave pass device, which sources additional load current without affecting the main feedback path. This linear master-slave technique [128] relaxes the demands for the error amplifier in the main feedback, but at the cost of increased dropout voltage, which is due to voltage drops across the current-sensing resistors. The non-linear master-slave regulator presented in [144] includes an analog and a digital feedback loop to control the master and slave pass devices, respectively. The slave pass device starts to supply a certain amount of current when I_L increases above a specific threshold, after which the master pass device has to supply only the difference. The advantage of these master-slave approaches is that the regulator can source the current of two pass devices at the speed and bandwidth of one [128]. In the non-linear case, however, during extreme load current changes, which require the threshold value to be crossed, the response and transition time of the digital feedback loop start to slow the circuit [128].

6.3.3 Improving Power Supply Rejection

Power supply rejection, which is defined as $PSR = 1/A_{IN} = V_{in}/V_{out}$, refers to the circuit's ability to regulate its output against small-signal variations in the input supply[2]. Figure 6.7 shows the PSR small-signal equivalent of a linear regulator [128], presented for the first time in [145]. This model assumes that the gate signal V_a varies as common-mode with respect to its corresponding source in such a way that V_{in}-dependent ac signals do not propagate through the transconductance G_P. The model consists of the feedthrough impedance Z_P and ground impedances Z_O and Z_{shunt}. Shunting impedance resulting from the negative feedback loop is given

[2]Note that the power supply rejection ratio (PSRR) often applied to amplifiers is defined as the ratio of the input-output gain A_V and supply-output gain A_{DD}.

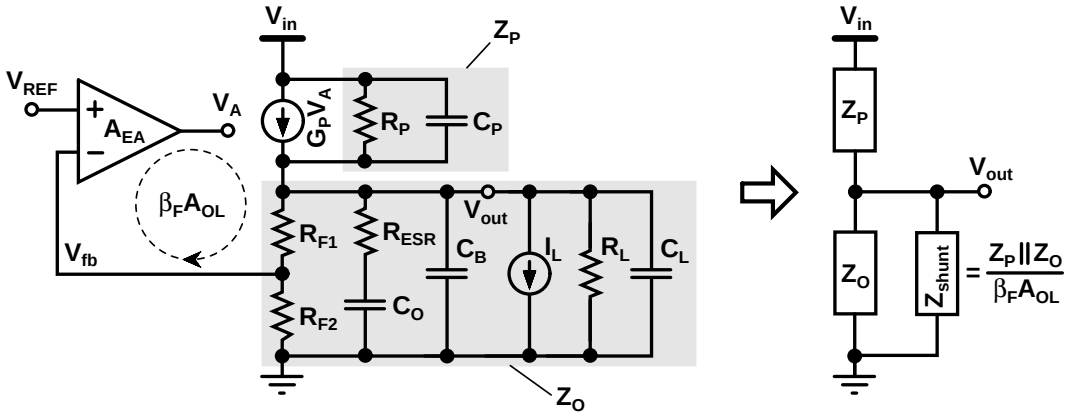


Figure 6.7: PSR small-signal model of a linear regulator.

by [128]

$$Z_{shunt} = \frac{Z_P||Z_O}{\beta_F A_{OL}} = \frac{Z_P||Z_O}{\beta_F \left[A_{EA} G_P \left(Z_P||Z_O\right)\right]} = \frac{1}{\beta_F A_{EA} G_P}, \tag{6.5}$$

where A_{EA} is the gain of the error amplifier. Generally, PSR can be improved by increasing Z_P and reducing $Z_O||Z_{shunt}$, as a result of which the use of both the negative feedback loop and the bypass capacitor is beneficial [128]. Because p_A resides at higher frequencies in the case of externally compensated linear regulators, when compared to internally compensated counterparts, the frequency range where Z_{shunt} is low (i.e., PSR is good) is extended. Generally, high values of C_O, C_B, and C_L dampen the peaking effect resulting from low p_A, whereas high-frequency PSR is limited by R_{ESR} and C_P.

There may be a need to improve the PSR of a fully-integrated LDO, because the absence of large off-chip capacitors increases the circuit's sensitivity to noise, particularly in the frequency range of 0.1-10 MHz [128], which is where dc-dc converters typically switch. Three basic methods to improve the PSR of an LDO are shown in Fig. 6.8: (a) an RC low-pass filter [146], (b) an LDO pre-regulator circuit [146], and (c) an NMOS cascode device [138, 139, 140, 141], each of which are located in the power path, thus increasing the dropout voltage of the overall regulator. The LDOs are illustrated here without an output filter and load for the sake of simplicity.

The large filter resistor $\mathrm{R_F}$, required for configuration (a) to provide a corner frequency of the order of 10-100 kHz in the absence of the large on-chip capacitor $\mathrm{C_F}$, increases the dropout voltage significantly. The disadvantage of configuration (b) is that the LDO pre-regulator is typically unable to suppress supply noise above 100 kHz [128], which is where suppression is needed most, because of the limited on-chip output capacitors. Configuration (c) provides an effective way to improve PSR over a wide range of frequencies. An RC low-pass filter is required in series with the gate of the cascode device $\mathrm{M_C}$ to prevent noise injection from the gate of $\mathrm{M_C}$ through the pass device to the output. Thanks to the absence of R_F in the power path, its size does not become a problem in this case. In order to yield a lower dropout voltage,

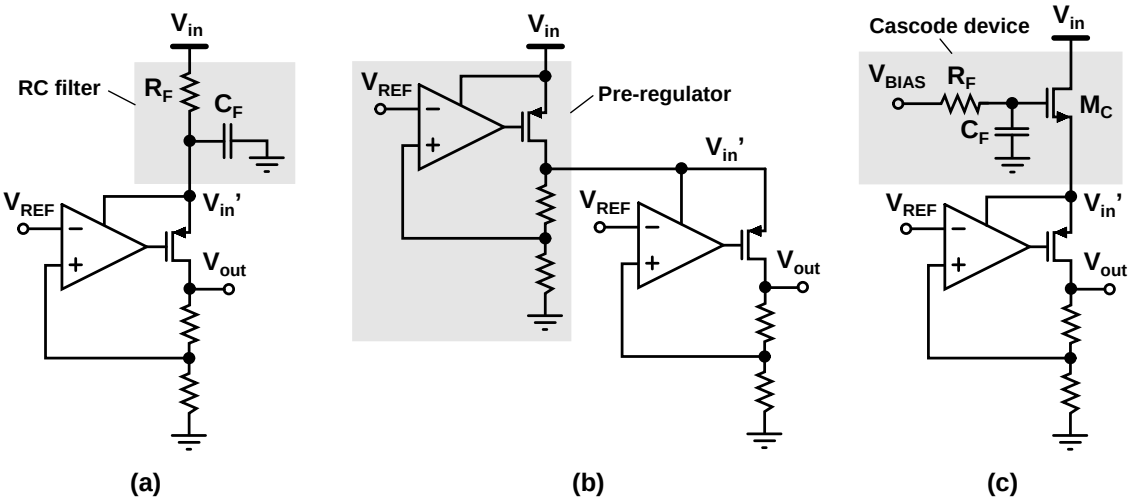


Figure 6.8: Basic methods to improve the PSR of an LDO: (a) RC low-pass filter, (b) LDO pre-regulator, and (c) NMOS cascode device.

it is practical to generate the biasing voltage V_{BIAS} by using a charge pump. The LDO circuits presented in [140] and [141] are based on configuration (c), and PSR improvements of roughly 30 dB across the entire frequency range have been reported in [141]. Different variations of configuration (c), although not as practical in low-voltage portable applications, have also been reported. The regulator presented in [138] uses an NMOS pass device with an NMOS cascode. In order to provide a low dropout voltage, two separate charge pumps are required to boost the gate of the NMOS cascode and the supply of the error amplifier. In [139], there is so much voltage headroom available that the V_{BIAS} of Fig. 6.8 (c) is connected directly to V_{in}.

6.4 Discussion

Linear regulators have become increasingly popular in the local on-chip voltage regulation of battery-powered systems because of their low complexity, low noise, and fast transient response. The potentially unstable two-pole response of a regulator can be compensated either externally or internally. The advantages of externally compensated regulators over their internally compensated counterparts include better transient accuracy and PSR performance, while internally compensated regulators make total on-chip integration possible and are particularly suitable for low-power applications.

A low-power LDO, which minimizes both the on-chip capacitance required and the minimum output current, was designed to take care of the SoC power management of the second sensor interface ASIC [P8]. In addition to the nested Miller compensation with multipath, the LDO topology that was chosen makes use of a feed-forward capacitor to provide the Q-reduction technique. The worst-case condition

for stability happens with the combination of zero load current and maximum load capacitance, i.e., when the output pole of the internally compensated LDO resides at its lowest frequency. Two LDOs are used to provide separate analog and digital regulated supply voltages of 1.0 V from a 1.2-2.75-V battery. Because of the insufficient characterization data of the standard digital cell library used in the design, the decimator had to be provided with an LDO of its own, with a programmable output voltage level ranging from 1.0 to 1.8 V.

The $\Delta\Sigma$ sensor front-end utilizing a tail-current-boosted Class AB operational amplifier was simulated to cause the worst-case charge transition of roughly 50 pC from the supply. Consequently, an LDO capable of supplying large current peaks with quite slow settling times had to be designed. In order to guarantee the maximum tolerable voltage drop of 100 mV at the LDO output, while avoiding the use of off-chip load capacitors, each LDO was equipped with a programmable 1-nF on-chip load capacitor. To minimize the silicon area required by these capacitors, metal-insulator-metal (MIM) capacitors were stacked above standard MOS capacitors. The LDO that was designed occupies 0.2 mm^2, its measured quiescent current was as low as 3.4 μA, while the measured line and load regulations were 0.5 mV/V and 6.9 mV/mA, respectively [P8].

7 Summary of Publications

This chapter briefly summarizes all the publications included in this thesis. The published results are based on the research on two low-power sensor interface ASICs designed for reading a capacitive 3-axis micro-accelerometer. The prototype circuits, presented in the publications [P1]-[P4] and partly in [P9], were fabricated in a 0.13-μm BiCMOS (bipolar complementary metal-oxide-semiconductor, i.e., a CMOS technology which includes bipolar transistors) technology, using 2.5-V tolerant high-voltage transistors, MIM capacitors, and high-resistivity polysilicon resistors. Npn bipolar transistors, which are not available in standard CMOS technology, were used only in the bandgap voltage reference. Low-voltage transistors were used only in the frequency reference designed for the micro-controller unit. The prototype circuits presented in the publications [P5]-[P8] and partly in [P9], were fabricated in a 0.25-μm BiCMOS technology, using MIM capacitors and high-resistivity polysilicon resistors. All the circuit structures used in these latter prototypes are implementable with standard CMOS technology.

[P1] A 3 μW, 2 MHz CMOS frequency reference for capacitive sensor applications

This paper presents a micropower 2-MHz frequency reference based on a source-coupled CMOS multivibrator. Neglecting the power dissipated by the output buffer, the frequency reference that was implemented typically dissipates 3.0 μW from a 1.8-V supply at room temperature. According to the measurements, the oscillation frequency stays within $\pm 2.5\%$ of the nominal frequency when both the supply and temperature ranges, i.e., 1.62-2.75 V and $-35 \ldots +85$°C, are considered. The results presented in this paper prove that the frequency reference that was designed is well suited for low-frequency, low-power sensor applications.

[P2] A micropower voltage, current, and temperature reference for a low-power capacitive sensor interface

A micropower voltage, current, and temperature reference is introduced in this paper. The core circuit comprises the Brokaw's bandgap reference, which requires the use of npn bipolar transistors, which are not available in the standard CMOS process. As a whole, this reference circuitry provides all the required reference voltages and currents, together with analog temperature information. Nominally, it draws 23.1 μA from a 1.8-V supply. According to the system measurements, the required resolutions, 10 bits for the reference voltages and 9 bits for the temperature reference, are achieved. The measured temperature coefficient of the voltage reference is 9.9 ppm/°C, while the output of the temperature reference is linear with a 4.9-mV/°C slope.

[P3] A 62μA interface ASIC for a capacitive 3-axis micro-accelerometer

In this paper, a low-power sensor interface ASIC for a capacitive 3-axis micro-

accelerometer is presented. The ASIC consists of a front-end, two algorithmic ADCs, two frequency references, and a voltage, current, and temperature reference circuit. Die area and power dissipation are reduced by using time-multiplexed sampling and varying duty cycles as low as 0.3%. The interface chip occupies an active area of 0.51 mm^2 and draws 62 μA from a 1.8-V supply while sampling each of four proof masses at 1 kHz and temperature at 100 Hz. The results measured with a $\pm$4-g capacitive 3-axis micro-accelerometer yield a dynamic range of 65 dB at a 100-Hz signal bandwidth.

[P4] A micropower interface ASIC for a capacitive 3-axis micro-accelerometer

This paper presents a micropower interface ASIC for a capacitive 3-axis micro-accelerometer. The IC includes a front-end, two algorithmic ADCs, two frequency references, and a voltage, current, and temperature reference circuit. Die area and power dissipation are reduced by using time-multiplexed sampling and varying duty cycles down to 0.3%. The chip, with a 0.51-mm^2 active area, draws 62 μA from a 1.8-V supply while sampling temperature at 100 Hz, and four proof masses, each at 1.04 kHz. The results measured with a $\pm$4-g capacitive 3-axis micro-accelerometer yield a sufficient dynamic range for 10-bit operation at a 100-Hz signal bandwidth. It is demonstrated that the use of an open-loop configuration for sensor readout is feasible for low-power applications.

[P5] A 1.5μW 1V 2nd-order $\Delta\Sigma$ sensor front-end with signal boosting and offset compensation for a capacitive 3-axis micro-accelerometer

A 2nd-order $\Delta\Sigma$ sensor front-end for a capacitive 3-axis micro-accelerometer is introduced in this paper. A method for signal boosting and offset compensation is also presented. The front-end, with a 0.49-mm^2 silicon area draws 1.5 μA from a 1.0-V supply while sampling each of three proof masses at 4.096 kHz. With a $\pm$2-g capacitive 3-axis accelerometer, an accuracy of 12 bits is achieved at a 1-Hz signal bandwidth.

[P6] A micropower low-dropout regulator with a programmable on-chip load capacitor for a low-power capacitive sensor interface

This paper presents a micropower LDO. With on-chip voltage and current references, and an on-chip 1-nF programmable load capacitor, it occupies an active silicon area of 0.18 mm^2. The LDO has an input voltage range of 1.2-2.75 V and a nominal output voltage of 1.0 V, and it is stable with zero load current over the load capacitance range of 0-1 nF. Including the reference circuits, the LDO typically consumes a quiescent current of 7.6 μA. According to the measurements, the regulated output has a temperature coefficient of 57.2 ppm/°C, a line regulation of 2.71 mV/V, and a load regulation of 1.64 mV/mA.

[P7] A 21.2 μA $\Delta\Sigma$-based interface ASIC for a capacitive 3-axis micro-accelerometer

In this paper, a micropower interface ASIC for a capacitive 3-axis micro-accelerometer is presented. The fully-integrated sensor interface consists of a $\Delta\Sigma$ sensor front-end, a decimator, a frequency reference, a clock generator for the front-end, a voltage and current reference, the required reference buffers, and the LDOs needed for system-on-chip power management. The interface provides operating modes for the 1- and 25-Hz signal bandwidths. The chip, with a 1.72-mm^2 active area, draws 21.2 μA in 1-Hz mode, and 97.6 μA in 25-Hz mode, from a 1.2-2.75-V supply. With a $\pm$2-g capacitive 3-axis accelerometer the noise results yield dynamic ranges of 70 and 67 dB for dc input signals in the 1- and 25-Hz modes, respectively. The measurement results that are presented prove that by using both open-loop configuration and inherent capacitance-to-digital conversion, an alternative low-voltage low-power sensor interface can be implemented.

[P8] A micropower $\Delta\Sigma$-based interface ASIC for a capacitive 3-axis micro-accelerometer

A fully-integrated micropower sensor interface ASIC for a capacitive 3-axis micro-accelerometer is presented in this paper. A detailed analysis with transfer functions is presented for the $\Delta\Sigma$ sensor front-end, which operates mechanically in an open-loop configuration. Furthermore, the interface IC includes a decimator, a frequency reference, a clock generator for the front-end, a voltage and current reference, the required reference buffers, and the LDOs needed for system-on-chip power management. The interface provides operating modes for the 1- and 25-Hz signal bandwidths. The chip, with a 1.73-mm^2 active area, typically draws 21.2 μA in the 1-Hz mode, and 97.6 μA in the 25-Hz mode, from a 1.2-2.75-V supply. The noise results yield dynamic ranges of 76 and 73 dB for a $\pm$4-g dc signal range in the 1- and 25-Hz modes, respectively. The measured $\pm$4-g dc ramps show non-linearities of the order of $\pm$0.35% from the full-scale range. According to the performance comparison, by using the chosen circuit techniques, a competitive, low-voltage, low-power, high-performance sensor interface can be implemented.

[P9] Impulse sensitivity function-based phase noise study for low-power source-coupled CMOS multivibrators

This paper presents two micropower frequency references based on a power-optimized source-coupled CMOS multivibrator. The 2.0-MHz frequency reference uses a nominal 1.8-2.5-V supply, while the 24.6/307.2-kHz frequency reference that provides two active modes operates with a 1.0-V supply. With 1-pF load capacitances, these frequency references typically consume 6.7 μA and 230/750 nA, respectively. This paper concentrates mainly on the phase noise study of the proposed frequency references. The procedure used to apply the ISF-based phase noise method to CMOS oscillators is described in detail. The phase noise results obtained with this method for the two multivibrators correlate well with the measurements.

8 Conclusions

In the MEMS inertial market, the consumer area is experiencing the strongest market growth and is expected to overtake the automotive sector in 2011. Small size, low power dissipation, and 3-axis sensing are the key features of MEMS accelerometers aimed at battery-powered consumer applications. As a respond to the aforementioned challenges, the research described in this thesis concentrates on the design of two low-power sensor interface ASICs [P4, P8] that were designed for reading a 3-axis bulk-micromachined capacitive accelerometer. In both designs the accelerometer readout is performed mechanically in an open-loop configuration, which supports the need for a simple implementation, i.e., small silicon area and power dissipation, and a limited voltage range available for electrostatic feedback. It is very important to consider electrostatic forces in an open-loop configuration, because they cause the reduction of the spring constant, nonlinearity, and, in extreme cases, pull-in. Regardless of the system configuration, the interface electronics requires a front-end circuit that converts the capacitive information from the mechanical sensor element to a voltage. The very small low-frequency signals available from micro-accelerometers, together with the large parasitics, set strict performance requirements for electronic interfaces. In addition to the sensor readout, i.e., the C/V and A/D conversions, and an application-specific amount of DSP, typically current and voltage references, frequency references, and supply voltage regulators are required to implement complete fully-integrated sensor interface ASICs. Including a temperature reference with a digital output, in turn, makes possible the compensation of temperature-dependent non-idealities in the DSP.

The first sensor interface ASIC [P4], with an active core area of 0.51 mm^2, was implemented in a 0.13-μm BiCMOS process. The chip was measured to draw 62 μA from a 1.8-V supply while sampling temperature at 100 Hz and four proof masses, each at 1.04 kHz. Die area and power dissipation were reduced by using time-multiplexed sampling and varying duty cycles down to 0.3%. With a ±4-g accelerometer, the measured noise floors in the x-, y-, and z-directions were 482, 639, and 662 $\mu g/\sqrt{Hz}$, respectively. These results yield a sufficient dynamic range for 10-bit operation in the 100-Hz bandwidth. The second ASIC [P8], with a 1.73-mm^2 active core area was implemented in a 0.25-μm BiCMOS process. This $\Delta\Sigma$-based sensor interface was designed to provide operating modes with 12-bit resolution for the 1- and 25-Hz signal bandwidths, from which the former was optimized for very low power dissipation at the cost of reduced bandwidth, and is intended, for example, for activity monitoring in otherwise powered-off devices. This chip was measured to typically draw 21.2 μA in the 1-Hz mode, and 97.6 μA in the 25-Hz mode, from a 1.2-2.75-V supply. In the 1- and 25-Hz modes with a ±4-g accelerometer, the measured noise floors in the x-, y-, and z-directions were 1080, 1100 and 930 $\mu g/\sqrt{Hz}$, and 360, 320 and 275 $\mu g/\sqrt{Hz}$, respectively. Both the sensor interface systems that were imple-

mented achieve competitive Figures of Merit[1] (FOMs) [P8], when compared with the best commercially available, low-g, low-power, accelerometers. The minimum possible supply voltage of the battery-powered $\Delta\Sigma$ sensor interface, i.e., 1.2 V, is significantly smaller than that of the other devices, i.e., $\geq$1.7 V.

The overall performance and silicon area of the second sensor interface ASIC could be further optimized by using direct wire bonding between the interface IC and the sensor, by avoiding the use of the third LDO by using a tailored digital standard cell library working down to 0.9 V, and by individually optimizing both remaining LDOs. Moreover, because the reference voltage buffer dominates the total current consumption, especially in the 25-Hz mode, an effort should be make to better optimize the demands for such buffers. As a possible future work, in addition to carefully considering the aforementioned points, a sensor interface ASIC capable of operating in the sub-1-V environment could be implemented. In order to manage with such low supply voltages, technology scaling, i.e., lower V_{TH} transistors, is required compared to the demonstrated designs. One of the topics that will certainly excite more and more attention in the future is energy autonomy. Therefore, as a next step from low-power 3-axis micro-accelerometers towards their fully autonomous counterparts, a micro-accelerometer system that harvests energy from one or several energy sources available in the ambient, such as motion, vibration, thermal, and RF radiation, could be studied. In order to enable the energy autonomy of a system over its entire lifetime, an energy harvester should be combined with a small-size rechargeable battery. Before the harvested power could be used to power the sensor interface electronics, it should be conditioned by using rectification and dc-dc conversion. As a result, from the IC design point of view, the related research topics would include power conditioning and ultra-low-power sensor interfacing. In order to keep the amount of harvested energy, as well as the size of the total system, practical, the overall system performance should likely be traded off for lower power dissipation.

[1]The updated version of the performance comparison figure presented in [P8] is included in errata.

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