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High-resolution continuous-time interface for micromachined capacitive accelerometer

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SUMMARY

A continuous-time accelerometer interface is feasible when high dynamic range together with wide signal band is required. In this paper, design of interface electronics for a capacitive sensor is presented. The interface design is focused on attaining resolutions up to 120 dB together with a signal bandwidth of 300 Hz. The essential circuit structures of the interface will be presented and analyzed in detail. Important sources of instabilities and issues that affect the dynamic properties of the sensor are discussed. Measured and simulated results of the closed-loop sensor will be provided to support the theory. Copyright © 2008 John Wiley & Sons, Ltd.

KEY WORDS: accelerometer; closed-loop; servo; MEMS; analog; continuous-time; high-resolution; high-performance

1. INTRODUCTION

Typically, high-precision capacitive accelerometers operate in a closed-loop, thus allowing us to reach for better linearity, resolution and higher signal band compared with an open-loop sensor interface. Although this is achieved mainly at the expense of increased power consumption, complexity or costs, the closed-loop operation provides features such as damping of high-Q resonance modes, which cannot be achieved in an open-loop configuration [1].

Capacitive accelerometers, operating as electromechanical sigma-delta loops, have gained increasing popularity [2]. However, in applications where high resolution and linearity and large signal band are the main requirements, an analog readout interface can provide an alternative way

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of implementing the accelerometer. Benefits of continuous-time readout are clear: elimination of noise folding effects [3], any residual motion [4] and requirements for very high clock frequencies, which are often needed to attain large bandwidth and resolution. One common reason for not using a continuous-time force-feedback loop for accelerometers is the potential threat of pull-in in the case of a shock condition [5]. This problem can be mainly overcome by preventing the short-circuit condition in the sensor element [6] and verified finally through simulations of the interface reverting back to stable operation despite the momentary shock.

New implementations of continuous-time accelerometers, especially those utilizing a force balancing feedback, are relatively scarce. Examples of earlier work are given in [6, 7], where the force-feedback is active in the signal band, which, on the other hand, is lower than the resonance frequency of the sensor. In [8] the force-feedback is active below the signal band of interest, hence leaving the sensor to operate in open-loop at the actual signal band. The high performance sensor of [9] clearly benefits from the possibility of using a sensitive sensor with a low resonance frequency, while the feedback increases the signal bandwidth up to the required value. However, very few details of the interface are presented. Compared with published work this paper presents detailed description of the interface electronics, which allows the signal bandwidth to be increased up to or even above the resonance frequency of the sensor, hence allowing a sensor with an optimized sensitivity to be used. Measured data proves the functionality of the interface. Further theoretical basis for recognizing the system stability and linearity affecting issues is also provided. The resulting high-performance sensor, where the signal band can be designed to cover also dc, is aimed at applications that require high-performance, for example, to replace ac-coupled geophones.

In this paper, first the structure and system-level design of the high-resolution continuous-time interface is presented in Section 2. The system description is followed by an analysis of the required building blocks of the interface and essential stability-limiting factors. In Section 3 the sensor dc linearity is addressed and the effect of higher frequency vibrational modes of the sensor is discussed. Finally, in Section 4 measured results of the closed-loop sensor are provided.

2. DESIGN AND PROPERTIES OF CLOSED-LOOP ACCELEROMETER

The block diagram of the accelerometer is shown in Figure 1. The bulk-micromachined sensor consists of a single seismic mass between two fixed electrodes. For continuous-time system, the feedback and the readout are separated in frequency domain. The differential carrier, fed to the fixed electrodes of the sensor, is used for the readout. Any mismatch between the capacitors of the sensor causes charge to flow to the feedback capacitor of the charge-sensitive amplifier (CSA). The carrier frequency signal is amplified using a chain of high-pass filters (HPF), which also prevents the feedback signal from saturating the readout. The carrier frequency signal is demodulated coherently using an in-phase sample of the original carrier. The downconverted signal, fed through a low-pass filter (LPF) and a controller, is used to balance the forces acting on the sensor seismic mass. The feedback, the controller output, is connected to the non-inverting input of the operational amplifier (OPAMP) in the CSA. The feedback voltage, connected to the sensor via the virtual ground, biases the middle electrode of the sensor in such a way that the electrostatic forces balance the sensor element.

In order to better understand the functionality of the interface, the system properties are examined next. The loop dynamics can be designed using a linear model for the system. The model can

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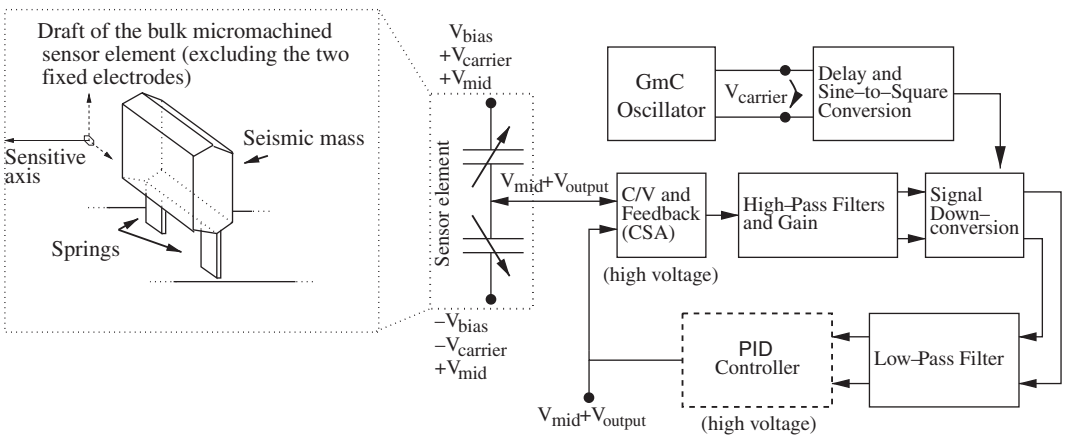

Figure 1. A block diagram of the accelerometer interface and the electrical model of the sensor. A draft of the sensor element used is also included. The blocks denoted using dashed and dotted lines are external to the ASIC.

be constructed initially by assuming that the transfer functions for the LPF, mixer, and HPF are frequency independent in the band of interest. Now, the system dynamics are determined by the controller

$$H_{\mathrm{PID}}(s)=\frac{K_i}{s}+K_0+\frac{sK_d}{s/\beta+1}=\frac{s^2A+sB+C}{s^2D+s} \tag{1}$$

together with the sensor (the resonator)

$$H_{\mathrm{RES}}(s)=\frac{1}{s^2M+s\gamma+K} \tag{2}$$

Coefficients K_i, K_0 and K_d are the gains of the integrator, the proportional controller and the differentiator, which together form the PID controller. The pole of the differentiator is determined by β, and the resonator parameters M, γ and K determine the sensor mass, damping coefficient and spring constant, respectively. The primary loop, denoting the dynamics of the actual closed-loop accelerometer, is shown in Figure 2, where G_{LPF}, G_{MIX} and G_{HPFs} represent the constant gains of the corresponding blocks, $G_{V/C}$ the gain of the CSA, $G_{F/V}$ the gain from voltage to force and $G_{C/X}$ the gain from proof mass position to capacitance [5]. A linear model for the system can be derived as the electrostatic force, which has a quadratic dependency on voltage, is fully linearized when the ideal symmetry of the capacitive half-bridge is assumed. It is also presumed that the interface operates linearly and that the sensor seismic mass–displacement induced by acceleration is negligible within the closed-loop.

The sensor is designed for a signal bandwidth of 300 Hz. The primary loop has four dominant poles, which can be set as desired by selecting proper four parameters (A,B,C,D) for the controller. A Butterworth-type polynomial was selected for the presented system. When the system output is taken from the output of the PID controller, it has two zeros, which depend on the controller and sensor properties. Hence, they cannot be directly controlled due to insufficient number of degrees of freedom in the selected controller. If the sensor output is taken from the output of the integrator

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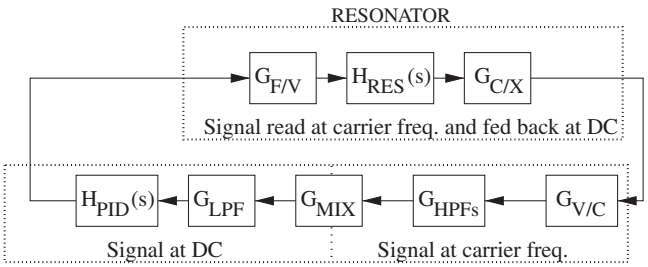

Figure 2. Linear model of the accelerometer. Only the primary vibration mode of the sensor is included in the model.

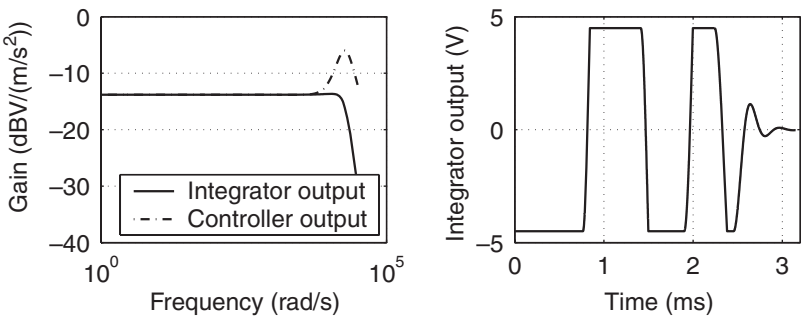

Figure 3. Left: sensor transfer function obtained using linear model. Right: sensor recovery from 1000g initial shock. The integrator output is limited to maximum voltage that is required during normal operation. By the end of settling, behavior corresponds to that of the linear model.

(I-controller) instead of the whole controller, the effect of the remaining single zero is very limited at the signal band as shown in Figure 3 (left). The effect of zeros is also alleviated when the actual signal bandwidth is smaller than the pole frequency of the closed-loop sensor. The pole frequency of the sensor indicates the location of the four dominant poles of the system.

After determining the desired coefficients for the PID controller, the LPF must be included in the model to ensure that its effect on the system dynamics remains small. Inclusion of the HPFs and the demodulator in the linear model is more complicated as the signal is modulated at the carrier frequency before the amplitude detection. These blocks typically have a negligible effect on the system dynamics.

With the sensor structure preventing short circuit from occurring and with a careful design of the loop, the accelerometer can also recover from a shock as shown by the simulation in Figure 3 (right), performed with Matlab Simulink. Similar behavior was also measured except that, in measurements, the parasitic vibrational modes of the sensor limited the settling time.

With a linear model only predicting the ideal behavior, one must take into account also the other loops caused by several different non-idealities. One loop is created by the feedback signal, connected to the CSA, which traverses not only the sensor (primary loop) but also the HPFs, due to finite attenuation at low frequencies. After this, the signal is upconverted and attenuated in the LPF before closing the loop after traveling once more through the demodulator. Insufficient attenuation, provided by the LPF and HPFs, results in an unstable system, the behavior of which

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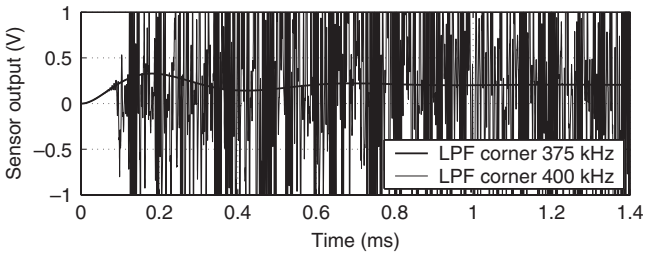

Figure 4. The figure shows a system response to an acceleration step of $1\,\mathrm{m/s^2}$ in two cases. In the latter case, the fifth-order LPF corner frequency is increased by 10% and the system becomes unstable. In these Matlab Simulink system simulations, the sensor has the four dominating poles at 2 kHz and the demodulator used is ideal.

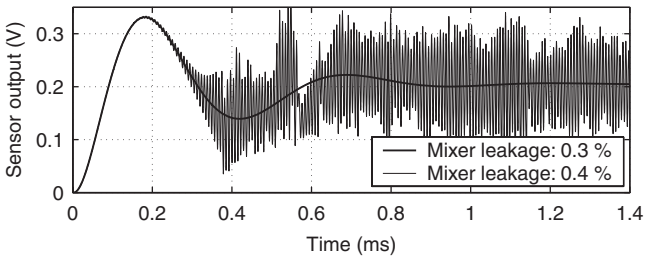

Figure 5. The figure shows a system response to an acceleration step of $1\,\mathrm{m/s^2}$. In the two cases of the figure the demodulator leakage is increased from 3 to 4%, which leads to uncontrollable oscillations. In these Matlab Simulink system simulations the sensor has the four dominating poles at 2 kHz.

is shown in Figure 4. In this case stability can be improved by increasing the attenuation, which the LPF provides at the carrier frequency and the HPFs at low frequencies.

Another important loop originates from the mixer non-idealities, which can lead to signal leakage. The leakage, together with a high-enough maximum gain in the loop, results in an oscillating system. This source of instability is problematic as, for example, start-up transients can easily saturate the mixer and cause the loop to oscillate. The LPF and HPFs, together with the leaking mixer, determine the gain, which is usually highest between the pass bands of the filters. The instability caused by the mixer leakage is shown in Figure 5. In the example case of the figure, the maximum loop gain is too high and should be considerably decreased. This can be accomplished by lowering the LPF corner frequency and increasing the HPFs corner frequencies. However, these actions must not compromise the stability of the primary loop because of, for example, excessive phase change caused by the LPF.

Technology used for the design of the interface is a 0.7 μm high-voltage (HV) CMOS technology with high-ohmic poly silicon resistors, analog capacitors and 5 V nominal supply. The technology offers also unoptimized bipolar transistors, vertical NPNs with a cut-off frequency (f_t) of roughly 1 GHz and lateral PNPs. Owing to wide base and resulting very low f_t, the use of PNPs is limited to dc sources. The bulk-micromachined sensor element used for simulations has a resonance frequency of 650 Hz, Q-value of 500 and dc sensitivity of $3.8\,\mathrm{pF}/g$. However, the element used for the measurements has the resonance at 450 Hz and Q-value of roughly 30. Despite the fairly

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low Q-value the Brownian equivalent acceleration noise is $60\,\mathrm{ng/Hz^{1/2}}$, which is low enough compared with the noise of the interface. The following sections describe the properties of the building blocks of the interface in detail.

2.1. Controller properties and readout gain

The gain of the readout is an important factor when determining the PID controller component values. For example, doubling the gain before the controller requires that controller gain is halved in order not to change the total gain. The gain can be halved by doubling the value of the controller resistors. Now that the noise performance has forced the capacitors to dominate the area of the controller, the doubling of the resistors will have only a small effect on the total chip area. The resulting noise power at the controller doubles, but when referred to the input of the readout, the noise is halved. Thus, high gain before the controller indicates that larger resistors and smaller capacitors can be used in the controller.

For a system with a maximum readout gain from the CSA input to the LPF output of 24 V/pF, the K_i would be 6.7 krad/s and $1/K_d$ 21 krad/s. Corresponding maximum tolerated input-referred noise of the controller is $0.5\,\mu\mathrm{V/Hz^{1/2}}$, when the controller is allowed to spend $\frac{1}{4}$ of the total noise voltage budget of the accelerometer (SNR of 120 dB, bandwidth of 300 Hz and system dominant poles at 3 kHz). This implies that the integrator resistor and capacitor values are, for example, $2\,\mathrm{M\Omega}$ and 75 pF and the corresponding derivator components $1\,\mathrm{M\Omega}$ and 50 pF. With $1.5g$ amplitude sine excitation at 300 Hz, the signal level at the LPF output stays within ± 1.1 V and thus indicates that the controller for the presented system is well integrable. Differential implementation of the controller offers a differential signal further to the A/D converter. However, any potential circuits following the controller must have a low-noise content, for this case $31\,\mathrm{nV/Hz^{1/2}}$ when comprising $\frac{1}{4}$ of the total noise voltage. Also reference voltages, used for biasing the sensor, must satisfy the same maximum noise density. This means that it is desirable not to have any active circuits between the controller and the CSA. Because of the noise requirements it is also rather difficult to split the PID controller into multiple sections (proportional controller, differentiator and integrator) so that the effect of uncontrollable zeros could be avoided (see Figure 3).

The capacitive signal of the sensor element decreases rapidly above the resonance frequency of the sensor. This indicates that, with a constant gain of the closed-loop accelerometer, the noise will start to increase with decreasing capacitive signal. Hence, although bandwidth can be increased through closed-loop operation, noise that is limited by electronics will increase rapidly, 40 dB/decade, above the resonance frequency of the open-loop sensor.

A schematic of a PID controller suitable for the purpose is shown in Figure 6. It is capable of realizing a pair of complex zeros, which is required when sensor bandwidth needs to be increased through the closed-loop operation and needs only two amplifiers. The infinite dc gain of the controller forces the signal at the controller input to zero at dc and effectively attenuates the low-frequency components. This, on the other hand, attenuates distortion that stems from the movement of the sensor seismic mass. For the implemented sensor, the controller is left external to allow easier control of system dynamics. The transfer function of the controller is

$$H_{\mathrm{PID}}(s) = -\frac{\dfrac{R_2 C_1 (R_x + R_1)}{R_1} s^2 + \left(\dfrac{R_2}{R_1} + \dfrac{C_1 R_x}{C_3 R_3} + \dfrac{C_1 R_2 (R_x + R_1)}{R_1 R_3 C_3} \right) s + \dfrac{R_2 + R_1}{C_3 R_3 R_1}}{R_x C_1 s^2 + s} \tag{3}$$

which corresponds directly to (1).

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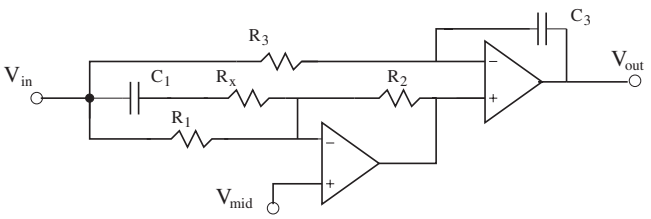

Figure 6. Structure of the external PID controller used. Topology enables a pair of complex zeros with two operational amplifiers.

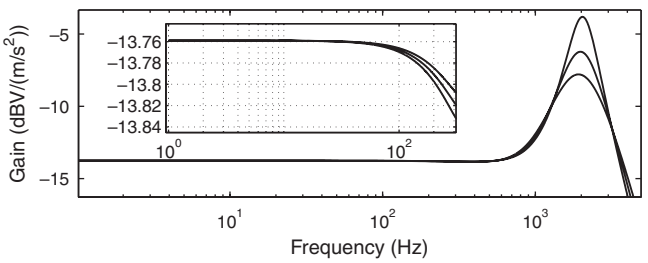

Figure 7. Gain transfer functions of the sensor, when the resistor values in the controller are assumed to vary ±10% from the nominal value. The nominal pole frequency of the sensor is 2 kHz.

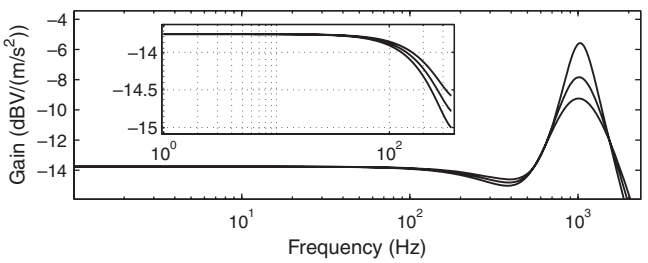

Figure 8. Gain transfer functions of the sensor, when the resistor values in the controller are assumed to vary ±10% from the nominal value. The nominal pole frequency of the sensor is 1 kHz.

In some cases, process variations require calibration to maintain stability of the sensor. Even with calibration, if the controller is integrated, the high-ohmic polysilicon resistors typically have a fairly high-temperature dependency. When the system pole frequency is set higher than the actual sensor signal bandwidth, the temperature effects at the signal band will decrease. This can be observed by comparing Figure 7 with a 2 kHz system pole frequency and Figure 8 with a 1 kHz pole frequency. In both cases, the sensor model is the same and the same signal bandwidth of 300 Hz is magnified in the figures.

2.2. Charge-sensitive amplifier

The CSA must be able to read the signal from the sensor at the carrier frequency and close the electrostatic feedback around dc. The feedback path requires low-noise properties at low

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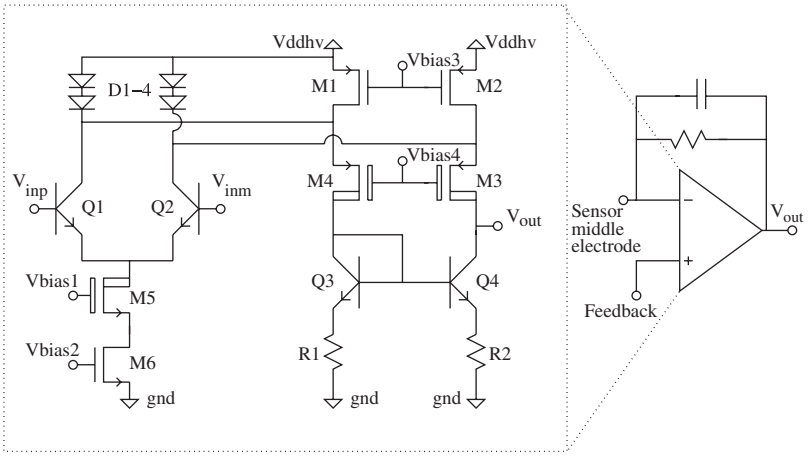

Figure 9. Operational amplifier of the HV CSA.

frequencies, implying very low flicker noise content. Low-noise operation is also required at the carrier frequency, where the signal is read from the sensor. The schematic of the folded cascode operational amplifier (OPAMP), which fulfills these requirements, is shown in Figure 9. The high-voltage supply (*Vddhv*) is used, as the electrostatic feedback requires voltages close to $\pm 3.1\,\mathrm{V}$ for $\pm 1.5g$ acceleration and V_{bias} of $3.5\,V$. The diodes D1-4 protect the low-voltage transistors M1 and M2 from excess drain–source voltage during power-up. BJT transistors $Q1$–$Q4$ are used to reduce flicker noise. For the same reason the use of NMOS transistors is totally avoided in the differential signal path as their flicker noise is considerably higher than in PMOS transistors. The SNR is given by

$$\mathrm{SNR} = 10\log\frac{Q_{\mathrm{signal}}^2}{2V_n^2(C_s + C_{\mathrm{FB}})^2 + I_n^2/\omega_c} \tag{4}$$

where Q_{signal} is the signal charge, C_s the total sensor capacitance, C_{FB} the CSA feedback capacitor, ω_c the carrier frequency, $V_n = 2kT/g_m = 2kTV_T/I_C$, $I_n = 2qI_C/\beta(\omega_c)$, I_C the single BJT collector current, k the Boltzmann constant, T the temperature, V_T the thermal voltage, $\beta(\omega_c)$ the BJT current gain at the carrier frequency, g_m the transistor transconductance and q the elementary charge. It is assumed that the carrier frequency is much higher than the corner frequency of the CSA. Now, the optimal I_C is given by

$$I_C = \sqrt{\frac{2\beta(\omega_c)\omega_c^2(C_s + C_{\mathrm{FB}})^2 kTV_T}{q}} \tag{5}$$

Simulated noise charge with the sensor connected is $0.1\,\mathrm{aC/Hz^{1/2}}$ at 3 MHz (carrier frequency), which is less than $\frac{1}{4}$ of the total noise voltage budget of the sensor. The noise density at the sensor middle electrode is $35\,\mathrm{nV/Hz^{1/2}}$ at 1 Hz and $4\,\mathrm{nV/Hz^{1/2}}$ at 100 Hz and contributes to total noise through the electrostatic feedback ($\frac{1}{4}$ of the budget corresponds to $31\,\mathrm{nV/Hz^{1/2}}$ for white noise). The feedback capacitor and resistor sizes are 2 pF and $1\,\mathrm{M\Omega}$, respectively. The gain bandwidth is 31 MHz and *Vddhv* is tolerated up to 25 V. The transistors M_1 and M_2 both supply $200\,\mu\mathrm{A}$,

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while 140 μA of this is consumed by the transistors of the input pair. The maximum allowed noise content of *Vddhv* is determined by the power supply rejection ratio of the amplifier. For the designed amplifier the noise content of *Vddhv* is allowed to be roughly $1\,\mu V/Hz^{1/2}$.

2.3. Carrier

The carrier frequency is determined, on the one hand, by the complexity of the filters, pole frequency of the sensor and, on the other hand, by the power consumption specifications and technology. It also relieves the design if the carrier frequency is higher than any parasitic vibration mode of the sensor. Selected frequency ω_c of the sinusoidal carrier is 3 MHz and it is generated using a GmC-oscillator. Compared with an open-loop sensor the carrier amplitude does not determine the sensor gain directly and therefore the amplitude stability requirements are considerably eased. Frequency stability is an important parameter, but relieved as well if the delays of the signal and clock path match at the frequency range where the oscillator drifts.

The most critical design parameters for the carrier generator are both the common mode signal and noise of the differential carrier. This is due to the large gain from common mode carrier to the output of the CSA, because of the sensor capacitors that can be considered parallel (see Figure 1). In order to achieve system SNR of 120 dB at a 300 Hz bandwidth, the common mode noise level must be below $14\,nV/Hz^{1/2}$ at the carrier frequency with a 2 V differential carrier amplitude, even if all the noise is assumed to come from this single source. This also rules out the square wave carrier as single gate delay mismatch in differentiality easily saturates the readout.

Differential noise of the carrier in a closed-loop system must be calculated for the maximum differential capacitance, typically occurring with the full-scale maximum frequency acceleration. Also, any mismatch between the sensor capacitors must also be taken into account. For an ideally balanced sensor, this noise source is negligible compared with common mode noise. As a comparison, an open-loop sensor with single-ended readout requires low-noise behavior from the differential signal also.

2.4. Demodulation

A coherent detection of envelope is utilized. A full-wave rectifier, used as the demodulator, is relatively simple to implement as a switching demodulator (see Figure 10). However, the duty ratio of the clock signals used for demodulation should be as close to 50% as possible to reduce mixer leakage. The amount of leakage tolerated depends on the filters and the attenuation they provide. The mixer also needs buffering, as the MOSFET switches cannot be loaded resistively due to flicker noise. The periodic noise simulation gives a mixer output noise density of $80\,nV/Hz^{1/2}$ at 1 Hz and $45\,nV/Hz^{1/2}$ at 100 Hz, which is effectively less than half of the noise density of the CSA. A Gilbert multiplier cell is also an alternative but more difficult to design with the high requirements on isolation, noise and linearity.

Because balancing the duty ratio is imperative, the comparator that converts the delayed carrier signal to a clock is equipped with the duty ratio balancing circuit shown in Figure 11. The generated clock is divided by two using a flip-flop and the dc component of the divided clock is extracted. This dc signal, always at mid-rail, is used as a reference for an integrator. The input of the integrator is the clock average, which corresponds to the duty ratio. As the divided clock has always an average value that corresponds to a duty ratio of 50%, the clock average is forced toward this value. This is accomplished by using the integrator output to tune the comparator offset. The available offset tuning range is minimized in order to reduce the effect of noise and offset of the

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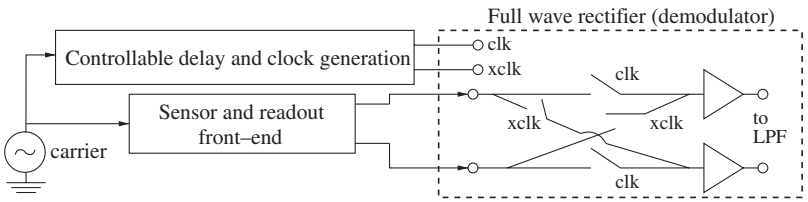

Figure 10. The demodulator with a pseudo-differential buffer, which prevents resistive loading of the switches.

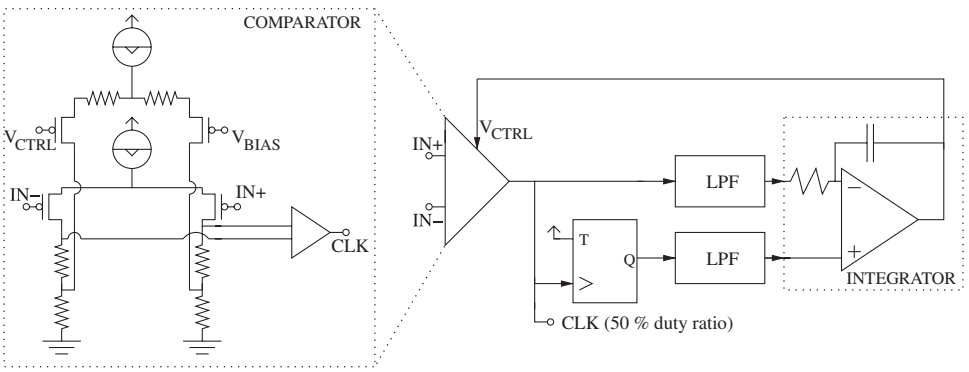

Figure 11. The circuit that generates the demodulator clock and balances the duty ratio. Input of the comparator is the sinusoidal, properly delayed sample of the carrier.

integrator. Also, the tuning range is designed to be smaller than the input amplitude to avoid a stable operating condition with a clock frequency of zero.

2.5. Filtering

The high-pass filters provide the necessary gain for the readout while attenuating low-frequency components as much as possible. In addition, they convert the signal to differential form, hence enhancing power supply insensitivity and relaxing the linearity requirements. The OPAMPs are designed as basic low-voltage folded cascode CMOS OPAMPs. Sufficient noise performance of the HPFs is easy to achieve, as the gain of the CSA is fairly large. The HPFs comprise four first-order filters, which have increasing corner frequencies of roughly 0.2, 0.4, 0.7 and 1 MHz and thus lower input-referred noise. Filters also provide controllable gain from 4 to 28 dB and thus allow controllable dynamics of the closed-loop sensor.

In order to be able to remove the high-frequency components after the demodulation without inflicting much delay, a sixth-order LPF is needed. The used Butterworth-type LPF has a controllable corner frequency from 200 to 400 kHz to allow controllable phase shift at low frequencies. The LPF is designed using three multiple feedback (MFB) sections shown in Figure 12. The OPAMP has a folded first stage to enable the use of NMOS input with a higher transconductance in the second stage and an NMOS free input stage in order to lower the overall flicker noise of the amplifier. The supply current of the first and second stage are nominally 120 μA (input pair

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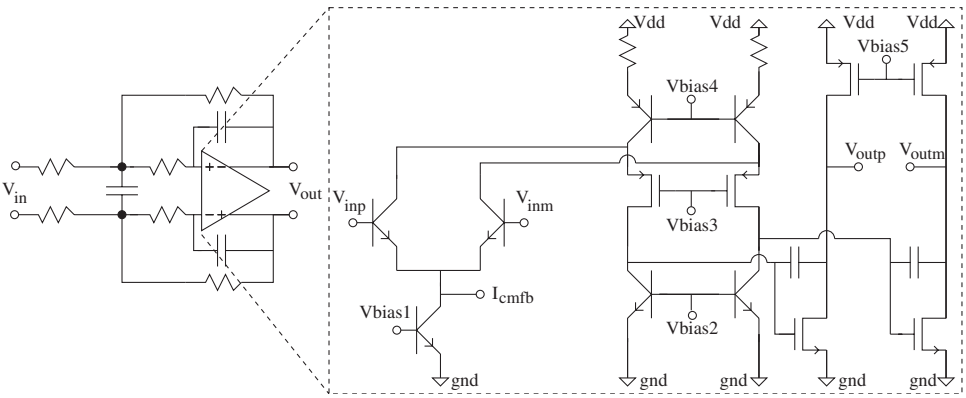

Figure 12. One of the three MFB cells in the LPF and the OPAMP used.

60 μA) and 600 μA, respectively, whereas the resulting gain bandwidth is about 20 MHz. A current mode common mode feedback is used due to the fairly slow and low current gain BJT transistors of the first stage.

The filters described above keep the sensor stable with roughly 5% mixer leakage, which corresponds to a demodulation carrier duty cycle of 47.5%, and the minimum carrier frequency of 2 MHz. The input-referred noise level of the LPF is $70\,\mathrm{nV/Hz^{1/2}}$ and the gain of the filter is 12 dB. The input-referred noise of HPFs is less than $20\,\mathrm{nV/Hz^{1/2}}$. The effective noise of the filters is sufficiently lower than the noise of the CSA.

3. SENSOR ELEMENT NON-IDEALITIES

The parasitic vibrational modes of the element are a severe system bandwidth and loop gain limiting factor. For the presented topology, the sources of instability can be recognized.

The sensor element together with the controller provides attenuation at high frequencies and the controller causes no phase shift after the pole at the highest frequency. However, the LPF of the loop starts to cause phase shift at roughly a decade below the corner frequency. The phase shift together with insufficient attenuation in the loop changes the location of the poles of a potential vibrational mode so that the system starts to oscillate spontaneously. This type of critical situation is formed when the modal frequency is high enough that the LPF causes some phase shift but no attenuation. In Figure 13, the location of the critical pole pair of a test loop is plotted. The loop consists of an LPF and a resonator (high Q-value). Instability can be avoided if the modal frequencies are sufficiently high or the gain at low frequencies is small.

For the measured sensor the system bandwidth was limited to roughly 1.5 kHz because of a vibrational mode at roughly 14 kHz. The measured maximum loop gain as a function of the LPF corner is plotted in Figure 14.

3.1. Non-linearity

The force-feedback is generally utilized to decrease the non-linearity causing effects on both electrostatic forces and the signal-dependent movement of the seismic mass in the sensor element.

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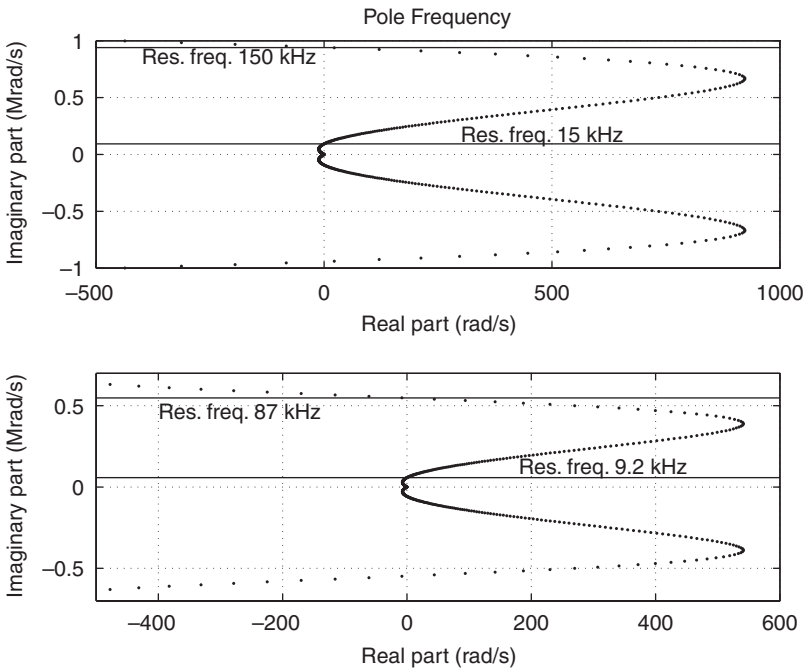

Figure 13. Dominant pole pair of the test feedback system with an LPF and a resonator forming the loop. With increasing resonance frequency, dc loop gain of 0.004 and Q-value of 100 000, the pole pair travels to the right half plane but returns to left half plane and remains there as the filter provides sufficient attenuation and phase change. The upper figure corresponds to a fifth-order Butterworth LPF with corner frequency of 189 kHz and the lower figure to a fourth-order LPF with corner frequency of 95 kHz. The horizontal lines indicate the resonance frequency at which the pole pair lies on the imaginary axis.

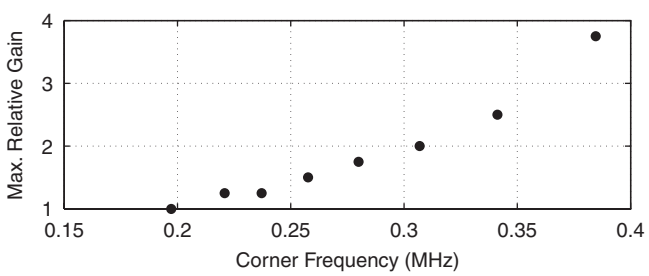

Figure 14. The figure shows the measured maximum loop gain of the system as a function of the LPF corner frequency. The gain is relative to nominal system gain and the system is required to remain marginally stable.

The electronics used for interfacing the element can be designed to reach linearity of up to 100 dB or more. Also, when the sensor bandwidth is increased, the sensitivity of the mass–displacement to ac acceleration is decreased, which further improves the linearity. However, few additional sources of non-linearity, which does not exist in an open-loop sensor, are related to the interface topology used here.

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A continuous-time force-feedback utilizes the signal capacitors of the sensor element (see Figure 1) for two purposes: to detect the difference in capacitance and as a voltage-to-force transducer. In the latter case the generated force is dependent on the square of the input voltage and the reduction of this inherent non-linearity is achieved by relying on the matching between the two capacitors, which cancels the second-order terms in the differential structure. Mismatch between the two capacitors results in second-order harmonic distortion.

In order to analyze the non-linearity, the two sensor capacitors, modeled as plate capacitors, can be expressed as

$$C_1 = \frac{K_1}{x_{01}+x} + C_{\text{par1}}, \quad C_2 = \frac{K_2}{x_{02}-x} + C_{\text{par2}} \tag{6}$$

and, further, the corresponding voltage-to-force transducers as

$$\begin{aligned} \mathbf{F}_1 &= \frac{\mathbf{u}_x}{2}\frac{\partial C_1}{\partial x}(V_B+\Delta V)^2 = \frac{K_1(V_B+\Delta V)^2}{2(x_{01}+x)^2} \\ \mathbf{F}_2 &= \frac{\mathbf{u}_x}{2}\frac{\partial C_2}{\partial x}(V_B-\Delta V)^2 = -\frac{K_2(V_B-\Delta V)^2}{2(x_{02}-x)^2} \end{aligned} \tag{7}$$

where $K_1 = \varepsilon_0 A_1$, $K_2 = \varepsilon_0 A_2$, in which A_1 and A_2 are the plate capacitor areas and ε_0 vacuum permittivity, x_{01} and x_{02} are the gap sizes, x the displacement, V_B the effective bias voltage and ΔV the signal voltage. The force has effect only in the direction of the sensor sensitive axis, denoted by the unity vector $\mathbf{u}_x$. The parasitic capacitors C_{par1} and C_{par2} model the parasitic cross coupling of the carrier signal to CSA input.

When dc non-linearity is considered, the first cause can be found in the unsymmetric parasitics C_{par1} and C_{par2}. This source of distortion can be evaluated by assigning $C_{\text{par1}} = \varepsilon K/x_0$, where ε is a parameter that determines the error magnitude, and $C_{\text{par2}} = 0$ and that remaining parameters are matched or $K_2 = K_1 = K$ and $x_{02} = x_{01} = x_0$. The closed-loop sensor has an integrator within the loop and the infinite dc gain forces the signal at the controller input to zero, providing that the system is operating correctly and the feedback is negative. If we assume that no offset is present after the demodulation, then also the carrier frequency signal average must be zero and $C_1 = C_2$. Using (6) we can calculate the resulting displacement x as

$$x = \frac{\varepsilon(x_0^2 - x^2)}{2x_0} \approx \frac{x_0\varepsilon}{2} \tag{8}$$

The resulting magnitude of the force affecting the seismic mass as a function of input voltage can be expressed using (7) and (8) as

$$F = |\mathbf{F}_1 + \mathbf{F}_2| \approx \Delta V \frac{K}{x_0^2}(2V_B - \varepsilon\Delta V) \tag{9}$$

Equivalent second-order harmonic distortion has magnitude of

$$\text{HD2} \approx \frac{\varepsilon}{4V_B} V_a \tag{10}$$

where V_a is the signal amplitude at the transducer input (at the sensor output).

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The second source of dc non-linearity is the unequal sensor capacitor areas. Now, if the variables are expressed as $C_{\text{par1}} = C_{\text{par2}} = 0$, $K_1 = K_2/(\varepsilon+1) = K$ and $x_{02} = x_{01} = x_0$, the resulting displacement x is

$$x = -\frac{\varepsilon}{2+\varepsilon} x_0 \approx -\frac{x_0 \varepsilon}{2} \tag{11}$$

Using (7) and (11) the force magnitude in this case can be expressed as

$$F \approx \Delta V \frac{K}{2x_0^2} \left(4V_B + \frac{\varepsilon}{1-\varepsilon} \Delta V \right) \tag{12}$$

Comparable second-order harmonic distortion has a magnitude of

$$\text{HD2} \approx \frac{\varepsilon}{1-\varepsilon} \frac{1}{8V_B} V_a \tag{13}$$

Unequal x_{02} and x_{01} will not cause distortion at low frequencies because when the feedback balances the sensor capacitors it also balances the voltage-to-force transducers. However, the transducers can also be equalized in the two previously described cases of imbalance. This can be performed, for example, by feeding a certain dc voltage to the loop before the loop controller. In case there is mismatch in K_1 and K_2 of (7) the dc component is used to pull the seismic mass aside from the center position in such a way that the area mismatch is compensated. If the original mismatch is caused by unsymmetric constant parts of (6), the dc component is used to balance the seismic mass back to the center position. Combinations of sensor imbalances can be also compensated as the Matlab Simulink simulation result in Figure 15 shows. Low sensitivity to the dc eases the generation of this control voltage. However, large mismatches will saturate the system and cannot therefore be compensated by using just dc voltage. Thus, it might be feasible to combine the dc tuning with a capacitor matrix for coarse tuning in parallel with the sensor element.

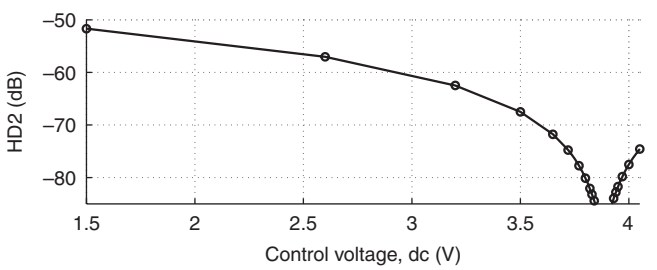

Figure 15. The half bridge sensor, modeled using plate capacitors, has area mismatch ($\varepsilon = 0.02$ in (10)), constant part mismatch ($\varepsilon = 0.02$ in (13)) and gap-size mismatch of 3% in the Matlab Simulink system simulation. The figure shows the second harmonic component as a function of dc that is summed to low-pass filter output (see Figure 1). The input of the system is a one g sinusoidal acceleration signal at 25 Hz.

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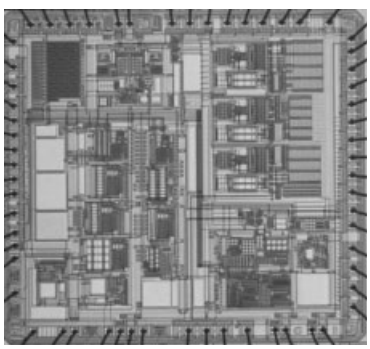
4. MEASURED CHARACTERISTICS OF THE SENSOR

The chip photomicrograph is shown in Figure 16(a). The total and block level chip area and the current consumption are summarized in Figure 16(b).

The gain transfer functions of the closed-loop and open-loop sensors are shown in Figure 18. The simplified measurement setup is shown in Figure 17, where the carrier is fed to the sensor through 100 pF capacitors and the external bias voltages through 5 kHz resistors. The components are selected for tolerable phase shift, attenuation and noise as well as for convenience for integration. The electrostatic excitation is performed by summing an attenuated common-mode low-frequency signal to the dc bias voltages and by sweeping the frequency of the signal. This signal applies an electrostatic force on the sensor, which the feedback compensates for hence revealing the characteristics of the loop. The three different gain transfer functions are obtained using a closed-loop sensor with altered gain of the loop. Increased gain moves the poles of the closed-loop system

(a)



(b)

Block	Nominal supply current (mA)	Area (mm^2)
GmC-oscillator	0.3	0.5
GmC-oscillator buffer	3.2	0.2
Controllable delay	2.3	0.8
CSA (high voltage supply)	0.5	0.3
HPFs	4.5	1.1
Mixer (with output buffer)	1.7	0.6
LPF	2.5	2.6
Complete chip	**15**	**16**

Figure 16. (a) The photomicrograph of the implemented chip and (b) chip area and current consumption of the on-chip sub-blocks.

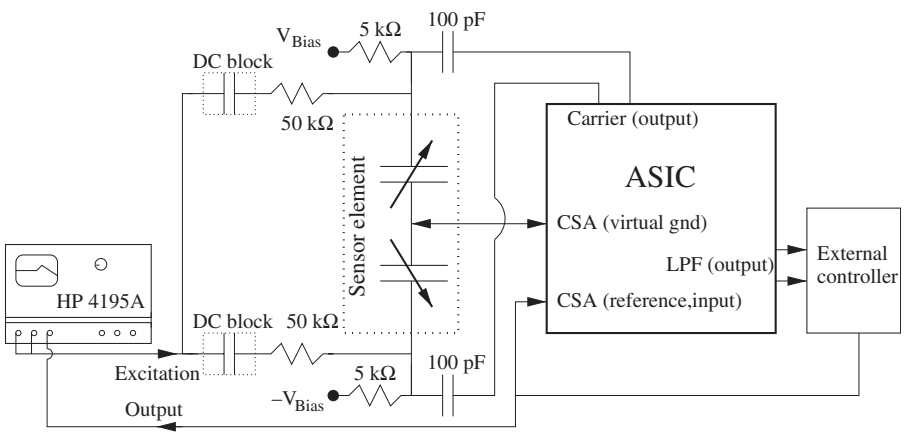


Figure 17. Simplified description of the measurement setup that is used for characterizing the sensor transfer functions.

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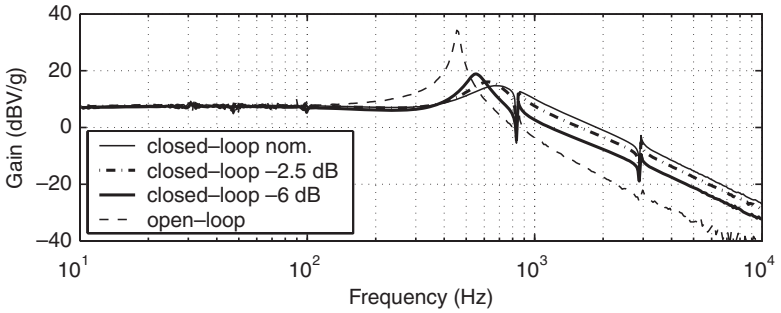

Figure 18. The gain transfer functions of the closed-loop and open-loop sensors.

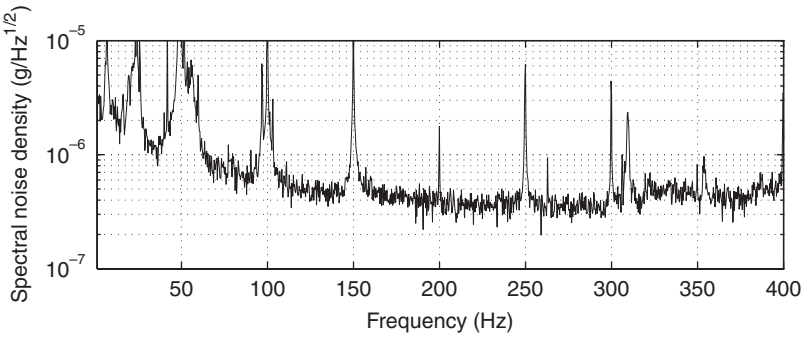

Figure 19. Measured noise floor of the sensor. The figure is scaled to correspond to noise spectral resolution and thus the magnitude of the external disturbances is not correct.

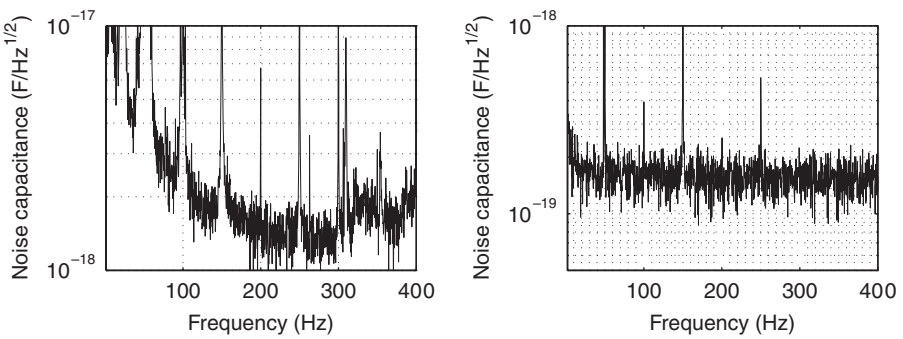

Figure 20. (a) The noise density in Figure 19 referred to capacitance at the CSA input and (b) the noise capacitance density of the readout from the CSA input to the LPF output. The differential rms detection voltage (carrier) is 2 V for both figures.

away from the origin and also lowers the gain maximum. The local gain minima indicate the sensor parasitic modes, one of which limits the maximum pole frequency of the sensor.

The noise floor of the closed-loop sensor is shown in Figure 19 and is obtained with a measurement setup of Figure 17 with the difference that the excitation is removed and the output is directly digitized. External disturbances, mainly at the harmonics of the line frequency, are clearly visible.

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Also an unknown source of low-frequency noise is present and the common mode noise of the carrier is higher than expected. For comparison, Figure 20(a) shows the noise of Figure 19 referred to signal capacitance and Figure 20(b) much lower noise level of the readout, i.e. from the CSA input to the LPF output. In the case of Figure 20(b) the sensor is replaced with a single constant capacitor that corresponds to the sensor element and hence excludes the effect of carrier noise. This explains the lower noise level. At lowest the noise level of the sensor is below $500\,\mathrm{ng/Hz^{1/2}}$, despite the excess carrier noise, whereas the full-scale input is $\pm 1.5g$.

5. CONCLUSIONS

Several aspects concerning the design of an analog closed-loop accelerometer were presented. The blocks required for the implementation of the interface are suitable for integration within a reasonable chip area. A stable sensor requires careful recognition of sources of instability, some of which are the leakage in the demodulator and insufficient attenuation in filters and, especially, parasitic vibrational modes of the sensor element. The common mode noise from the carrier generator is identified as a dominant noise source, which indicates that the system is also sensitive to non-differential noise from references.

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