Publication X

Lasse Aaltonen, Mikko Saukoski, and Kari Halonen. 2005. Design of clock generating fully integrated PLL using low frequency reference signal. In: Proceedings of the 17th European Conference on Circuit Theory and Design (ECCTD 2005). Cork, Ireland. 28 August - 2 September 2005. Volume 1, pages 161-164. ISBN 0-7803-9066-0.

Design of Clock Generating Fully Integrated PLL Using Low Frequency Reference Signal

Lasse Aaltonen * Mikko Saukoski * Kari Halonen *

***Abstract* — Systems including for example micromechanical oscillators can provide a frequency reference, which can be in the order of few kilohertz. This paper describes a design procedure for a fully integrated charge pump phase locked loop (PLL), which can utilise low reference frequencies. Noise is taken into account in the design process and simulated example of a PLL is presented. Presented theory allows the design of a fully integrated PLL in favour of either noise or power consumption.**

1 INTRODUCTION

Phase locked loops (PLLs) are basic building blocks for analog and digital systems, in which they are used for clock generation or recovery, demodulation or frequency synthetizer applications. PLL uses an external reference signal and adjusts the output clock signals according to the reference.

In systems utilizing a combination of micromechanical and microelectronic components, such as MEMS sensors, a mechanical resonator can provide a stable and accurate frequency reference. If the mechanical structure itself is a resonating sensor, external electronics is required to process the electrical signal to a more feasible form. If a PLL is attached to the system, it can provide clock signals for A/D converter, digital circuitry and resonator excitation, for example.

2 STRUCTURE OF PLL

The charge pump PLL topology is studied in this paper (see Fig. 1). Digital implementation of phase and frequency detection (PFD) and extremely simple loop filter (LF) structure enable the implementation of PLL with moderate chip area. An example PLL is designed and simulated for implementation with a 0.7 μm CMOS process and 5 volt supply voltage.

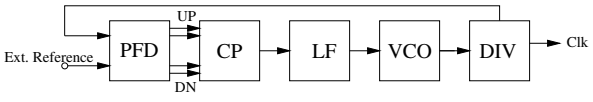

Figure 1: Block diagram of a charge pump PLL.

*Electronic Circuit Design Laboratory, Helsinki University of Technology, Finland, e-mail: ljaalton@ecdl.hut.fi, tel.: +358 9 451 2278, fax: +358 9 451 2269.

Due to the low reference frequency the filter will be the most significant chip area consumer. For this reason single ended structure is chosen for the filter (see Fig. 2). Smallest area consumption can be obtained using a high ohmic polysilicon resistor and gate capacitance of transistor as a non-floating capacitor. In order to linearise the gate capacitance, the transistor should remain biased in strong inversion. Active realisation of the resistor is also possible but would have limited voltage swing and large area due to high resistance value and complex realisation. The resistor will provide a large parasitic capacitance towards substrate. This capacitance can be utilised as an additional capacitor denoted as C_2. Impedance of the loop filter in Fig. 2 with C_2 excluded is

$$Z(s) = \frac{RCs + 1}{sC}, \tag{1}$$

where R is the resistor and C the capacitor value.

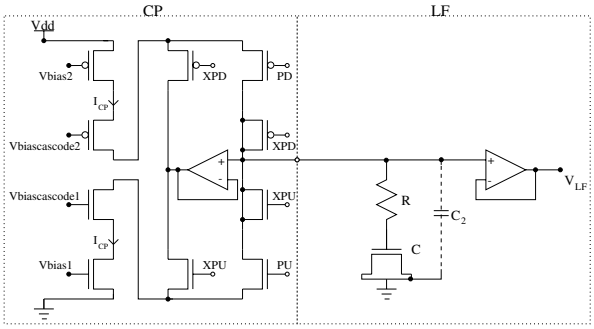

Figure 2: PLL loop filter and charge pump.

A cascode current mirror is suitable for charge pump (CP) implementation (see Fig. 2). Current source transistors are kept in saturation continuously to avoid long delays at the moment of switching and dummy switches can be used to suppress charge injection errors. Suitable charge pump configurations are presented in [1].

2.1 Sizing of the Components in the PLL

Due to rather low clock frequencies the realisation of digital blocks PFD and frequency divider DIV is straightforward and these blocks are therefore not treated in this paper. For the PLL transfer function we need a linear model for each block within

the PLL. Therefore we denote the ratio between input and output frequency of DIV with N, PFD gain with $K_{PFD} = I_{CP}/(2\pi)$, where I_{CP} is the charge pump current, and the gain of the voltage controlled oscillator (VCO) with K_{VCO}. Furthermore, by using equation (1) for the loop filter impedance, we obtain the transfer function from the phase of the reference to the loop filter voltage as

$$\frac{V_{LF}(s)}{\phi(s)} = \frac{\frac{I}{2\pi}\frac{R}{}s^2 + \frac{I}{2\pi C}s}{s^2 + \frac{K}{2\pi N}\frac{I}{}\frac{R}{}s + \frac{K}{2\pi CN}\frac{I}{}}. \quad (2)$$

To calculate the four unknown parameters R, C, K_{VCO} and I_{CP} in equation (2) we first define the gain of the VCO. For this purpose we must know the frequency range $\Delta\omega_{REF}$ in which the reference varies. We also need the available tuning range ΔV of VCO, which is ultimately limited by the supply voltage. We should leave some margin to the VCO gain by scaling the actual tuning range by the worst case minimum gain caused by component size variation. We can write for the VCO gain

$$K_{VCO} = \frac{\Delta\omega_{REF}}{\Delta V}N. \quad (3)$$

The loop filter chip area can be optimised by writing an equation for the LF area

$$A_{LF}(I_{CP}) = A_C C(I_{CP}) + A_R R(I_{CP}), \quad (4)$$

where A_C is the capacitance area density and A_R is the resistance area density. By defining the damping factor ζ and natural frequency ω_N from (2) and solving

$$R(I_{CP}) = \frac{4\pi\omega_N\zeta N}{K_{VCO}I_{CP}} = \frac{2\zeta}{C\omega_N}, \quad (5)$$

and

$$C(I_{CP}) = \frac{K_{VCO}I_{CP}}{2\pi\omega_N^2 N}, \quad (6)$$

$C(I_{CP})$ and $R(I_{CP})$ can be substituted to equation (4). Minimum area is obtained by differentiating $A_{LF}(I_{CP})$ with respect to I_{CP} and setting the derivative zero. This yields

$$I_{CP} = \sqrt{\frac{8\pi^2\omega_N^3 A_R N^2\zeta}{K_{VCO}^2 A_C}}. \quad (7)$$

After calculation of I_{CP}, equations (5) and (6) can be used to define suitable resistor and capacitor sizes.

To consider an example case, we set the reference frequency range to be from 5 kHz to 10 kHz and the scaled VCO tuning range to be roughly 2 V. Using equation (3) we get K_{VCO} to be 16*N $krad/(sV)$. Now we must define the natural frequency which must be low enough compared to the lowest reference frequency [2]. Thus we require ω_N to be 2.5 $krad/s$. A damping coefficient ζ of 0.45 is chosen instead of critical damping to save chip area. Process dependent coefficients $A_R = 4{\cdot}10^{-15}\ m^2/\Omega$ and $A_C = 500\ m^2/F$. Now using equations (7), (6) and (5) we get $I_{CP} = 130\ nA$, $C = 54\ pF$ and $R = 6.7\ M\Omega$. If RI_{CP} is too high compared to tuning range (0.9 V of this case can be tolerated), VCO gain must be increased. Higher gain will increase bandwidth and damping of the PLL but will also contribute to additional phase noise by increasing the effect of the loop filter noise.

3 PHASE NOISE

Relaxation oscillator is a suitable topology for implementing the oscillator in a low frequency PLL. This is mostly due to the large tuning range and simple and reliable structure. In addition this structure can be optimised for low power consumption. Disadvantage of this structure is a high level of phase noise. We will next consider different mechanisms by which white and flicker noise transform into phase noise.

3.1 Noisy Frequency Controlling Current

If the oscillator is current controlled we can write for the frequency $\omega(t) = K_{CCO}I(t)$, the integral of which gives the timevarying phase. K_{CCO} is the gain and $I(t)$ frequency controlling current. Noise component is written as $I(t) = I_n\cos(\omega_n t)$, where ω_n is the frequency of the noise component and I_n amplitude, which corresponds to the spectral density of current noise. Now we write the fundamental frequency ω_0 component of the output signal into form

$$v_0 = A_0\cos[\omega_0 t + K_{CCO}I_n\int\cos(\omega_n t)dt]. \quad (8)$$

Phase noise $L(\Delta\omega)$ at frequency offset $\Delta\omega = \omega_n$ can now be written using equation (8). Due to integration, we consider only flicker noise and replace I_n by $I_{nf}/f^{1/2}$. Now we get the equation for phase noise into form

$$L(\Delta f) \approx 10\log\left(\frac{K_{CCO}I_{nf}}{4\pi\Delta f^{1.5}}\right)^2, \quad (9)$$

where I_{nf} is the rms value of noise at 1 Hz and Δf frequency offset, at which phase noise is evaluated [3].

3.2 Noise During Voltage Comparison

The effect of noise at the moment of state changing in a relaxation oscillator can be evaluated using two integrator oscillator model to obtain the noise shaping properties [3]. Phase noise can be obtained by comparing magnitudes of signal and noise.

The two integrator open loop transfer function is $H(s) = -(\omega_0/s)^2$, where ω_0 is the fundamental frequency. In closed loop configuration, the gain transfer function can be written as

$$\left|\frac{Y[j2\pi(f_0+\Delta f)]}{X[j2\pi(f_0+\Delta f)]}\right|^2 \approx \frac{1}{4}\left(\frac{f_0}{\Delta f}\right)^2, \qquad (10)$$

where $\Delta\omega = 2\pi\Delta f$ is the offset frequency at which the noise amplification is calculated. When we know the peak-to-peak voltage of the signal in the oscillator denoted with V_H, we can write the equation for phase noise as

$$L(\Delta\omega) \approx 10\log\left(\frac{m}{4}\frac{f_0^2}{\Delta f^2}\frac{V_n^2}{V_H^2}\right). \qquad (11)$$

In this equation V_n denotes rms noise voltage at frequency $nf_0 + \Delta f$ (n is a positive integer) and m spesifies the number of harmonics of ω_0 from which the noise folding is taken into account. Unknown m can thus be determined by simulating the noise bandwidth of the comparator using discrete frequency noise sources and examining the effect of these sources to spectrum.

If we consider only low frequency noise we replace V_n in equation (11) with $V_{nf}/f^{1/2}$, where V_{nf} is the flicker noise voltage rms value at 1 Hz. Value of m in this case is 1.

4 VCO

Design procedure of the oscillator must take into consideration major noise contributors and sensitivity to the power supply variations. The latter is done by using differential structure for the VCO.

The structure of the designed VCO is shown in Fig. 3. The VCO consists of a CCO i.e. a current controlled oscillator and simple transconductance block (GM). CCO contains comparator (COMP) with internal hysteresis and floating capacitor between two current sources (DIFFCS). PMOS transistors are preferred over NMOS transistors in current sources because flicker noise is substantially higher in NMOS devices. The gain of the VCO is given as

$$K_{VCO} = \frac{\pi}{R_{COMP}I_{BCOMP}C_{VCO}R_{GM}}, \qquad (12)$$

where R_{COMP} is the resistor and I_{BCOMP} the bias current of the comparator, C_{VCO} is the capacitor of VCO and R_{GM} the resistor of GM block. One can also add dc current I_{dc} to I_{ctrl} to enable control voltage independent oscillation frequency, if the VCO gain this requires.

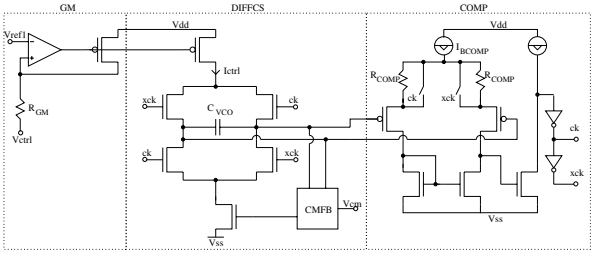

Figure 3: Structure of the VCO.

4.1 Phase Noise in VCO

White noise is taken into account only by dimensioning transistors in the comparator input pair. White noise content can be minimised by maximising input pair transconductance.

To be able to investigate the flicker noise effect we write the equation for MOSFET noise current

$$I_n^2 = (2\mu I_D K_F)/(L_C^2 f), \qquad (13)$$

where I_D is the transistor channel current, μ is carrier mobility, K_F flicker noise coefficient and L_C transistor channel length. By substituting equation (13) into (9) we get

$$L(\Delta f) \approx 10\log\left(\frac{f_0^2 2\mu K_F}{4f^3}\frac{1}{I_D L_C^2}\right), \qquad (14)$$

which is the same result that we would get by substituting equation (13) into (11) and writing $V_H = I_{BCOMP}R_{COMP}$, where $I_D = I_{BCOMP}$, and for noise voltage $V_n = R_{COMP}I_{nf}/f$. Flicker noise of the comparator input pair is attenuated due to the differential structure of the VCO. The only design-dependent variables in equation (14) are current I_D and channel length L_C. For total phase noise, sum of noise power from all sources must be calculated, i.e. equations (9) and (11) with both flicker and white noise taken into account. One must notice that neither white noise in I_{BCOMP} nor resistor flicker noise nor effect of charge pump non-idealities are analysed. In addition, reduction of flicker noise below the level of loop filter resistor thermal noise is ineffective. The noise bandwidth of the resistor is limited by C_2 in Fig. 2.

4.2 Component Values in VCO

The effect of frequency division must be taken into account when phase noise of particular output frequency is calculated. This can be done by changing

K_{CCO} and f_0 in equations (9) and (11) to match the output frequency of interest. When power consumption is one parameter of interest, we can select maximum current I_{BCOMP} for the biasing of the comparator and use equation (14) at a typical output frequency f_0 and offset Δf to define minimum length of transistor channel L. Comparator speed must remain adequate though the current is minimised. As the biasing current is defined, we can calculate $R_{COMP} = V_H/I_{BCOMP}$ by maximising hysteresis V_H (minimise equation (11)) of the comparator.

Using maximum tuning voltage ΔV (see section 2.1) and typical control current I_{ctrl}, which satisfies power consumption requirements, we can calculate $R_{GM} = \Delta V/I_{ctrl}$. After this we can select minimum channel length of the current source transistor, which satisfies phase noise properties, using equation (9) with I_{ctrl} and $K_{VCO}/R_{GM} = K_{CCO}$.

In our example case total N is equal to 512. We select $I_{BCOMP} = 100\ \mu A$ and resistor value will thus be 15 $k\Omega$ with $V_H = 1.5\ V$. We calculate that $R_{GM} = 100\ k\Omega$, when $\Delta V = 2\ V$ and $I_{ctrl} = 20\ \mu A$. The size of C_{VCO} can be determined from equation (12). Using previously calculated values (see section 2.1) we obtain capacitor value of 2 pF. Drawn layout of the PLL consumes 0.4 mm^2.

5 SIMULATION RESULTS

The stability and settling of the designed PLL were simulated with transient analysis. Figure 4 shows both theoretical and simulated step responses. Theoretical curve corresponds to natural frequency

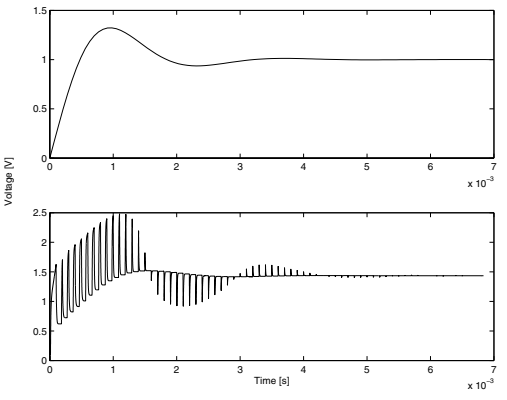

Figure 4: Theoretical (top) and simulated (bottom) step responses.

ω_N of 2.59 $krad/s$ and damping coefficient of 0.46. Equivalent simulated numbers are 2.50 $krad/s$ and 0.45.

The phase noise theory of equation (11) was verified by setting a sinusoidal voltage source with amplitude $V_n = 100\ \mu V$ to VCO comparator input in series with capacitor C_{VCO}. Fig. 5 (left) shows the spectrum of VCO output when sinusoidal error is near third harmonic of oscillation frequency 4.47 MHz. Fig. 5 (right) shows the theoretical and simulated effect of low frequency (30 kHz, 10 nA) noise component in current $I_{BCOMP} = 100\ \mu A$.

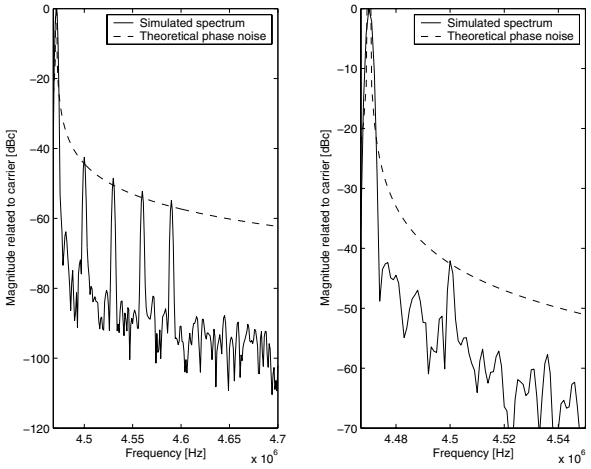

Figure 5: Left: Folding of sinusoidal noise round third harmonic. Right: Effect of low frequency sinusoidal noise in comparator bias.

6 CONCLUSIONS

A design flow and implementation example of a fully integrated PLL using low frequency reference was presented in this paper. Proposed topology allows the implementation within reasonable chip area. Noise theory is presented to recognise the dominant noise sources and to evaluate phase noise in the VCO.

Acknowledgements

The authors wish to thank National Technology Agency of Finland (TEKES) and VTI Technologies Oy for financial support.

References

[1] W. Rhee, "Design of High-Performance CMOS Charge Pumps in Phase-Locked Loops", ISCAS '99, vol. 2, pp. 545-548, 1999.

[2] M. Van Paemel,"Analysis of a Charge-Pump PLL:A New Model", IEEE Transactions on Communications, vol. 42, no. 7, pp. 2490 - 2498, 1994.

[3] B. Razavi, "A Study of Phase Noise in CMOS Oscillators", IEEE Journal of Solid-State Circuits, vol. 31, no. 3, pp. 331-343, 1996.