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Noise analysis of comparator performed sine-to-square conversion

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ABSTRACT: This paper describes a theoretical analysis of sine-to-square conversion when noise is included in the conversion process. The analysis is done for conversion performed by a comparator. As a result of the analysis, a simple method for calculating the spectrum of clock resulting from noisy conversion process is obtained. It will also be shown that the conversion process can easily lead to poor quality of the clock signal and that special attention should be paid when the clock is intended to be used for edge sensitive digital logic. To support the derived theory, simulation results will be presented.

1 Introduction

In different mixed-mode signal processing systems, there is occasionally a need to convert a sinusoidal signal to a square wave. This square wave can then be used as a clock signal for the system. The conversion involves detecting the zero-crossing points of the sinusoid, and is usually performed with a continuous-time comparator. An example of a basic sine-to-square conversion system and typical waveforms is shown in Fig. 1.

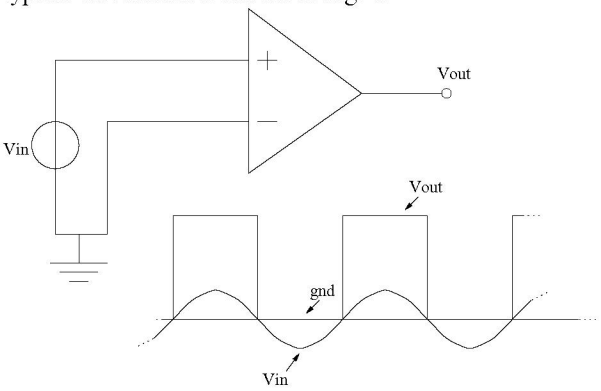

Fig. 1: A sine-to-square conversion system and typical waveforms.

A system where this kind of conversion is required is presented in [1]. There, a phase-locked loop (PLL) is locked to a high-Q micromechanical resonator, the output of which is sinusoidal by nature. The PLL then provides synchronous clocks for the rest of the system. Another common example is related to clock generation for data-converters, where a clock is supplied to a chip as a sinusoidal signal. The signal is then converted to a square wave by a digital input buffer in the chip periphery and the conversion process adds noise to the clock. Effect of clock jitter is analysed for example in [2]. The third example involves analog demodulation that is performed with a switching modulator. If the demodulation is done with a sinusoidal carrier, the carrier must be converted to a square wave before it can be used to control the switches.

Together with the desired signal, electrical signals always contain noise. Noise in the sinusoidal signal introduces uncertainty in the positions of the rising and falling edges of the created square wave. In the worst case, it can also cause additional "false" transitions to the output signal in the zero-crossing point. To ensure that the conversion results in a good-quality clock signal, the limits imposed by noise must be thoroughly understood. This way, the maximum allowable noise level in the input signal can be determined.

This paper presents analysis of the effects of noise to the conversion from a sinusoidal signal to a square wave. First, the RMS jitter caused by general time domain noise is analysed. Thereafter, the spectrum of the output square wave resulting from a noisy sinusoidal input signal is evaluated. Guidelines are given for both determining the noise budget and for the design of the comparator. Finally, the paper is finished with some concluding remarks.

2 Noise during state change of comparator

The input of the comparator during state change is shown in Fig. 2. Ideally, the comparator output would change its value exactly at the zero crossing point of the input sinusoid. However, due to noise or distortion, the edge of the output square wave will deviate from its ideal position. The magnitude of the deviation can be calculated. The deviation will be calculated for general time domain noise.

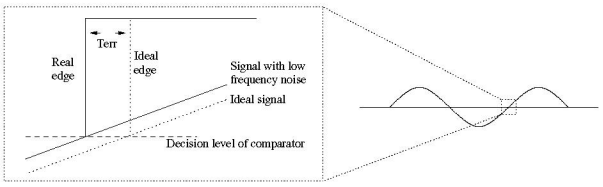

Fig. 2: Comparator input at the moment of output state change.

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In order to enable the analysis, some requirements for the system are made. First, the comparator is ideal with respect to both noise and speed. Second, the derivative of the noise should always remain smaller than the derivative of the input signal at the zero crossing point. If the latter condition is not met, the noise will result in additional switching of comparator. This will in most cases lead to severe deterioration of system performance when the square wave is used for discrete time circuits. This situation is depicted in Fig. 3.

The comparator input signal is sinusoidal with some noise included and can be written as

$$V_{in}(t) = A\sin(\frac{2\pi}{T}t) + V_N(t), \quad (1)$$

where A is the amplitude and T the period of the input sine and $V_N(t)$ the time domain noise summed to the sine. The RMS deviation of the output square wave edge from the ideal position can be evaluated by linearizing the input signal to the zero crossing point. Linearization gives

$$V_{in}(t) = A\frac{2\pi}{T}t + V_{NRMS}, \quad (2)$$

where the constant RMS noise voltage V_{NRMS} represents the noise component, which has small derivative compared to actual input sine and can thus be evaluated to be constant. Solving t from the previous equation and by assuming that the comparator changes its state at zero input voltage, the RMS timing error or jitter of both rising and falling edges can be written as

$$T_{err} = \frac{V_{NRMS}T}{2\pi A}. \quad (3)$$

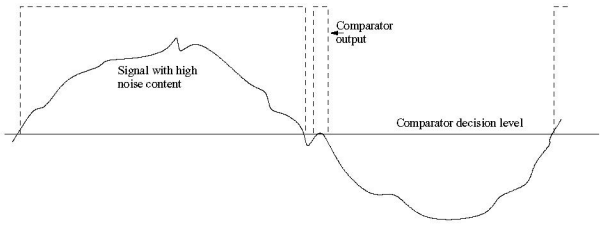

Fig. 3: Additional switching of comparator output due to excess noise at the input.

3 Spectrum of clock generated using noisy reference

To examine the spectrum of a noisy clock, the noise and output square wave is first investigated in time domain. To calculate the output spectrum, we first examine the output pulse train, which is formed by the error pulses. The error pulses denote the difference between ideal and noisy clock signal. The time domain representation of the error signal can be written by summing all the error pulses that are approximated to occur at the point, where comparator changes its state. Now the starting and the ending point of the error pulse depend on the current noise value. The infinite sum can be written as

$$f_j(t) = V_{sq}\sum_{n=-\infty}^{\infty}\begin{bmatrix}(\theta(t+T_N(nT_s)+nT_s)\\ -\theta(t-T_N(nT_s)+nT_s))\end{bmatrix}, \quad (4)$$

where, V_{sq} is the square wave peak-to-peak voltage, $T_s=T/2$ denotes the sampling interval, θ is a unity step function, and T_N can be obtained from

$$T_N(t) = \frac{TV_N(t)}{4\pi A}. \quad (5)$$

Now, equation (4) requires the condition that the derivative of the input sine is larger than the derivative of the V_N at the zero crossing point. The Fourier transformation [3] of equation (4) is

$$\begin{aligned} F_j(\omega) &= \int_{-\infty}^{\infty} f_j(t)e^{-j\omega t}dt \\ &= V_{sq}\sum_{n=-\infty}^{\infty}\left[\frac{2\sin(T_N(nT_s)\omega)}{\omega}e^{j\omega nT_s}\right], \end{aligned} \quad (6)$$

in which $T_N(nT_s)\omega << 1$ and thus equation (6) can be approximated as

$$F_j(\omega) \approx V_{sq}\sum_{n=-\infty}^{\infty}\left[2T_N(nT_s)e^{j\omega nT_s}\right]. \quad (7)$$

Now, the term $2V_N(nT_s)$ is independent of ω and inverse Fourier transformation [3] of equation (7) gives

$$\begin{aligned} f_j(t) &= \frac{1}{2\pi}\int_{-\infty}^{\infty} F_j(\omega)e^{j\omega t}d\omega \\ &= V_{sq}\sum_{n=-\infty}^{\infty}\left[2T_N(nT_s)\delta(t+nT_s)\right]. \end{aligned} \quad (8)$$

As the values of T_N are irrelevant everywhere except when $t=-nT_s$, equation (8) can be written as

$$f_j(t) = 2V_{sq}T_N(t)\sum_{n=-\infty}^{\infty}\delta(t+nT_s). \quad (9)$$

For the pulse train, the Fourier series [3] representation can be written as

$$S_i(t) = \frac{1}{T_s} + \frac{2}{T_s}\sum_{n=1}^{\infty}\cos(2\omega_c nt), \quad (10)$$

when $\omega_c = 2\pi/T = 4\pi/T_s$. By using equations (10), (9) and (5) the error signal can be written as

$$f_j(t) = \left[1 + 2\sum_{n=1}^{\infty}\cos(2\omega_c nt)\right]\frac{V_{sq}V_N(t)}{A\pi}. \quad (11)$$

In case the clock is used in a digital circuit, for example in a phase-frequency detectors of a phase locked loop [4], which are sensitive only to rising or falling edge, the error signal can be written as

$$f_j(t) = \left[1 + 2\sum_{n=1}^{\infty}\cos(\omega_c nt)\right]\frac{V_{sq}V_N(t)}{2A\pi}. \quad (12)$$

For the ideal clock signal, the Fourier series is similar to the Fourier series of a square wave [3], i.e.

$$S_{sq}(t) = \frac{V_{sq}}{2} + \frac{V_{sq}}{n\pi}\sum_{n=1}^{\infty}\begin{bmatrix}(1-\cos(n\pi))\times \\ \sin(\omega_c nt)\end{bmatrix} \quad (13)$$

Combination of equations (11) and (13) gives the actual signal at the comparator output,

$$f_{clk}(t) = \frac{V_{sq}}{2} + \frac{V_{sq}}{n\pi}\sum_{n=1}^{\infty}\begin{bmatrix}(1-\cos(n\pi))\times \\ \sin(\omega_c nt)\end{bmatrix} + \left[1+2\sum_{n=1}^{\infty}\cos(2\omega_c nt)\right]\frac{V_{sq}V_N(t)}{A\pi} \quad (14)$$

Derived equation (14) proves that the noise can be considered as an amplitude modulating signal and the clock spectrum can be plotted with a simple multiplication without need to analyze the time domain signal, where the noise information is stored in pulse width. One should also take into account the assumptions and properties of the obtained result. First, the assumption made between equations (6) and (7) limits the use of equation (14) to a sufficiently small number of harmonics *n*. The number will be determined by the relation between the RMS timing noise and the clock period. Second, one must notice that the obtained time domain clock signal now contains impulses, not pulses, at the zero crossing point of the comparator input sine. Thus, both the impulse with zero width and the pulse, which has its width determined by noise, have the same area. Simulation result shown in Fig. (4) is obtained using an ideal comparator with 1 *V* amplitude sinusoidal input, containing 1 *mV* amplitude sinusoidal distortion at 0.3 *MHz*, 1.5 *MHz*, 2.4 *MHz*, 3.2 *MHz* and 5.1 *MHz*. The theoretical result obtained using equation (14) follows the simulated one accurately with $n \leq 10$.

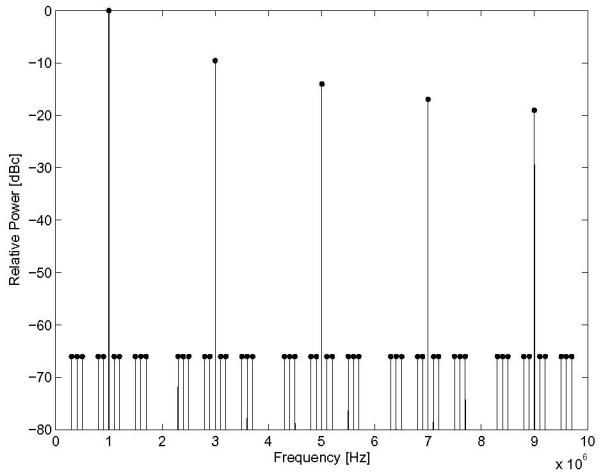

Fig. 4: Simulated (solid) and theoretical (dotted) clock spectrums with 1 MHz fundamental frequency.

4 Calculation of spectrum for noisy clock

The calculation of the spectrum for clock is straightforward, in case the comparator input signal has a known frequency domain noise content. If the noise spectral power at the comparator input has general form of $N^2(\omega)$, the sampling operation occurring at the comparator folds the noise according to

$$N_T(\omega_n) = \sqrt{\sum_{m=1}^{\infty}\begin{bmatrix}N^2(\omega_n)+ \\ N^2(2\omega_c m-\omega_n)+ \\ N^2(2\omega_c m+\omega_n)\end{bmatrix}}. \quad (15)$$

The spectrum of noisy clock can be plotted by substituting $N_T(\omega_n)$ to equation (14) so that

$$V_N(t) = \sum_{\omega_n}\sqrt{2}N_T(\omega_n)\sin(\omega_n t), \quad (16)$$

with values of ω_n ranging from 0 to ω_c. This determines all the noise frequencies that can be expressed, with noise spectrum recurring at each odd harmonic clock frequency. By performing these operations, the noise spectral density will be shown by the sinusoidal components, each representing spectral noise voltage at certain frequency ω_n. The $N^2(\omega)$ used for simulation is given by equation

$$N^2(\omega) = \frac{V_w^2 + \left(\frac{V_{1/f}^2}{\omega}\right)}{1+\left(\frac{\omega}{\omega_{corner}}\right)^2}, \quad (17)$$

where the white noise spectral power density V^2_w = 1.8 pV^2/Hz, flicker noise power density at 1 *Hz* $V^2_{1/f}$ = 1.8 $\mu V^2/Hz$ and corner frequency ω_{corner}=20 *MHz*.

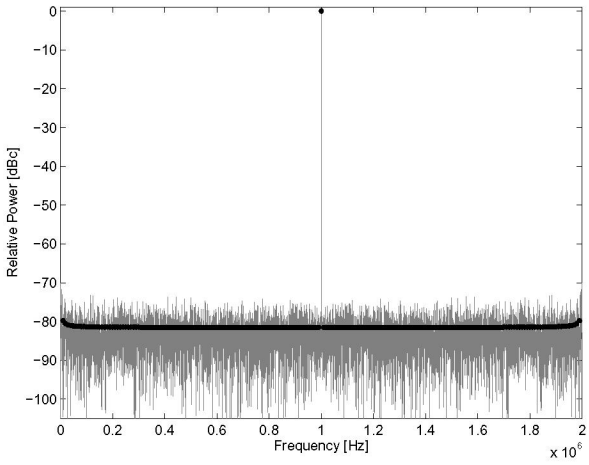

Fig. 5: Simulated (solid) and theoretical clock (dotted) spectrums when the clock is generated from noisy sinusoidal reference.

The simulation result together with a theoretical result, obtained using (17), (16), (15) and (14), is shown in Fig. (5) with frequency resolution of 250. An ideal comparator with 1 V amplitude sinusoidal input was used in the simulation.

5 Comparator design

The analysis presented was done for an ideal comparator, as the noise level of comparator input signal is usually larger than that of the comparator itself. This is true especially when the signal needs to be amplified before the conversion. However, some remarks can be made about the design of comparator. First, comparator speed should be as low as the system can tolerate, in order to decrease the noise bandwidth. The phase error caused by delay can be compensated for example using high pass filters to advance the phase before the conversion. Small amount of hysteresis can alleviate the additional switching, but will not have effect on the actual timing error, which results from noise. Second, signal amplitude at the comparator input should be maximized so that the comparator will not limit the conversion accuracy. Third, closed form analysis of comparator noise bandwidth is troublesome and requires simulations for accurate determination. However, comparator input flicker noise can be directly included in the noise analysis, as it typically has low enough corner frequency to fit within the comparator bandwidth.

6 Conclusions

Theoretical analysis was presented to enable straightforward calculation of spectrum for a noisy clock in case the clock is generated from sine using a comparator. Simulation results were presented in order to verify the theory. In general, without careful consideration of reference signal noise content and speed of comparator, the resulting square wave can easily have very poor quality. Thus, it is imperative to consider noise in clock generation process when high system performance is required.

7 Acknowledgements

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