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On-chip Digitally Tunable High Voltage Generator for Electrostatic Control of Micromechanical Devices

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Abstract— **Micromechanical structures with capacitive readout provide a feasible alternative for feedback by utilizing electrostatic forces without any requirement for additional electrodes. For this purpose high voltages are often required. This paper presents circuit structures for on-chip high voltage generation. A high voltage amplifier with digitally controllable output or a high voltage DAC is implemented and, as an example application, the DAC is used for quadrature compensation of a microelectromechanical gyroscope. The implemented high voltage generator achieves output voltages between zero and 27 V in 29 mV steps. The charge pump output voltage is limited in all cases to prevent reliability problems.**

I. Introduction

Miniature mechanical structures in sensors, micromachined switches in telecommunication and micromirrors in optical transmission are examples cases, which often require some control by means of a force applied to the mechanical structure. In microstructures electrostatic coupling can be utilized and the required electronics can be integrated together with the rest of the electronic interface. Still, control voltages can be relatively high, which calls for some level of charge pumping together with regulation of voltage.

High voltage (HV) control with bandwidth of few kilohertz can be generated on-chip when the required load current remains sufficiently small. In such a case, the required HV generator can be implemented within moderate chip area. For this purpose following blocks are needed: A charge pump (CP) to increase the voltage above the supply, a regulator or an amplifier for setting the output of the charge pump to a certain desired level and a simple digital-to-analog converter (DAC) to control the regulator and the output voltage digitally. Implementation of these circuits is discussed in this paper and finally measurement results are obtained for an open-loop high voltage DAC. As an application example of the high voltage DAC, a closed-loop quadrature control of a microelectromechanical gyroscope [1] is implemented and measured.

II. Structure of the High Voltage Generator

The block diagram of the high voltage generating system is shown in Fig. 1. The charge pump with an internal limiter generates a high supply voltage for a linear high voltage amplifier (HVA). The output voltage of the low voltage (LV) DAC is amplified to a desired level with the HVA.

When high voltages are required, the voltage tolerance of components must not be exceeded to avoid reliability problems. This can be ensured by limiting the charge pump output voltage to the required level within the temperature and load variation and in process corners. A separate LV DAC and a linear HVA is a more feasible alternative for accurate output voltage generation compared to a case where a single HV DAC is used. This is a valid assumption in case the required voltages are higher than the gate-source voltage tolerance of transistors. In such a case, protecting MOS devices from excess oxide stress would require a complex switch control scheme.

III. Charge Pump Configuration with Output Voltage Control

Few different methods exist to produce an accurate output voltage level in the charge pump. Method for controlling the switching frequency is proposed in [2]. In this method, the frequency is regulated according to the pump load or the pump output voltage. A method, where a delta-sigma controller is used to reduce the tones of a regular pulse frequency modulation technique, is presented in [3].

If the voltage levels required for the pump are higher than maximum gate-source voltages of transistors, the use of a traditional level shifter is not possible. Full scale clock signals cannot be used either, which prevents the use of cascaded voltage doublers [4] without a complicated clock generator. Thus, the Dickson-type [5] charge pump would be the most flexible to generate high on-chip voltages. Chip area can be utilized more efficiently by creating first medium voltage clock signals, which can then be used for pumping in the second charge pump. This way, LV capacitors with higher capacitance density can be used for creating the medium voltage and

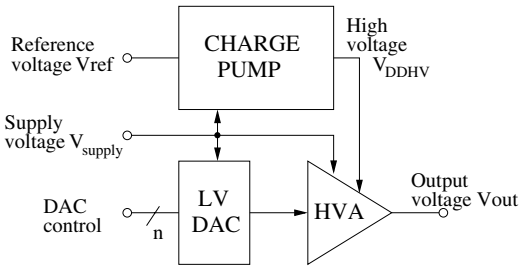

Fig. 1. Block diagram of the HV generator.

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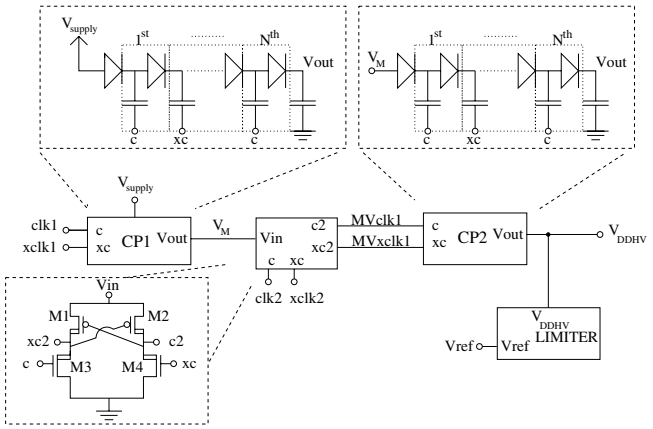

Fig. 2. Block diagram of the charge pump with the limiter.

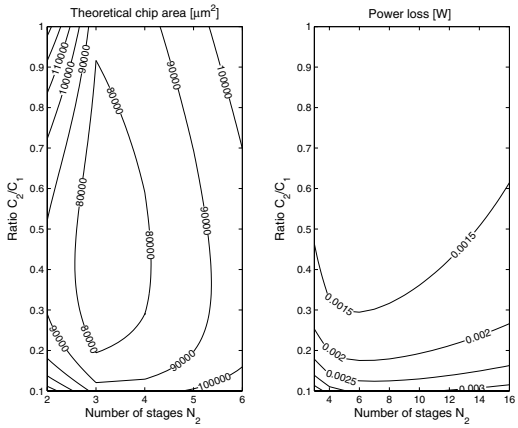

Fig. 3. Theoretical chip area (left) and power loss due to bottom plate parasitics (right).

further, by using the medium voltage clock, the effect of diode forward voltage drop is reduced [6]. A block diagram of the system is presented in Fig. 2.

In order to create a fully integrated charge pump for electrostatic control of micromechanical structures, the maximum required speed is limited purely by the capacitive load. For applications with narrow bandwidth, it is feasible to create all the required voltages on-chip with minimum area. For this purpose, the optimal structure of the charge pump can be found. The size of capacitor C_2 in the pump topology used can be solved from equation for the output voltage [6]

$$V_D = \frac{(N_2+1)(N_2+1)(V_{DD}-V_F)}{1+N_2N_1x} - \frac{N_2+1}{1+N_2N_1x}\frac{I_0N_1}{C_1f_1} - V_F(N_2+1) - \frac{I_0N_2}{C_2f_2}, \quad (1)$$

where I_0 and V_D are the desired load current and output voltage, C the pump capacitor, f the pump clock frequency, N the number of pump stages, V_{DD} the supply voltage, V_F the diode forward voltage drop and subindexes 1 and 2 refer to CP1 and CP2 in Fig. 2. The variable x tells the effective size of second stage bottom plate parasitics and equals $C_{p2}f_2/(C_1f_1)$ with $C_{p2} = 0.3C_2$. Now, with the area densities of a capacitors, C_{A1}, C_{A2} and the diode area A_D, the total charge pump area A_{TOT} can be written as

$$A_{TOT} = N_1(\frac{C_1}{C_{A1}} + A_D) + N_2(\frac{C_2}{C_{A2}} + A_D) + 2A_D. \quad (2)$$

The required size of pump capacitor C_2 can be solved using (1), while $N_1 = 2$ is determined by components available in technology used. An example plot of theoretical A_{TOT} in Fig. 3 is obtained by substituting C_2 into (2) and by using typical values of 30 V, 5 V, 0.66 V, 16 MHz, 2 MHz and 17 μA for V_D, V_{DD}, V_F, f_1, f_2 and I_0, respectively. The current magnitude I_0 is dictated by the HVA in Fig. 1 and feedback components of the limiter. Parasitic power consumption of bottom plate parasitics of the pump capacitors, which is significant for integrated capacitors [4], is given as

$$P_{par} = f_1N_1C_{p1}V_{DD}^2 + f_2N_2C_{p2}V_M^2, \quad (3)$$

where $C_{p1} = 0.3C_1$ and $C_{p2} = 0.3C_2$ denote the bottom plate parasitic of a single pump capacitor and V_M is the medium voltage shown in Fig. 2. A minimum of A_{TOT} can be found at $N_2 = 3$ and $C_2/C_1 = 0.45$. At this point, the pump unloaded voltage is 45 V. Compared to regular Dickson-type pump with minimum chip area, also presented in [7], and the same load conditions, the pump structure used enables roughly 20 % smaller chip area with some increase in supply current. The difference in chip areas becomes more evident with larger difference in the charge pump output and the supply voltage.

When the operation occurs near the maximum voltage tolerances of the components, the output voltage of the charge pump can be limited simply by adding suitable amount of extra load. The load control can also be performed by directly controlling the HVA bias current as long as the stability of the amplifier is ensured. This way, no spurious components and only a small amount of additional noise from the limiter will be generated to the charge pump output at frequencies lower than the pump clock. The implemented structure of the limiter is shown in Fig. 4. The V_{DDHV} is limited using LV reference Vref and the feedback is implemented using polysilicon resistors. Resistors were used instead of any switched capacitor implementation due to limited gate-source voltage tolerance of the transistors. With a single stage LV amplifier, the stability

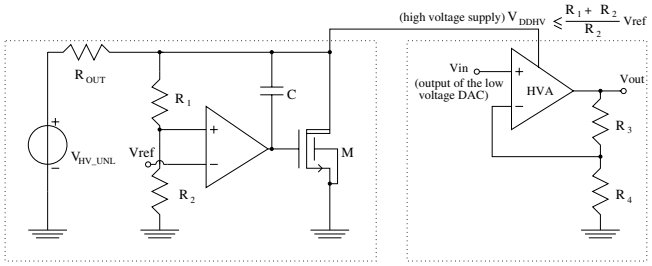

Fig. 4. Linear model of the limiter and the charge pump (left) and the high voltage amplifier in the feedback configuration used (right).

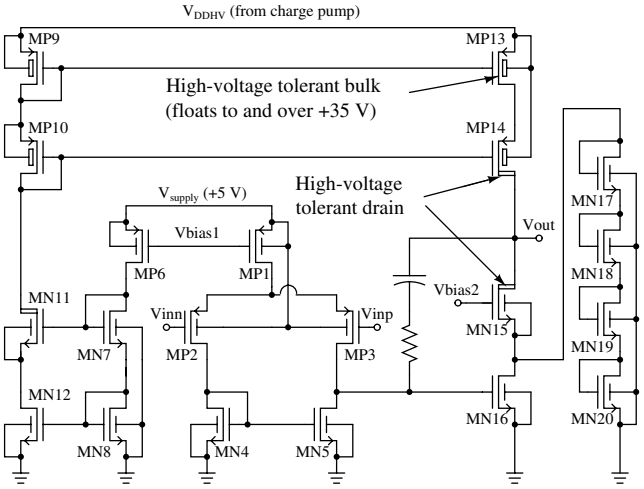

Fig. 5. A schematic view of the high voltage amplifier.

of the two stage structure can be ensured by applying similar methods as those used for two stage amplifiers.

IV. High Voltage Amplifier

The purpose of this amplifier is to amplify the output of the LV DAC to cover the full high voltage tuning range. The amplifier is designed as a two stage Miller-compensated operational amplifier, where the first stage operates with the nominal supply voltage and the second stage is powered by the charge pump. This configuration reduces charge pump load and chip area. The structure of the amplifier is shown in Fig. 5. The cascode transistors are used for blocking the high voltages and to enable the use of floating LV PMOS transistors for an accurate current mirror. The diode cascade (MN17 – MN20) prevents the drain of the NMOS transistor MN16 from floating to and above the LV supply when the first stage drives this transistor to off state. The amplifier draws a current of 11 μA from the pump output, 10 μA of which is the current consumed by the second stage. The current magnitude is mostly dictated by the chip area of the charge pump and feedback components (Fig. 4, R_3 and R_4) and, on the other hand, by the required signal bandwidth and total current consumption. Thus, the current magnitude cannot be decreased merely according to the bandwidth requirements. The resistor sizes used in the design are 6 $M\Omega$ and 0.6 $M\Omega$, which enable an accurate absolute gain of 11. When using resistors this large, the phase change in the feedback should be carefully analyzed. In some cases, the effect of the phase droop can be alleviated using capacitors in parallel with the resistors to correct voltage division and phase change at higher frequencies.

V. Low Voltage DAC

As the digital control signals are used only in LV circuit configurations, the implementation of the DAC is straightforward. The selected converter topology is a resistor string DAC, which has guaranteed monotonicity. Its output voltage range is suitable for driving the HVA. For the electrostatic control of a gyroscope the DAC has a 4-bit part for coarse tuning enabling output voltage over the whole HVA output range and a 7-bit fine tuning part with LSB of 2.6 mV. The fine tuning range is designed to cover possible temperature effects, which need to be compensated.

VI. Gyroscope and High Voltage Quadrature Compensation

The quadrature compensation of a micromachined gyroscope is implemented using the presented HV DAC to generate the high voltage control signal. The double gimbal gyroscope used is shown in Fig. 6. If the ideal operation is considered and the inner (primary, driven) resonator is excited to maximum usable vibration amplitude, only the Coriolis force, resulting from rotation about the sensitive axis, will cause vibration to couple from the primary resonator to the outer (secondary) resonator. By detecting the vibration amplitude of the secondary resonator the magnitude of the angular velocity can be calculated.

In reality, there are several mechanisms, which cause error to the secondary signal amplitude [8]. One of these is the signal that results from coupling of primary resonator vibration to the secondary resonator due to misalignment between the two resonators. The resulting signal is in quadrature with respect to the angular velocity signal and theoretically, could be completely rejected by using phase coherent detection of the vibration amplitude. However, the magnitude of this quadrature signal component can be order of magnitude higher than the full scale angular velocity signal and will thus most likely limit the dynamic range and cause error when even a slight phase mismatch is present during the amplitude detection.

Sufficient electrostatic force is required to compensate the quadrature signal, which further denotes that high voltages are required. When the HV source is combined with a controller, the temperature stability of various references is relieved. Again, the phase error in the amplitude detection must be considered. The phase error together with the applied compensation method and the properties of the compensation loop, including the sensor and the electronics, dictate the minimum required control voltage step size. As the electrostatic force is dependent on voltage squared, the minimum control voltage step size must be defined for maximum control voltages. For the presented case, the LSB size of 29 mV corresponds to roughly 30 percent change of quadrature signal when referred to the full scale angular velocity signal.

VII. Measurement Results

The chip was implemented using a 0.7 μm double-metal, double-poly high voltage BiCMOS process that offers high-ohmic polysilicon resistors, good-quality analog capacitors and floating diodes. The chip microphotograph is shown in Fig. 6 and the effective area is 1.2 mm^2. The charge pump with limited output draws a current of 2.8 mA from a 5 V supply. The DAC open loop performance is shown in Fig. 7. Table I shows the measured linearity of both the fine tune part and the calibratable part of the DAC.

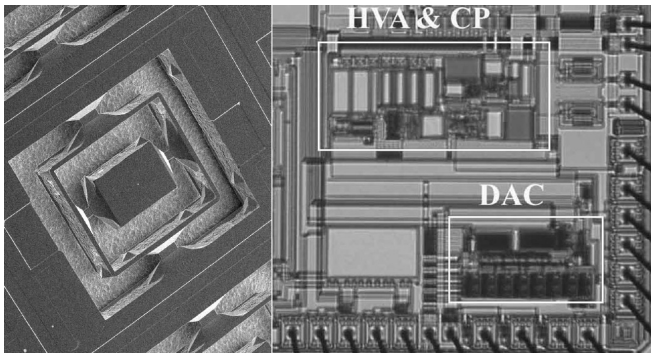

Fig. 6. Left: SEM picture of the gyroscope's structural wafer (picture courtesy of VTI Technologies Oy, Vantaa, Finland). Right: A microphotograph of the implemented chip.

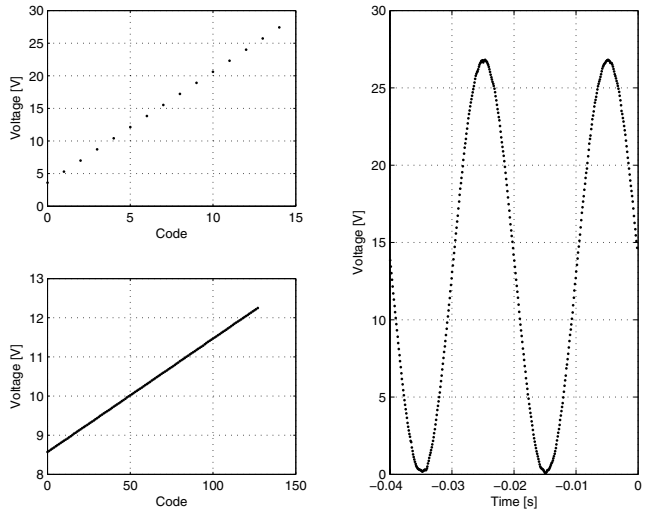

Fig. 7. Output voltages of the high voltage DAC calibratable part (upper left) and fine tune part (lower left). Rail-to-rail sinusoidal output of the HVA with an analog input (right).

Closed loop effect of the quadrature control is shown in Fig. 8 with a zero external angular velocity signal and an extra phase error ϕ_{err} between the demodulator clock and the secondary resonator signal. The phase error causes the quadrature control signal to couple to the angular velocity channel. The ratio of Q and I channel components is given by $cos(\phi_{err})/sin(\phi_{err})$. The used quadrature controller integrates the quadrature signal to zero while the finite resolution of the DAC results in oscillation of control voltage with an amplitude of $V_{LSB}/2$.

VIII. Conclusions

A fully integrated digitally controllable HV generator was presented. The implemented circuit enables use of high voltages between 0 and 27 V in 29 mV steps for electrostatic control in microelectromechanical devices with less than 3 mA current from 5 V supply. The presented structure consists of a charge pump with limited output to prevent reliability problems, a high voltage amplifier to amplify the LV signal to full output range and a LV DAC to enable digital controllability. As an example application of the high voltage DAC, electrostatic control of micromachined gyroscope was presented.

TABLE I

The high voltage DAC LSB sizes and maximum INL and DNL.

DAC: 4-bit Calibratable Section		**DAC: 7-bit Fine Tune Section**	
LSB [V]	1.700	LSB [mV]	28.95
INL [LSB]	0.00445	INL [LSB]	0.227
DNL [LSB]	0.00143	DNL [LSB]	0.140

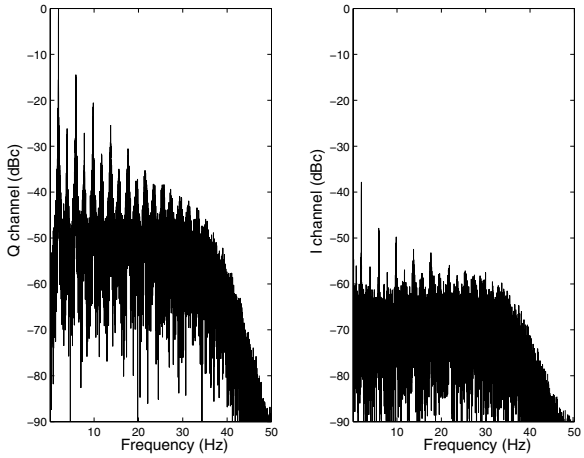

Fig. 8. Measured secondary resonator signals after demodulation. Q channel signal (left) and I channel or angular velocity signal (right) with ϕ_{err} of $0.8°$.

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