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High Resolution Analog-to-Digital Converter for Low-Frequency High-Voltage Signals

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***Abstract*— In this paper, a design and measurements of a high resolution analog-to-digital converter (ADC) will be presented. The implemented $\Sigma\Delta$-ADC is combined with a low-noise buffer which enables the use of a single-ended input signal with maximum value of twice the nominal supply. The designed system was measured to achieve input referred noise voltage density of 220 $nV/\sqrt{Hz}$ and a bandwidth up to 1 kHz. The presented system will be applied for digitizing the output of a continuous-time accelerometer.**

I. Introduction

Inertial sensors are providing digital output more and more commonly nowadays. The microelectromechanical accelerometers or gyroscopes typically have either an inherent digital output [1], [2] or it is created by adding a separate ADC to a continuous-time sensor. The first of the two alternatives is gaining increasing popularity especially due to lowered power consumption. If for example noise prevents the use of switched-capacitor (SC) front-end for the mechanical element, a continuous-time interface [3] is used and a separate ADC is added to the system. In this case, care must be taken so that the ADC does not interfere with the functionality of the actual sensor.

Oversampling ADCs are commonly used in applications where the resolution of Nyquist rate ADCs is not sufficient. This is typically the case when the converter relies on component matching and the accuracy is limited to roughly 12 bits. In case the noise limited resolution up to 120 dB at narrow signal band is required, the oversampling converters offer the only feasible solution. [4]

Commonly used SC ADCs set fairly high requirements on the driver with respect to both speed and noise. The requirements are further emphasized when the signal band is located close to dc and flicker noise must be effectively suppressed. An option to SC ADC is a continuous-time $\Sigma\Delta$-ADC, which easies the requirements of the ADC driver, but on the other hand suffers from increased sensitivity to clock jitter [5]. Continuous time ADCs neither enable the use of traditional SC techniques for low frequency noise reduction [6].

This paper presents the design of a differential third order $\Sigma\Delta$-ADC together with a buffer that is capable of using single-ended high-voltage input. The low-frequency noise content is reduced by using bipolar input pair for the buffer and correlated double sampling (CDS) technique for the ADC.

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Section II gives the structure of the ADC and section III the properties of the ADC buffer. In section IV measured results are presented.

II. ADC

The ADC is designed for a 120 dB resolution at a maximum signal bandwidth of 1 kHz. The block diagram of the third order single stage $\Sigma\Delta$-ADC is shown in Fig. 1. The converter has a single bit output and the nominal supply and clock frequency are 5 V and 2 MHz, respectively. The capacitors used are analog MOS capacitors. Quantization noise limited signal-to-noise ratio of the ADC is more than 160 dB.

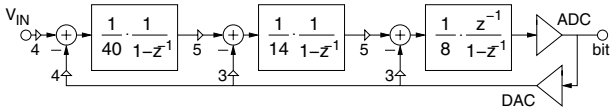

Fig. 1. Block diagram of the implemented $\Sigma\Delta$-ADC. The feedback and the signal gains at different stages are marked in the figure.

As the signal band concentrates at low frequencies not only the switch noise and the operational amplifier (opamp) white noise but also any low frequency noise must be carefully taken into account. Reduction of the inherent low frequency noise of the opamp requires typically MOSFET devices with considerably increased channel area. The resulting increase of parasitic capacitance might cause additional stability and noise issues. Therefore, low-frequency noise reducing SC techniques such as CDS or chopper stabilization are commonly used [6].

The opamp used for the first integrator of the modulator is shown in Fig. 2. Generally, the telescopic amplifiers allow high transconductance with respect to the supply current. In this case the current of the input pair is 60 $\%$ of the total ADC supply current, while rest of the current is consumed by biasing structures of the first integrator and the complete second and third integrators together with the comparator.

In telescopic amplifiers the single-ended signal amplitude is limited to

$$V_{a\_se} = V_{CM\_out} - (V_{CM\_in} - V_T + V_{DS4,5}), \qquad (1)$$

where V_{CM_out} and V_{CM_in} are the output and the input common-mode (CM) levels, V_T the threshold voltage of the input pair transistors and $V_{DS4,5}$ the drain-source saturation voltage of cascodes. Although only a theoretical result, the equation clearly indicates that the input CM should be as low as possible to maximize the output swing.

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The schematic of the common-mode feedback (CMFB) used for every amplifier of the ADC is also shown in Fig. 2. It is capable of keeping the CM level in both clock phases.

For $\Sigma\Delta$-ADC the voltage-mode signals between the integrator stages can be scaled so that the maximum swing fits within the linear operating range of the opamp without changing the signal or noise transfer functions. Depending on the ADC topology used, the first integrator gain is fairly small, which can also been seen in Fig. 1. When the signal needs aggressive scaling, because of the small linear range of the amplifier, the integrator gain is decreased so that the linearity is preserved. Especially in the first integrator, the size of the input capacitors is determined by kT/C-noise and cannot therefore be changed. Hence, the only controllable parameter is the feedback capacitor, which already dominates the chip area and whose bottom plate parasitic can limit the speed and the power consumption. Therefore the need for scaling should be minimized. For the designed ADC, with the V_{CM_in} selected high enough to stabilize the tail current and V_{CM_out} at mid-rail, the V_{a_se} is 1.5 V.

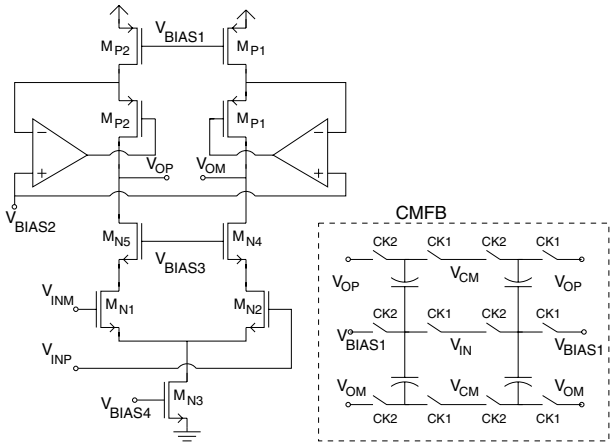

Fig. 2. A simplified schematic of the telescopic operational amplifier used for the first integrator. The output impedance of the PMOS-transistors is increased by using regulated cascode transistors and hence, the output impedance of the amplifier is limited by NMOS-transistors to roughly 70 dB. The encircled area shows the common-mode feedback used for the amplifiers of the ADC.

The first integrator of the ADC is shown in Fig. 3. During the sampling phase the opamp offset is stored in C_{DS1} and C_{DS2}, while capacitors C_{A1} and C_{A2} bias the CM level at the opamp input to correct value. The input signal $V_{INP} - V_{INM}$ is also sampled. During the charge transfer phase, the charge stored in sampling capacitors C_{I1} and C_{I2} is transferred to the feedback capacitors C_{FB1} and C_{FB2}, while CDS capacitors C_{DS1} and C_{DS2} operate as floating voltage sources and cancel the low frequency noise at the input of the opamp. Hence, the opamp input can be biased to voltage close to ground rail in the both clock phases, while the output operates around mid-rail.

The switches used in the integrator are mainly transmission gates, denoted with TG, while switches operating near ground rail are plain NMOS transistors. The descending edge of the input sampling clock is delayed for bottom plate sampling. Common capacitors are used for both sampling and feedback.

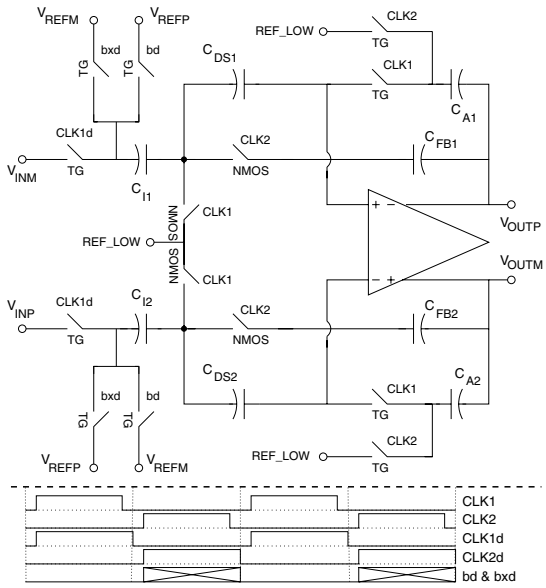

Fig. 3. The block diagram of the first integrator in the ADC. Topology enables the use of different common-mode levels for the amplifier input and output together with correlated double sampling technique. The clock phases depicted are used for the whole ADC. The feedback phases bd and bxd are both clocked at $clk2d$. The phase bxd is the inverted version of bd.

The second integrator, shown in Fig. 4, has input capacitor values divided roughly by ten compared to the first amplifier. When referring to the input the second integrator noise is divided by the first integrator gain, which is 30 dB at the signal band edge, at 1 kHz. All the integrators use the feedback at the same clock phase $CLK2$.

III. ADC Buffer

The optimal structure of the buffer that is suitable for driving the ADC depends solely on type of input that needs to be digitized. In a typical occasion the input voltage range would fit within nominal supply rails, in which case a suitable CMOS or BiCMOS unity gain buffer would be the best option to avoid extra noise from feedback components. Independent on the topology the buffer must settle within half a clock cycle and have a low flicker noise together with low enough white noise content to prevent heavy noise folding.

In current case, the single-ended source has CM level of 6 V and maximum amplitude of 3.2 V. In order to avoid heavy loading of the 12 V high-voltage (HV) supply, the buffer should draw the most current from the nominal supply. Because of the single-ended HV signal source, resistors are used as feedback components although they cause excess noise and loading of the signal source. To change the input to differential signal and between the nominal supply rails, the amplifier of Fig. 5 is used. The CM level at the opamp input is given as

$$V_{CM\_OPA\_IN} = \frac{V_{INM} + V_{INP}}{4} + \frac{V_{REF\_MID\_RAIL}}{2}, \quad (2)$$

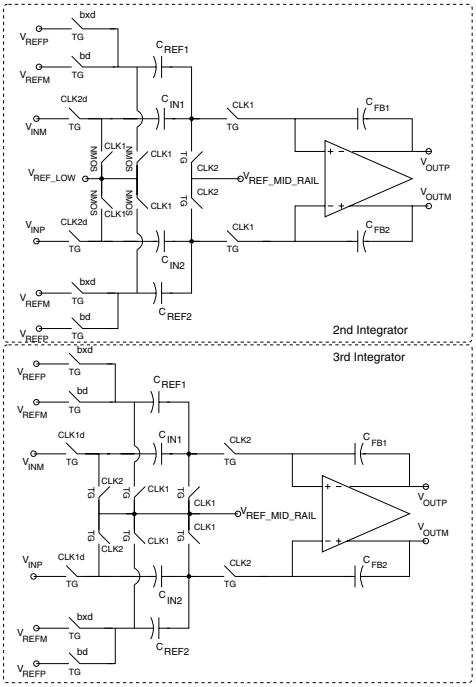

Fig. 4. The block diagram of the second and third integrator in the ADC. The second integrator utilizes a telescopic amplifier and therefore also two common-mode levels. Third integrator employs a folded-cascode amplifier and only a single common mode level at mid-rail is required. The third integrator is followed by a comparator whose input is evaluated at the descending edge of the clock phase $CLK2$.

when all the resistors have equal values. With $V_{REF\_MID\_RAIL}$ of 2.5 V, the reference input V_{INM} of 6 V and the signal input V_{INP} values ranging from 2.8 to 9.2 V, the CM level at the operational amplifier input varies between 3.45 and 5.05 V. The size of the resistors, 25 $k\Omega$, is selected on the basis of noise and increased power consumption it causes. With these resistor values the opamp produces 30 $\%$ of the total noise power. The bandwidth of the buffer, 25 MHz, allows fast enough settling, but folding also increases the white noise by 13 dB at the signal band.

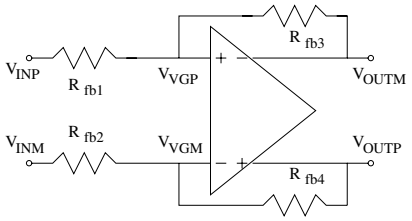

Fig. 5. The block diagram of the unity gain, ADC driving buffer.

The opamp for the buffer is required to tolerate input CM levels above the nominal supply. The simplified schematic of the two stage amplifier with HV first stage is shown in Fig. 6. A bipolar input pair is used in order to both reduce the flicker noise and allow use of high voltages. The low voltage PMOS transistors, M_{P2} and M_{P1}, function as accurate low flicker noise current sources, which are protected by diodes D_1 and D_2. NMOS transistors are not used in the first stage because of their significant flicker noise level. The second stage that uses nominal supply drives the sampling capacitors of the ADC. The folded first stage enables the use of an NMOS input with higher transconductance for the second stage. The output CM

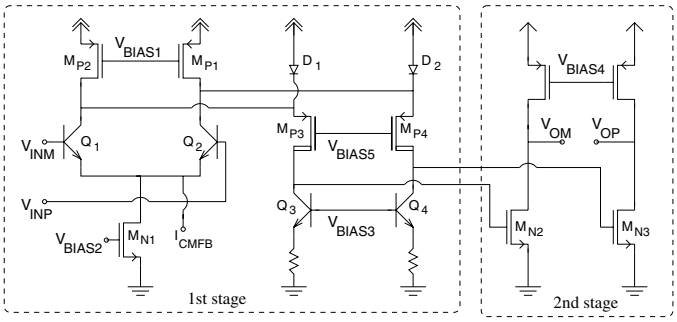

Fig. 6. The operational amplifier used for the unity gain buffer that is driving the ADC. The bipolar transistors at the input tolerate high voltages and produce less low-frequency noise compared to a MOSFET input pair. The high-voltage supply is fed only to the input pair whereas the second stage uses the nominal supply, same as the ADC.

level is controlled by a single CMFB of Fig. 7, which controls the tail current of the input pair. The CMFB is straightforward to stabilize by setting its transconductance smaller compared to the differential pair, but extensive simulations are required to confirm that the tail current control does not cause stability or linearity issues. Unlike for opamp with PMOS first stage input and NMOS second stage input or vice versa, the used topology does not have a stable operation point with both inputs and outputs at either supply rail and zero current flow through the amplifier.

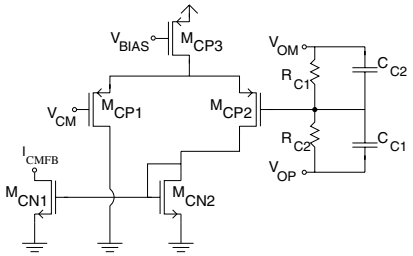

Fig. 7. The common-mode feedback that is used to stabilize the output common-mode voltage of the ADC buffer.

IV. Measured Results

The chip was implemented using a 0.7 μm triple-metal, double-poly HV CMOS process. The chip microphotograph is shown in Fig. 8. The current drawn from the nominal supply by the ADC is 2 mA and by the buffer 1.5 mA. The HV supply current is 50 μA.

The separately measured linearity of both the ADC and the buffer is shown in Fig. 9. The input referred noise of the ADC is shown in Fig. 10. The data is measured with a low-noise dc signal of 3.1 V at the input. The distortion at harmonics of line frequency couple through references and supply.

The noise of the buffer is shown in Fig. 11. It is measured by shorting both inputs to the CM reference. The folding will multiply the white noise voltage by a factor of four, which means that the buffer induces noise of roughly 200

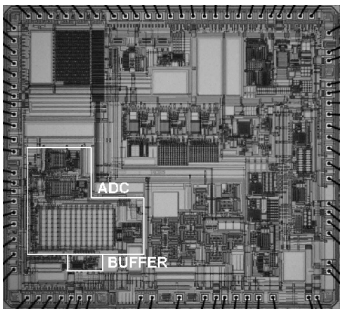

Fig. 8. The chip microphotograph with encircled areas marking the ADC and the ADC buffer. The areas of the ADC and buffer are 2.6 mm^2 and 0.15 mm^2, respectively. The total chip size is 24.5 mm^2

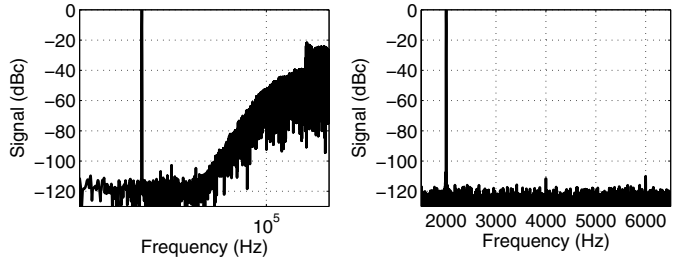

Fig. 9. Linearity of the independent ADC (left) and buffer (right). Both are measured with the same signal amplitude of 5.6 V peak-to-peak. For the ADC the SFDR is 102 dB and for the buffer 110 dB. The excess ADC noise derives from the signal generator.

$nV/Hz^{1/2}$ and dominates the noise of the combined ADC and buffer. Although the on-chip configuration does not allow measurements of the noise performance of the combination directly, the linearity of the ADC and buffer is shown in Fig. 12. Now, the effect of the uncharacterized on-chip signal source is included in the figure and hence, the measurement depicts only the worst case linearity. The configuration allows also integrated 1.5 $k\Omega$ resistors to be added between the buffer and ADC to both linearize the settling and also limit the noise bandwidth. These resistors basically limit the linearity to 80 dB with same signal of 4.7 V that was also used for measurement with no resistors. According to simulations the noise voltage would halve when the resistors are used. Now the calculated input referred noise of the buffered ADC in the two cases would be 130 $nV/Hz^{1/2}$ with and 220 $nV/Hz^{1/2}$ without the band limiting resistors. The maximum sinusoidal input signal is 2 V rms.

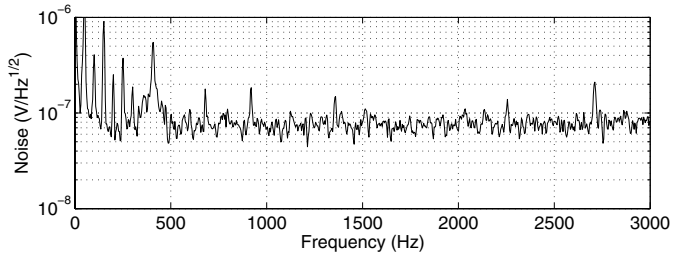

Fig. 10. Input referred noise of the ADC. The white noise level is 80 $nV/Hz^{1/2}$.

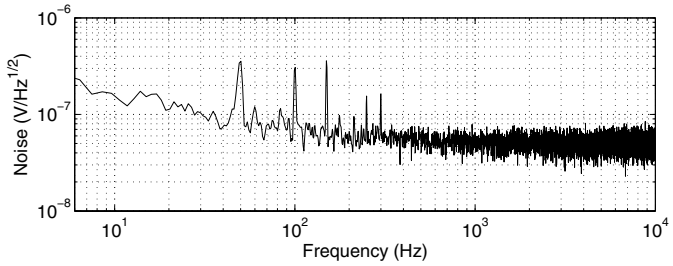

Fig. 11. Input referred noise of the buffer. The white noise level is 50 $nV/Hz^{1/2}$.

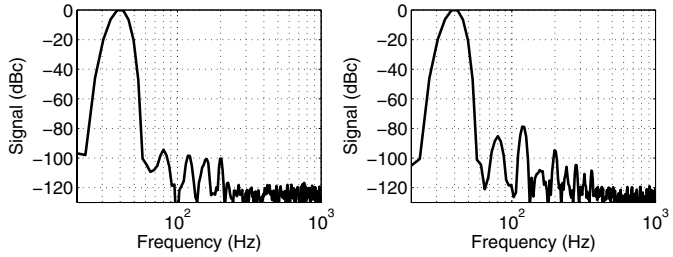

Fig. 12. Left: Linearity of the buffered ADC without resistors between the buffer and the ADC. The HD2 and HD3 are -95 dB and -98 dB, respectively. Right: Linearity with 1.5 $k\Omega$ resistors between the ADC and the buffer. The HD2 and HD3 are -85 dB and -79 dB, respectively. In both measurements the 40 Hz signal at the ADC input has an amplitude of 4.7 V peak-to-peak.

V. Conclusions

A design and measurements of a buffered ADC were presented. The buffer is capable of interfacing single-ended signals and voltages higher than the nominal supply. The input referred noise of the system is limited by the folded noise of the buffer, which is high due to resistive feedback components. The measured results indicate low flicker noise level for both the ADC and the buffer, which allows small signal bands to be digitized accurately. The first integrator of the $\Sigma\Delta$ allows the use of two different CM levels together with CDS technique, while the buffer relies on bipolar transistors to reduce flicker noise.

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