Publication V

Lasse Aaltonen, Timo Speeti, Mikko Saukoski, and Kari Halonen. 2009. An interface for a 300°/s capacitive 2-axis micro-gyroscope with pseudo-CT readout. In: Digest of Technical Papers of the 2009 IEEE International Solid-State Circuits Conference (ISSCC 2009). San Francisco, CA, USA. 8-12 February 2009. Pages 344-345. ISBN 978-1-4244-3457-2.

© 2009 Institute of Electrical and Electronics Engineers (IEEE)

Reprinted, with permission, from IEEE.

This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of Aalto University's products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee.org.

By choosing to view this document, you agree to all provisions of the copyright laws protecting it.

Please click on paper title to view Visual Supplement.

20.3 An Interface for a 300°/s Capacitive 2-Axis Micro-Gyroscope with Pseudo-CT Readout

Lasse Aaltonen[1], Timo Speeti[1], Mikko Saukoski[1,2], Kari Halonen[1]

[1]Helsinki University of Technology, Espoo, Finland
[2]ELMOS Semiconductor, Dortmund, Germany.

The widespread use of capacitive MEMS vibratory gyroscopes is powerfully driven by low cost [1]; this is partly determined by factors such as die area and the number of necessary external components. Important properties of gyroscopes also include a short start-up time, and resolution that has been recently improved by applying the mode-matching technique [2,3]. However, the electromechanical feedback loop for active-mode matching requires additional DSP and chip area, and involves an additional slowly settling loop during the sensor start-up. The pseudo-continuous-time (CT) secondary (sense) readout technique introduced in this paper is applied to the open-loop secondary readout of a gyroscope operating in the low-pass region. The technique alleviates the issues related to complexity and area as well as to the large time constants of the CT readout [4,5] without compromising noise performance or start-up time. The proposed 5.4mW gyroscope interface includes an on-chip HV charge-pump (CP) for excitation and signal detection.

The block diagram of the interface is shown in Fig. 20.3.1. Reliable start-up and clock generation require a CT readout to be used for the drive (primary) loop, although its use can be avoided in the secondary channels. The lossy loop integrator provides the required phase shift, while decreasing the gain at higher frequencies, hence reducing sensitivity to the parasitic resonance modes of the drive resonator. The HPFs provide low-noise gain and remove the offset of preceding blocks; this is also important for the sine-to-square conversion that is required to generate a reference clock for the system. To prevent excess phase noise and glitches in the clock, the noise BW of the amplified primary signal is limited in the integrator before feeding the sine wave to the reference clock generator. In the generator, the signal is led to a comparator through a passive HPF (-3dB @ 200Hz) that removes any remaining offset. The phase shift from the charge-sensitive amplifier (CSA) input to the comparator input can be tuned to 90° with a 1° error over the temperature range. The resulting clock is used as a reference for the fully integrated PLL and as a clock for the amplitude controller, which controls the drive loop dynamics and start-up. During initial start-up, the SC amplitude controller receives few random clock pulses due to the loop DC settling, and amplifies the input signal, V_{ref4}. The resulting DC control signal maximizes the VGA gain and the drive signal quickly reaches the CP limited level. When the primary signal has increased sufficiently, the signal amplitude settles to the level defined by V_{ref4}. In the amplitude controller, filter HPF_3, which isolates the SC controller from the CT readout, has feedback MOSFETs that are also used in CSA, HPF_1 and HPF_2. The additional capacitor C_F of value 1pF, not present in a similar biasing scheme reported in [5], levels the voltage across the biasing MOSFET M_B and prevents the shifting of the amplifier input common-mode (CM) with increasing signal amplitude. The temperature-insensitive capacitive feedback components of the CSA and HPFs provide stable gain. Hence, to stabilize the gyroscope gain, the controller input is connected to the HPF_1 output. The amplitude extraction is enabled by the 90° phase difference between the subsampling controller and the clock, generated after the integrator. The amplitude is sampled to C_{C2}, while R_{C1} limits the noise band, and C_{C5} removes the 1/f noise and offset.

The schematic of the secondary readout is shown in Fig. 20.3.2. The quadrature signal is electrically compensated by feeding a sample of the primary signal (Fig. 20.3.1) through a tunable capacitor matrix (15fF–500fF). This compact quadrature nulling method prevents the front-end from saturating. The purpose of the pseudo-CT readout technique is to integrate the input current by half a period and hence reveal the amplitude without sampling the signal. The integration of the ideal secondary resonator current, at 90° phase difference compared with primary signal, starts when φ_{r1} goes low. To remove kT/C noise at the CSA output, φ_{r2} goes low $T_P/8$ later, as in the CDS SC interface of [6]. The VGA integrates the CSA output by half of the period to extract the amplitude. Sampling is performed by the notch filter, before which the noise BW is limited by using resistors R_{BWp} and R_{BWn} instead of the VGA bias to preserve the linearity of the CT signal. The minimum BW is determined by the maximum allowed phase droop.

In the proposed readout circuit (Fig. 20.3.2) the integration periods occur with a delay of $T_P/4$ and the resulting output sample period is $T_S=1/f_S=3/2T_P$. Every second sample (at φ_i and φ_{ix}) reveals the angular velocity and every other one (at φ_q and φ_{qx}) the quadrature signal amplitude, while the information is modulated at $f_S/2$. The notch filter rectifies the signal, thus upconverting 1/f noise and offset. The notch at $f_S/2$ removes the upconverted disturbances. Another notch filter is used to extract the quadrature amplitude by sampling the input in φ_q and φ_{qx} instead of φ_i and φ_{ix}. The CSA gain is limited by input leakage currents that change the CSA output with a constant slope during the integration period. The CSA also determines the power consumption and noise performance of the readout. When the signal in the quadrature phase is zeroed using quadrature compensation, the derivative and hence sensitivity to phase noise is minimized at the descending edge of φ_i and φ_{ix}, which corresponds to the sampling point.

The prototype is fabricated in a 0.35µm HVCMOS technology. The chip (Fig. 20.3.6) area is 7.9mm^2 with an active area of 2.5mm^2. The chip is combined with a 2-axis micro-gyroscope on a PCB and measured using off-chip references. The DC transfer functions from input angular velocity to sensor output, measured at the full input range of ±300°/s and in the temperature range from -10 to 90°C, are shown in Fig. 20.3.3. The noise floors of the sensor, shown in Fig. 20.3.4(a,b), are measured with DC detection of 8.75V, created on-chip using a 2V external V_{ref3}. Though the secondary resonators are symmetrical, the quadrature signal levels differ, which affects the interface noise properties. In addition, the compensation cannot fully remove the y-channel quadrature signal, which impairs the linearity and noise performance. The x-channel noise is dominated by the excessive flicker noise of the front-end, and increased by parasitic capacitance on the PCB and cross-coupled drive noise at frequencies above 10Hz. In Fig. 20.3.4(c,d) both channels are shown during start-up. The start-up begins when CP reset is removed, and in 0.4s the secondary channels reach the final zero-rate output (ZRO) with a maximum error of ±6°/s.

The ASIC for the 2-axis gyroscope draws 1.8mA from the 3V nominal supply. The proposed pseudo-CT readout technique offers reduced complexity, inherent amplitude detection and chopper stabilization, with minimal noise increase compared with the CT interface. The system parameters and performance are summarized in Fig. 20.3.5.

Acknowledgments:
We thank VTI Technologies for providing the sensor elements and for funding, and the Finnish Funding Agency for Technology and Innovation for funding.

References:
[1] J. Geen, "Very Low Cost Gyroscopes," *Proc. IEEE Sensors*, pp. 537-540, Oct.-Nov. 2005.
[2] C. Ezekwe and B. Boser, "A Mode-Matching ΔΣ Closed-Loop Vibratory-Gyroscope Readout Interface with a 0.004°/s/√Hz Noise Floor over a 50 Hz Band," *ISSCC Dig. Tech. Papers*, pp. 580-581, Feb. 2008.
[3] A. Sharma, M. Zaman and F. Ayazi, "A 0.2°/hr Micro-Gyroscope with Automatic CMOS Mode Matching," *ISSCC Dig. Tech. Papers*, pp. 386-387, Feb. 2007.
[4] J. Geen, et al., "Single-Chip Surface Micromachined Integrated Gyroscope with 50°/h Allan Deviation," *IEEE J. Solid State Circuits*, vol. 37, no. 12, pp. 1860-1866, Dec. 2002.
[5] M. Saukoski, et al., "Integrated Readout and Control Electronics for a Microelectromechanical Angular Velocity Sensor," *ESSCIRC Dig. Tech. Papers*, pp. 243-246, Sep. 2006.
[6] X. Jiang, et al., "A Monolithic Surface Micromachined Z-Axis Gyroscope with Digital Output," *Dig. Symp. VLSI Circuits*, pp. 16-19, June 2000.

 978-1-4244-3457-2/09/$25.00 ©2009 IEEE

Please click on paper title to view Visual Supplement.

Authorized licensed use limited to: Teknillinen Korkeakoulu. Downloaded on January 13, 2010 at 00:17 from IEEE Xplore. Restrictions apply.

Please click on paper title to view Visual Supplement.

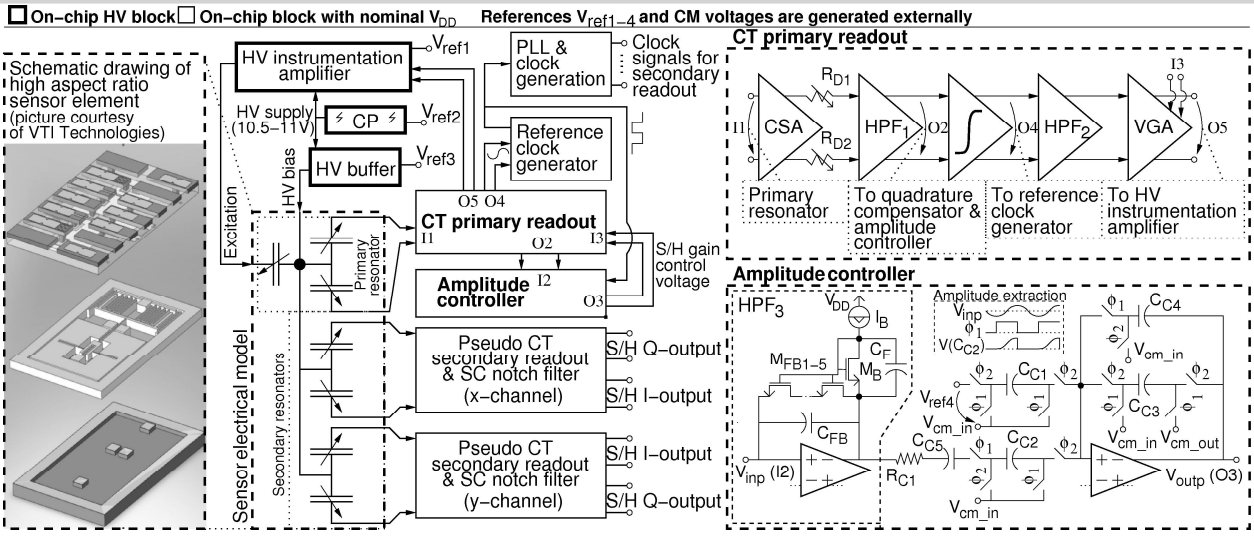

Figure 20.3.1: Block diagram of the interface including an electrical model and schematic drawing of the sensor element, together with more detailed structures of both the CT primary readout and amplitude controller (half of the differential circuit is shown).

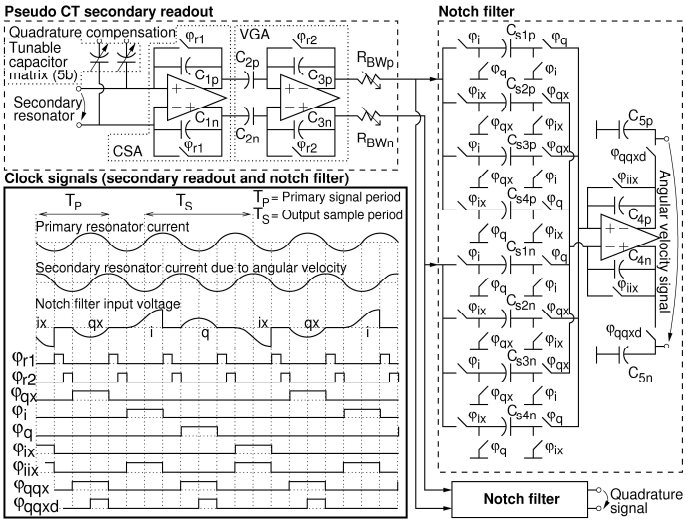

Figure 20.3.2: Schematic and used clock signals of the secondary readout channel, which consists of the pseudo-CT readout and the SC notch filters.

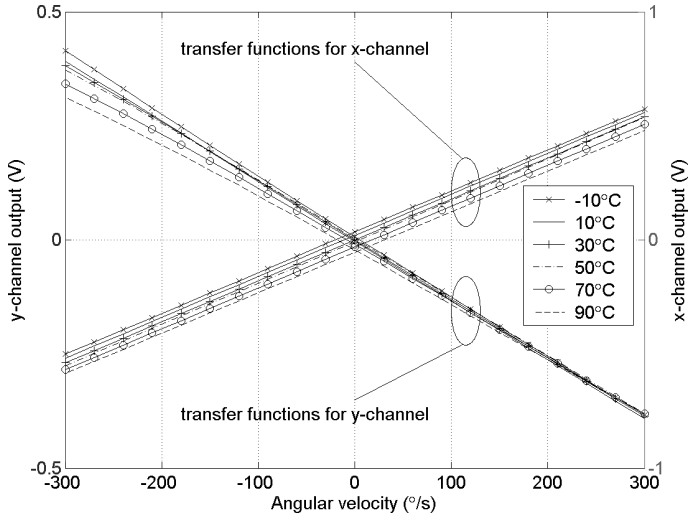

Figure 20.3.3: Transfer functions from DC angular velocity to sensor output voltage for both channels at temperatures from -10 to 90°C in steps of 30°/s and 20°C.

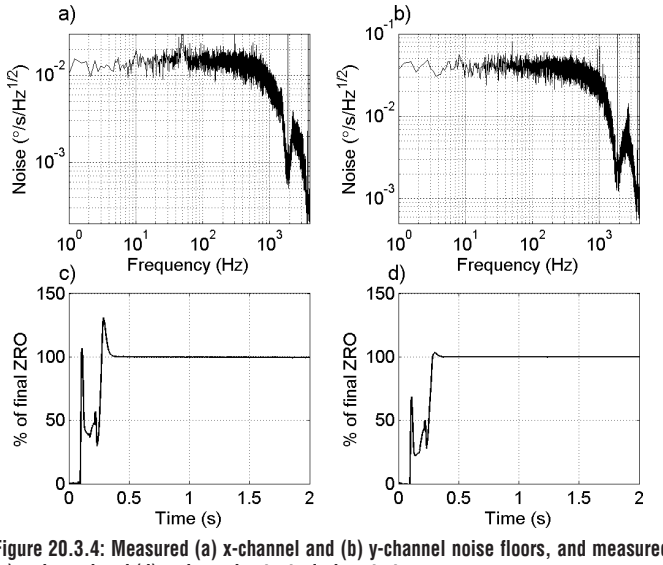

Figure 20.3.4: Measured (a) x-channel and (b) y-channel noise floors, and measured (c) x-channel and (d) y-channel outputs during start-up.

Process technology	0.35µm 2P4M HVCMOS					
Chip area (mm^2)	7.9 (active area 2.5)					
Supply voltage (V)	2.5-3.6					
Chip supply current (mA)	1.8					
Charge-pump / Three CSAs (% of tot.)	35 / 42					
	x-axis			**y-axis**		
Full-scale signal (°/s)	±300			±300		
Signal bandwidth max. (Hz)	300			300		
Spot noise (°/s/√Hz)	0.015			0.041		
Start-up time, to ±6°/s of the final ZRO (s)	0.4			0.4		
	-10°C	**30°C**	**90°C**	**-10°C**	**30°C**	**90°C**
Gain (mV/(°/s))	1.79	1.80	1.78	1.33	1.29	1.17
DC linearity (% of full-scale)	0.085	0.07	0.14	1.6	1.1	3.4
ZRO change from -10 to 90°C (°/s)	50			23		

Element properties	Primary	Secondary **x-axis**	Secondary **y-axis**
Resonance frequency (kHz)	5.7	8.1	7.6
Full-scale, 300°/s, signal (fF)	-	9	9

Figure 20.3.5: Summary of the measured performance and the open-loop characteristics of the sensor element.

Please click on paper title to view Visual Supplement.

Authorized licensed use limited to: Teknillinen Korkeakoulu. Downloaded on January 13, 2010 at 00:17 from IEEE Xplore. Restrictions apply.

Please click on paper title to view Visual Supplement.

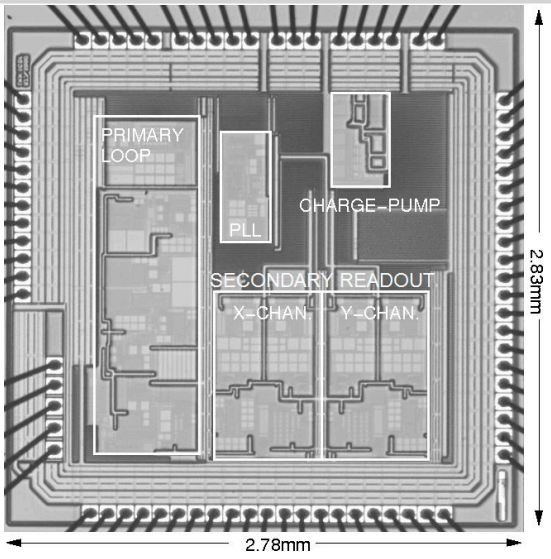

Figure 20.3.6: Die micrograph.

978-1-4244-3457-2/09/$25.00 ©2009 IEEE

Please click on paper title to view Visual Supplement.

Authorized licensed use limited to: Teknillinen Korkeakoulu. Downloaded on January 13, 2010 at 00:17 from IEEE Xplore. Restrictions apply.