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# Pseudo-Continuous-Time Readout Circuit for a 300°/s Capacitive 2-Axis Micro-Gyroscope

Lasse Aaltonen, *Student Member, IEEE*, and Kari A. I. Halonen, *Member, IEEE*

***Abstract*—The interface for a capacitive 2-axis micro-gyroscope is implemented in a 0.35-$\mu$m HVCMOS technology with an active area of 2.5 mm$^2$. Compared to a regular continuous-time interface with large on-chip RC time constants, the reduction of the chip area is made possible by the pseudo-continuous-time readout technique, of which a detailed analysis is presented in this paper. The technique allows a dc biasing voltage to be used for the detection and does not require any large RC time constants to be implemented. For the sensor that was implemented the x- and y axis noise floors are 0.015°/s/$\sqrt{\text{Hz}}$ and 0.041°/s/$\sqrt{\text{Hz}}$. The supply current and voltage for the chip, including the charge pump and the drive and sense interfaces, are 1.8 mA and 2.5–3.6 V, respectively. The supply current of a single sense readout channel is approximately 0.4 mA.**

***Index Terms*—Angular velocity, capacitive, gyroscope, interface electronics, MEMS, pseudo-CT, 2-axis.**

## I. Introduction

ANGULAR velocity sensors are devices which are used to measure the rotation rate of a body with respect to an inertial frame of reference. The MEMS (Micro-Electro-Mechanical Systems) technology offers the possibility of manufacturing medium- to high-accuracy, extremely compact angular velocity sensors [1]. At the same time, being a mass fabrication technology, MEMS allows a reduction in the costs per single unit, provided that the quantities manufactured are sufficient. Because of the continuously evolving and growing MEMS market and the clear benefits of miniaturizing, MEMS sensors are still under active research.

A typical MEMS angular velocity sensor is a vibratory gyroscope, which comprises two resonators. One is forced to oscillate, while the other, functioning as an accelerometer, senses the orthogonal movement of the oscillating resonator. The angular rate gives rise to Coriolis acceleration, which couples the vibration from the driven (primary) resonator to the sense (secondary) resonator. The resulting signal, which is directly proportional to the angular velocity, is amplitude modulated at the resonance frequency $\omega_c$. The driven resonator motion also couples to the sense resonator because of mechanical imperfections. This parasitic signal component is 90° phase shifted compared to the Coriolis signal, and is therefore commonly referred to as a quadrature signal.

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The authors are with the SMARAD-2/Electronic Circuit Design Laboratory, Helsinki University of Technology, FI-02015 TKK, Finland (e-mail: lasse.aaltonen@ecdl.tkk.fi; kari.halonen@ecdl.tkk.fi).

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The techniques related to the capacitive detection of motion in MEMS gyroscopes can be divided into two main groups of interfaces, discrete-time (DT) and continuous-time (CT). The former category mostly involves switched-capacitor (SC) circuits, the majority of which are electromechanical delta-sigma ($\Delta\Sigma$) closed-loop gyroscopes [2]–[6]. The success of $\Delta\Sigma$ interfaces is mostly due to the inherent digital output and electrostatic feedback force, which is a linear function of the pulse density. CT interfaces are commonly used for the open-loop detection of angular velocity [7]–[10]. In these cases a dc biasing voltage, referring to the voltage across the sensor capacitors, can be used to convert the capacitive, amplitude-modulated angular velocity signal into current and further to voltage. Another alternative is to detect the signal using an ac carrier so that the signal becomes amplitude-modulated twice [11]–[13]. This method allows the signal to be detected at a frequency band where the flicker noise of the readout electronics is attenuated below the white noise floor, and the implementation of large, area-consuming *RC* time constants can be avoided. However, the rms ac detection voltage that is attained is lower compared to the dc detection voltage, and the additional amplitude demodulation complicates the design. CT front-ends with dc and ac detection voltages are depicted in Fig. 1(a) and (b), and a simple SC front-end in Fig. 1(c). The front-ends (a) and (b) can be considered charge-sensitive amplifiers, as the feedback is capacitive at the signal frequency. Assuming that $\Delta C$ in Fig. 1 is the signal, modulated at the resonance frequency, and the feedback impedances $Z_{FB}$ provide a dc feedback, $V_{out}$ in Fig. 1(a) is generated by $\Delta C$ only. Unlike in (a), in (b) and (c) the ac detection voltage causes $V_{out}$ also to depend on any existing static mismatch between the sensor capacitors or the feedback impedances, which can be significant compared to $\Delta C$. The circuits (b) and (c) must also tolerate a high common-mode (CM) signal current as a result of the static common-mode capacitances $C_c$ [2].

The pseudo-CT readout technique [14], which is analyzed in detail in this paper, allows the signal readout to be simplified and the chip area, i.e., the costs, to be reduced. The technique falls between the two categories, DT and CT. The continuous signal current resulting from the element is integrated for half a primary resonance period in order to resolve the signal amplitude. The readout handles the signal as continuous during the integration and samples it at the very end of the integration period, hence allowing inherent amplitude detection and noise bandwidth limiting before the sampling. The operation can be compared with the integrate-and-dump technique and boxcar integrator, which are, for example, applied in [15] for downconversion in a radio receiver and in [6] for the realization of the sensor front-end for the closed-loop $\Delta\Sigma$ interface.

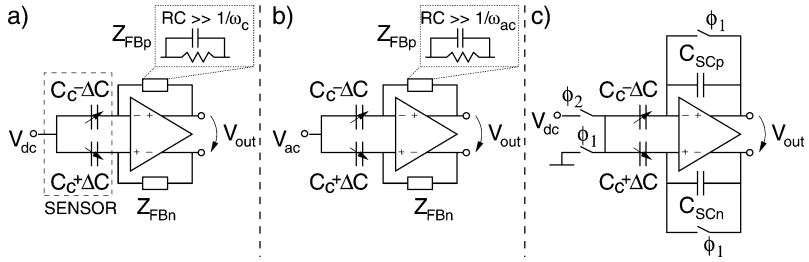


Fig. 1. CT transimpedance front-ends using dc detection voltage in (a) and ac detection voltage, $V_{\rm ac}$ at $\omega_{\rm ac}$, in (b), and an SC front-end in (c). The resonance frequency $\omega_c$ is much smaller than the frequency of the ac detection voltage $\omega_{\rm ac}$.

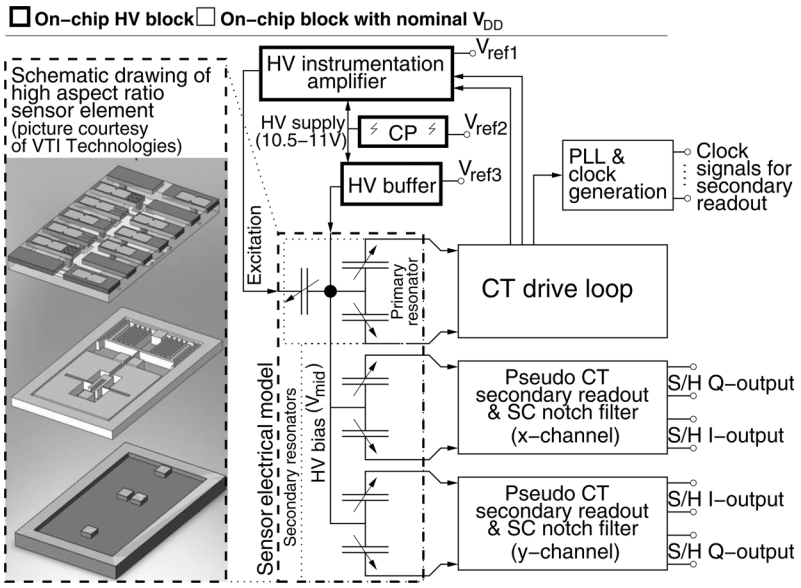


Fig. 2. The block diagram of the interface and a schematic drawing of the sensor element.

The paper is organized as follows. Section II introduces the structure of the interface electronics. In Section III the readout technique is presented in detail, together with the noise and linearity analysis. Comprehensive measurement results are given in Section IV. Section V concludes the paper.

## II. Structure of the Interface

The structure of the interface for a capacitive gyroscope is shown in Fig. 2, together with a schematic drawing of the sensor element. The element has an in-plane drive mode with comb excitation and detection and two out-of-plane torsional sense modes with parallel plate detection. This configuration can be modeled using two pairs of capacitors for the secondary detection and one pair for the primary. In addition, the excitation can be modeled as a single variable capacitor. The potential of the structural wafer is common for each capacitor and the high-voltage (HV) bias of this node, defined by the external low-voltage reference $V_{\rm ref3}$, is denoted by $V_{\rm mid}$.

The difference between the voltage $V_{\rm mid}$ and the dc levels set by the detection and actuation circuits defines both the dc detection voltage and the force of the electrostatic excitation. The voltage $V_{\rm mid}$, 10.35 V, is high in order to maximize the detected charge and the excitation force. The voltage is limited on the one hand by the negative spring created by the dc bias across the sensor capacitors and on the other hand by the poor efficiency of the on-chip HV generation [16]. In addition to the bias-generating amplifier (HV buffer), the charge pump (CP) also provides the supply for the HV instrumentation amplifier, which creates the excitation signal. The CM level of the excitation signal, 3.25 V, allows a sufficient excitation force.

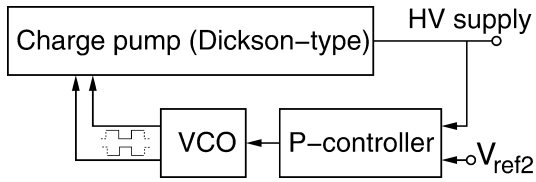


Fig. 3. The block diagram of the on-chip charge pump.

The HV supply is generated by the on-chip CP shown in Fig. 3, which operates in a closed-loop in order to reduce the variation of the CP output voltage over process and temperature. The regulation of the CP clock frequency by using a continuous-time proportional controller allows the CP output to be filtered efficiently, as the amount of filtering capacitance at the pump output is only limited by the available chip area. This is due to the fact that the stability of the closed-loop CP increases with a reduction in the speed of the open-loop CP. The regulation method ensures that the lowest ripple frequency is equal to the frequency of the voltage-controlled oscillator (VCO) and that

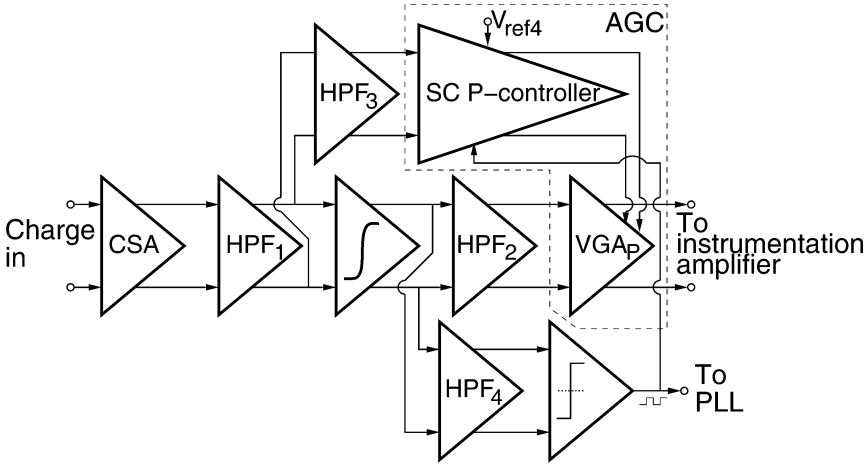


Fig. 4. The block diagram of the drive channel readout and automatic gain control.

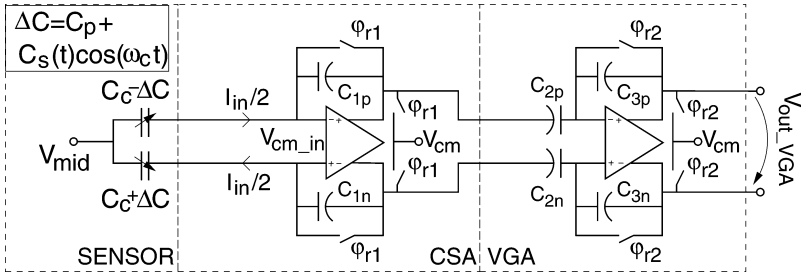


Fig. 5. The block diagram of the pseudo-CT readout electronics.

the duty cycle at the VCO output stays at 50%. The HV supply voltage, approximately $8\mathrm{V}_{\mathrm{ref2}}$, is determined by the low-voltage reference $\mathrm{V}_{\mathrm{ref2}}$. The HV circuits are discussed in detail in [17].

Unlike the secondary readout, the drive loop in Fig. 4 is designed to be CT [14]. The high-pass filters (HPF) provide low-noise gain and prevent the readout from saturating as a result of accumulating offsets. The integrator implements the 90° phase shift, which is required in order to make the loop oscillate and to maximize the positive loop gain. The integrator also limits the noise bandwidth and thus only a passive $\mathrm{HPF}_4$ is required to remove the low-frequency noise before the drive channel signal is fed to the comparator, which generates the sampling clock for the amplitude controller. Now that the input to the SC proportional controller (P-controller) is taken before the integrator, the 90° phase difference between the input signal and the clock allows the amplitude to be sampled. The controller compares the reference $\mathrm{V}_{\mathrm{ref4}}$ with the input amplitude and outputs the amplified difference. The output is connected to define the gain of the variable gain amplifier (VGA) in order to minimize the difference between $\mathrm{V}_{\mathrm{ref4}}$ and the input amplitude, i.e., to stabilize the amplitude of the drive resonator vibration. The $\mathrm{VGA}_P$ output is converted into single-ended in the HV instrumentation amplifier, which makes a HV ac excitation signal and maximized excitation force possible during start-up.

The clock generated by the comparator is also utilized as a reference for the PLL [18]. The clock signals generated by the PLL and the clock generator are further used for the open-loop sense readout channels, which comprise the pseudo-CT readout stage and the notch filter. The pseudo-CT stage converts the capacitive signal into voltage, which is sampled by the notch filter. The filter upconverts the additive flicker noise of the readout and removes it. The filter also produces the final analog outputs, the angular velocity (I-output) and the quadrature signal (Q-output). In the following sections a detailed analysis of the pseudo-CT secondary readout is presented.

## III. Pseudo-Continuous-Time Readout

The pseudo-CT front-end circuitry, which utilizes dc detection voltage, is shown in Fig. 5. The charge-sensitive amplifier (CSA) converts the signal current into voltage, while the VGA with a 2-bit gain control allows the signal to be further amplified to the final, desired level. The input to the front-end is low-impedance, either true ground during reset $(\phi_{r1})$ or virtual ground during charge transfer. The input also presents a low-impedance for CM signals, $\mathrm{V}_{\mathrm{cm\_in}}$, because the common-mode feedback (CMFB) input is taken from the amplifier input in order to keep the detection voltage constant. Hence, the continuous input current $I_{in}$ can be written as

$$I_{in} = 2\omega_c C_s(t) \sin(\omega_c t) V_{\mathrm{det}} \tag{1}$$

where $\omega_c$ is the primary resonance frequency, $C_s(t)$ the single-ended signal capacitance modulated at $\omega_c$, and $\mathrm{V}_{\mathrm{det}}$ the detection voltage $\mathrm{V}_{\mathrm{mid}} - \mathrm{V}_{\mathrm{cm\_in}}$. The CSA starts to integrate this signal current when the reset period ends. As an example, a fixed-rate sense signal with zero quadrature, together with the clock signals, is depicted in Fig. 6. The CSA reset $\phi_{r1}$ ends

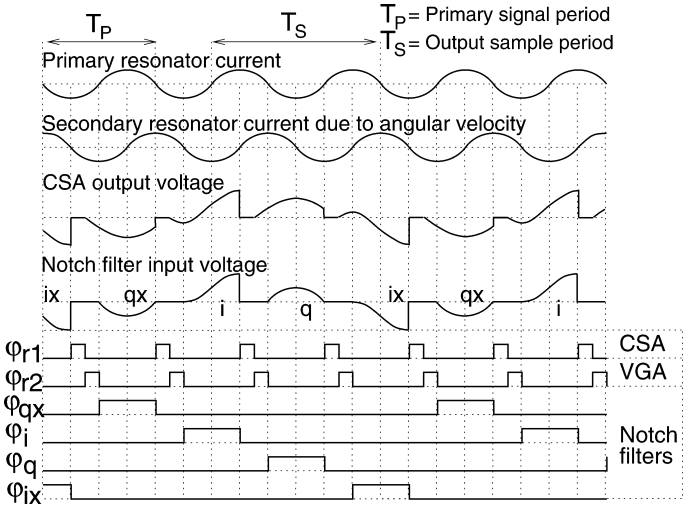


Fig. 6. The sampling clocks together with the reset signals.

when the VGA reset $\phi_{r2}$ begins. In this way the noise sampled to the CSA feedback capacitors $C_1$ is also stored to the capacitors $C_2$. Hence, when $\phi_{r2}$ turns low and the current flow through $C_2$ is directed into $C_3$, the sampled noise does not affect the voltage at the VGA output. The time when the $\phi_{r2}$ ends always occurs at one of the two zero crossing points of the input Coriolis signal current, when the angular velocity is detected. During the integration the output signal of the VGA is also fed to the sampling capacitors of the SC notch filter, which is shown in Fig. 7. The filter samples the VGA output after the integration period of $T_P/2$. The sampling capacitors ($C_{1-4}$) are preceded by the resistors $R_{\rm BW}$, which limit the noise bandwidth before the sampling.

As the integration periods occur with a delay of $T_P/4$ (see Fig. 6) and the time for integration is equal to $T_P/2$, the VGA output is sampled at a rate of $4/(3T_P)$. Successive samples correspond to the quadrature and angular velocity peak-to-peak amplitudes, which are sampled by the two notch filters shown in Fig. 7. Hence, the sample frequency at the output of each notch filter is $1/T_S = 2/(3T_P)$, half the rate at which the VGA is sampled. The complete interface includes two identical sense readout channels (see Fig. 2), and a total of four identical notch filters are utilized to output two angular velocity outputs and two quadrature outputs.

The notch filters sample the VGA output at the falling edge of the sampling clocks, $\phi_i$, $\phi_{ix}$, $\phi_q$ and $\phi_{qx}$ in Fig. 6. As the VGA output is sampled at a rate of $4/(T_P3)$, every other one of the angular velocity samples and quadrature samples is inverted. The necessary downconversion is performed by the notch filters. For example, the angular velocity signal is sampled at $\phi_i$ and $\phi_{ix}$, and the corresponding samples are transferred to angular velocity output with positive and negative gain, repectively. As a result of demodulation the flicker noise and offset at the input of the filters will be upconverted. The filters calculate a moving average of two successive samples, which results in a transfer function from the demodulated notch filter input to the filter output

$$H_{\rm notch}(z) = 0.625(1 + z^{-1}). \quad (2)$$

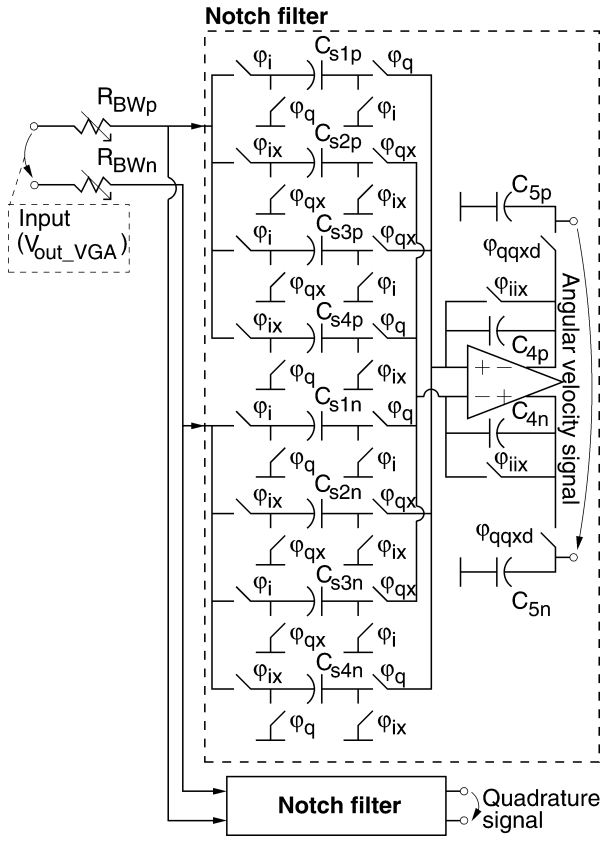


Fig. 7. The schematic of the notch filter.

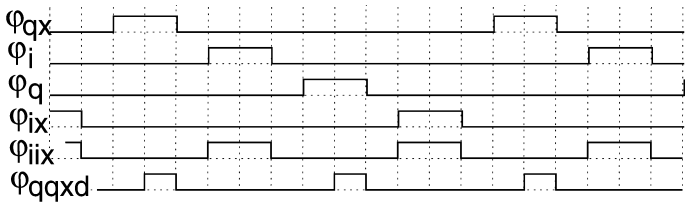


Fig. 8. The clock signals for the notch filter.

The notch at half the sample frequency removes the upconverted noise.

All the clock signals for the notch filter are shown in Fig. 8. At the end of phase $\phi_i$ the input voltage is sampled to the capacitors $C_{s1}$ and $C_{s3}$ and the feedback capacitors $C_4$ are reset. At the beginning of the next clock cycle $\phi_q$ the charge, from $C_{s1}$, and, with different polarity, from $C_{s4}$, stored in the previous phase $\phi_{ix}$, is moved to the feedback capacitors. During $\phi_q$ the charge in $C_{s3}$ and $C_{s2}$ remains unchanged. Now, any dc at the filter input is canceled with an accuracy defined by matching, when charges with reverse polarities are summed at the feedback capacitors. In order to be able to use the output as CT, the values at the hold capacitors $C_5$ are updated with a delay, so that the settling of the amplifier is not visible at the output. The operating cycle remains similar each time a new output sample is generated. All the sampling capacitors have the same nominal capacitance value and the gain of the filter is 1.25 at the input signal frequency. The second notch filter in Fig. 7 extracts the quadrature signal. It samples the input at $\phi_q$ and $\phi_{qx}$.

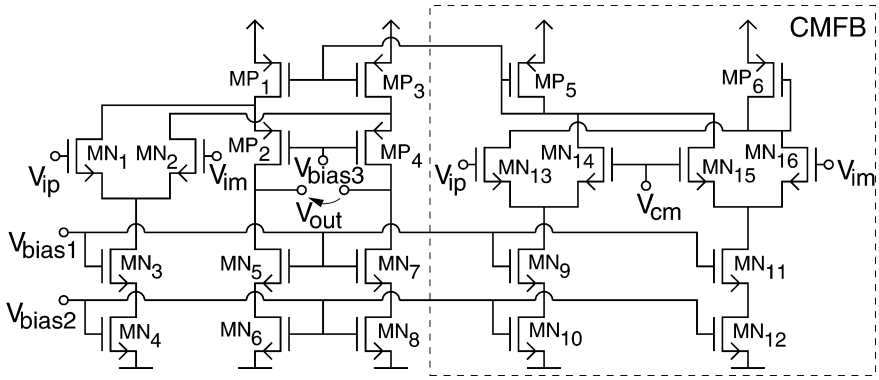


Fig. 9. The schematic of the operational amplifier in the CSA.

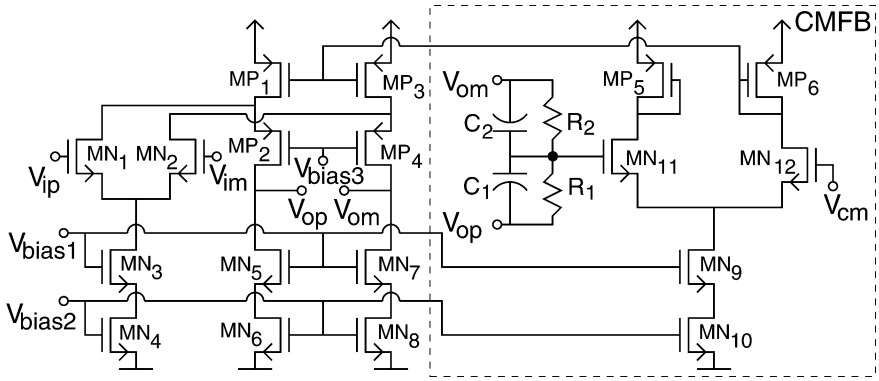


Fig. 10. The schematic of the operational amplifier in the VGA.

When the operation of a single sense channel, which now requires two gain stages and an active filter, is being considered, the electronics could be simplified even further. In the simplest case, a single gain stage together with a passive SC filter stage would be sufficient for the detection of the angular velocity. However, in this case the amplifier would have to reach the full output signal range, also including the potential CM signal resulting from input leakage currents.

### A. Implementation

The operational amplifier (opamp) for the CSA is shown in Fig. 9. The topology of the differential amplifier is a basic folded cascode. As the continuous time input to the CSA is a signal current modulated at $\omega_c$, which is typically below 30 kHz, the requirement for the slew rate is likely to be low. Now a significant saving in the supply current is made possible by reducing the current of the folded stage, i.e., the transistors $MN_6$ and $MN_8$. Additionally, this allows increased gain, improved stability, and less noise, especially from the current sources $MN_6$ and $MN_8$, as a result of their reduced transconductance.

The transconductance of the input pair is typically fairly high in order to reduce the thermal noise, which results in a wide gain-bandwidth product (GBW). During the reset phase, the feedback switch forms a low-pass filter in the feedback path, together with any capacitance connected to the input. In order to increase the corner frequency of this parasitic filter in such a way that it does not impair the stability of the reset amplifier, a very small on-resistance of the switch is required. This requirement is not compatible with the requirement for a small leakage current. Hence, the reset is performed by also shorting the outputs of the amplifier, as shown in Fig. 5, whereas the feedback switch is implemented using a transistor with a minimum channel width.

The opamp for the VGA in Fig. 10 is also a folded cascode amplifier. Compared with the CSA, the noise requirement of this stage is considerably relieved and the transconductance is determined by linearity rather than the noise. Still, as the capacitive load inflicted by the SC filter is moderately large, the CSA current, 300 $\mu$A, is nominally only 7.5 times the current of the VGA, 40 $\mu$A. The opamp of the SC filter is a Miller-compensated amplifier with a rail-to-rail output and a supply current smaller than 10 $\mu$A.

The requirements imposed on the CMFB circuits of the amplifiers are different. The CMFB of the CSA is connected to the input and the CM level is set through the feedback components. With this configuration the differential amplitude at the CMFB input remains minimal and the CMFB topology shown in Fig. 9 can be used to extract the CM level. The VGA, on the other hand, has a high differential output amplitude, which must not saturate the CMFB. Hence, the CM level is extracted from the output using a passive *RC* network, as shown in Fig. 10. It should also be noted that the CSA output CM level changes according to $I_{\mathrm{leak}}/C_1$, where $I_{\mathrm{leak}}$ is the magnitude of the CM leakage current at the CSA input and $C_1$ the CSA feedback capacitor. The resulting output CM variation must also be tolerated at the VGA input. The readout was designed to tolerate $I_{\mathrm{leak}}$ up to 1 nA.

### B. Linearity

When the interface electronics are being considered, the linearity of the pseudo-CT readout can be evaluated at $\omega_c$ by dc

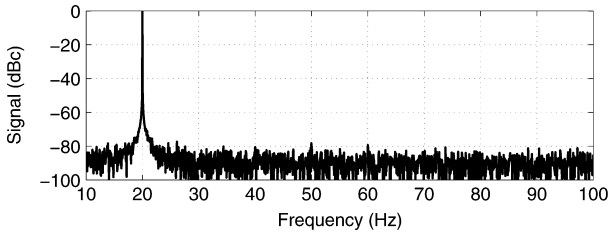


Fig. 11. The measured linearity of one of the sense readout channels with an external AM modulated signal.

biasing the CSA and the VGA properly. The linearity is comparable with a regular CT readout (see Fig. 1(a)) with dc detection voltage, and with linear resistors for any potentially required dc feedback.

The readout electronics that was implemented was measured using an external AM input signal, with a 20-Hz modulation frequency and a 6-kHz carrier, 2.5-V supply, proper clock signals from the PLL, and external discrete capacitors to replace the sensor element. The input signal level was set to be roughly equal to the maximum full-scale angular velocity input. The spectrum of the continuous sense readout output is shown in Fig. 11 with the second and the third harmonic components roughly 80 dB below the signal.

### C. Noise Performance of the Readout

In order for the noise performance of the gyroscope to be evaluated, the transfer function of the noise from the CSA output to the notch filter output is derived in this section. Further, in the next section the dominant sources of noise are referred to the output of the CSA. For the following analysis it is expected that the additional noise inflicted by the VGA and the SC filter, which samples the CSA output, will be negligible because of the high gain of the CSA.

The simplified configuration of the VGA and the noise bandwidth-limiting stage is shown in Fig. 12. If the $R_{bw\_lim}$ is assumed to be zero, the voltage after the integration can be written as

$$V_{n\_out}(I_{n\_in}) = -\frac{1}{C_3}\int_0^{T_P/2} I_{n\_in}(t)dt \tag{3}$$

where $T_P$ is the primary (drive, carrier) signal period and the rest of the parameters, together with $C_2$, are shown in Fig. 12. If the noise spectral components $V_{n\_in}$ are represented as discrete sine components with amplitude $\sqrt{2}V_{ndens}$, frequency $\omega_n$, and random phase $\phi_n$, the definite integral for the VGA output can be written as

$$\begin{aligned} &V_{n\_out}(\omega_n,\phi_n) \\ &\quad= -\frac{C_2}{C_3}\int_0^{T_P/2}\frac{d[\sqrt{2}V_{ndens}\sin(\omega_n t+\phi_n)]}{dt}dt \\ &\quad= \frac{C_2}{C_3}\sqrt{2}V_{ndens}[\sin(\phi_n)-\sin(\omega_n T_P/2+\phi_n)]. \end{aligned} \tag{4}$$

The equation is valid for both the circuit topologies in Fig. 12. When the rms value of all equally probable phase values $\phi_n$ is calculated, the output noise density, $V_{n\_out}$, can be written at the input of the sampler as

$$V_{n\_out}(\omega_n) = \frac{C_2}{C_3}\sqrt{2}V_{ndens}\sqrt{1-\cos\left(\frac{\omega_n T_P}{2}\right)} \tag{5}$$

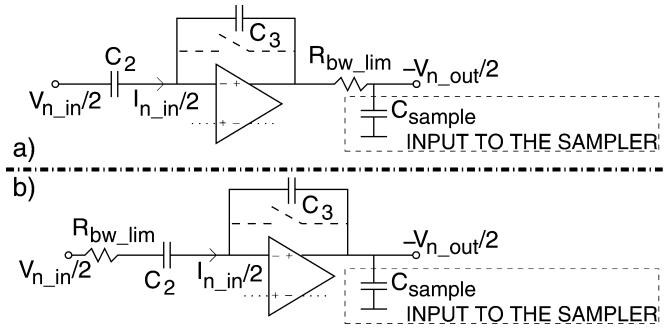


Fig. 12. The configuration during the integration phase for calculating the noise transfer function. The simplified circuit includes the VGA, the noise bandwidth-limiting resistor, and the sampling capacitor. Topology (a) corresponds to the circuit that was implemented, whereas (b) realizes the noise bandwidth reduction more efficiently. $V_{n\_in}$ corresponds to the CSA output. Half of the differential circuits are shown.

where the noise density $V_{ndens}$ is considered white. When the noise bandwidth reduction is taken into account and $R_{bw\_lim}$ is assigned a non-zero value, a new expression must be formed for $V_{n\_out}$. In order to prevent the input noise from folding, the noise bandwidth should be limited both at the beginning and at the end of the integration. The circuit in Fig. 12(a), which corresponds to the circuit that was implemented, enables the noise bandwidth to be reduced at the end of the integration period, but fails to do so at the beginning of the integration. This is because the current flowing through the reset switch is directed through $C_3$ when the reset period ends. As the noise bandwidth is not limited, the current flowing through the reset switch is sampled, and hence the noise is folded when the integration begins. In order to solve the problem, the noise bandwidth of the input current $I_{n\_in}$, should be limited. This can be done, for example, by simply moving $R_{bw\_lim}$ to the input of the VGA, as shown in Fig. 12(b).

The noise density before sampling can be rewritten for Fig. 12(b) with non-zero $R_{bw\_lim}$ using (3) and

$$I_{n\_in}(t) = \frac{d\left(C_2\sqrt{\frac{2}{(\omega_n/\omega_p)^2+1}}V_{ndens}\sin(\omega_n t+\phi_n)\right)}{dt} \tag{6}$$

where $\omega_p$ corresponds to the pole caused by the $R_{bw\_lim}$ and $C_2$ in Fig. 12(b). Hence, (5) for Fig. 12(b) with non-zero $R_{bw\_lim}$ can be written as

$$V_{n\_out}(\omega_n) = \sqrt{\frac{2}{(\omega_n/\omega_p)^2+1}}\frac{C_2}{C_3}V_{ndens}\sqrt{1-\cos\left(\frac{\omega_n T_P}{2}\right)}. \tag{7}$$

The integral of (7) for white noise over the frequency band ranging from 0 to infinity results in rms output noise. As the sampling frequency is equal to $2f_c/3$, the rms noise can be written back to noise density as

$$\begin{aligned} V_{n\_out\_\text{sampled}} &= V_{n\_out\_rms}\Big/\sqrt{\frac{f_c}{3}} \\ &\approx \frac{C_2}{C_3}V_{ndens}\sqrt{\frac{\omega_p}{2}\frac{3}{f_c}} \end{aligned} \tag{8}$$

where $f_c = \omega_c/(2\pi) = 1/T_P$ is the carrier frequency.

An example simulation is run with the parameters $V_{ndens} = 13\ \mu\text{V}/\sqrt{\text{Hz}}$, $f_c = 6$ kHz, $C_2 = C_3 = 1pF$, and with mul-

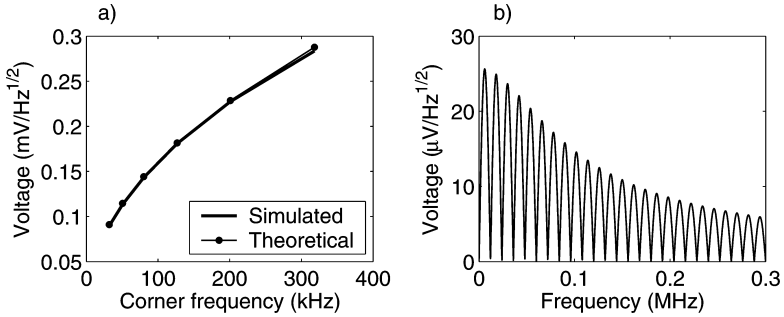


Fig. 13. In (a), the simulated output noise density of the circuit in Fig. 12(b) with white input noise voltage density and a theoretical value obtained using (8). In (b), (7) is plotted using values that correspond to figure (a) at a corner frequency of 100 kHz.

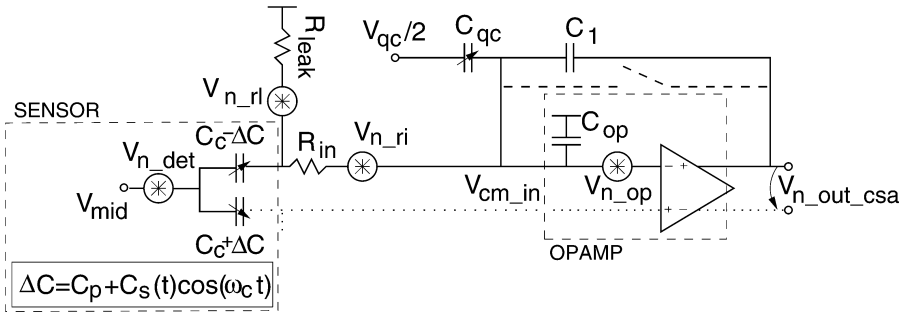


Fig. 14. The CSA during charge integration for noise modeling. Half of the differential CSA is shown.

tiple values of $\omega_p$. The results are compared to (8) and shown in Fig. 13. The noise spectral density before sampling (7), which corresponds to one of the noise density values after sampling, is plotted in the same figure.

If $V_{n\_in}$ is flicker noise, $V_{ndens}$ in (7) should be replaced by $V_{ndens\_f}/\sqrt{\omega_n}$, where $V_{ndens\_f}$ represents the value of the flicker noise at $\omega_n = 1$. In a similar way any arbitrary frequency dependency of $V_{n\_in}(\omega_n)$ can be taken into account. In these cases the rms output noise can be calculated by numerically integrating (7).

The output signal value can be expressed as

$$V_{out\_s} = 4C_s V_{\rm det}\frac{C_2}{C_1 C_3} \tag{9}$$

which has been calculated using (3) for $I_{n\_in}(t) = 2C_2C_sV_{\rm det}/C_1 d[\cos(\omega_c t + \phi_{\rm err})]/{\rm dt}$, and zero phase error $\phi_{\rm err}$. The carrier frequency $\omega_c$ is equal to $2\pi/T_P$; $V_{\rm det}$ is the dc detection voltage, $C_s$ the single-ended signal capacitance, and $C_1$ the CSA feedback capacitance (see Fig. 14). It is also assumed that the signal capacitance $C_s$ is constant during a single integration period. By using (9) and (8), and by setting $V_{out\_s}$ equal to $V_{n\_out\_\rm sampled}$, $C_s$ can be solved for the equivalent noise capacitance density

$$C_n = \frac{C_1}{V_{\rm det}}\sqrt{\frac{\omega_p}{32}\frac{3}{f_c}}V_{ndens} \tag{10}$$

where $V_{ndens}$ corresponds to the white spectral noise density at the CSA output. The ratio $\omega_p/f_c$ is limited by $\phi_{\rm err}$, which increases if $\omega_p$ is placed at a lower frequency. The phase error determines not only the signal gain, but also the magnitude of the leakage of the quadrature signal to the angular velocity output.

The jitter of the VGA reset and sampling clock will also introduce noise to the output. The magnitude of the noise inflicted by the jitter is directly proportional to the signal derivative at the sampling instant. The rms output noise can be approximated as

$$V_{n\_out\_rms} = \sqrt{2}\omega_c V_{\rm aiq}\frac{C_2}{C_3}|\phi_{\rm err}|T_J \tag{11}$$

where $V_{\rm aiq}$ is the VGA input amplitude, which also includes any quadrature signal that potentially exists. When the phase error $\phi_{\rm err}$ is zeroed, the derivative of the output signal at the sampling instant becomes zero and the rms cycle jitter $T_J$ has a minimal effect on the output noise. With a small non-zero phase error, or if a quadrature signal exists, the sensitivity to jitter increases, and can be approximated using the equation. The equation assumes that the correlation between the jitter at the beginning and at the end of the integration is zero.

### D. Effective Noise Sources

The configuration when the reset is inactive, during which time the CSA noise and other sources of noise should be considered, is shown in Fig. 14. The noise of the reset phase does not affect the system output as the VGA begins the integration later than the CSA. The noise, sampled after the CSA reset phase ends, forms a mere dc voltage at the VGA input, which does not affect the integration result. The node $V_{n\_out\_\rm csa}$ corresponds to the input noise voltage density of the VGA $V_{n\_in}$. The simplified noise transfer functions of each source of noise to the CSA output are shown in Table I. The conditions under which the simplifications are made are also listed in the table.

One of the contributors of noise to $V_{n\_in}$ is the noise of the opamp of the CSA $V_{n\_op}$, which is amplified to the output with high gain. Details about the noise optimization of the CSA can be found in, for example, [19].

The detection voltage $\rm V_{det}$ is defined as a dc voltage $V_{\rm mid} - V_{cm\_in}$ and hence noise in the detection voltage $V_{n\_\rm det}$ can orig-

TABLE I
THE APPROXIMATE NOISE TRANSFER FUNCTIONS TO CSA OUTPUT DURING THE INTEGRATION PHASE

| | |
|---|---|
| $\frac{V_{n\_out\_csa}}{V_{n\_rl}}(\omega_n)$ | $\frac{1}{\omega_n C_1 R_{leak}}$ |
| $\frac{V_{n\_out\_csa}}{V_{n\_ri}}$ | $\frac{C_c}{C_1}$ |
| $\frac{V_{n\_out\_csa}}{V_{n\_det}}(t)$ | $\frac{2[C_p+C_s(t)\cos(\omega_c t)]}{C_1}$ |
| $\frac{V_{n\_out\_csa}}{V_{qc}}$ | $\frac{C_{qc}}{C_1}$ |
| $\frac{V_{n\_out\_csa}}{V_{n\_op}}$ | $\frac{C_{qc}+C_{op}+C_1+C_c}{C_1}$ |

Conditions for the equations to be valid for (7):

- $V_{n\_out\_csa} = V_{ndens}$
- $\frac{1}{(C_c+\Delta C)R_{in}} \gg \omega_p$, $R_{leak} \gg R_{in}$
- Sources $V_{n\_rl}$, $V_{n\_ri}$ and $V_{n\_op}$ contain the noise of both symmetric components in the differential circuit (only half shown in Fig. 14)
- The loop (CSA) gain-bandwidth product $\gg \omega_p$

inate either from the bias $V_{\rm mid}$ or the input CM voltage $V_{cm\_in}$. As shown in Fig. 13(b), the noise near dc does not affect the output. Hence, the difference in the constant parts of the sensor capacitors, $C_p$, does not increase sensitivity to the very low-frequency noise of the detection voltage. However, the signal capacitance $C_s$ can upconvert the low-frequency noise or any drift in the dc detection voltage and sets the limit for the maximum permitted low-frequency noise voltage. The required SNR of the detection voltage around dc is comparable to the required SNR of the output voltage and hence this noise specification is fairly easy to meet. On the other hand, the mismatch between the parasitics, $C_p$, can be substantial compared to the signal capacitance and sets more stringent requirements for the noise of the detection voltage at and above the carrier frequency $\omega_c$.

The input resistor $R_{in}$, which exists because of, for example, ESD protection or wiring, introduces an additional source of noise. If the amplifier is considered to have a MOSFET input pair with $V_{n\_op}^2$ of 16 kT/$(3g_m)$ and the resistor noise $V_{r\_in}^2$ is 8 kTR$_{in}$, both the noise sources can be approximated to contribute an equal amount of noise to the output when

$$g_m = \frac{2}{3R_{in}}\left(\frac{C_1 + C_c + C_{\rm qc} + C_{op}}{C_c}\right)^2 \qquad (12)$$

where $g_m$ is the transconductance of a single input transistor, $T$ the absolute temperature, and $k$ the Boltzmann constant.

The leakage currents, described by the resistor $R_{\rm leak}$, also contribute to the output noise when the resistance value is small enough ($\sim$10 G$\Omega$). It can also be noted that, as the noise density at the CSA output is inversely proportional to the frequency (see Table I), the effect of noise bandwidth limiting can be ignored when the noise resulting from leakage is considered.

As the quadrature compensation is performed using a sample of the primary signal to cancel the quadrature signal current [14], the compensation forms an additional noise source that is represented in Fig. 14 by the compensation voltage $V_{\rm qc}$. Now $C_{\rm qc}$ is used to define the correct magnitude of the compensation current. Clearly, the worst-case noise requirement of $V_{\rm qc}$ corresponds to the maximum capacitance.

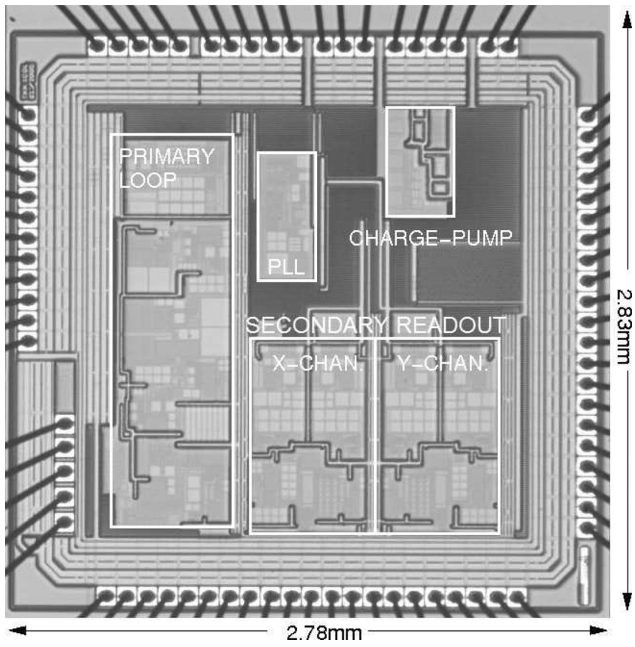


Fig. 15. A microphotograph of the chip; the encircled areas indicate the active on-chip circuitry.

## IV. MEASURED RESULTS

The interface prototype is fabricated in a 0.35-$\mu$m HVCMOS technology and requires no external components, excluding the references. The area of the chip (see Fig. 15) is 7.9 mm$^2$, with an active area of 2.5 mm$^2$. The separately packaged chip and micro-gyroscope are combined on a printed circuit board.

The measured dc linearities at temperatures ranging from $-10$ to 90°C for the x-channel and y-channel are shown in Figs. 16 and 17, respectively. As the residual error indicates, the non-linearity in the x-channel is below 0.1% of the full-scale signal at all temperatures. In addition, the overall gain variation is about one percent. The relatively high offset variation,

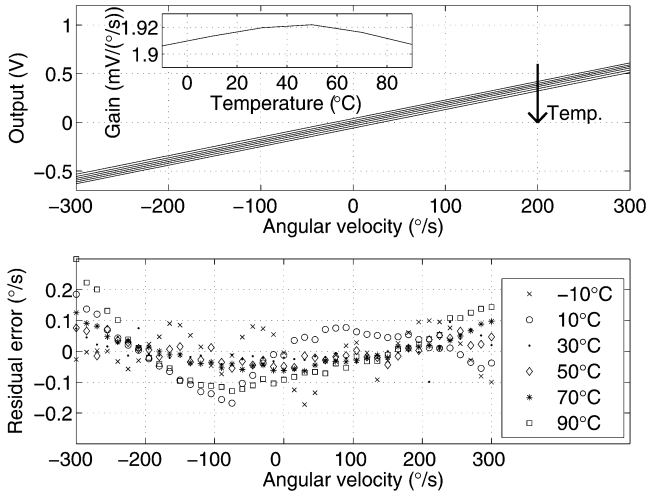


Fig. 16. The dc linearity of the x-channel and the residual error after the fitting of a first-order polynomial. The inset figure shows the gain variation over the temperature range.

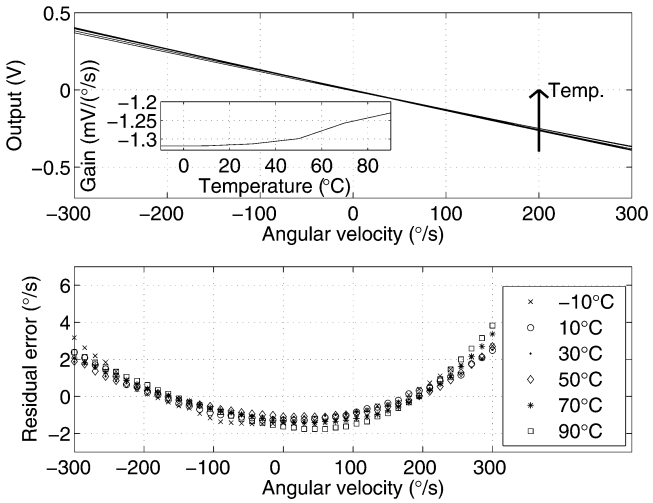


Fig. 17. The dc linearity of the y-channel and the residual error after the fitting of a first-order polynomial. The inset figure shows the gain variation over the temperature range.

0.5°/s/°C, is mostly due to the excitation signal that cross-couples to the secondary readout (see Fig. 2). This cross-coupling results in an additional in-phase component that cannot be rejected [20]. The phase error $\phi_{\rm err}$ was calculated to vary between 1° and 3°, using the in-phase information in Fig. 16 and the corresponding leakage to quadrature shown in Fig. 18.

The y-channel zero-rate offset (ZRO) stability is about 0.06°/s/°C, while $|\phi_{\rm err}|$ is below 1°. Hence, in this channel the cross-coupling of the drive signal is considerably smaller. The linearity is impaired as a result of the high ZRO, the source of which is most probably the excitation signal, which excites motion in the secondary resonator as a result of mechanical nonidealities (direct excitation) [20]. The non-linearity in the y-channel is below 1.5% of the full-scale signal at all temperatures. Example waveforms from the x- and y-channel readout output are shown in Fig. 19.

The typical noise floors for both channels are shown in Fig. 20. The average noise density in the x-channel between

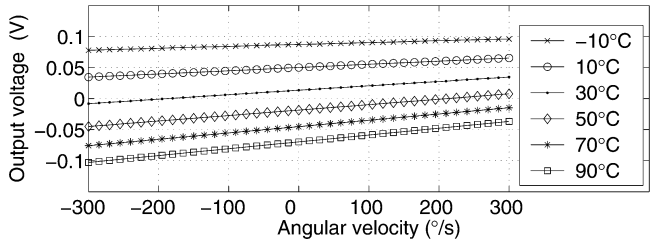


Fig. 18. The quadrature component in the x-channel as a function of angular velocity and temperature.

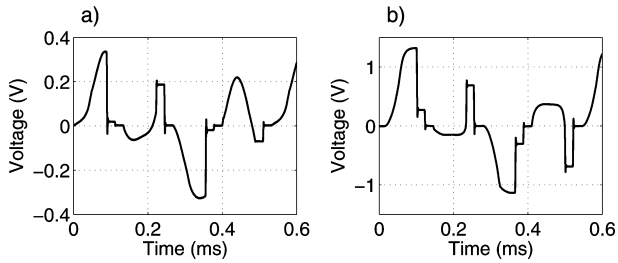


Fig. 19. The zero-rate notch filter input from: (a) the x-channel, and (b) the y-channel.

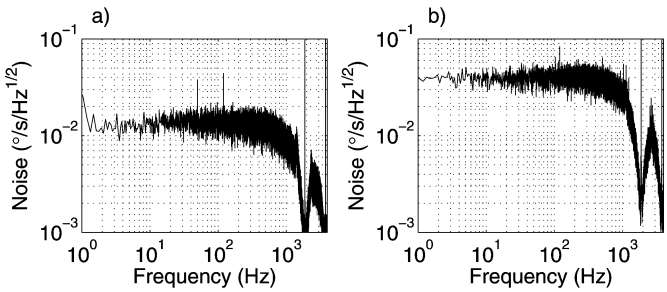


Fig. 20. The noise floor in: (a) the x-channel, and (b) the y-channel with no extra filtering.

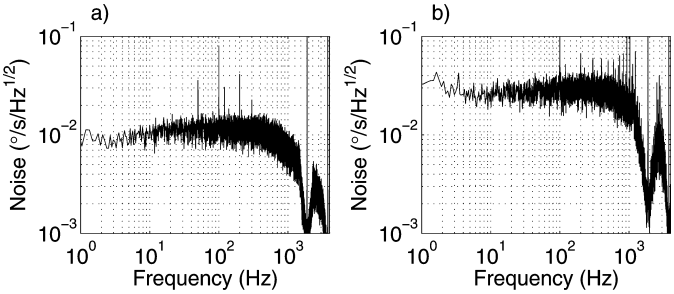


Fig. 21. The noise floor in: (a) the x-channel, and (b) the y-channel with the middle electrode noise filtered above 15 Hz.

0 and 300 Hz is 0.015 °/s/$\sqrt{\rm Hz}$ and that in the y-channel 0.041°/s/$\sqrt{\rm Hz}$. The notch is visible at the Nyquist frequency $f_c/3$ of 1.9 kHz. In order for the dominant noise sources to be determined, first, the middle electrode bias is low-pass filtered. The resulting noise floors are shown in Fig. 21 and the average noise densities between 0 and 300 Hz are $0.012°/s/\sqrt{\rm Hz}$ and $0.031°/s/\sqrt{\rm Hz}$ for x- and y-channel, respectively. With the overall noise lowered, it also becomes more evident that, especially in the x-channel, the noise increases towards higher frequencies. The increase in noise results from the strong

TABLE II
THE SINGLE-ENDED SIGNAL AND NOISE CAPACITANCES OF THE SENSOR

| Channel | $C_s$ $(aF/(^\circ/s))$ | $C_n$, total $(aF/\sqrt{Hz})$ | $C_n$, due $V_{n\_mid}$ $(aF/\sqrt{Hz})$ | $C_n$, due $V_{qc}$ $(aF/\sqrt{Hz})$ | $C_n$, due $V_{n\_rl}$,$V_{n\_ri}$, $V_{n\_op}$ $(aF/\sqrt{Hz})$ |
|---|---|---|---|---|---|
| X | 13 | 0.19 | 0.12 | 0.04 | 0.12 |
| Y | 13 | 0.51 | 0.34 | 0.31 | 0.22 |

Note: The effect of $V_{n\_mid}$ is due to non-zero $C_p$ in Fig. 14

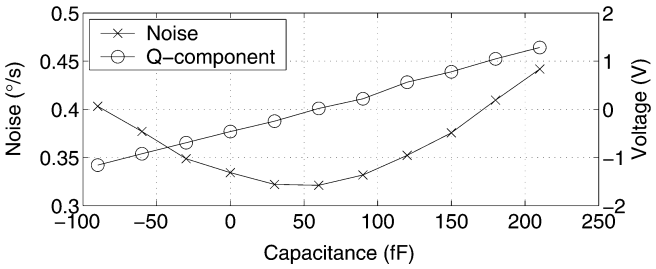


Fig. 22. The in-phase rms noise (bandwidth 500 Hz) and quadrature voltage at the x-channel output as a function of quadrature compensation capacitance.

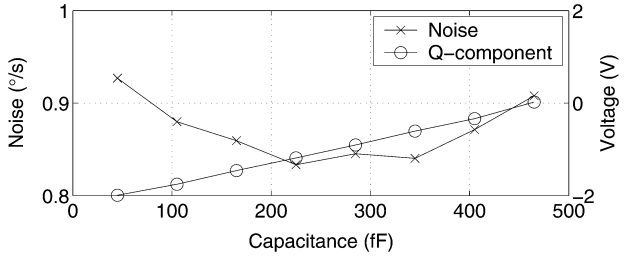


Fig. 23. The in-phase rms noise (bandwidth 500 Hz) and quadrature voltage at the y-channel output as a function of quadrature compensation capacitance.

capacitive coupling of the primary channel excitation signal noise.

Another potentially significant contributor of noise is the quadrature signal, which can cause both jitter-inflicted noise, (11), and additive noise as a result of quadrature compensation, $V_{\rm qc}$ in Fig. 14. The first of the two components should exhibit a noise minimum at the point where the quadrature component is minimized, i.e., at the point where the derivative at the sampling instant is zeroed. On the other hand the latter noise component, which simply couples noise from the drive channel, is zero when the coupling is zero. Now, when the quadrature compensation capacitance $C_{\rm qc}$ (Fig. 14) is swept, the ideal noise minimum coincides with the quadrature zero crossing point, indicating that the noise in the drive channel is negligible. The x-channel noise in Fig. 22 corresponds moderately well to the ideal case and the noise minimum is clearly visible. However, the noise minimum is slightly shifted towards zero capacitance, compared to the capacitance value, which actually minimizes the quadrature signal. In the y-channel, in Fig. 23 the same effect is emphasized.

### A. Summarized Noise Sources of the Gyroscope

The single-ended signal and total noise capacitance densities for the two channels are shown in Table II. The noise density corresponds to the average density between 0 and 300 Hz. The table also shows noise capacitances listed according to the main contributors of noise shown in Fig. 14.

Noise in the dc detection voltage $V_{n\_\rm det}$ generated on-chip, roughly $800\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, is not filtered to avoid external components. $V_{n\_\rm det}$ hence becomes a significant contributor of noise when the static mismatch between the sensor capacitors, $2C_p$, is more than roughly 100 fF. Another significant noise source, the quadrature compensation voltage $V_{\rm qc}$, starts to add noise when large quadrature components need to be compensated. Thus, the effect of noise in $V_{\rm qc}$ is significant only in the y-channel. In this case the SNR of $V_{\rm qc}$, roughly 108 dB at $f_c$ for spectral noise power, is not sufficient. The noise performance was also impaired by the flicker noise of the CSAs, the power of which was about 10 times the expected magnitude, and the leakage. These two noise components increase the total noise both through $V_{n\_op}$ and $V_{n\_rl}$, and through $V_{\rm qc}$. The high level of flicker noise also means that the supply current of the CSAs could be reduced without the increasing thermal noise affecting the total noise. A more unexpected source of noise, the cross-coupled excitation signal with the equivalent $C_n$ of 0.09 in the x-channel, is due to the automatic gain control (AGC) of the drive loop in Fig. 4. The AGC exhibits low noise at low offsets from the carrier, because the response of the drive resonator to amplitude control is strong at low offset frequencies. At higher offsets the signal from the high-Q resonator decreases and the noise inflicted by the P-controller is amplified and also becomes visible in the noise spectrum of Fig. 21(a).

The effect of $V_{n\_\rm det}$ and the noise from $V_{\rm qc}$ and AGC could be removed by filtering the middle-electrode $V_{\rm mid}$ and the amplitude control signal using external capacitors and by using electrostic quadrature nulling [10]. This would, however, add to the costs and complexity of the interface.

The properties of the sensor are summarized in Table III. Compared with the single axis gyroscope in [10], the supply current and active chip area have decreased by roughly a factor of three.

## V. CONCLUSION

An analysis of a pseudo-CT readout technique for a capacitive microgyroscope was presented. The sense readout utilizes a pseudo-CT readout chain including two gain stages and an active SC filter, hence allowing a low-complexity sense readout with an analog output. The pseudo-CT readout enables the dc detection voltage to be used, together with inherent amplitude detection. The supply current and the chip area of a single readout channel are roughly 0.4 mA and 0.5 $\mathrm{mm}^2$, respectively. Most of the current is consumed by the CSA,

TABLE III
SUMMARY OF THE SENSOR PROPERTIES

| | |
|---|---|
| Process technology | 0.35 $\mu m$ HVCMOS |
| Chip area ($mm^2$) | 7.9 (active area 2.5) |
| Supply voltage ($V$)/current ($mA$) | 2.5-3.6/1.8 |
| Detection voltage, dc ($V$) | 9.1 |
| Full-scale signal ($^\circ/s$) | $\pm$300 |
| Signal bandwidth max. ($Hz$) | 300 |
| Spot noise for x/y ($^\circ/s/\sqrt{Hz}$) | 0.015/0.041 |
| Start-up time, to $\pm 6$ $^\circ/s$ of the final ZRO ($s$) | 0.4 |
| Gain at 300 $K$ for x/y ($mV/(^\circ/s)$) | 1.9/1.3 |
| Gain shift from -10 to 90 $^\circ C$ for x/y (%) | 1/7 |
| Max. dc non-linearity for x/y (% of full-scale) | 0.1/1.5 |
| Bias stability for x/y ($^\circ/hr$) | 25/33 |
| ZRO shift from -10 to 90 $^\circ C$ ($^\circ/s$) | 50/6 |

| **Element properties** | Drive | Sense (x) | Sense (y) |
|---|---|---|---|
| Resonance frequency ($kHz$) | 5.8 | 7.9 | 7.5 |
| Full-scale, 300 $^\circ/s$, signal $C_s$ ($fF$) | - | 3.9 | 3.9 |

and the chip area is dominated by the SC filters. In the sensor that was implemented the flicker noise of the front-ends, the noise inflicted by the quadrature signal, and the noise in the dc detection voltage are the most significant sources of noise, and they limit the x and y axis noise floors to 0.015°/s/$\sqrt{\text{Hz}}$ and 0.041°/s/$\sqrt{\text{Hz}}$. Another significant factor in the increasing noise content is the incomplete limiting of the noise bandwidth, which results in excess noise folding. In order to address the problem, an improved circuit with the corresponding theory of noise performance was presented in Section III-C.

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## REFERENCES

[1] N. Yazdi, F. Ayazi, and K. Najafi, "Micromachined inertial sensors," *Proc. IEEE*, vol. 86, no. 8, pp. 1640–1659, Aug. 1998.

[2] X. Jiang, J. I. Seeger, M. Kraft, and B. E. Boser, "A monolithic surface micromachined Z axis gyroscope with digital output," in *Symp. VLSI Circuits Dig. Tech. Papers*, Honolulu, HI, Jun. 2000, pp. 16–19.

[3] V. P. Petkov and B. E. Boser, "A fourth-order $\Sigma\Delta$ interface for micromachined inertial sensors," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1602–1609, Aug. 2005.

[4] U.-M. Gómez *et al.*, "New surface micromachined angular rate sensor for vehicle stabilizing systems in automotive applications," in *Proc. Int. Conf. Solid-State Sensors, Actuators and Microsystems*, Seoul, Korea, Jun. 2005, pp. 184–187.

[5] Y. Dong, M. Kraft, and W. Redman-White, "Micromachined vibratory gyroscopes controlled by a high-order bandpass sigma-delta modulator," *IEEE Sensors J.*, vol. 7, no. 1, pp. 59–69, Jan. 2007.

[6] C. D. Ezekwe and B. E. Boser, "A mode-matching $\Sigma\Delta$ closed-loop vibratory gyroscope readout interface with a 0.004°/s/$\sqrt{\text{Hz}}$ noise floor over a 50 Hz band," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 3039–3048, Dec. 2008.

[7] S. R. Zarabadi, P. E. Castello-Borelly, and J. D. Johnson, "An angular rate sensor interface IC," in *Proc. IEEE Custom Integrated Circuits Conf.*, San Diego, CA, May 1996, pp. 311–314.

[8] J. A. Geen, S. J. Sherman, J. F. Chang, and S. R. Lewis, "Single-chip surface micromachined integrated gyroscope with 50°/h Allan deviation," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1860–1866, Dec. 2002.

[9] A. Sharma, M. F. Zaman, and F. Ayazi, "A 104-dB dynamic range transimpedance-based CMOS ASIC for tuning fork microgyroscopes," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1790–1802, Aug. 2007.

[10] M. Saukoski, L. Aaltonen, T. Salo, and K. Halonen, "Interface and control electronics for a bulk micromachined capacitive gyroscope," *Sens. Actuators A*, vol. 147, no. 1, pp. 183–193, Sep. 2008.

[11] G. E. Boser, "Electronics for micromachined inertial sensors," in *Proc. IEEE Transducers'97*, Chicago, IL, Jun. 1997, pp. 1169–1172.

[12] L. Aaltonen, M. Saukoski, and K. Halonen, "Upconverting capacitance-to-voltage converter for readout of a micromechanical gyroscope," in *Proc. IEEE Norchip Conf.*, Linköping, Sweden, Nov. 2006, pp. 267–270.

[13] C. Zhang, T. Yin, and Q.-S. Wu, "A large dynamic range CMOS readout circuit for MEMS vibratory gyroscope," in *Proc. IEEE SENSORS Conf.*, Lecce, Italy, Oct. 2008, pp. 1123–1126.

[14] L. Aaltonen, T. Speeti, M. Saukoski, and K. Halonen, "An interface for a 300°/s capacitive 2 axis micro-gyroscope with pseudo-CT readout," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, Feb. 2009, pp. 344–345.
[15] S. Karvonen, T. A. D. Riley, and J. Kostamovaara, "A CMOS quadrature charge-domain sampling circuit with 66-dB SFDR up to 100 MHz," *IEEE Trans. Circuits Syst. I*, vol. 52, no. 2, pp. 292–304, Feb. 2005.
[16] D. Baderna, A. Cabrini, M. Pasotti, and G. Torelli, "Power efficiency evaluation in Dickson and voltage doubler charge pump topologies," *Microelectron. J.*, vol. 37, no. 10, pp. 1128–1135, Oct. 2006.
[17] L. Aaltonen and K. Halonen, "On-chip charge-pump with continuous frequency regulation for precision high-voltage generation," in *Proc. IEEE Prime'09*, Cork, Ireland, Jul. 2009, pp. 68–71.
[18] T. Speeti, L. Aaltonen, and K. Halonen, "Integrated charge-pump phase-locked loop with SC-loop filter for capacitive microsensor readout," in *Proc. IEEE Int. Symp. Circuits Syst.*, Taipei, Taiwan, May 2009, pp. 1373–1376.
[19] M. Steyaert, Z. Y. Chang, and W. Sansen, "Low-noise monolithic amplifier design: Bipolar versus CMOS," *Analog Integrated Circuit and Signal Processing*, vol. 1, no. 1, pp. 9–19, Mar. 1991.
[20] M. Saukoski, L. Aaltonen, and K. Halonen, "Zero-rate output and quadrature compensation in vibratory MEMS gyroscopes," *IEEE Sensors J.*, vol. 7, no. 12, pp. 1639–1652, Dec. 2007.

**Lasse Aaltonen** (S'07) received the M.Sc. and Lic.Sc. degrees in electrical engineering from Helsinki University of Technology (TKK), Espoo, Finland, in 2004 and 2006, respectively. He is currently working towards his doctoral degree in the Electronic Circuit Design Laboratory, TKK.

His main research interest is in the design of electronics for microelectromechanical sensors.

**Kari A. I. Halonen** (M'03) received the M.Sc. degree in electrical engineering from the Helsinki University of Technology, Finland, in 1982, and the Ph.D. degree in electrical engineering from the Katholieke Universiteit Leuven, Belgium, in 1987.

Since 1988 he has been with the Electronic Circuit Design Laboratory, Helsinki University of Technology. From 1993 he was an Associate Professor, and since 1997 a full Professor at the Faculty of Electrical Engineering and Telecommunications. He became the Head of Electronic Circuit Design Laboratory in 1998 and he was appointed as the Head of Department of Micro and Nano Sciences in 2007. He specializes in CMOS and BiCMOS analog and RF integrated circuits, particularly for telecommunication and sensor applications. He is the author or coauthor over 300 international and national conference and journal publications on analog and RF integrated circuits.

Prof. Halonen is currently an associate editor of IEEE JOURNAL OF SOLID-STATE CIRCUITS, and has been an associate editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, a guest editor for IEEE JOURNAL OF SOLID-STATE CIRCUITS, and the Technical Program Committee Chairman for European Solid-State Circuits Conference 2000. He was awarded the Beatrice Winner Award in ISSCC Conference 2002. He is a TPC member of ESSCIRC and ISSCC.