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On-Chip Charge-Pump with Continuous Frequency Regulation for Precision High-Voltage Generation

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***Abstract*— Closed-loop operation of charge-pumps is often taken advantage of in order to improve efficiency and to reduce the charge-pump output impedance and heavy sensitivity to supply and process variations. A fully integrated charge-pump, which utilizes continuous frequency control for the closed-loop operation, is presented in this paper. This means of control allows the charge-pump clock to settle to correct frequency according to current load while maintaining 50 % duty ratio of the clock. The final high-voltage signal is generated by using a closed-loop amplifier, for which the pump creates the supply, and which then amplifies the desired low-voltage signal to correct level. The implemented pump with the regulator has an active chip area of 0.14 mm^2 and creates a nominal output of 10 V with 29 μA load current and 2.5 V minimum supply.**

I. Introduction

Miniature mechanical structures in sensors, micromachined switches in telecommunication and micromirrors in optical transmission are example cases, which often require some control by means of a force applied to the mechanical structure. In microstructures electrostatic coupling can be utilized and the required electronics can be integrated together with the rest of the electronic interface. Still, control voltages can be relatively high, which calls for some level of charge pumping. In addition to sufficient voltage level, sensor applications such as detection of small signal capacitances, for example in gyroscopes [1], require the voltage to be stable and free of spurious components and excessive noise. This prevents the use of regulation methods such as that in [2], which can result in excess ripple at the pump output. However, the required high-voltage (HV) signals can be generated on-chip and the efficiency can be traded for noise, start-up time and full integration of the pump when the CP supply current is small compared to the total supply current of the system.

Implementation of low-noise HV generation is discussed in this paper. The closed-loop operation allows to reduce the voltage variation, to improve the efficiency of the pump and to speed up the start-up. To achieve a sufficient accuracy, bandwidth and control range of the final HV signal, the pump output is used to power two closed-loop high voltage amplifiers, which create the final outputs by amplifying the desired low-voltage input signals. The possibility of the periodic clock control to produce spurious components at the pump output, as explained in [3], is evaded by introducing continuous frequency control method. Compared to the improved periodic control method of [3], which also allows reduction of the output ripple voltage, the oscillator operates inside the loop in the proposed system. This relaxes the design requirements of the clock generator. Periodic ripple at the charge pump output can also be removed by converting it into pseudo-random noise using delta-sigma modulation [4]. It, however, results in more complex system, than the one proposed in this paper.

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II. Design of the High Voltage Generator

A top-level block diagram of the HV system is shown in Fig. 1. The CP is used to produce a filtered HV supply for two amplifiers. The two amplifiers create accurate HV output signals according to the low-voltage (LV) inputs.

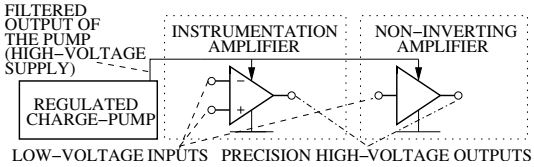

Fig. 1. Block diagram of the HV system.

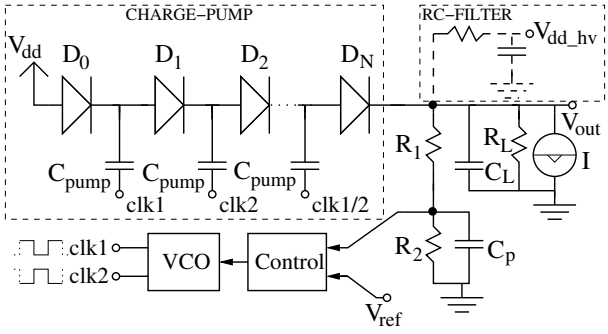

Fig. 2. Block diagram of the regulated CP.

The regulated CP block diagram is shown in Fig. 2, where a Dickson-type pump [5] creates the high voltage output. The output voltage V_{out} is scaled and compared to a LV reference V_{ref}. The difference of the voltages is fed through a controller to a voltage-controlled oscillator (VCO), which controls the pumping frequency and, hence, the output impedance of the pump. In the implemented pump the RC-loop denoted with dashed lines is used to filter the pump output before using it as a supply for the two HV amplifiers. Now, the current source I, corresponding to the amplifiers, is connected directly to pump output to ease the derivation of a linear model. The effect of the implemented RC-loop on the operation of the final CP is negligible.

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The regulated pump, denoted with solid lines in Fig. 2, can be modeled as a linear system shown in Fig. 3. The core CP is composed of the voltage source, which models the voltage change across the pump output resistance when a clock frequency change is applied, and the pump equivalent output resistance at the current operating point. The dominant pole of the system is defined by this equivalent pump output resistance (R_o), the load resistance (R_L) and the filtering load capacitor (C_L). The LV reference (V_{ref}) is compared to the pump output voltage (V_{out}) that is scaled using resistors R_1 and R_2. The parasitic pole, modeled in the system, is inflicted by the capacitor C_p. The voltage difference is converted to frequency with a constant gain defined by the VCO gain (K_{vco}) and the controller gain (K_{ctrl}). The frequency mode signal further closes the loop by defining the change of the pump voltage. For more accurate modeling, additional frequency dependencies of gain, for example at the controller, can be taken into account.

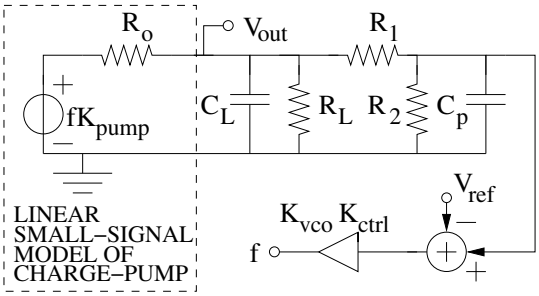

Fig. 3. Linear model of the regulated CP.

By using the model of Fig. 3, the linear transfer function of the system can be derived. The output resistance,

$$R_o = \frac{\Delta V_{tot}}{I_L} = \frac{N}{f_{clk} C_{pump}}, \tag{1}$$

defined by clock frequency f_{clk}, the number of pump stages N and the pump capacitor C_{pump}, can be used to calculate the gain from frequency to voltage,

$$K_{pump} = \frac{d(\Delta V_{tot})}{df} = I_L \frac{dR_o}{df} = -\frac{I_L N}{f_{clk}^2 C_{pump}}. \tag{2}$$

Here the effective load current I_L is defined by the resistive load (R_L, R_1 and R_2) and the current mode load I,

$$I_L = V_{out}(\frac{1}{R_L} + \frac{1}{R_1 + R_2}) + I, \tag{3}$$

by assuming that the closed-loop operation allows the V_{out} to settle to the value defined as $V_{ref}(1 + R_1/R_2)$. The clock frequency at this correct dc operating point can be calculated as

$$f_{clk} = \frac{I_L N}{C_{pump} \Delta V_{tot}}, \tag{4}$$

where the difference between the unloaded and loaded CP outputs

$$\Delta V_{tot} = (N + 1)(V_{dd} - V_d) - V_{out}. \tag{5}$$

The constants V_d and V_{dd} are the forward bias diode voltage and the nominal supply voltage, respectively.

TABLE I

PARAMETERS FOR THE EXAMPLE SYSTEM. THE STEP IS APPLIED TO THE REFERENCE VOLTAGE.

parameter	value	parameter	value
I	200 μA	R_1	7 $M\Omega$
R_2	1 $M\Omega$	R_L	∞
C_L	2 nF (Fig. 4), 4 nF (Fig. 5)	K_{vco}	3e8 Hz/V
N	7	V_{ref}	1.25 V
C_{pump}	10 pF	V_{dd}	3 V
V_d	0.65 V	C_p	5 pF
K_{ctrl}	1	Step size	0.01 V

The loop dominant pole is

$$\omega_o = 1/(\frac{R_0 R_L}{R_0 + R_L} C_L), \tag{6}$$

whereas the parasitic pole can be written as

$$\omega_p = 1/(\frac{R_1 R_2}{R_1 + R_2} C_p). \tag{7}$$

The loop gain of the system is

$$K_L = \frac{R_L}{R_L + R_o} K_{ctrl} K_{vco} K_{pump} \frac{R_2}{R_1 + R_2}. \tag{8}$$

Finally, the transfer function from the reference to the output voltage can be expressed as

$$\frac{V_{out}}{V_{ref}}(s) = \frac{\frac{R_1+R_2}{R_2}(1 + \frac{s}{\omega_p})}{\frac{s^2}{-\omega_p \omega_o K_L} + \frac{s}{K_L}(\frac{1}{-\omega_o} + \frac{1}{-\omega_p}) + \frac{K_L - 1}{K_L}}. \tag{9}$$

The negative coefficients will disappear after substituting (2) and (8) to (9). During derivation of (9) it is assumed that $R_o \ll R_1$.

A. Simulated Example System

The simulated closed-loop CP, also depicted with solid lines in Fig. 2, has the parameters given in table I. The VCO and the P-controller used are ideal, resistors and capacitors contain no parasitic properties and the diode models are identical to those used for the actual design.

For simulations, the pump is allowed to settle to correct operation point, after which a positive and a negative small-signal steps are applied to the reference voltage. The two step responses are shown in Figs. 4 and 5. In Fig. 4 the parasitic capacitor starts to delay the phase of the feedback before the unity gain frequency of the loop. The increasing instability can be seen as increased overshoot. When the load (filtering) capacitor size is doubled, in Fig. 5, the ripple at the pump output is halved and the stability increased, which can be observed as decreased overshoot.

In order to minimize the start-up or settling time, or to increase the loop gain, the delay in the feedback path should be minimized. On the other hand precise HV generation, with an accuracy of millivolts, by using just the CP is fairly difficult as the high loop-gain is typically achieved with a low-frequency dominant pole. Large capacitive load slows down the system large signal settling, for example during start-up. This results from difficulty of achieving proper functionality of the pump at very wide range of clock frequencies, which are required

in order to allow the feedback to speed up the system during large transients.

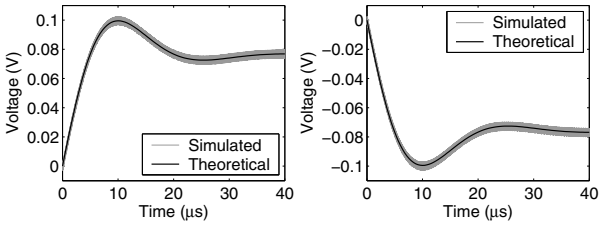

Fig. 4. Example system simulation with parameters shown in table I. The negative and positive steps are applied to V_{ref} and the curves depict the output voltage V_{out}.

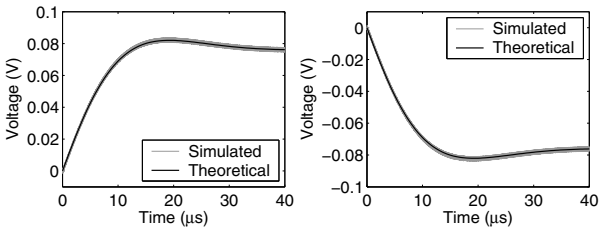

Fig. 5. Example system simulation with parameters shown in table I and with increased load capacitance. The negative and positive steps are applied to V_{ref} and the curves depict the output voltage V_{out}.

B. Implemented HV System

The top-level of the implemented system corresponds to Fig. 1, while the regulated pump is shown in Fig. 2 and has designed characteristics shown in table II. The first four stages of the pump utilize LV poly-poly-capacitors and the last five stages HV sandwich-capacitors with lower density but higher voltage tolerance. The CP area is optimized at lowest supply [6], [7]. The total load capacitance is difficult to evaluate precisely due to extensive amount of parasitic capacitance, which was taken advantage of. However, the designed value of C_L is 20 pF.

The proportional controller and the VCO are shown in Fig. 6. Here, the pump output, before the RC-filtering, is scaled using resistors R_1 and R_2. The scaled voltage is fed to the controller, which creates a current that is proportional to difference between the scaled output and the reference V_{ref}. The current is converted to voltage in a diode connected NMOS and mirrored further to the oscillator. In the oscillator the load of the oscillator core comprises two diode connected and two linear region PMOS-transistors, which have control current dependent biasing. This load configuration is used to stabilize the output swing as a function of the control current and, hence, to linearize the frequency dependency of control current. The maximum frequency of the VCO is 60 MHz, limited by the control current range. It is important to verify that during, for example, start-up, the controller is not capable of saturating the VCO. In fact, the maximum freqency should be limited to value, which allows the minimum output resistance of the CP [8]. The low swing of the oscillator core is transformed to rail-to-rail signal at the push-pull stage. The output clock is used, after buffering, to drive the CP.

The two HV amplifiers both use the operational amplifier (opamp) shown in Fig. 7. To minimize the number of area

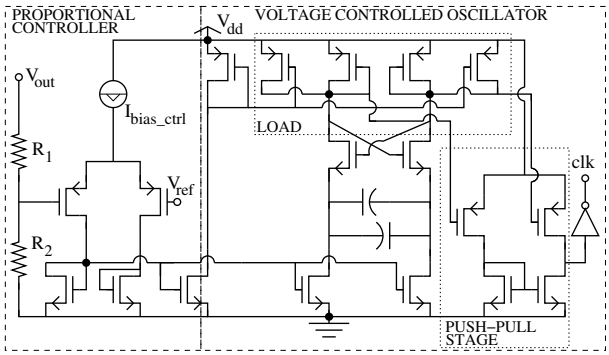

Fig. 6. The implemented resistors R_1 and R_2, the controller and the VCO.

TABLE II

DESIGNED TYPICAL PARAMETERS OF THE ON-CHIP, REGULATED CP.

parameter	value	parameter	value
R_L	∞	R_1	3 $M\Omega$
R_2	0.4 $M\Omega$	$K_{vco} \cdot K_{ctrl}$	6e8 Hz/V
N	9	V_{ref}	1.25 V
C_{pump}	1.6-1.1 pF	V_{dd}	2.5-3.6 V
I	20 μA		

consuming HV transistors and the pump load current, the opamp has a LV first stage and no cascode transistors in the second stage. Folded first stage allows input common-mode levels up to V_{dd}. The HV output stage and bias branch of the two amplifiers determine the CP current mode load.

The feedback of the amplifiers is sized so that less than 3 μA is taken by the feedback resistors at 10 V output voltage. As the large resistors together with the opamp input capacitance would impair the phase margin, small capacitors are added to the feedback path to provide phase compensation around the amplifier unity gain frequency.

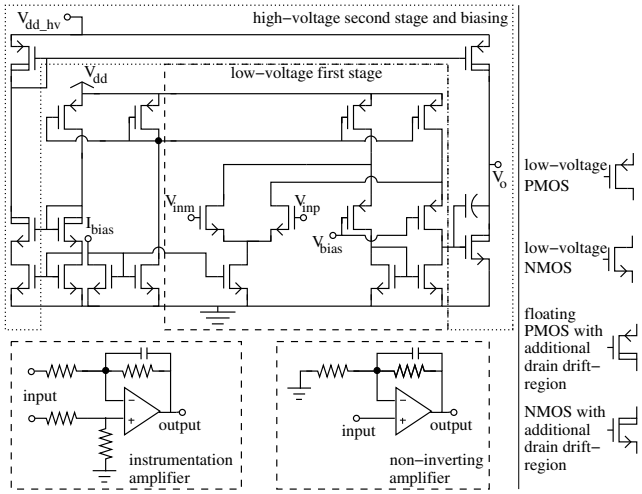

Fig. 7. The amplifiers, for which the CP creates the supply, and the schematic of the operational amplifier used.

III. MEASURED RESULTS

The technology used is 0.35-μm HV CMOS. The chip microphotographs are shown in Fig. 8 and the two sections of

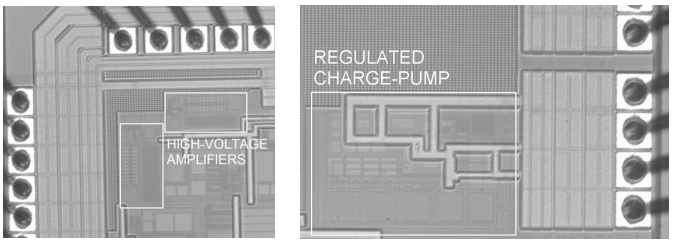

Fig. 8. The chip microphotographs showing the regions of the chip where the HV circuits are located.

the chip represent the regions where the HV blocks are located. The encircled areas of the regulated CP and the amplifiers are 0.14 and 0.08 mm^2, respectively. Roughly half of the regulated CP area is taken by the filtering capacitance.

The regulated CP start-up at three different values of supply voltage is shown in Fig. 9a. Increasing the supply voltage decreases the required clock frequency, which increases the loop gain and the frequency of the loop dominant pole. This can be observed also in the figure despite the large-signal step. The system exhibits no overshoot, which proves that the delay in the feedback path is sufficiently small. The measured output impedance of the regulated CP is 23 $k\Omega$ (V_{dd} = 3 V) and the series resistance of the RC-filter (see Fig. 2) is 25 $k\Omega$. The rms noise at the CP output is 0.8 mV (V_{dd} = 3 V).

The loop gain is not sufficient to keep the pump output accurately at the desired level, $V_{ref}(R_1 + R_2)/R_2 = 10$ V, due to the simple controller and the RC-filter used. The final dc regulation is performed by the high dc power supply rejection ratio of the closed-loop amplifiers. The open-loop dc gain of the opamp used is approximately 120 dB. The CP related data is summarized in table III, which shows also the pump load current and the supply current. Although the efficiency, partly limited by the pump capacitor bottom plate capacitances, is optimized at the same point as the area [7], the efficiency remains poor due to the large parasitics of the on-chip capacitors and losses in clock generation and diodes.

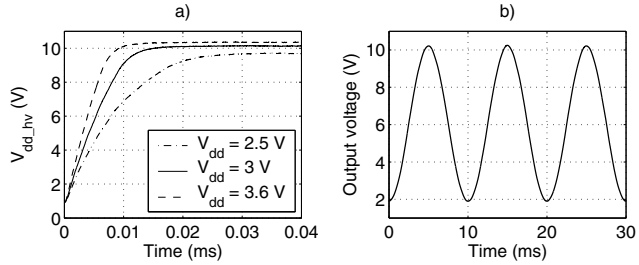

Fig. 9. a) The regulated CP output during start-up with nominal load current and at different supply voltages. b) Maximum signal, linearity better than 50 dB, at the non-inverting amplifier output.

As the opamps are identical in the two amplifiers, only the measured results of the non-inverting amplifier are presented. Fig. 9b depicts the maximum linear range of the amplifier. The input referred rms noise spectrum of the amplifier is shown in Fig. 10a and the gain transfer function in Fig. 10b, both up to 500 kHz. Clearly, no undesired spurious components are visible at the amplifier output and the noise is dominated by the amplifier input resistance.

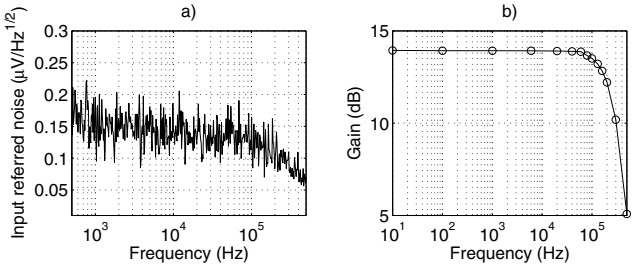

Fig. 10. a) Input referred noise of the non-inverting amplifier. b) Gain transfer function of the non-inverting amplifier.

TABLE III

MEASURED CP PROPERTIES AT DIFFERENT SUPPLY VOLTAGES.

Supply (V)	2.5	3.0	3.6
Supply current (μA)	636	539	502
V_{dd_hv} (V)	9.8	10.2	10.4
I_L (μA)	29	29	29
Efficiency (%)	18	18	17

IV. CONCLUSIONS

A regulated CP structure is proposed in this paper. The pumping frequency is continuously controlled, which prevents any spurious components from appearing below the actual pumping frequency. Proportional control of the frequency is straightforward to stabilize by ensuring that the filtering pole at the pump output dominates over other poles of the loop. As the frequency is not tied to any predetermined value, the frequency can increase during large transients, hence speeding up for example the pump start-up. The presented linear model, although introduced for a Dickson-type CP, is not limited to this type of charge-pumps. The implemented pump with the regulator has an active chip area of 0.14 mm^2 and creates a nominal output of 10 V with 29 μA load current. The final high precision HV signals over wide voltage range are generated using closed-loop amplifiers, supplied by the CP.

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