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Integrated Charge-Pump Phase-Locked Loop with SC-Loop Filter for Capacitive Microsensor Readout

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***Abstract*— In this paper, simulated and measured phase noise characteristics for a charge-pump phase-locked loop (PLL) with a switched capacitor loop filter are presented. The PLL is fabricated using a 0.35 μm high-voltage CMOS technology. The PLL is designed for a reference frequency range from 3 kHz to 10 kHz, for divider value of 32, and to operate in temperature range from 40 $^{\circ}C$ to +85 $^{\circ}C$ and with 2.5 to 3.6 V supply. Measured results indicate that the SC-filter can be used to replace the conventional RC-filter in order to reduce area.**

I. Introduction

Fast development of the microfabrication techniques has made possible a significant cost reduction of miniaturized sensors enabling their use in various new applications. Sensors such as angular velocity sensors or accelerometers have been applied increasingly in, for example mobile phones and game controllers.

Interfacing sensors requires often clocking of switched capacitor (SC) -circuits or digital signal processing (DSP). Typically a phase-locked loop (PLL) is used to generate the required clock signals. When the micromechanical element is used to provide the reference signal, the frequency in these cases can be low, in kilohertz range. To maintain adequate damping factor and natural frequency of the loop, high resistance and capacitance values of the RC-loop filter, in addition to small charge pump (CP) currents, has to be used. At audio frequencies, the integrated resistor and capacitor of the RC-loop filter in the charge-pump phase-locked loop forms the biggest single block of the circuit. The method presented in [1] for replacing the area consuming resistor in the loop filter with a simple switched capacitor equivalent, allows significantly decreased area of the loop filter, especially when high-ohmic polysilicon resistors are not available in the technology used.

II. Structure of the phase-locked loop

A charge-pump PLL with a square wave output was selected for the implementation due to its well characterized operation and suitability for integration. It consists of a phase frequency detector (PFD), a charge pump, a loop filter (LF), a voltage controlled oscillator (VCO) and a divider as illustrated in the

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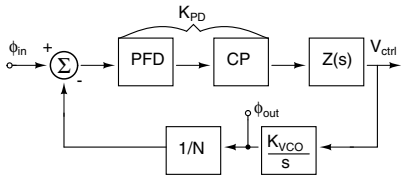

Fig. 1. Block diagram of the charge pump PLL.

Fig. 1. The closed-loop linear model of the designed PLL can be presented as

$$H(s) = \frac{V_{ctrl}}{\phi_{in}} = \frac{sK_{PD}Z(s)}{s + K_{PD}Z(s)K_{VCO}/N}, \qquad (1)$$

where K_{PD} is the combined gain of the phase-frequency detector and the charge pump, $Z(s)$ is the impedance of the loop filter, K_{VCO} is the gain of the VCO and N is the division ratio.

The phase-frequency detector is implemented using standard NOR-gates as for example in [2]. The divider is a digital down counter, which is implemented using T flip-flops. The divider has a fixed division ratio of 32.

The designed charge pump is a single-ended cascode current mirror that has 3-bit control over the current. The control is realized with the bits B1-B3 as shown in Fig. 2. Use of the cascode topology reduces a mismatch between the currents. This reduces the phase offset and more importantly the reference spurs [3]. The current sources are kept in saturation by using a unity-gain amplifier, which is connected between output of the pump and drains of switch transistors SW_1 and SW_2. This minimizes the dead zone and the timing uncertainty.

The voltage controlled oscillator of the design is a combination of a voltage controlled current source (VCCS) and a current controlled oscillator (ICO). In the VCCS, a source degenerated NMOS transistor, MN_1 in Fig. 3, acts as the input device and converts the voltage to current. Resistance value of a R_{VCCS} is designed to be much higher than the transconductance of the MN_1 to achieve as linear response from control current to control voltage as possible. The transistors MP_1 and MP_2 mirror this control current to node I_{ctrl}, which is connected to the ICO and controls the frequency of the oscillator. With bits B_1 and B_2 it is possible to adjust the gain of the VCCS, thus enabling compensation of the process variations. The current from the external current source, I_{REF} in Fig. 3, guarantees the oscillation at zero control voltage.

The core of the ICO is a single-ended cross-coupled CMOS multivibrator as shown in Fig. 4 [4]. In the traditional multi-

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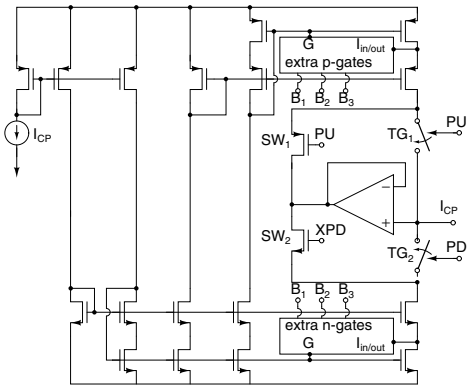

Fig. 2. Schematic of the charge pump.

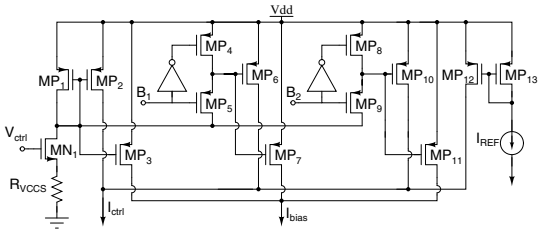

Fig. 3. Schematic of the VCCS.

vibrator, the voltage swing over the capacitance C_{ICO} varies significantly over the control current [5]. The transistors MN_1-MN_3 in Fig. 4 are used to stabilize the voltage swing over the capacitor C_{ICO} inside the tuning range of the VCO. The current I_{bias} from the VCCS to the transistor MN_1 in the Fig. 4 is directly proportional to the current I_{ctrl}. As the control current of the ICO changes the current trough MN_2 also changes. This dependency of the current through the transistor MN_2 leads to the constant current trough the transistor MN_5 despite the control current, thus the voltage swing over the C_{ICO} is stabilized and the frequency becomes a linear function of the control current.

The SC-type loop filter consists of an integration capacitance as in a basic RC-type filter and the switched capacitance, which represents the resistance of the RC counterpart as shown in

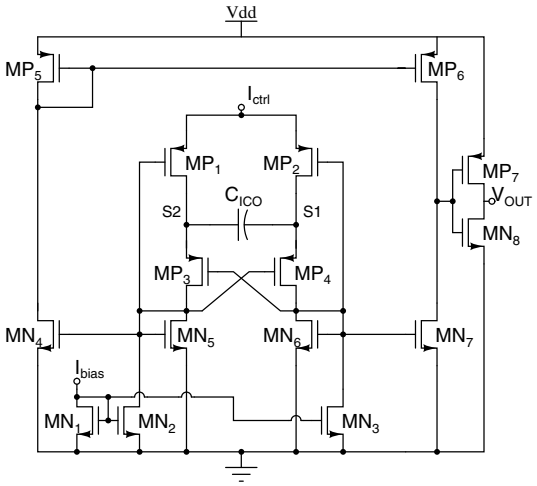

Fig. 4. Schematic of the ICO.

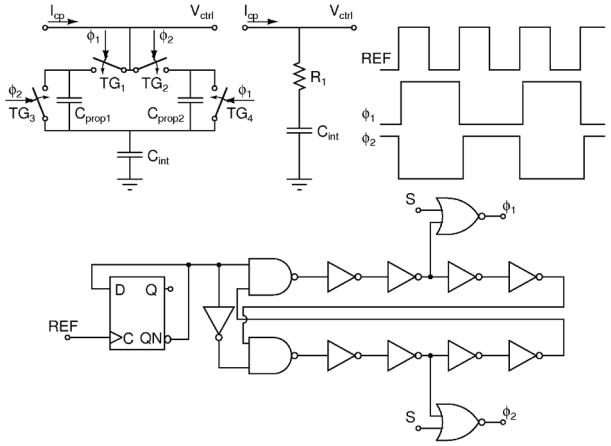

Fig. 5. Implemented SC- and RC-filters, control signals for the SC-filter and clock generator for the control signals of the SC-filter. The signal S is the enable signal.

TABLE I

LINEAR MODELS FOR THE SUBBLOCKS OF THE PLL.

Block	Linear model
PDF + CP	$K_{PD} = \frac{I_{CP}}{2\pi}$
LF	$Z_{RC}(s) = \frac{sC_{int}R_1+1}{sC_{int}}$, $Z_{SC}(s) = \frac{sC_{int}+C_{prop}f_{ref}}{sC_{int}C_{prop}f_{ref}}$
VCO	$K_{VCO} = \frac{f_{out}}{V_{ctrl}} = \frac{1}{4R_{VCCS}V_{swing}C_{ICO}}$
Divider	N

Fig. 5. This figure also shows the control signals of the SC-filter and the schematic of the clock generator. The equivalent resistance of the SC-filter in Fig. 5 can be written [1] as

$$R_{eq} = R_1 = \frac{T}{C_{prop}} = \frac{1}{C_{prop}f_{ref}}, \tag{2}$$

where T is a period of the reference signal, f_{ref} is the frequency of the reference and C_{prop} is the switched capacitor. When the linear models of the subblocks of the PLL and the impedances of the loop filters from TABLE I are substituted in to (1) we get

$$\omega = \sqrt{\frac{G_P I_{CP}}{8\pi V_{swing}C_{ICO}R_{VCCS}C_{int}N}} \tag{3}$$

TABLE II

COMPONENT SIZES IN THE LOOP FILTER, CHARGE PUMP CURRENTS, NATURAL FREQUENCY AND DAMPING FACTOR OF THE PLL AND AREAS OF THE LOOP FILTERS.

	RC	**SC**
$\mathbf{I_{CP}[nA]}$	20 - 120	20 - 120
$\mathbf{R_1[M\Omega]}$	12	-
$\mathbf{C_{prop}[pF]}$	-	3.6
$\omega\mathbf{[Hz]}$	130 - 343	263 - 510
$\zeta[]$	0.24 - 0.60	0.28 - 0.71
$\mathbf{Area[mm^2]}$	0.023	0.015

for the natural frequency of the loop, when G_P is the current mirror ratio in Fig. 3, and

$$\zeta_{RC} = \sqrt{\frac{R_1^2 G_P I_{CP} C_{int}}{32\pi V_{swing} C_{ICO} R_{VCCS} N}} \quad (4)$$

for the damping factor of the PLL with the RC-filter. The damping factor of the loop with the SC-filter can be written as

$$\zeta_{SC} = \sqrt{\frac{G_P I_{CP} C_{int}}{32\pi V_{swing} C_{ICO} R_{VCCS} N C_{prop}^2 f_{ref}^2}}. \quad (5)$$

If the bandwidth of the loop is designed to be narrow, attenuation of the high frequency components is higher but the settling time of the loop is longer and the VCO phase noise dominates over the reference phase noise. Because of the wide reference range, the SC-loop filter requires adjustment of the damping factor and the nominal frequency of the loop. If the gain of the VCO is set, then there are two methods that are used to control the damping factor: first, adjusting the charge pump current and second, changing the size of the integration capacitor. Control over the damping factor is implemented by controlling the charge pump current with 3-bits between 20 nA and 120 nA. There is also possibility to use two different integration capacitance values, which are 12.1 pF and 16.1 pF.

TABLE II lists the component sizes of the RC- and SC-loop filter, used charge pump currents and the corresponding dynamics of the designed PLL. The areas of the loop filters are also listed in the table. Area reduction is possible by using the SC-filter especially when high-ohmic polysilicon is not available. In this design the small difference between the areas of the filters is due to the moderately poor capacitance density of the integrated poly-poly capacitors and high density of the high-ohmic polysilicon resistors.

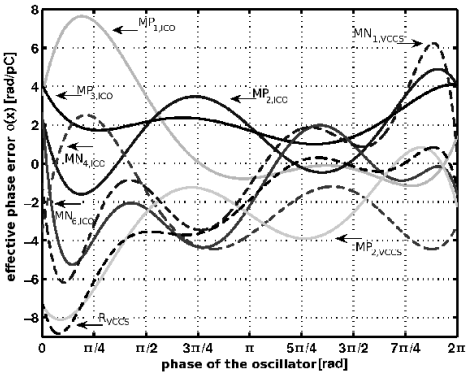

Fig. 6. Phase errors of the elements of the VCO.

III. Phase noise

Phase noise analysis of the VCO is carried out with a conventional transient noise simulations and with an impulse response method [6] where a 0.5 fC charge is injected one by one in parallel with the elements of the VCCS and ICO. The effect of the injected charge is different at different phases

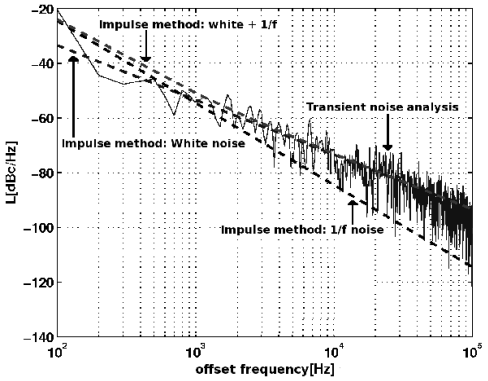

Fig. 7. Simulated phase noise spectra of the VCO with transient noise analysis and with impulse method with 6 kHz reference frequency.

of the output signal as shown in Fig. 6. In this figure x-axis represents the phase of the VCO output and y-axis represents the effective phase error of the element caused by the impulse. High rms value of the $\phi(x)$ denotes high sensitivity to white noise and high dc value high sensitivity to 1/f noise [6]. Simulations indicated that the dominant noise sources of the VCO are the transistors $MP_{1,VCCS}$, $MP_{6,VCCS}$ and $MP_{10,VCCS}$.

The phase noise spectrum, $L\{\Delta f\}$, of the VCO can be calculated from the simulated impulse responses of the different elements. Fig. 7 shows the calculated phase noise spectra of the VCO and the effect of the white noise and 1/f-noise to $L\{\Delta f\}$ separately. In the same figure there is also the simulated phase noise spectrum of the VCO. The figure shows good correspondence between the transient noise analysis and the impulse method. It should also be noticed that in this design the noise of the loop filter is not significant due to current mirror ratio G_P smaller than unity.

IV. Measurement Results

Fig. 8 shows the microphotograph of the implemented ASIC and the magnified microphotograph of the PLL. The area of the chip is 7.9 mm^2 and the active area is 4.6 mm^2. The area of the PLL is 0.13 mm^2, where the RC-loop filter takes 0.023 mm^2, and the SC-loop filter 0.015 mm^2. Simulated current consumption of the PLL is 7.3 μA, of which the VCO consumes 4.2 μA and the charge pump 2.9 μA. The division ratio N is constant, 32.

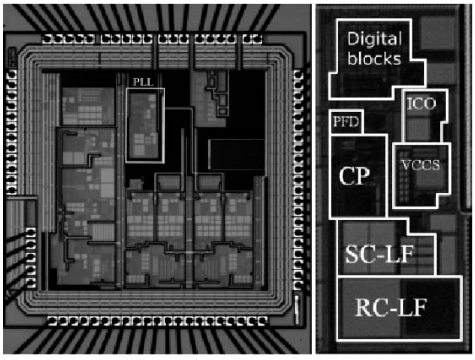

Fig. 8. Microphotograph of the ASIC.

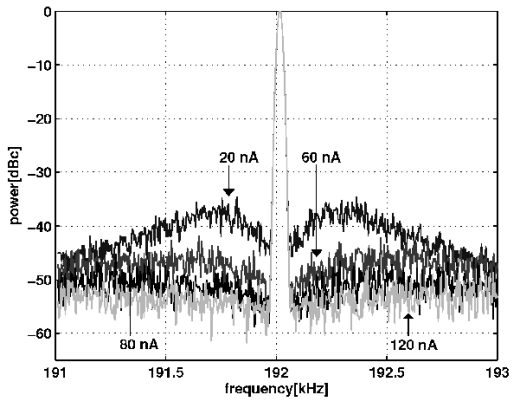

Fig. 9. Effect of the bandwidth and the damping factor to the phase noise of the PLL with the RC-filter.

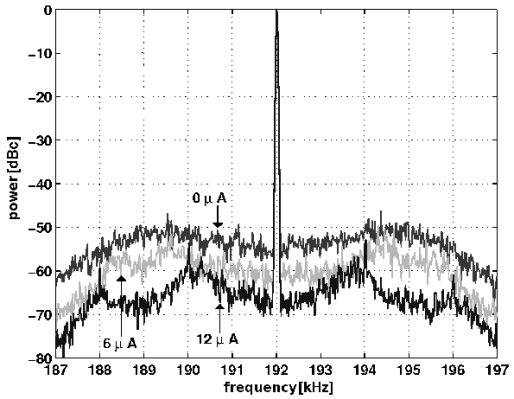

Fig. 10. Effect of the loop filter voltage (external current) to the phase noise of the PLL with the SC-filter.

The effect of the loop bandwidth to the phase noise of the PLL can be examined by altering the charge pump current. Fig. 9 presents a measured spectrum of the PLL with the RC-filter with four different charge pump current values. Currents 20 nA, 60 nA, 80 nA and 120 nA correspond to the bandwidths of 130 Hz, 225 Hz, 259 Hz and 318 Hz respectively. Damping factors for those currents are 0.24, 0.42, 0.49 and 0.6 respectively.

From Fig. 9 we can see that as the bandwidth of the loop is increased the phase noise near the carrier frequency is reduced. The damping factor also depends on the charge pump current. This means that the noise is reduced not only because of the bandwidth. As the damping factor increases gain peak is reduced thus the phase noise of the PLL is reduced.

Effect of the loop filter voltage can be examined with different external currents for the VCCS. When I_{REF} in the Fig. 3 is increased the operating point of the VCO if moved upwards and required frequency is attained with a lower V_{ctrl}. Fig. 10 shows the phase noise of the PLL with SC-filter with three different external currents. Noise level near the fundament is reduced with increased external current. This is because of the noise from the current mirror in VCCS is reduced. It should be noticed that when the operating point of the VCO is changed upwards the tuning range of the oscillator

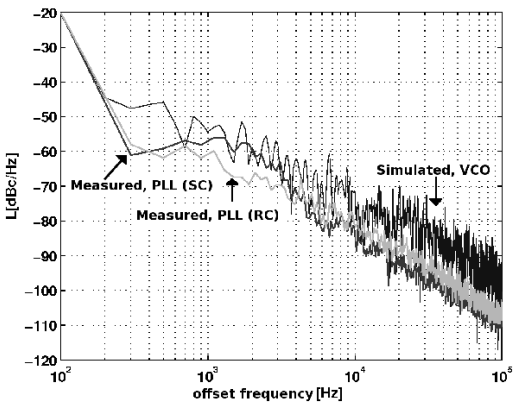

Fig. 11. Simulated spectrum of the VCO and measured spectra of the PLL with SC- and with RC-filter.

is also shifted to higher frequencies. When the external current is increased enough, noise peaks at one third of the reference frequency are revealed. Source of these spikes is most likely the cross-coupling of clock signals, which exist on-chip at the frequency $f_{ref}/3$.

Fig. 11 presents a comparison between the simulated spectrum of the VCO and measured spectra of the PLL. It shows that a measured spectrum of the PLL with the SC-loop filter is equivalent to that of the RC-filter.

V. Conclusions

In this paper, the phase noise characteristics and the measurement results of a low frequency PLL with an SC-loop filter were presented. The simulated current consumption is 7.3 μA. The tuning range of the PLL was measured to be from 3 kHz to 11 kHz with both filter types. The phase noise over the tuning range at 100 kHz offset frequency was measured to be from 102 dBc/Hz to 110 dBc/Hz with the RC-filter and 103 dBc/Hz to 108 dBc/Hz with the SC-filter. With further decreasing reference frequency the significance of leakage current increases, which must be considered in the design. Measurements verified that the RC-loop filter can be replaced with the very simple SC-loop filter in order to remove the high-ohmic polysilicon resistor of the loop filter.

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