Publication P3

Mika Kämäräinen, Mikko Saukoski, Matti Paavola, Jere A. M. Järvinen, Mika Laiho, and Kari A. I. Halonen. 2009. A micropower front end for three-axis capacitive microaccelerometers. IEEE Transactions on Instrumentation and Measurement, volume 58, number 10, pages 3642-3652.

# A Micropower Front End for Three-Axis Capacitive Microaccelerometers

Mika Kämäräinen, *Student Member, IEEE*, Mikko Saukoski, *Member, IEEE*, Matti Paavola, *Student Member, IEEE*, Jere A. M. Järvinen, Mika Laiho, *Member, IEEE*, and Kari A. I. Halonen, *Member, IEEE*

***Abstract*—This paper presents the measurement results of a micropower switched-capacitor front end that was designed for three-axis capacitive microaccelerometers. The designed front end can reduce the distorting effects of the electrostatic forces and can be used in single-ended and differential modes. The front end was realized with a 0.13-$\mu$m bipolar complimentary metal–oxide–semiconductor process. The silicon area of the front end is 0.30 mm$^2$. The measurements show that the functionality of the front end follows the theory in both modes. Consuming 20 $\mu$A from a 1.8-V supply, it achieves noise densities of 424, 607, and 590 $\mu g/\sqrt{\text{Hz}}$ in the $x$-, $y$-, and $z$-directions, respectively, when each mass is sampled at 1 kHz in the differential mode.**

***Index Terms*—Electrostatic forces, low-power circuit, sensor front end, switched-capacitor circuit, three-axis capacitive accelerometer.**

## I. Introduction

MICROACCELEROMETERS are micromachined acceleration sensors with dimensions that range from 1 to 100 $\mu$m. The devices are, for example, piezoelectrical, piezoresistive, or capacitive. Compared to the other techniques, capacitive accelerometers have advantages such as zero static biasing current and excellent thermal stability. Furthermore, by using bulk micromachined devices with a large seismic mass, very high sensitivity can be reached.

With a proper configuration, a single capacitive accelerometer can simultaneously measure accelerations along all three axes [1]–[3]. The devices are built in such a way that the seismic mass forms four differential capacitor pairs. By measuring these capacitances and taking their proper linear combinations, all three vector components of linear acceleration (in the $x$-, $y$-, and $z$-directions) can be estimated. With four differential detection capacitances, these devices also offer redundancy so that fault conditions can be detected.

Manuscript received May 28, 2008; revised July 10, 2008. First published June 19, 2009; current version published September 16, 2009. This work was supported in part by the Nokia Research Center, VTI Technologies, and the Finnish Funding Agency for Technology and Innovation (TEKES). The Associate Editor coordinating the review process for this paper was Dr. Subhas Mukhopadhyay.

M. Kämäräinen, M. Paavola, and K. A. I. Halonen are with the SMARAD-2/Electronic Circuit Design Laboratory, Helsinki University of Technology, 02150 Espoo, Finland (e-mail: mpkamara@ecdl.tkk.fi; mhpaavol@ecdl.tkk.fi; karih@ecdl.tkk.fi).

M. Saukoski was with the SMARAD-2/Electronic Circuit Design Laboratory, Helsinki University of Technology, 02150 Espoo, Finland. He is now with ELMOS Semiconductor AG, 44227 Dortmund, Germany (e-mail: mikko.saukoski@elmos.eu).

J. A. M. Järvinen was with the SMARAD-2/Electronic Circuit Design Laboratory, Helsinki University of Technology, 02150 Espoo, Finland. He is now with the Power Management DC–DC Converter Group, Texas Instruments, 02150 Espoo, Finland (e-mail: j-jarvinen@ti.com).

M. Laiho is with the SMARAD-2/Electronic Circuit Design Laboratory, Helsinki University of Technology, 02150 Espoo, Finland, and also with the Microelectronics Laboratory, University of Turku, 20520 Turku, Finland (e-mail: mlaiho@ecdl.tkk.fi).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIM.2009.2018700

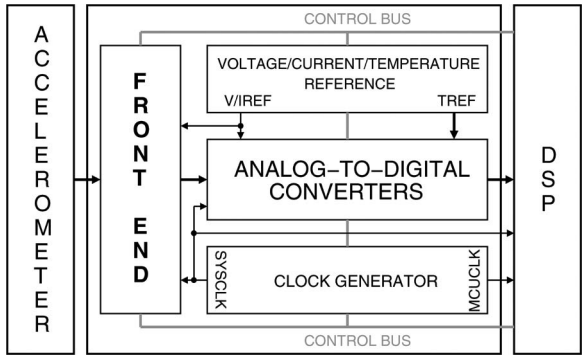


Fig. 1. Low-power interface for a three-axis capacitive accelerometer.

An inexpensive yet reliable and highly sensitive three-axis accelerometer with low power consumption would have a wide range of applications—from hand-held mobile terminals and toys to industrial applications and automotive chassis control systems. To realize this kind of sensor, the readout electronics have to be integrated together with the sensor element, forming a microelectromechanical system. The accelerometer should ideally have a fully digital output.

To design a capacitive accelerometer front end with a wide linear acceleration range, the nonsymmetrical signal-dependent electrostatic forces in the sensor element have to carefully be considered [4]. In the electromechanical force-balancing $\Sigma\Delta$ loop, the mass of the accelerometer is ideally kept in a constant position, and therefore, the electrostatic forces do not have an effect on linearity. This idea was first published in 1990 in [5], and a majority of the high-performance microaccelerometers that have been published [6]–[10] are based on it. The electromechanical force-balancing loop can also be realized as a continuous-time circuit. However, there are only a few published implementations [11]–[13]. The front end in this paper [14], in contrast, operates in an open-loop configuration. The reasons for this approach are simple implementation that reduces both silicon area and power dissipation, and a limited voltage range that is available for electrostatic feedback.

The front end is a part of a low-power interface application-specific integrated circuit (ASIC) for a three-axis capacitive accelerometer [15], [16], as shown in Fig. 1. The front end converts the capacitive acceleration information of the three-axis accelerometer into voltage. The two analog-to-digital

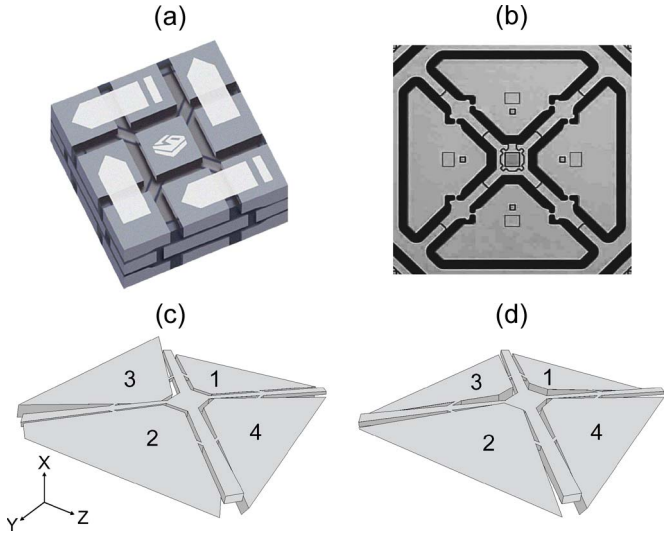


Fig. 2. (a) Encapsulated accelerometer [1]. (b) Top view of the structural element of the accelerometer (images courtesy of VTI Technologies, Vantaa, Finland). Sensor element under (c) $z$-directional and (d) $x$-directional acceleration.

converters (ADCs) convert the acceleration and temperature information into a digital form. The clock generator provides a system clock (SYSCLK) of 2 MHz and a microcontroller unit clock (MCUCLK) of 1–50 MHz. The bandgap-based voltage (V), current (I), and temperature (T) reference provides all reference voltages and currents, as well as temperature information. The off-chip digital signal processor (DSP) that is currently implemented with computer software controls the functioning of the system.

This paper is organized as follows. Section II describes the capacitive sensor element and the designed front end, Section III presents the experimental results, and finally, conclusions are drawn in Section IV.

## II. Front-End Design

In this section, first, the structure and the operation of a three-axis capacitive accelerometer are explained. Then, the designed front end and the operational amplifiers are presented.

### A. Accelerometer

A three-axis capacitive accelerometer and its operation are illustrated in Fig. 2. The sensor element consists of four differential capacitor pairs, which have a common middle electrode but top and bottom electrodes of their own. Acceleration causes torque, which tilts the proof masses. This causes the capacitance to change. For example, in Fig. 2(c), the sensor element is under $z$-directional acceleration. In this case, only masses 3 and 4 react by tilting in opposite directions. In Fig. 2(d), the sensor element is under acceleration in the $x$-direction. In that case, all four masses tilt in the same direction. By reading the capacitances with a front end, the accelerations in all three directions can be found as

$$\begin{bmatrix} a_x \\ a_y \\ a_z \end{bmatrix} = \frac{\sqrt{2}}{A_{C/a}} \begin{bmatrix} 1 & 1 & 1 & 1 \\ -1 & 1 & 0 & 0 \\ 0 & 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} \Delta C_{D1} \\ \Delta C_{D2} \\ \Delta C_{D3} \\ \Delta C_{D4} \end{bmatrix} \quad (1)$$

where $a_x$, $a_y$, and $a_z$ are the three linear acceleration components, $A_{C/a}$ is the gain from the acceleration in the direction of the sensitive axis of each mass to the capacitance, and $\Delta C_{Dn}$, with $n = 1$, 2, 3, or 4, are the capacitance differences of the sensor capacitors ($\Delta C_{Dn} = C_{DP(n)} - C_{DN(n)}$). Equation (1) assumes that the gain $A_{C/a}$ is equal for all four masses. The subindexing that was used corresponds to the numbering of the proof masses in Fig. 2. The $\sqrt{2}$ coefficient in (1) is caused by the 45° angle between any acceleration vector (x, y, or z) and the sensitive axes of the masses that respond to the acceleration.

### B. Designed Circuit

To reduce the distorting effects of the electrostatic forces, the single-ended self-balancing bridge [17] was chosen as the starting point in the design of the front end. In the designed front end in Fig. 3, time-multiplexed sampling is used to read the four masses of the three-axis accelerometer, because the masses have a common middle electrode. Time multiplexing enables the reading of one, two, or four masses (1-, 2-, or 3-axis operation). By using time multiplexing, the power dissipation and the die area of the designed front end are also reduced. The performance of the front end was further improved by adding the following options: 1) correlated double sampling (CDS) to reduce noise; 2) chopper stabilization to reduce offset voltage and noise; and 3) a differential mode to study its effects on the performance of the front end and to make a more effective use of the signal range in the subsequent ADC possible.

The attractive electrostatic force between the electrodes of a parallel-plate capacitor is

$$F = \frac{Q^2}{2\varepsilon_r \varepsilon_0 A} \quad (2)$$

where $Q$ is the charge in the capacitor, $A$ is the plate area, $\varepsilon_r$ is the relative permittivity of the insulator, and $\varepsilon_0$ is the permittivity of vacuum. Under acceleration, the capacitances $C_{DP(n)}$ and $C_{DN(n)}$ are not equal. Therefore, the electrostatic forces are also nonequal if these capacitors are biased by a constant voltage. This inequality of the electrostatic forces causes distortion [4]. Thus, to retain the wide linear region of the accelerometer, these forces have to be balanced.

The self-balancing bridge changes the voltage of the middle electrode $\mathrm{D_{MID}}$ such that the charges in the sensor capacitors $\mathrm{C_{DP(n)}}$ and $\mathrm{C_{DN(n)}}$ are equal, and thus, the electrostatic forces are also equal. In the basic operating mode, when CDS and chopper stabilization are not used, this balance is achieved by repeating the two main clock phases, i.e., reset phase $\phi_2$ and measurement phase $\phi_1$, as shown in Fig. 3. At the beginning of clock phase $\phi_2$, the mass being read is changed, and the output voltage of the previous cycle is loaded into the capacitors $\mathrm{C_{4P}}$ and $\mathrm{C_{4N}}$. This voltage was stored in the capacitors $\mathrm{C_{3Pn}}$ and $\mathrm{C_{3Nn}}$ of the latter integrator. Thus, the voltage of $\mathrm{D_{MID}}$ is equal to $V_{OUTP}$. During clock phase $\phi_2$, the output is in hold mode and, thus, can be sampled by the ADC. In clock phase $\phi_1$, the mass being read is connected to the reference voltages, and the difference of the charges that flow into $\mathrm{C_{DP(n)}}$ and $\mathrm{C_{DN(n)}}$ is integrated. This same cycle is repeated after the other three masses are read in turn. The output voltage $V_{OUT}$ and, thus, the

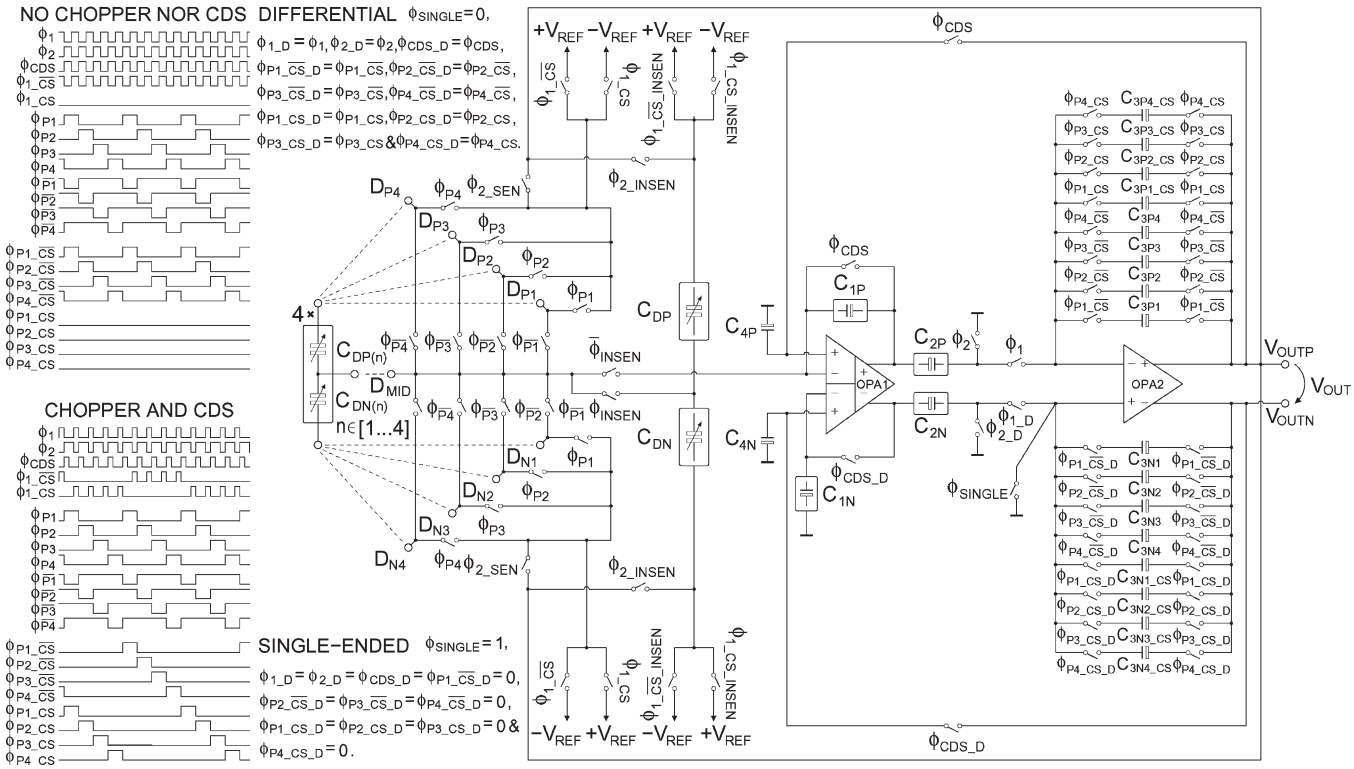


Fig. 3. Schematic of the front end.

voltage of $\mathrm{D_{MID}}$ changes until charge balance is achieved, and the electrostatic forces are thus equal.

To solve this balance voltage, the transfer functions for the different modes of the front end have to be derived. In the differential mode, the transfer function is

$$H_D(z) = \frac{V_{OUT}}{V_{REF}} = \frac{2 \cdot \left(C_{DP(n)} - C_{DN(n)}\right)}{\frac{C_1 C_3}{C_2}(1 - z^{-1}) + \left(C_{DP(n)} + C_{DN(n)}\right) z^{-1}} \quad (3)$$

for each $n \in \{1, \ldots, 4\}$. In Fig. 3, the upper and lower branches are identical, and therefore, only the first characters of the subindices of the capacitors in (3) are used. Similarly, in the single-ended mode, the transfer function is

$$H_S(z) = \frac{V_{OUT}}{V_{REF}} = \frac{C_{DP(n)} - C_{DN(n)}}{\frac{C_1 C_3}{C_2}(1 - z^{-1}) + \left(C_{DP(n)} + C_{DN(n)}\right) z^{-1}}. \quad (4)$$

By comparing (3) and (4), it is shown that the transfer functions are otherwise equal, except that the signal gain in the differential mode is twice as large as that in the single-ended mode.

At dc, the transfer functions simplify to

$$H_S(1) = \frac{C_{DP(n)} - C_{DN(n)}}{C_{DP(n)} + C_{DN(n)}}$$
$$H_D(1) = 2 \cdot \frac{C_{DP(n)} - C_{DN(n)}}{C_{DP(n)} + C_{DN(n)}}. \quad (5)$$

If the capacitors $C_{\mathrm{DP(n)}}$ and $C_{\mathrm{DN(n)}}$ are modeled as simple parallel-plate capacitors, their capacitances under acceleration can be written as

$$C_{DP(n)} = \frac{A\varepsilon_r\varepsilon_0}{d - \Delta d} = C_0\left(\frac{d}{d - \Delta d}\right)$$
$$C_{DN(n)} = \frac{A\varepsilon_r\varepsilon_0}{d + \Delta d} = C_0\left(\frac{d}{d + \Delta d}\right). \quad (6)$$

Here, $d$ is the initial distance between the capacitor plates, $\Delta d$ is the change in the plate distance that is induced by acceleration, and $C_0$ is the capacitance with $\Delta d = 0$. By substituting (6) into the dc transfer functions (5), the equations,

$$H_S(1) = \frac{\Delta d}{d}$$
$$H_D(1) = 2 \cdot \frac{\Delta d}{d} \quad (7)$$

are achieved. These equations show that the output voltage of the front end is ratiometric; in other words, the output voltage is linearly proportional to $\Delta d$ and, hence, to the acceleration in both operating modes.

As aforementioned, the output voltage $V_{OUTP}$ is equal to the voltage of $\mathrm{D_{MID}}$. Therefore, after the balance voltage is reached, the absolute values of the charges in the capacitors $\mathrm{C_{DP(n)}}$ and $\mathrm{C_{DN(n)}}$ can be calculated as

$$|Q_{DP}| = |Q_{DN}| = C_0 V_{REF} \quad (8)$$

where $Q_{DP}$ is the charge in $\mathrm{C_{DP(n)}}$, and $Q_{DN}$ is the charge in $\mathrm{C_{DN(n)}}$. The output voltage $V_{OUTP}$ is the same in both

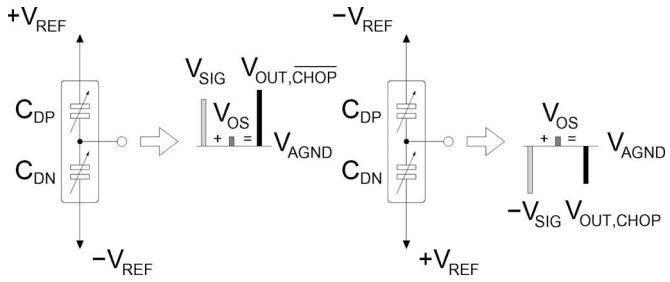


Fig. 4. Mass is read with noninverted and inverted reference voltages in chopper stabilization.

operating modes; thus, the sizes of the charges $|Q_{DP}|$ and $|Q_{DN}|$ are also independent of the operating mode that was used. Based on (8), it is shown that the charges are equal, and therefore, the electrostatic forces are balanced.

The previous analyses assume that the capacitors $\mathrm{C_{DP(n)}}$ and $\mathrm{C_{DN(n)}}$ can be modeled as parallel-plate capacitors and the acceleration is constant all the time. When the tilting movement of the masses is taken into account, the ratiometricy is no longer perfectly valid. In addition, if the acceleration changes, it takes time for the front end to achieve a new balance voltage. Therefore, if the acceleration is time varying, the front end follows this change and does not achieve the balance voltage, which increases the distorting effects of the electrostatic forces. The frequency range of interest is usually close to or is at dc, and thus, the difference between the balance voltage and the real output voltage becomes negligible if the sampling frequency is high compared to the signal frequency.

When CDS is used, an extra clock phase $\phi_{CDS}$ is required. In the case of chopper stabilization, the masses are read with inverted and noninverted reference voltages, as shown in Fig. 4. Hence, the signal $V_{SIG}$ changes its sign, but the offset voltage of the front end $V_{OS}$ does not. By dividing the difference of $V_{OUT,\overline{CHOP}}$ and $V_{OUT,CHOP}$ by two, the final output voltage becomes

$$V_{OUT} = \frac{V_{SIG} + V_{OS} - (-V_{SIG} + V_{OS})}{2}. \qquad (9)$$

It is shown that the offset voltage $V_{OS}$ is eliminated. Both output voltages are stored in their own integrator capacitors. Thus, extra capacitors and clock phases are required to implement chopper stabilization.

When the differential mode is used, the first amplifier operates as a differential difference amplifier (DDA) [18]. Making the signal path after the first amplifier differential results in a larger full-scale signal at the cost of higher power dissipation and larger die area. Capacitors $\mathrm{C_{1P}}$, $\mathrm{C_{1N}}$, $\mathrm{C_{2P}}$, and $\mathrm{C_{2N}}$ are implemented as matrices to enable the adjustment of the $-3$ dB-point of the front end according to transfer functions (3) and (4). The binary weighted capacitor matrices $\mathrm{C_{DP}}$ and $\mathrm{C_{DN}}$ constitute an internal sensor model that can be used in the measurements. The capacitance values of the matrices can be adjusted from 0 to 3.875 pF, with steps of 0.125 pF. The clock signals of the internal sensor model $\phi_{XX\_INSEN}$ are active only when the internal sensor model is used.

### C. Amplifiers

The operational amplifiers account for a major part of the current consumption in the front end. To minimize power dissipation while driving a capacitive load, a tail-current-boosted class-AB operational amplifier [19] is utilized. In such an amplifier, the bias current increases quadratically proportional to the differential input voltage. The input pair is designed to operate in weak inversion under quiescent conditions, i.e., when the differential input voltage is zero. This approach maximizes the current efficiency $g_m/I_D$, where $g_m$ is the transconductance of the device, and $I_D$ is the biasing current.

The DDA OPA1 that was used in the front end is shown in Fig. 5(a). The original implementation in [19] has been converted into a DDA by adding another tail-current-boosted input pair and summing the currents. The mode between the single-ended and the DDA operations can be chosen with the enable signal ENA_DIFF. Other differences, compared to the original implementation, are the differential outputs and the additional diodes where the biasing currents $I_{BIAS}$ are steered instead of mirroring them to the output, thus slightly saving in current consumption.

The second amplifier OPA2 of the front end is shown in Fig. 5(b). Signal ENA_DIFF is implemented to choose between the single-ended and differential operations. In the single-ended mode, the negative output is disabled, and current-mirroring ratios are changed with transistors MN1 and MN2 to keep the gain–bandwidth product (GBW) constant. The GBW could also be retained by increasing the overall biasing current, but this case would have an adverse effect on the current consumption of the front end. To increase the dc gain of the amplifier, transistors MN3 and MN4 were added to sink a fraction of the biasing current of the input pair [20]. The cost of the higher dc gain is the lower second pole, which decreases the phase margin.

The amplifiers use the same double-sampling common-mode feedback (CMFB) topology as shown in Fig. 5(c). In the DDA, asymmetrical loading of the differential outputs due to the front-end configuration was taken into account when designing the CMFB circuit. The CMFB of the DDA is dynamically biased by mirroring the currents from the outputs of the operational amplifier. When the amplifiers operate in the single-ended mode, the CMFB circuits are disabled.

## III. Experimental Results

The front end was realized with a 0.13-$\mu$m bipolar complimentary metal–oxide–semiconductor (BiCMOS) process that offers metal–insulator–metal capacitors, 2.5-V tolerant high-voltage analog transistors, and high-resistivity polysilicon resistors. Bipolar transistors and resistors were not used in the front-end design. Therefore, the front end is implementable with any standard complimentary metal–oxide–semiconductor (CMOS) technology. The microphotograph of the front end is shown in Fig. 6. The silicon area of the front end is 0.30 mm$^2$. The chips were encapsulated into an 80-lead plastic quad flat package. The goals of the measurements were to verify the functionality of the front end and to compare the performances of the single-ended and the differential modes.

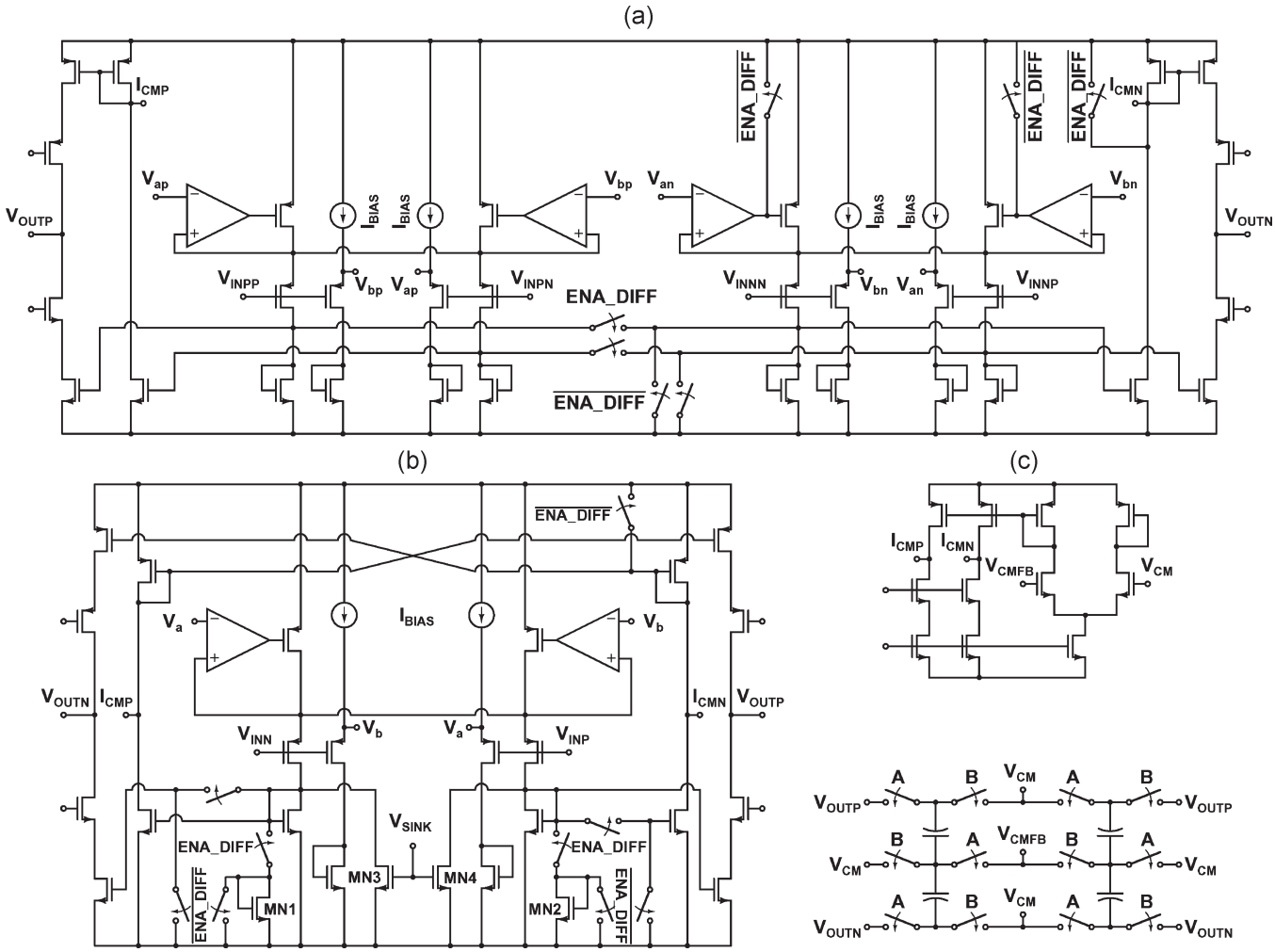


Fig. 5. Schematics of (a) the DDA OPA1, (b) the operational amplifier OPA2, and (c) the double-sampling CMFB circuit that was used in the amplifiers.

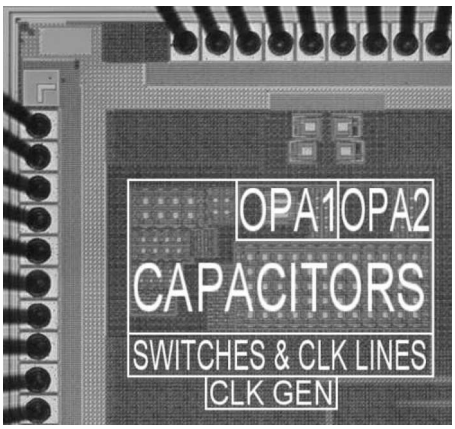


Fig. 6. Microphotograph of the front end.

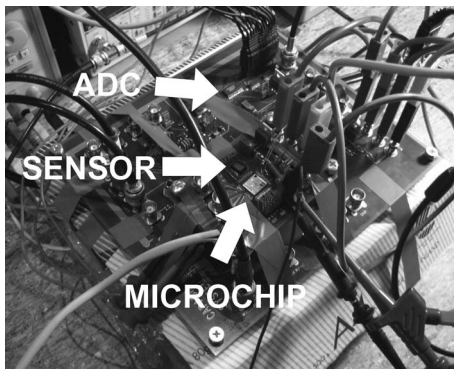


Fig. 7. Measurement Setup 1.

The supply voltage that was used was 1.8 V. The current consumption of the front end was measured to be 14 $\mu$A in the single-ended mode and 20 $\mu$A in the differential mode when each of the four masses were sampled at 1 kHz. The current consumption approximately varies within 1–2 $\mu$A from chip to chip. The aforementioned current consumptions are the worst case values.

Two different kinds of measurement setups were used. In Measurement Setup 1, both the interface ASIC and an external $\pm$4-g three-axis capacitive accelerometer were mounted on the same printed circuit board (PCB), as shown in Fig. 7. In Measurement Setup 2, the internal sensor model was used, and the measured chip was mounted into a test socket, which made a quick changing of the chips possible. In both measurement setups, the output voltage of the front end was converted to a single-ended voltage and was amplified with an external instrumentation amplifier (e.g., Burr-Brown INA111). In the

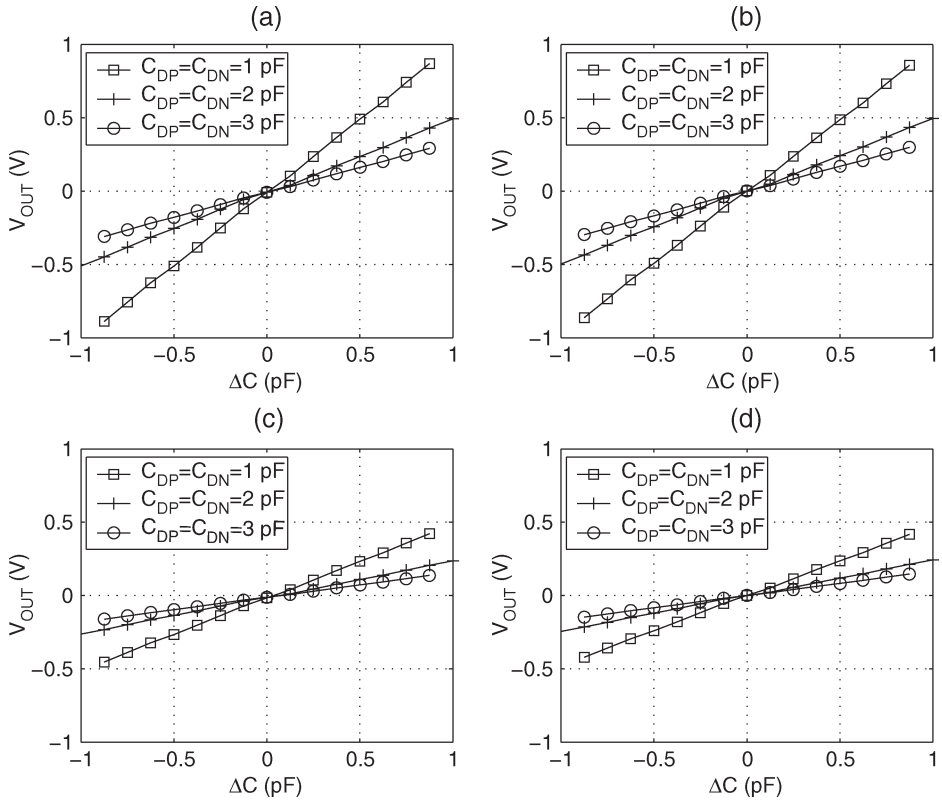


Fig. 8. Transfer-function measurements in the differential mode (a) with CDS and (b) with CDS and chopper stabilization. Transfer-function measurements in the single-ended mode (c) with CDS and (d) with CDS and chopper stabilization.

single-ended mode, $V_{OUTN}$ was connected to the on-chip 0.9-V analog ground. The output voltage of the instrumentation amplifier was converted into the digital domain by using a 12-bit external ADC (e.g., Analog Devices AD7492AR-5). Between the output of the instrumentation amplifier and the input of the ADC, there was a unity-gain buffer, which was realized with an operational amplifier (e.g., Analog Devices AD8626). The on-chip reference voltages and bias currents were used in the measurements. One signal generator was used to provide the main clock signal of the front end, bypassing the on-chip SYSCLK.

The structure of each of the following sections is given as follows. First, the goals and the measurement settings are introduced. Then, the measurement results are presented. Finally, the section is closed with a discussion of the achieved results.

### A. Transfer-Function Measurements at DC

Measurement Setup 2 with the internal sensor model was used to confirm the dc transfer functions of (5). Three different values for the base capacitances of the capacitor matrices $C_{DP}$ and $C_{DN}$, 1, 2, and 3 pF, were used. The reference voltage $V_{REF}$ was 0.5 V. By incrementing the difference of the capacitor matrices by steps of 0.25 pF, taking 16 384 samples with a sampling rate of 1 kHz from the output voltage of the instrumentation amplifier with a unity gain using the ADC, and calculating the average of these samples for every capacitance step, the curves for the output voltage of the front end, as a function of the capacitance change of each matrix $\Delta C$, can be obtained. These curves, as shown in Fig. 8, were measured with and without chopper stabilization. CDS was used in all cases.

TABLE I
TRANSFER-FUNCTION MEASUREMENTS FOR THE SINGLE-ENDED MODE

| No chopper stabilization | | | | |
|---|---|---|---|---|
| $C_{DP}$, $C_{DN}$ | Slope $[V/pF]$ | | | Offset voltage $[mV]$ |
| | Measured | Calculated | Rel. error | |
| $1\,pF$ | 0.4965 | 1/2 | 0.0070 | -15.6 |
| $2\,pF$ | 0.2472 | 1/4 | 0.0112 | -13.1 |
| $3\,pF$ | 0.1687 | 1/6 | 0.0122 | -11.8 |
| Chopper stabilization | | | | |
| $C_{DP}$, $C_{DN}$ | Slope $[V/pF]$ | | | Offset voltage $[mV]$ |
| | Measured | Calculated | Rel. error | |
| $1\,pF$ | 0.4753 | 1/2 | 0.0494 | -1.2 |
| $2\,pF$ | 0.2416 | 1/4 | 0.0336 | -0.7 |
| $3\,pF$ | 0.1670 | 1/6 | 0.0020 | 0.0 |

A linear function was fitted to the points of each curve that was obtained by using Matlab. According to these functions, both slopes and offset voltages were determined. The comparison between the measured and theoretical results is shown in Tables I and II. It is noticed that the front end realizes the transfer functions of (5) quite well. The differences can partly be explained by the abundant nonsymmetric wiring and chemical–mechanical polishing (CMP) fillers under the capacitors, which may cause a mismatch between the capacitor matrices. The output of the front end is directly connected to the input of the instrumentation amplifier, and therefore, the load at the second amplifier OPA2 is quite large. The weakened settling of the amplifier OPA2 may be shown in the slopes of chopper stabilization measurements, because fast settling is

TABLE II
TRANSFER-FUNCTION MEASUREMENTS FOR THE DIFFERENTIAL MODE

| No chopper stabilization | | | | |
|---|---|---|---|---|
| $C_{DP}$, $C_{DN}$ | Slope $[V/pF]$ | | | Offset voltage $[mV]$ |
| | Measured | Calculated | Rel. error | |
| $1\,pF$ | 0.9977 | 1 | 0.0023 | -8.5 |
| $2\,pF$ | 0.4964 | 1/2 | 0.0072 | -9.3 |
| $3\,pF$ | 0.3383 | 1/3 | 0.0149 | -8.6 |
| Chopper stabilization | | | | |
| $C_{DP}$, $C_{DN}$ | Slope $[V/pF]$ | | | Offset voltage $[mV]$ |
| | Measured | Calculated | Rel. error | |
| $1\,pF$ | 0.9761 | 1 | 0.0239 | -1.7 |
| $2\,pF$ | 0.4905 | 1/2 | 0.0190 | -1.0 |
| $3\,pF$ | 0.3380 | 1/3 | 0.0140 | 0.5 |

needed when the output voltage alternately changes to negative and positive values, as shown in Fig. 4.

### B. Noise Measurements

Measurement Setup 1 and the external $\pm 4$-g three-axis capacitive accelerometer were used in the noise performance measurements of the front end. The reference voltage $V_{REF}$ was set to a maximum of 0.85 V, and the gain of the instrumentation amplifier was six. This condition maximized the sensitivity of the front end and ensured that the measured noise contribution of the external components was minimized. In the measurements, first, the front-end noise in a single mass data was analyzed. By knowing the noise in a single mass data, the noises of $x$-, $y$-, and $z$-directions could be approximated. These approximations were confirmed by calculating the noises of $x$-, $y$-, and $z$-directions from the data of the four masses.

The 10 700-point fast Fourier transform (FFT) plots for one mass measured in different configurations are shown in Fig. 9. The signal was recorded from the external ADC output. A moving average of 21 points was used to smooth these spectra. Each proof mass was sampled at 1 kHz in the differential mode. By comparing these spectra, it is shown that CDS reduces the noise level by approximately 6 dB compared to the case in which both CDS and chopper stabilization are disabled. Furthermore, chopper stabilization modulates the offset and flicker noise of the front end to the vicinity of half of the sampling frequency.

The noises of the individual masses can be converted to the noises of the three linear acceleration components through (1). As mentioned in the context of the accelerometer, this equation assumes that all masses have equal sensitivities. The $\sqrt{2}$ coefficient causes an increase of 3 dB in the noise levels of all three directions. In the $y$- and $z$-directions, the subtraction of the two signals with opposite signs causes a reduction of 3 dB in the noise levels. These two directions thus have the same noise levels as the individual masses, but the subtraction removes the flicker noise and offset. In the $x$-direction, the summation of four signals causes a 3-dB reduction in the noise level compared to the noise level of the individual masses. This summation does not remove the flicker noise or the offset. However, these components can be removed by using chopper stabilization without a penalty in the power dissipation.

The 10 700-point FFT plots that were measured for $x$- and $z$-directional accelerations with CDS and with and without chopper stabilization in the differential mode are shown in Fig. 10. A moving average of 21 points was again used to smooth the spectra, and each proof mass was sampled at 1 kHz. As predicted earlier, the flicker noise is removed in the $y$- and $z$-directions without using chopper stabilization in contrast to the case of the $x$-direction. The low-frequency noise floors that were measured in the $x$-, $y$-, and $z$-directions when using CDS, chopper stabilization, and the differential mode are 424, 607, and 590 $\mu\text{g}/\sqrt{\text{Hz}}$, respectively. The reason that the results of the differential mode are better than the system measurements in [16] may be explained by the fact that, in the system measurements, the noise of the ADC partially dominated the total output noise.

The low-frequency noise floors in the $x$-, $y$-, and $z$-directions for the single-ended mode, when both CDS and chopper stabilization were used, are 490, 681, and 549 $\mu\text{g}/\sqrt{\text{Hz}}$, respectively. One possible reason that the single-ended results are better than those presented with the system measurements in [16], is shown by comparing Figs. 11 and 12, in which the noise spectra of the system and the front end are shown in the single-ended mode. In Fig. 11, the noise level is higher than in Fig. 12, and the noise has the shape of white noise, which indicates that the noise is not limited by the front end. The source of this white noise could be the on-chip ADC, because its noise is white, and it was optimized for the differential mode. The reason for the large deviation of the noise in the $z$-direction in the single-ended mode was still unknown to the authors at the time of writing.

The noise measurement results of the single-ended and the differential modes yield a dynamic range for a 10-bit operation at 100-Hz bandwidth, with a $\pm 4$-g full-scale signal.

### C. Leakage Current Measurements

By using Measurement Setup 2, the temperature dependencies of the offset error caused by various leakage currents, particularly those occurring in the switches that sample the reference voltages into the sensor, were measured, and the difference of the operating modes were compared in the worst case conditions.

The worst case conditions from the viewpoint of the leakage currents are the slow sampling frequency, small sensor capacitances, and high reference voltages. Sampling frequencies of 100 Hz and 1 kHz were used in the single mass-operating mode. The internal sensor model with 2-pF capacitance values for $\text{C}_{\text{DP}}$ and $\text{C}_{\text{DN}}$ was used. If the reference voltages $-V_{REF}$ and $+V_{REF}$ are large, in the extreme the supply voltages, then the switches that are near the reference voltages, shown in Fig. 3, are dominant subthreshold leakage sources, because the bulk effect does not increase the threshold voltage [21]. In the designed front end, the threshold voltages are increased by using nonminimum-length switches. However, the subthreshold leakage may be large; hence, the maximum 0.85-V reference voltage $V_{REF}$ was used in the measurements.

The temperature dependencies of the output voltage of the front end that were measured in the single-ended and differential modes at different sampling frequencies are shown in

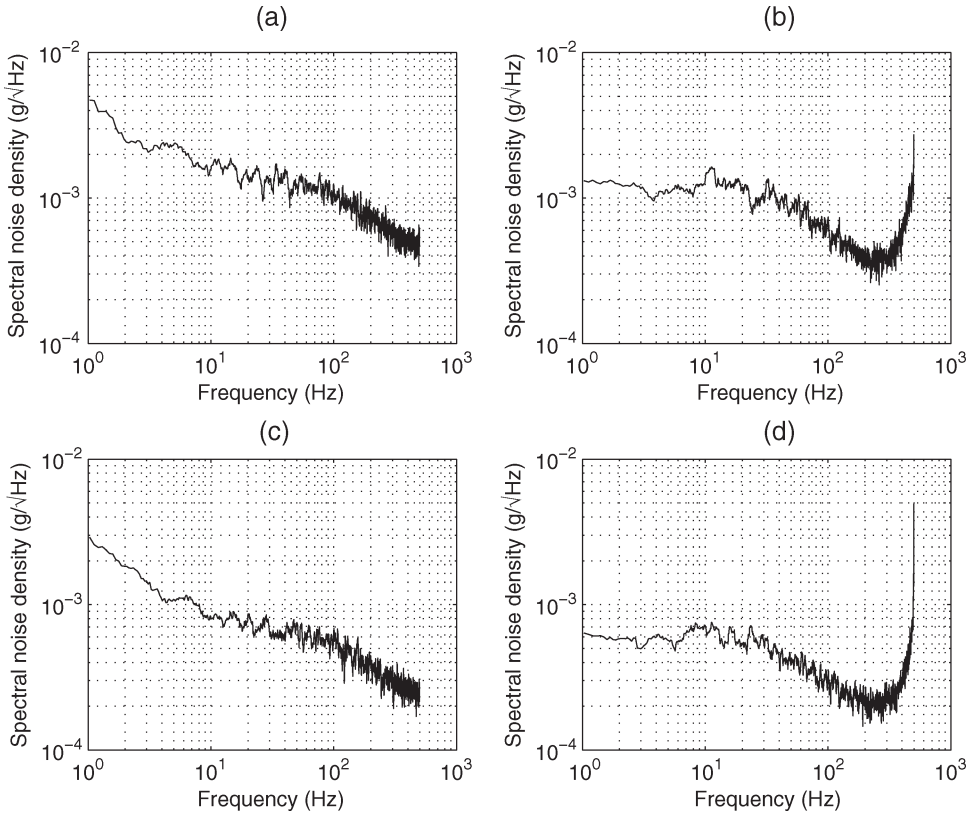


Fig. 9. Measured noise spectra for one mass (a) without CDS and chopper stabilization, (b) with chopper stabilization only, (c) with CDS only, and (d) with CDS and chopper stabilization (with 10 700-point FFT, no windowing, moving average of 21 points, and a sampling frequency of 1 kHz in the differential mode).

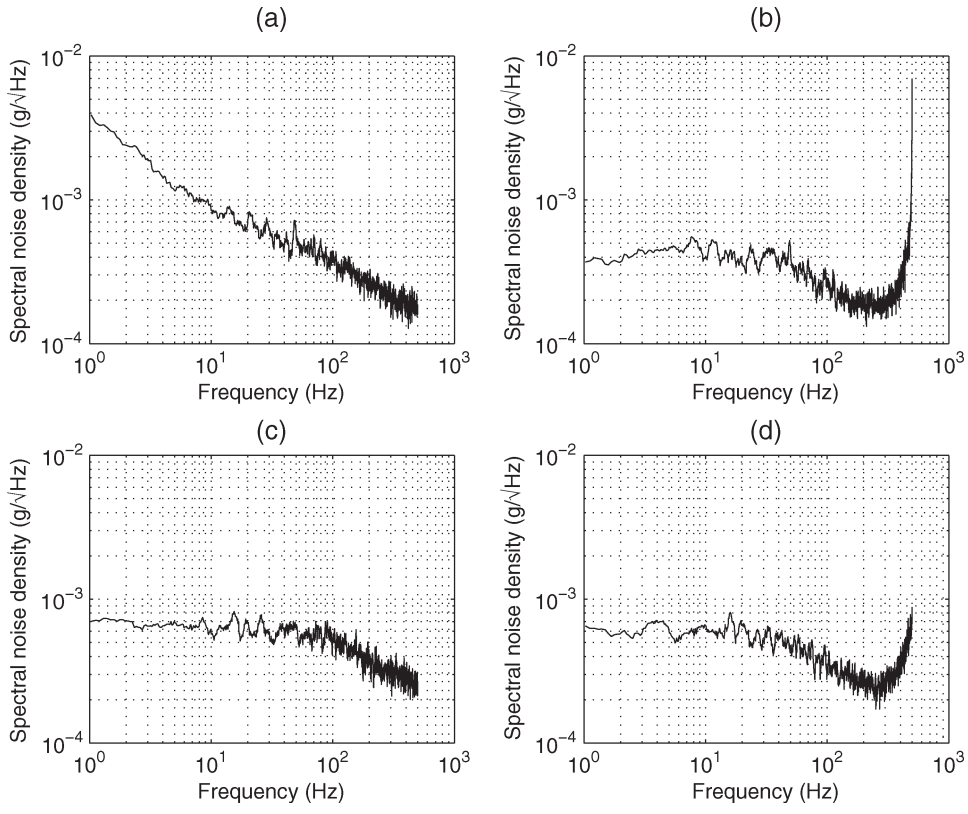


Fig. 10. Measured noise spectra for (a) $x$-direction with CDS, (b) $x$-direction with CDS and chopper stabilization, (c) $z$-direction with CDS, and (d) $z$-direction with CDS and chopper stabilization (with 10 700-point FFT, no windowing, moving average of 21 points, and a sampling frequency 1 kHz in the differential mode).

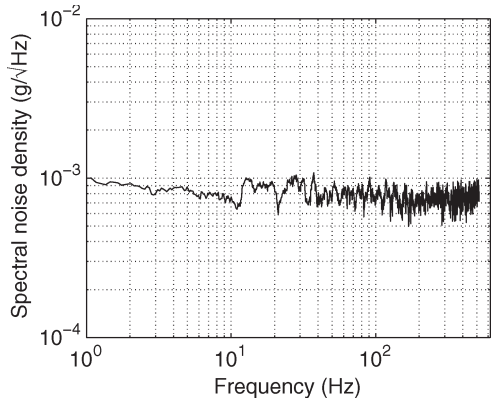


Fig. 11. Measured 10 700-point FFT for the $y$-direction when the system was measured using CDS, chopper stabilization, and the on-chip ADC.

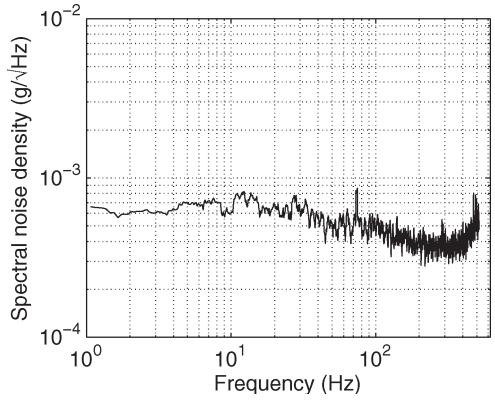


Fig. 12. Measured 10 700-point FFT for the $y$-direction when the front end was measured using CDS, chopper stabilization, and the external ADC.

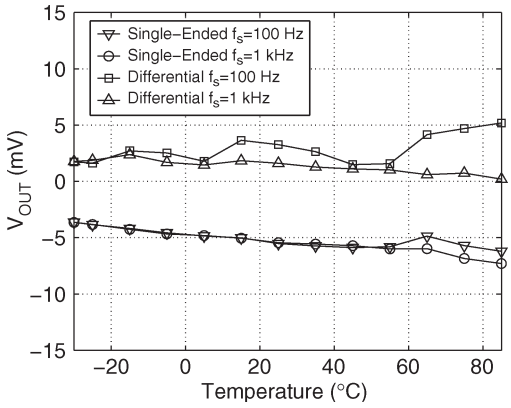


Fig. 13. Measured temperature dependencies of the output voltage of the front end. To compare the results of the operating modes, the results of differential mode were divided by two.

TABLE III
RESULTS OF THE LEAKAGE CURRENT MEASUREMENTS

| Operating mode | Sampling frequency $[kHz]$ | Output voltage $[mV]$ | | |
|---|---|---|---|---|
| | | min | max | max-min |
| Single-ended | 0.1 | -6.2 | -3.6 | 2.6 |
| Single-ended | 1 | -7.3 | -3.6 | 3.7 |
| Differential | 0.1 | 1.5 | 5.2 | 3.7 |
| Differential | 1 | 0.2 | 2.4 | 2.2 |

Fig. 13. To compare the results of the operating modes, the differential mode results were divided by two. The results in Fig. 13 have been collected in Table III.

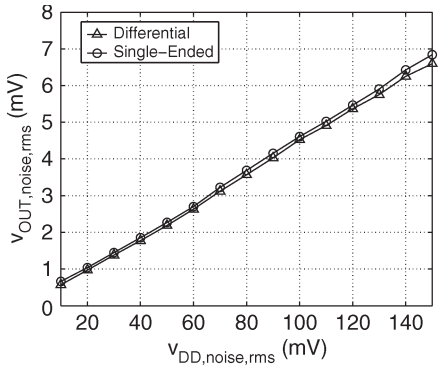


Fig. 14. PSRR measurement results. To compare the results of the operating modes, the results of differential mode were divided by two.

The results of the leakage current measurements indicate that the offset-voltage drifts are a few millivolts and that there is no significant difference between the single-ended and differential modes. According to the data sheets, the instrumentation amplifier and the operational amplifier have typical offset-voltage drifts of 1.4 and 0.3 mV from $-30$ °C to $+85$ °C, respectively. The results in Table III are partly explained by the offset drifts of the PCB components, and therefore, the offset drift of the front end cannot accurately be defined.

### D. PSRR Measurements

In the power supply rejection ratio (PSRR) measurements, the goal was to find out whether the differential mode operation would improve the PSRR over the single-ended mode. Measurement Setup 2 and the internal sensor model were used in the PSRR measurements. The size of the capacitors $C_{DP}$ and $C_{DN}$ was 2 pF. The reference voltage $V_{REF}$ was 0.5 V, and CDS was used. White noise with root-mean-square (RMS) values between 10 and 150 mV and with a bandwidth of 200 kHz was added to the 1.8-V supply. For different RMS values of the white-noise level, the standard deviations of the output voltage of the front end were calculated. These results have been plotted in Fig. 14. Again, the results of the differential mode were divided by two to make them comparable with the results of the single-ended mode.

The results indicate that the PSRR of the front end is independent of the operating mode that was used. The reason for this behavior might be that the input signal of the first integrator is single ended. Although the results are the same, note that the front end is just a part of the sensor interface. Therefore, it is important that the signal is differential to the following building blocks as it is to ADCs, because the differential signal is less sensitive to interference that comes from digital circuitry for example.

### E. System Measurements

In the system measurements, the front end that operates in the differential mode was measured as a part of the whole system in Fig. 1 in a rate table [16]. All four masses were read at a 1.04-kHz sampling frequency that was generated by the on-chip SYSCLK. The reference voltage $V_{REF}$ was 0.85 V, and CDS

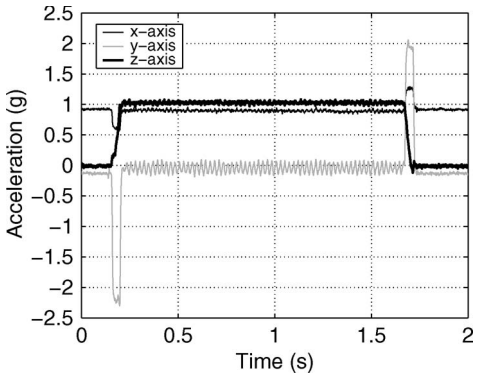


Fig. 15. Acceleration pulse of $+1$ g in the $z$-direction.

TABLE IV
PERFORMANCE SUMMARY

| | | | |
|---|---|---|---|
| Process | $0.13\text{-}\mu m$ BiCMOS | | |
| Supply | $1.8\,V$ | | |
| Active area | $0.30\,mm^2$ | | |
| Mode | Single-ended | Differential | |
| $f_s$/mass | 1 | 1 | $(kHz)$ |
| $I_{avg}$ | $\leq 14$ | $\leq 20$ | $(\mu A)$ |
| Noise floor | | | |
| x-axis | 490 | 424 | $(\mu g/\sqrt{Hz})$ |
| y-axis | 681 | 607 | $(\mu g/\sqrt{Hz})$ |
| z-axis | 549 | 590 | $(\mu g/\sqrt{Hz})$ |

was used. The external ADC was replaced with the on-chip ADC. Only the supply voltages were brought from outside the chip. Centrifugal acceleration $a = r\omega^2$, where $r$ is the distance of the sensor element from the center of the rate table, and $\omega$ is the angular velocity, was used to generate an acceleration pulse of $+1$ g in the $z$-direction.

Based on the response shown in Fig. 15, it is shown that, as a part of the system, the front end provides a $z$-directional acceleration signal of $+1$ g. The resultant of the accelerations in the $x$- and $y$-directions corresponds to the earth's gravity, because the sensor is slightly slanted on the PCB. The angular acceleration and deceleration $\alpha$ of the rate table cause a tangential acceleration component $a = r\alpha$, which is clearly shown in the $y$-directional acceleration curve. The varying acceleration in the $y$-direction is caused by the cogging torque of the rate table. The overall performance of the front end is summarized in Table IV. The system measurements have been published in more detail in [16].

## IV. CONCLUSION

In this paper, a micropower front end for three-axis capacitive microaccelerometers that was implemented in the $0.13\text{-}\mu$m BiCMOS process has been presented. The front end with a 0.30-mm$^2$ silicon area draws 20 $\mu$A from a 1.8-V supply while sampling four masses, each at 1 kHz, when the differential mode was used. With a three-axis capacitive accelerometer with $\pm 4$ g full-scale range, the measured noise floors in the $x$-, $y$-, and $z$-directions are 424, 607, and 590 $\mu g/\sqrt{\text{Hz}}$, respectively. The measurements show that the functionality of the front end follows the theory in the single-ended and differential modes. All the measurements suggest that the performance of the single-ended front end is very close to the differential front end. However, according to the viewpoint of the system, the differential signal from the front end is less sensitive to interference, which is achieved at the expense of the current consumption and the silicon area.

The silicon area of the front end can remarkably be decreased by removing the internal sensor model and by optimizing the sizes of the capacitor matrices. The current consumption of the front end can be lowered by adding a power-down mode. In that case, after the front end had been read and had stored a new value, it would sleep until it is time to read the next value. In system [16], the front end is always active, and therefore, a part of the voltage reference also has to be always active. Hence, by using the power-down mode in the front end, not only the current consumption of the front end but also the current consumption of the voltage reference is saved. The other blocks of the system used the power-down mode with success.

## ACKNOWLEDGMENT

The authors would like to thank VTI Technologies for providing the sensor elements, together with the assistance and equipment in the rate-table measurements, in particular T. Elo for his time, which made the measurements possible. L. Aaltonen of the SMARAD-2/Electronic Circuit Design Laboratory is acknowledged for many valuable discussions and advice during the course of this paper, and P. Rahikkala, T. Rapinoja, and O. Viitala for their assistance in drawing the layout.

## REFERENCES

[1] T. Lehtonen and J. Thurau, "Monolithic accelerometer for 3D measurements," in *Advanced Microsystems for Automotive Applications*, J. Valldorf and W. Gessner, Eds. Berlin, Germany: Springer-Verlag, 2004, pp. 11–22.

[2] R. Puers and S. Reyntjens, "Design and processing experiments of a new miniaturized capacitive triaxial accelerometer," *Sens. Actuators A: Phys.*, vol. 68, no. 1–3, pp. 324–328, Jun. 1998.

[3] T. Mineta, S. Kobayashi, Y. Watanabe, S. Kanauchi, I. Nakagawa, E. Suganurma, and M. Esashi, "Three-axis capacitive accelerometer with uniform axial sensitivities," *J. Micromech. Microeng.*, vol. 6, no. 4, pp. 431–435, Dec. 1996.

[4] M. Kämäräinen, M. Saukoski, and K. Halonen, "A micropower front-end for capacitive microaccelerometers," in *Proc. IEEE Norchip Conf.*, Linköping, Sweden, Nov. 2006, pp. 261–266.

[5] W. Henrion, L. DiSanza, M. Ip, S. Terry, and H. Jerman, "Wide dynamic range direct digital accelerometer," in *Tech. Dig. Solid-State Sensor Actuator Workshop*, Hilton Head Island, SC, Jun. 1990, pp. 153–157.

[6] M. Lemkin, M. Ortiz, N. Wongkomet, B. E. Boser, and J. Smith, "A 3-axis surface micromachined $\Sigma\Delta$ accelerometer," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, Feb. 1997, pp. 202–203.

[7] M. Lemkin and B. E. Boser, "A three-axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics," *IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 456–468, Apr. 1999.

[8] C. Condemine, N. Delorme, J. Soen, J. Durupt, J.-P. Blanc, M. Belleville, and A. Besançon-Voda, "A 0.8mA 50Hz 15b SNDR $\Delta\Sigma$ closed-loop 10g accelerometer using an $8^{\text{th}}$-order digital compensator," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, Feb. 2005, pp. 248–249.

[9] B. V. Amini, R. Abdolvand, and F. Ayazi, "A 4.5mW closed-loop $\Delta\Sigma$ micro-gravity CMOS-SOI accelerometer," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, Feb. 2006, pp. 288–289.

[10] B. V. Amini, R. Abdolvand, and F. Ayazi, "A 4.5-mW closed-loop $\Delta\Sigma$ micro-gravity CMOS SOI accelerometer," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2983–2991, Dec. 2006.
[11] L. Aaltonen, P. Rahikkala, M. Saukoski, and K. Halonen, "Continuous time interface for $\pm$1.5 g closed-loop accelerometer," in *Proc. IEEE Int. Conf. IC Des. Technol.*, Austin, TX, May 2007, pp. 187–190.
[12] L. Aaltonen, P. Rahikkala, M. Saukoski, and K. Halonen, "High resolution analog interface for micromachined capacitive accelerometer," in *Proc. IEEE Eur. Conf. Circuit Theory Des.*, Sevilla, Spain, Aug. 2007, pp. 96–99.
[13] J. Bernstein, R. Miller, W. Kelley, and P. Ward, "Low-noise MEMS vibration sensor for geophysical applications," *J. Microelectromech. Syst.*, vol. 8, no. 4, pp. 433–438, Dec. 1999.
[14] M. Kämäräinen, M. Saukoski, M. Paavola, and K. Halonen, "A 20 $\mu$A front-end for three-axis capacitive microaccelerometers," in *Proc. IEEE Instrum. Meas. Technol. Conf.*, Warsaw, Poland, May 2007, pp. 1–5.
[15] M. Paavola, M. Kämäräinen, J. Järvinen, M. Saukoski, M. Laiho, and K. Halonen, "A 62$\mu$A interface ASIC for a capacitive 3-axis micro-accelerometer," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, Feb. 2007, pp. 318–319.
[16] M. Paavola, M. Kämäräinen, J. Järvinen, M. Saukoski, M. Laiho, and K. Halonen, "A micropower interface ASIC for a capacitive 3-axis micro-accelerometer," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2651–2665, Dec. 2007.
[17] H. Leuthold and F. Rudolf, "An ASIC for high-resolution capacitive microaccelerometers," *Sens. Actuators A: Phys.*, vol. 21, no. 1–3, pp. 278–281, Feb. 1990.
[18] H. Alzaher and M. Ismail, "A CMOS fully balanced differential difference amplifier and its applications," *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 48, no. 6, pp. 614–620, Jun. 2001.
[19] R. Harjani, R. Heineke, and F. Wang, "An integrated low-voltage class AB CMOS OTA," *IEEE J. Solid-State Circuits*, vol. 34, no. 2, pp. 134–142, Feb. 1999.
[20] L. Yao, M. Steyaert, and W. Sansen, "A 0.8-V 8-$\mu$W CMOS OTA with 50-dB gain and 1.2-MHz GBW in 18-pF load," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Estoril, Portugal, Sep. 2003, pp. 297–300.
[21] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003.

**Mika Kämäräinen** (S'07) was born in Helsinki, Finland, in 1975. He received the M.Sc. and Lic.Sc. degrees in electrical engineering in 2006 and 2007, respectively, from the Helsinki University of Technology (TKK), Espoo, Finland, where he is currently working toward the D.Sc. degree in electrical engineering in the SMARAD-2/Electronic Circuit Design Laboratory.

His research interests include low-voltage low-power analog circuit designs related to sensor front ends.

**Mikko Saukoski** (S'06–M'09) was born in Savukoski, Finland, in 1978. He received the M.Sc. and D.Sc. degrees in electrical engineering from the Helsinki University of Technology (TKK), Espoo, Finland, in 2004 and 2008, respectively.

From 2003 to 2007, he was a Research Assistant and then a Research Engineer with the SMARAD-2/Electronic Circuit Design Laboratory, TKK. Since 2008, he has been with ELMOS Semiconductor AG, Dortmund, Germany, as a Systems Design Engineer with ELMOS Microsystems. His research interests include microelectromechanical sensors and actuators, and low-voltage low-power high-accuracy analog circuit design.

**Matti Paavola** (S'06) was born in Kaustinen, Finland, in 1980. He received the M.Sc. and Lic.Sc. degrees in electrical engineering in 2005 and 2007, respectively, from the Helsinki University of Technology (TKK), Espoo, Finland, where he is currently working toward the D.Sc. degree in electrical engineering in the SMARAD-2/Electronic Circuit Design Laboratory.

His research interests include low-voltage low-power analog circuit designs related to sensor interfaces.

**Jere A. M. Järvinen** was born in Espoo, Finland, in 1977. He received the M.Sc. and D.Sc. degrees in electrical engineering from the Helsinki University of Technology (TKK), Espoo, Finland, in 2002 and 2008, respectively.

From 2002 to 2006, he was a Research Engineer with the SMARAD-2/Electronic Circuit Design Laboratory, TKK. He is currently with the Power Management DC–DC Converter Group, Texas Instruments, Espoo. His research interests include low-power mixed-signal applications.

**Mika Laiho** (M'04) was born in Parkano, Finland, in 1973. He received the M.Sc., Lic.Sc., and D.Sc. degrees in electrical engineering from the Helsinki University of Technology (TKK), Espoo, Finland, in 1999, 2001, and 2003, respectively.

He joined the SMARAD-2/Electronic Circuit Design Laboratory, TKK in 1998. He is currently a Senior Researcher with the Microelectronics Laboratory, University of Turku, Turku, Finland. His research interests include neuromorphic vision chips, array processor realizations, and mixed-mode integrated circuits for sensor interfaces.

**Kari A. I. Halonen** (M'02) received the M.Sc. degree in electrical engineering from the Helsinki University of Technology (TKK), Espoo, Finland, in 1982, and the Ph.D. degree in electrical engineering from the Katholieke Universiteit Leuven, Leuven, Belgium, in 1987.

Since 1988, he has been with the SMARAD-2/Electronic Circuit Design Laboratory, TKK. From 1993 to 1997, he was an Associate Professor and, since 1997, a Full Professor with the Faculty of Electrical Engineering and Telecommunications. He became the Head of the Electronic Circuit Design Laboratory in 1998. He specializes in CMOS and BiCMOS analog integrated circuits, particularly for telecommunication applications. He is the author or a coauthor of more than 200 international and national conference proceedings and journal publications on analog integrated circuits.

Prof. Halonen is a member of Technical Program Committee (TPC) of the European Solid-State Circuits Conference (ESSCIRC) and International Solid-State Circuits Conference (ISSCC). He was the TPC Chairman of ESSCIRC 2000. He has been an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I and a Guest Editor of the IEEE JOURNAL ON SOLID-STATE CIRCUITS. He received the Beatrice Winner Award at the ISSCC 2002.